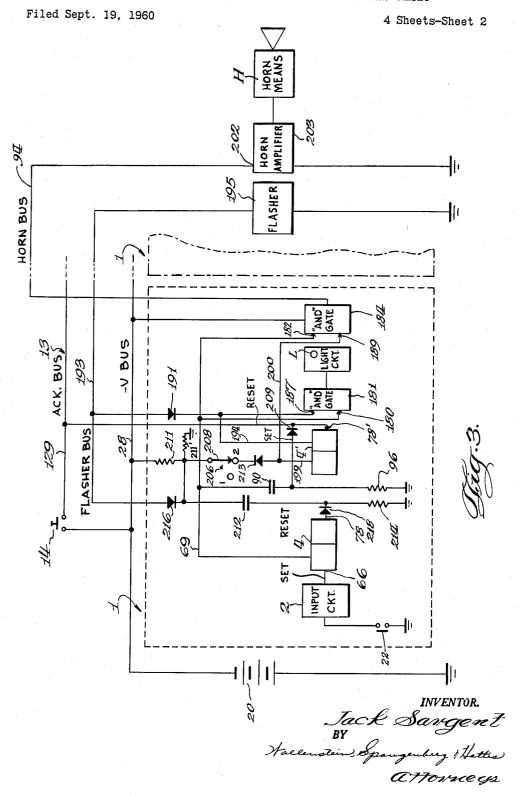
ANNUNCIATOR SYSTEM WITH ACKNOWLEDGMENT AND RESET

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ANNUNCIATOR SYSTEM WITH ACKNOWLEDGMENT AND RESET



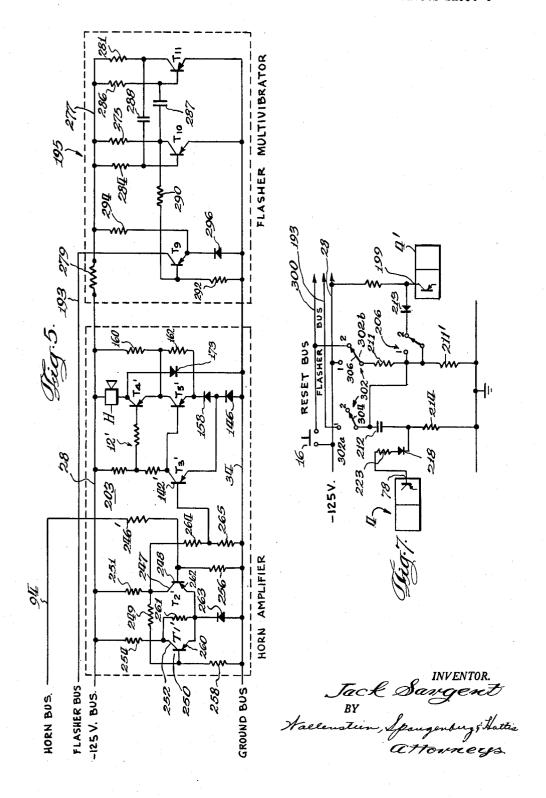
ANNUNCIATOR SYSTEM WITH ACKNOWLEDGMENT AND RESET

Filed Sept. 19, 1960	4 Sheets-Sheet 3
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ANNUNCIATOR SYSTEM WITH ACKNOWLEDGMENT AND RESET

Filed Sept. 19, 1960

4 Sheets-Sheet 4



3,136,982 ANNUNCIATOR SYSTEM WITH ACKNOWLEDG-MENT AND RESET

Jack Sargent, Chicago, Ill., assignor, by mesne assignments, to Scam Instrument Corporation, Skokie, Ill., a corporation of Illinois

Filed Sept. 19, 1960, Ser. No. 56,896 8 Claims. (Cl. 340-213.1)

This invention relates to annunciator systems of the 10 type wherein a visual alarm unit, such as a light unit, is provided for each variable to be monitored, and, when the variable becomes abnormal, a pair of field contacts are actuated to operate the visual alarm unit which indicates that the variable involved has just become abnormal. A manually operable acknowledgement switch is usually provided, which, when operated, changes the indication of the visual alarm unit to indicate that the alarm has been acknowledged by the operator. Usually, an audible alarm is also included to attract the operator's attention to a central control panel containing the visual alarm units associated with practically all of the variables to be monitored in the plant involved, so that the operator can determine at a glance the condition of all of the

For the most part, annunciator systems of the kind just described have heretofore been hydraulically or relay controlled systems, and these systems left much to be desired from the standpoint of reliability because of mechanical wear and, in the case of the relays, additionally because 30 the relay coils sometimes burned out. Obviously, it is quite important for annunciator systems to be reliable, since otherwise, they could not fulfill their intended purpose. More recently, static control elements, such as to replace relays to provide a system of improved reliability. Such annunciator systems have also been recently developed operating with transistor control elements. Although the annunciator systems have proven satisfactory for many purposes, they have certain drawbacks over- 40 come by the present invention. For example, magnetic core as well as transistor annunciator systems have required special power supplies. The provision of special power supplies not only increases the expense of the system but, more importantly, reduces materially the re- 45 liability of the system. Failure of a power supply will, of course, result in breakdown of the entire system.

Transistors are generally operated from low voltage power supplies. Typical voltage limitations of transistors are 25 volts for the more common, economical transistors 50 and 45 and 85 volts for the more expensive and less common types. Low voltage operation means high current requirements in transistor circuits controlling light sources and the like. For example, in the case of a 4 or 5 watt lamp, the current required for a single lamp is frequently in the order of ½ of an ampere. Where a large number of points are being monitored by the annunciator system, the potential current requirements where a large number of variables are simultaneously abnormal can be quite high. Problems of overheating of certain components in the power supply carrying common load current, and providing good regulation where load requirements vary widely as in the case of annunciator systems create exceedingly difficult problems.

Particular difficulty has been encountered in providing 65 static annunciator systems for monitoring power stations. Power stations commonly have a 125 volt D.C. battery supply source for the control circuits which operate the power station. These control circuits have generally been relay systems which operate readily at such voltages. To operate static annunciator systems from such a power source has heretofore required special converters for pro-

viding the necessary voltages for operating the static control elements involved. In the case of annunciators using transistors, the required low voltage could not satisfactorily be supplied by merely adding a common resistor voltage divider circuit since this voltage divider must be able to carry a high and widely varying current where the aforesaid overheating and regulation problems would obviously be present. Prior to the present invention it was believed necessary to utilize either a motor generator converter which converted the relatively high direct current battery supply voltage directly to a low direct current voltage, or a vibrator which converted the battery voltage to pulsating or alternating current which was fed through a transformer to provide the necessary low volt-The use of these converters provide cost, reliability and, to a lesser but nonetheless significant extent, regulation problems.

It is, accordingly, one of the objects of the invention to provide a static element annunciator system, preferably a transistor annunciator system, which is capable of operating directly from a 125 volt direct current voltage source, such as the battery supply commonly found in power stations.

Many of the static annunciator systems heretofore de-25 veloped used flip-flop (bistable) circuits as basic control These bistable circuits frequently operated from capacitor pulse-forming networks in turn controlled by field contacts controlled directly by the variables in-The reliability of these annunciator systems were sometimes adversely affected by the presence of large distributed capacity in the lines where long distances separated the field contacts from the pulse-forming networks.

Another one of the objects of the invention, therefore, magnetic cores, have been used in annunicator systems 35 is to provide a static element annunciator system utilizing bistable circuits where the distributed capacity of long lines interconnecting the field contacts with the associated bistable control circuits do not adversely affect the operation of the bistable circuits.

In accordance with one aspect of the invention, there is associated with each variable to be monitored a bistable circuit including a pair of transistor control elements each having a pair of load terminals commonly referred to as emitter and collector electrodes and a control terminal commonly referred to as a base electrode. Where type PNP transistors are utilized, a resistor is connected between the collector electrode of each transistor and the negative terminal of the high direct current voltage source whose magnitude is many times greater than that of the applied voltage source for which the transistors are designed to operate. The emitter electrode thereof is connected to the other terminal of the direct current voltage source. A resistor is connected between the collector electrode of each transistor and the base electrode of the other transistor forming the associated bistable control circuit. Another resistor is connected between each base electrode and the positive terminal of the direct current voltage source. The values of the aforementioned resistors are so proportioned that they effectively act as a voltage divider which reduces the voltage at the collector electrodes to a low value to which the transistors are normally designed to operate. It is apparent that none of the resistors referred to carry any substantial current since they only carry the current required for the associated bistable circuit. Thus, no overheating or regulation problems are involved as would be the case if a common voltage divider network were to be utilized to drop the voltage of the source of direct current voltage to the proper value. The other transistors of the annunciator circuit are similarly operated from the high voltage direct current voltage source.

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Various types of relay annunciator systems have become popular in recent years. In one type, the visual and audible alarm signals for a momentary abnormal variable are locked-in so that the alarm information is preserved until a record of the momentary trouble is made. Another type is referred to as a non-lock-in system where the visual and audible alarm signals for a momentary alarm are not maintained. The lock-in type of annunciator system, in addition to having a manual acknowledgement switch for silencing the audible signal and, in many 10 cases, changing the initial visual indication involved to a different acknowledged indication, includes a manual reset switch for terminating the visual signal when the variable returns to normal after acknowledgement. This is referred to as a manual reset feature. Annunciator 15 systems made with static elements, particularly transistors, have offered some but not all of these features. For example, there is a need for transistorized annunciator systems which provides in a simple and reliable manner a selection of lock-in and non-lock-in operation, and/or 20 shown in FIG. 3; a selection of manual reset and automatic reset operation after acknowledgement.

It is, accordingly, an object of the present invention to provide a reliable static element annunciator system, providing for a selection of non-lock-in and lock-in operation, and/or manual reset and automatic reset operation.

FIG. 7 illust of FIGS. 4 and reset operation.

In accordance with another aspect of the present invention, each set of field contacts is arranged to feed a continuous set signal to one of the control terminals of 30 the associated bistable circuit. Where transistors are used as the static elements in the bistable circuit, the set signal is a direct current potential. A unique reset circuit is associated with another control terminal of the bistable circuit which continuously prepares the bistable 35 circuit for a reset operation which becomes effective when the set signal is removed by the return of the variable involved to normal. This arrangement results in a fast acting bistable circuit which is not adversely affected by the distributed capacitance in the long lines connecting 40 remotely located field contacts to the annunciator circuit. Such capacitance could slow down the response of a bistable circuit responding to a pulse generated by operation of the field contacts to a point where an abnormal variable would not be detected. The reset circuit preferably includes a source of reset pulses which are continuously coupled to the reset control terminal of the bistable circuit so that a reset operation may occur substantially immediately after the field contacts return to their normal condition to disconnect the aforementioned set signal from the bistable circuit. Connections are made from the bistable control circuit to an associated visual alarm control circuit so that the alarm light becomes de-energized as soon as the variable returns to normal. This is the non-lock-in operation referred to above. If it is desired to lock-in an initial alarm indication of the variable (which might be abnormal only momentarily), a manual select switch may be provided to de-couple or inhibit the effect of the reset pulses. In the preferred form of the invention, a second bistable circuit is provided for each variable which is initially set by the initial triggering of the first-mentioned bistable circuit, the set condition thereof inhibiting the effect of said reset pulses on the first bistable circuit until reset by operation of a manually operable acknowledgement switch. The acknowledgement switch in such case may be properly called a reset switch (and is referred to as such in some of the claims herein). The aforementioned manual select switch is used to selectively couple and uncouple the inhibit output of the second bistable circuit to provide for a selec- 70 tion of lock-in or non-lock-in operation.

Where manual reset operation is desired, the aforesaid source of continuous reset pulses may be removed from the circuit or de-coupled therefrom, and a manual reset switch added to the circuit which resets the first-mentioned 75

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bistable circuit after the reset inhibit effect of the second bistable circuit is terminated by operation of the acknowledgement switch. Removal of the continuous reset pulses provides lock-in after acknowledgement.

Other objects, advantages and features of the invention will become apparent upon making reference to the specification to follow, the claims and the drawings wherein:

FIG. 1 is a schematic diagram of a transistorized annunciator system of the invention providing a simple non-flashing visual alarm sequence;

FIG. 1a shows a printed circuit card which holds the circuit components exclusive to a single variable;

FIG. 2 is a table illustrating the various conditions of operation of the annunciator system of FIG. 1;

FIG. 3 is a simplified box diagram of another annunciator system providing a flashing visual sequence and a selection of lock-in and non-lock-in operation;

FIGS. 4 and 5 are a schematic diagram of a preferred transistorizer embodiment of the annunciator system shown in FIG. 3:

FIG. 6 is a table illustrating the conditions of operation of the circuit of FIGS. 4 and 5; and

FIG. 7 illustrates a minor modification of the circuit of FIGS. 4 and 5 which provide for an optional manual reset operation.

Non-Flashing Transistorized Annunciator System

The annunciator system shown in FIG. 1 is made of PNP type transistors, resistors, diodes and capacitors forming a light control circuit comprising a signal input circuit 2, a bistable circuit 4 and a light amplifier circuit 6 associated with each variable. A horn control circuit 7 is provided comprising a bistable circuit 10 and a horn amplifier circuit 12 in common with all variables. The light control circuits exclusive to the variables (only one of which appears in FIG. 1) are connected in parallel between various buses generally indicated by reference numeral 13. Most of the components making up each control circuit are placed on a single printed circuit card 14 shown in FIG. 1a which can be mounted in plugin relation to connectors mounted on a common frame. The common horn circuits 10 and 12 can be mounted on a similar printed circuit card not shown. Each light control circuit controls the operation of an alarm lamp L and the horn circuits control a horn H.

Before discussing the annunciator system in detail, it would be helpful to review the basic sequence of operation of each alarm lamp and horn. When a particular variable goes abnormal, the associated alarm lamp L is operated to a steady bright condition and the common horn H is sounded. A manually operable acknowledgement switch 14 is provided in common with all of the control circuits and, when momentarily depressed, silences the horn H. A common manually operable reset switch 16 is also provided which, when momentarily operated, extinguishes the alarm lamp L only if the associated variable has returned to normal.

In accordance with one aspect of the invention, substantially all of the transistors used in the annunciator 60 circuit are low (e.g., 25 volts) voltage transistors arranged in a unique circuit to be described where they are operated directly from a relatively high direct current voltage source 20, such as 125 volts commonly found in direct current battery supply systems of power 55 stations.

The condition of the basic variable being monitored is identified by the position of a set of field contacts 22 (which may be bi-metal temperature responsive contacts in the case of a temperature variable, bellow-operated contacts in the case of a pressure variable, etc.) located at the situs of the variable involved. Each set of field contacts 22, which are illustrated as normally-opened contacts which are closed when the associated variable becomes abnormal, are usually connected by long conductors 23 to connecting terminals 24 of the signal in-

put circuit 2. FIG. 1 also shows in dotted lines a normally-closed set of field contacts 22' connected through long conductors to connecting terminals 25, which contacts may be substituted for the normally-open contacts. When operating with normally-open field contacts, a 5 jumper 26 is connected between the terminals 25. The upper of the terminals 25 is connected to a common negative voltage bus 28 leading to the negative terminal of the battery source 20. The bottom terminal 25 extends through a resistor 30 to the upper field contact 10 connecting terminal 24. The bottom field contact connecting terminal is connected to a common grounded bus 34 leading to the positive terminal of the battery source 20. A resistor 35 is connected between the terminals 24. The signal input circuit further includes a 15 of these resistors may be as follows: filter network comprising a resistor 42 connected between resistors 30 and 36 and capacitor 44 connected to the common ground bus 34. The filter network further includes a resistor 46 connected between the juncture of resistor 42 and filter capacitor 44 and a resistor 48 con- 20 nected to the ground bus 34. The filter network bypasses sharp noise impulses which may be picked up in the field conductors 23 which could initiate a false alarm.

The value of filter capacitor 44 depends, in part, upon a consideration of the minimum switch closure time which 25 the annunciator circuit is to respond, and the length of the line extending between the field contacts and the signal input circuit. FIG. 1 shows a lock-in circuit which holds alarm signals for momentary abnormal variables where the field contacts may close for a period of only 700 micro-seconds (or longer). This means that the time constant of the signal input circuit must be sufficiently short that a 700-micro-second closure time will result in actuation of the control circuit. A 400 microsecond time constant is suitable for a 700 micro-second 35 switch closure time. The value of filter capacitor 44 and the length of the conductors 23 extending to the field contacts affect the time constant of the signal input circuit in proportion to the magnitude of these parameters. For a line length of from 1000 to 2000 feet, a 40 filter capacitor value of .01 microfarad is satisfactory. In the exemplary signal input circuit now being described, the various resistors described may have the following

> R30-100,000 ohms R36—220,000 ohms R42—82,000 ohms R46-82,000 ohms R48-6,800 ohms

In some instances, the customer may desire to control some auxiliary device directly from the field contacts, and, accordingly, a control coil (not shown) may be placed in series or parallel with the field contacts. The presence of a relay coil in the signal input circuit could result in the generation of large positive voltage spikes when current is suddenly interrupted in the relay coil which could damage a transistor T3 connected in the signal input circuit. To prevent the coupling of these voltage spikes to the transistor T3, a diode 50 is connected across resistor 48 to short circuit any positive voltage pulses to ground. The upper terminal of resistor 48 is connected to the control terminal or base electrode 52 of transistor T3.

The closure of the normally-open field contacts 22 (or the opening of the normally-closed contacts 22') results in the application of positive or ground potential to the input of the signal input circuit. This potential appears at the base electrode 52 to render the same nonconductive.

The transistor T3 is a low voltage PNP junction tran sistor whose emitter electrode 54 is connected to a biasing silicon diode 56 in turn connected to the common ground bus 34. The diode 56 is connected to offer a low impedance path for normal transistor current flow. 75

The diode 56 may, for example, provide a ½ volt bias for transistor T3 and other transistors to which it is connected. The collector electrode 56 of the transistor T3 is connected to a load resistor 58 in turn connected to the common negative voltage bus 28.

The low voltage transistor T3 (as well as most of the other transistors of the annunciator circuit) may be a Motorola type 2N1191 having a 25 volt emitter to collector voltage rating. A resistor 60 and a resistor 62 are accordingly connected in series between the collector electrode 56 and the common ground bus 34. The values of resistors 58, 60 and 62 are so proportioned that when the transistor T3 is non-conductive, the voltage at the collector electrode is less than 25 volts. Typical values

> R58-225,000 ohms R60-47,000 ohms -4,700 ohms R62-

The ratio of the value of resistor 58 to resistors 62 and 60 is exceedingly higher than is normally found in transistor circuits since one of the main functions of resistor 58 is to drop the high direct current voltage (-125 v.) to less than 25 volts. It is significant that in the use of transistors in annunciator systems that no one prior to the present invention has modified the usual resistor value ratios to adapt the transistors for use with high direct current voltage supply sources such as is commonly available in power stations and the like. Rather, as above explained, the prior art has resorted to more costly and less reliable converters.

The transistor T3 and the associated resistors form a voltage inversion circuit for providing the proper control voltage conditions for the flip-flop or bistable circuit 4.

The bistable circuit 4 comprises a pair of PNP transistors T4 and T5 like transistors T3 having two control input terminals 63 and 64. The control input terminal 62 is at the juncture of resistors 60 and 62 which is connected to the base electrode 66 of the transistor T4. The collector electrode 68 of transistor T4 is connected through a resistor 70 to the common negative voltage bus 28. The emitter electrode 72 of transistor T4 is connected to a common bias line 76 leading to the upper terminal of the biasing diode 56.

The other transistor T5 of the bistable circuit has its base electrode 78 connected to the control input terminal 64. The transistor T5 has its base electrode 78 connected to the common biasing line 76 extending to the biasing diode 56. A resistor 80 extends between the control input terminal 64 and the common ground bus 34. A resistor \$2 is connected between the control input terminal 64 and the collector electrode 63 of the transistor T4. A resistor 84 is connected between the collector electrode 86 of the transistor T5 and the common negative voltage bus 28. A resistor 88 is connected between the collector electrode 86 of transistor T5 and the control input terminal 63 associated with the base electrode 66 of the transistor T4. The resistors 82 and 88 are thus located in feed-back branches extending from the outputs of the respective transistors T4 and T5 to the control electrodes of the other of same to thereby provide a bistable or flip-flop circuit action In accordance with the present invention these resistors, however, perform an added important function in cooperation with resistor pairs 70-80 and 84-62 which is to reduce the negative 125 volts applied voltages to a low voltage (below 25 volts) applied across the collector and base electrodes of transistors T4 and T5. Typical values for the resistors of the bistable control circuit just described are as follows:

> R70 and R74-100,000 ohms R62 and R80-4,700 ohms R82-27,000 ohms R88-22,000 ohms

Initially, transistor T3 is in a relatively high conductive state due to the presence of a negative potential on its base electrode 52. In this state, the collector electrode 56 of transistor T3 is near ground potential which renders the left hand transistor T4 of bistable circuit 4 non-conductive which, in turn, makes the right hand transistor T5 thereof normally conductive. When field contacts 22 close to render transistor T3 non-conductive in the manner described above, the resulting negative potential appearing on the collector electrode 56 forces 10 bistable transistor T4 into conduction which, in turn, renders bistable transistor T5 non-conductive.

The bistable circuit 4 may also be set into the conductive state just described by closure of a manually operable test push-button switch 85 connected between com- 15 mon test bus 87 and the negative voltage bus 28. The control input terminal 63 or base electrode 66 of each control circuit 1 is connected to the test bus. Depression of the test switch will test the operation of the annunciator by creating identical signal conditions as closure 20 tion of the control circuit 1, this condition will provide of contacts 22.

The bistable circuit 4 can be reset to its normal stable state by the reset switch 16 provided the field contacts 22 are re-opened. The reset switch 16 is connected between a common reset bus 89 and the negative voltage bus 28. When the reset switch is momentarily depressed, a negative potential is coupled to the base electrode 78 of the transistor T5 to effect a high conductive state thereof. This will result in the operation of the left hand transistors T4 to a relatively non-conductive state.

Before the variable associated with the control circuit now being described goes abnormal, the left hand transistor T4 thereof is non-conductive and the potential of the collector electrode 68 thereof will be negative. A capacitor 90 is connected between the collector electrode 35 68 and a resistor 91 connected to the ground bus 34. The capacitor 90 initially charges to the negative potential on the collector electrode through the resistor 91. When the varaible goes abnormal and the bistable circuit 4 is triggered into a state where transistor T4 is conductive, the 40 voltage at the collector electrode 68 is near ground potential which effects the discharge of the capacitor 90 through the resistor 91. A positive pulse is thereby generated across the resistor 91. The capacitor 90 and the resistor 91 effectively form what is commonly referred 45 to as a differentiating network. This positive pulse is coupled through a resistor 92 and an isolating rectifier 93 connected to pass positive pulses to a common horn bus 94 which connects with the horn bistable circuit 10. The horn bistable circuit is triggered into a state which 50 effects energization of the horn H in a manner to be ex-

The aforesaid drop in potential at the collector electrode 68 of transistor T4 is coupled through a resistor 102 to the base electrode 104 of a low voltage, low power 55 PNP junction type control transistor T1. A resistor 105 is connected between the base electrode 104 and the ground bus 34. The collector electrode 106 of the transistor T1 is connected through a resistor 108 to the negative voltage bus 28. The emitter electrode 110 of the 60 transistor T1 is connected through a biasing diode 112 to the ground bus 34.

Transistor T1 controls the operation of a high voltage PNP junction transistor T2 which, for example, may be a general transistor type GT 1402 having a rating of 85 65 volts. A high voltage transistor is expensive relative to low voltage transistors and is used here because the load circuit thereof includes the lamp L which has a much lower voltage rating. The base electrode 111 of this transistor is connected to the collector electrode 106 70 of the transistor T1. The emitter electrode 113 of the transistor T2 is connected by a silicon biasing diode 115 to the upper terminal of the biasing diode 112 and by a resistor 122 to the negative voltage bus 28. The col-

through the lamp L to the negative voltage bus 28. A resistor 119 is connected between the collector electrode 117 and the ground bus 34. This resistor 119 drops the voltage across the transistor to 85 volts when it is nonconductive and allows sufficient current to flow through the lamp L to light the same dimly. In the case where the lamp L is a 6 watt lamp, the resistor 119 may be a 3300 ohm 4 watt resistor.

Under normal operating conditions of the control circuit where the left hand transistor T4 of bistable circuit 4 is non-conductive, a negative potential is coupled through the resistor 102 to the base electrode 104 of transistor T1 which renders the same highly conductive. When the associated variable goes abnormal and the bistable transistor is triggered into a highly conductive state, a potential near ground potential is fed to the base electrode 104 of transistor T1 to render the same non-con-

When transistor T1 is conductive during normal operasomething less than 1 volt negative at the base electrode 111 of the transistor T2. The combination of the two diodes 112 and 115 connected in series with the emitter electrode 113 of transistor T2 and resistor 122 provides a voltage in the neighborhood of 1 volt at the emitter electrode 113, so that the base electrode of transistor T2 is positive with respect to the emitter electrode, thereby rendering the transistor T2 non-conductive. When the variable involved goes abnormal, and the transistor T1 accordingly becomes non-conductive, a negative potential appears at the base electrode 11 of power transistor T2 thereby rendering the latter transistor highly conductive to light the lamp L brightly. The emitter to base voltage when transistor T2 conducts is quite low (.5 volt) so that the voltage at the collector electrode of transistor T1 is well below 25 volts. The operating conditions of the light amplifier circuit are returned to their normal state where light 6 is dimly lit when the bistable circuit 4 is reset by operation of reset switch 16 (when the variable returns to normal in the manner previously explained).

As previously indicated, when any variable in the system goes abnormal, a positive voltage pulse appears on the horn bus 94 capable of triggering a horn bistable circuit 10. The bistable circuit 10 is similar to the light bistable circuit 4 previously described in detail so that the details of the circuit 10 will not be described. It is sufficient to say that bistable circuit 10 has transistors T1' and T2' of the same low power type as the low voltage, low power transistors T1 and T2. The left hand transistor T1' is normally conductive and the right hand transistor T2' is normally non-conductive. Also the horn bistable circuit includes load resistors 70' and 84', feedback resistors 82' and 88', and control circuit resistors 62' and 80' which are so proportioned that the voltage applied between the collector and emitter electrodes of transistors T1' and T2' never exceed the rated value of the low voltage transistors, which, for example, is approximately 25 volts.

The horn bistable circuit 10 has two control signal inputs both extending to the base electrode 125 of the transistor T1'. One of these inputs includes a resistor 127 extending from a common acknowledgement bus 129 to the base electrode 125. The other input includes a resistor 131 extending from the common horn bus 94 to the base electrode 125. The acknowledgement bus 129 is connected to the negative voltage bus 28 through a normally-open manually operable pushbutton switch 14. When one of the variables in the system becomes abnormal and the horn bus 94 is accordingly pulsed with a positive voltage, this potential fed to the base electrode 125 renders the transistor T1' non-conductive and the transistor T2' conductive. When the acknowledgement switch 14 is momentarily depressed, negative potential is coulector electrode 117 of the transistor T2 is connected 75 pled to the base electrode 125 which results in the return

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of the transistor T1' to a conductive state and the other transistor T2' to a non-conductive state.

A control voltage is coupled from the horn bistable circuit 10 to a pair of resistors 134 and 136 connected in series between the collector electrode 138 of the right hand transistor T2' and the ground bus 34. A connection 140 extends from the juncture of resistors 134 and 136 to the base electrode 142 of a low voltage, low power, PNP junction transistor T3' located in the horn amplifier circuit 12. The emitter electrode 144 of the 10 transistor T3' is connected to a biasing diode 146 in turn connected to the ground bus 34. The collector electrode 146 thereof is connected through a pair of series connected resistors 148 and 150 to the negative power bus A connection 152 is made between the collector 15 electrode 146 of transistor T3' and the base electrode 154 of a high voltage (85 volts) power transistor T5'. The emitter electrode 156 of the transistor T5' is connected through a biasing diode 158 to the upper terminal of the other biasing diode 146. Proper biasing voltage con- 20 ditions are obtained for the transistor T5' by a pair of resistors 160 and 162 connected in series between the negative voltage bus 28 and the upper terminal of the biasing diode 158. A connection 164 is made between the juncture of resistors 160 and 162 and the collector 25 electrode 156 of transistor T5'.

The load circuit of transistor 154 includes a power transistor T4' which is identical to transistor T5' and the horn 11 connected to the negative voltage bus 28. The emitter electrode 165 of the transistor T4' is connected 30 to the collector electrode 166 of transistor T5'. The base electrode 167 of the transistor T4' is connected through a resistor 169 to the juncture of resistors 150 and 148. The collector electrode 171 of the transistor T4' is connected to the horn. To protect the transistors against 35 reverse voltage spikes which may be developed in the circuit due to the inductive kick in the coil of the horn 11, a ground clamping diode 173 is connected between the juncture of the horn 11 and the collector electrode 171 of transistor T4' and the ground bus 34 so as to bypass 40 positive pulses generated in the horn coil.

The transistor T3' is normally in a conductive state, and when the horn bistable circuit 10 is triggered by the positive pulse on the horn bus 94 to render the right hand transistor T2' conductive, this results in the coupling of a near ground potential to the base electrode 142 of the normally-conductive transistor T3' to render the same non-conductive. This, in turn, creates voltage conditions which effect the conduction of the transistor T4' and T5' to energize the horn. When the acknowledgement switch 14 is momentarily depressed to reset the bistable circuit 10, the voltage conditions in the horn amplifier circuit are reversed to render the transistors T4' and T5' non-conductive to de-energize the horn.

The Optional Abnormal Lock-In and Non-Lock-In Annunciatory System of FIGS. 3 Through 6

Refer now particularly to FIG. 3 which illustrates a basic box diagram of an embodiment of the present invention providing optional and lock-in and non-lock-in operation. In accordance with the broadest aspects of this form of the invention, the various control circuits 1 connected in parallel across the buses 13, 94, 193 and 28 may be made of any type of static components including, for example, magnetic core control elements and the like. This circuit may include normally open (or normally closed) field contacts 22 associated with a signal input circuit 2 and a bistable circuit 4. When the field contacts 22 are moved to their abnormal variable indicating position, a continuous control voltage is coupled through the signal input circuit 2 to a control input terminal 66 of the bistable circuit 4 to set the same into one of its two possible output conditions. The bistable circuit 4 has another control input terminal 78 which is effective to reset the bistable circuit upon receiving a pulse of a 75 horn H.

given polarity as, for example, a negative pulse. When the bistable circuit 4 is initially set by the control voltage at the control input terminal 66, an output line 69 connects a source of relatively positive potential to a differentiating network comprised by capacitor 90 and resistor 96 and also to one of the inputs 180 of a light control "and" gate 181 and one of the inputs 182 of a horn control "and" gate 184. The "and" gates 181 and 184 respectively have second inputs 187 and 139. In the circuit illustrated, if positive (ground) potential is present simultaneously on both of the inputs of either "and" gate, the associated light L or horn H will be energized. The second input 187 of the light control "and" gate 181 extends through a rectifier 191, arranged to pass positive (ground) potential from a common flasher bus 193. A flashing unit 195 common to all of the control circuits is connected between the flasher bus 193 and ground potential which will be assumed to be positive with respect to the other reference potential to be described, which is negative. The flasher 195 continuously feeds positive pulses at a visible pulse repetition rate to the flasher bus 193. It is apparent when the bistable circuit 4 is initially set by the movement of the field contacts 22 to an abnormal variable indicating condition that the light control "and" gate 181 will have simultaneous positive voltage inputs occurring at a visible flashing rate. Accordingly, the associated light L will be energized at a visible flashing rate.

When the associated variable initially becomes abnormal, the aforesaid positive voltage fed to the differentiating network comprising capacitor 90 and resistor 96 generates a momentary positive pulse across resistor 96 which is coupled through a diode 209 (connected to block negative pulses generated by the discharging of capacitors 90) to the control input terminal 78' of a bistable circuit 4' which is similar to the bistable circuit 4. This positive pulse sets the bistable circuit 4' into one of two positive output conditions. An output line 194 extends from the bistable circuit 4' to the input 187 of the light control "and" gate 181. The output line 194 and the connection of the rectifier 191 extending from the flasher bus 193 to the input 187 constitutes an "or" connection. The voltage on the output line 194 of the bistable circuit 4' has a negative potential when the bistable circuit 4' is initially set when the associated variable becomes abnormal, and a positive potential when the bistable circuit 4' is reset. Reset of this bistable circuit is obtained by the momentary depression of acknowledgement pushbutton switch 14 which connects a source of negative potential from nega-50 tive bus 28 to the control input terminal 78' of the bi-stable circuit 4'. The resulting continuous positive voltage on the output line 194 fed to the "and" gate input 187 will, in conjunction with the continuous positive voltage fed to the input 180 thereof from the output line 69 of 55 bistable circuit 4, open the light control gate 181 continuously to operate the lamp L steadily.

The bistable circuit 4' has an output terminal 199 whose voltage conditions are opposite to those appearing on the associated output line 194 whereby the output terminal 199 has a relatively negative potential when the associated bistable circuit is set in response to the abnormality of the associated variable and has a relatively positive potential when the bistable circuit is reset by operation of the acknowledgement switch 14. When the associated variable initially becomes abnormal, the two inputs 182 and 189 of the horn control "and" gate 184 will respectively have a positive potential applied thereto from bistable output line 69 of bistable circuit 4 and outline line 200 connected to output terminal 199. In the particular circuit being described, this will result in the feeding of negative potential from the negative bus 28 to the common horn bus 94. The negative potential on the horn bus 94 is fed to the input terminal 202 of a common horn amplifier circuit 203 which will energize the associated

As previously indicated, the annunciator circuit now being described provides for optional non-lock-in and lock-in operation. To this end, a manual switch 206 is provide having a movable contact 208 selectively engageable with stationary contact Nos. 1 or 2. When the movable contact is in position No. 1, the circuit provides nonlock-in operation where the condition of the lamp L follows the position of the field contacts 22, and when it is in position No. 2 it provides a lock-in operation where momentary abnormal variables will be indicated by an 10 indication on lamp L which can only be removed by operation of the manual acknowledgement switch 14. To effect de-energization of the lamp L it is necessary to reset the bistable circuit 4. In the embodiment of the invention now being described, a unique reset circuit for the 15 bistable circuit is provided which most advantageously includes a series connected resistor 211 and 211' connected between the negative voltage bus 28 and ground, a capacitor 212 connected between resistor 211 and a resistor 214 connected to ground. A rectifier 216 is con- 20 nected between the juncture of capacitor 212 and resistor 211 and the flasher bus 193. As previously indicated, the flasher bus 193 is pulsed with positive (or ground) pulses at a visible fiashing rate. When a positive (or ground) pulse appears on the bus 193, this effectively provides a short circuit between the upper capacitor plate and ground which causes the capacitor 212 to discharge through resistor 214 providing a positive pulse thereacross. The ungrounded end of resistor 214 is connected through a rectifier 218 to the control input terminal 78 of the bistable circuit 4. The rectifier 218 blocks the positive pulses developed across the resistor 214. However, upon momentary disappearance of a positive pulse from the flasher bus 193, the capacitor 212 recharges to a negative voltage which provides a negative pulse across the resistor 35 214. This pulse passes through rectifier 218 to trigger the bistable circuit 4 provided the aforementioned control voltage fed to the other control input terminal of the bestable circuit 4 is removed by return of the field contacts 22 to their normal variable indicating position. 40 Until the latter control voltage is removed from the bistable circuit 4, the bistable circuit is effectively desensitized (i.e., incapable of being reset).

Optional lock-in operation is provided by the connection of the output terminal 199 of the bistable circuit 4' through a rectifier 213 connected to pass only positive (or ground) potential, the No. 2 position of switch 206, and the movable contact 208 to the juncture between the capacitor 212 and the rectifier 216 leading to the flasher bus 193. When the bistable circuit 4' is in a normal or reset condition, the output terminal 199 has a negative potential blocked by the rectifier 213. When the associated variable becomes abnormal, a positive (ground) potential appears at output terminal 199, which is coupled through rectifier 213 and switch 206 to the upper plate of capacitor 212 which discharges and maintains it discharged until acknowledgement, which prevents reset of the bistable 4 by the pulsations on flasher bus 193. After acknowledgement, however, the potential of output terminal 199 becomes negative again and thus has no effect on capacitor 212, so that the pulses then fed to the capacitor circuit from the flasher bus 193 are effected to generate the negative pulses across the resistor 214 which can reset the bistable circuit 4 when the associated variable returns to normal.

Refer now to FIGS. 4 and 5 showing a preferred transistor embodiment of the annunciator system shown in FIG. 3. Many of the component parts of this circuit are substantially identical to that shown in FIG. 1 and are identified by similar reference characters. For example, the input circuit 40 in FIG. 4 is identical to input circuit 2 in FIG. 1. Likewise, the bistable circuits 4 and 4' each are substantially identical to the transistor bistable circuit 4 in the embodiment of FIG. 1. Many of the interconnections of these circuits with the president and

of the annunciator systems are, however, different and these will be described in detail. The control input terminal 66 of bistable circuit 4 in FIG. 3 is the base electrode of the left hand transistor T4 and the control input terminal 78 shown therein is the base electrode of the right hand transistor T5. The rectifier 218 is connected through a current-limiting resistor 223 to the base electrode 78 and the output line 69 extends from the collector electrode of the left hand transistor T4. The control input terminal 78' of the bistable circuit 4' is the base electrode of the right hand transistor T5' and the rectifier 209 connected to the base electrode 78' is coupled through a resistor 224 to the juncture of capacitor 90 and resistor 91. A voltage dropping resistor 219' is connected between the acknowledgement bus 129 and the line leading to the base electrode 78'.

The input 180 to the "and" gate 181 is connected through a resistor 225 to the base electrode 142' of a transistor T1 forming part of a light control circuit which, except for the "and" input connections, is similar to the circuit associated with transistor T1 in FIG. 1, and the corresponding elements thereof are similarly numbered. The input 187 to the "and" gate 181 is connected through a resistor 228 to the base electrode 142' of the transistor T1. The exemplary values for resistors 225 and 228 are 82,000 ohms and 33,000 ohms, respectively. The resistance values of the rest of the circuit associated with transistor T1 may be the same as that previously indicated for the corresponding circuit in FIG. 1.

The output line 194 of the bistable circuit 4' is connected from the collector electrode of the right hand bistable transistor T5' and through a resistor 230 (of an exemplary value of 47,000 ohms) to the input 187 of "and" gate 181 at the juncture of rectifier 191 and resistor 228. The impedance relationships and circuit connections are such that the transistor T1 will be conductive unless positive or ground potential is simultaneously applied to both inputs 180 and 187.

When transistor T1 is rendered non-conductive, a high voltage transistor T2 having a load circuit including the lamp L is rendered conductive to light the lamp L. The circuit associated with transistor T2 is substantially identical to the circuit of transistor T2 in the embodiment of FIG. 1 previously described.

The control input terminal 182 of the horn control "and" gate 184 is connected through a resistor 231 to the base electrode 233 of a low voltage, low power transistor T3. This transistor T8 and associated circuit has no counterpart in the embodiment of FIG. 1 and thus will now be described in detail. The other control input terminal 189 of the "and" gate 184 is connected through a resistor 235 to the base electrode 233 of the transistor T8. The collector electrode 238 of transistor T8 is connected through a resistor 240 to the negative voltage bus 28 and through a resistor 242 and an isolating rectifier 244 arranged to couple only a negative voltage to the common horn bus 94. The emitter electrode 246 of transistor T8 is connected to the common bus line 76 leading to the biasing diode 56 physically shown in FIG. 4 below the input circuit transistor T3.

The manner in which the horn "and" gate operates is similar to light "and" gate 181. Thus, resistors 231 and 235 in relation with the other resistors connected thereto provide a normally highly conductive condition for transistor T8 when ground or positive potential is absent from either inputs terminals 187 or 189 and provides a non-conductive condition of transistor T8 when positive potential is simultaneously present at these input terminals. The non-conductive condition of transistor T8 will result in the coupling of the negative potential of the negative voltage bus to the horn bus 94.

As shown in FIG. 5, the horn bus 94 is connected through a resistor 246' to the base electrode 248 of a low voltage, low power transistor T2' forming part of an aminterconnections of these circuits with the various parts 75 pliffer circuit resembling the bistable circuits 4 and 4'

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with one of the feedback paths removed. The collector electrode 247 of transistor T2' is coupled through a feedback resistor 249 to the base electrode 250 of transistor T1' and through a resistor 251 to the negative voltage The collector electrode 252 of transistor T1' is coupled through a resistor 254 to the negative voltage bus 28. The base electrodes 248 and 250 are respectively coupled to the ground bus 34 through resistors 256 and 258. A voltage dividing resistor 261 (22,000 ohms) is connected between collector electrode 252 and the emitter 10 electrode 260 of transistor T1', the latter electrode as well as the emitter electrode 262 of transistor T2' being connected to ground bus 34 through a biasing diode 263. The values of the various resistors just described are similar to the corresponding resistors of the bistable cir- 15 cuits 4 and 4'.

When the variable goes abnormal and a negative pulse is fed to the horn bus 94 and thence to the base electrode 248 of transistor T2', the transistor T2' is rendered conductive. (Initially this transistor is non-conductive 20 and the associated transistor T1' is conductive.) When transistor T2' is rendered conductive, the transistor T1' is made non-conductive by the appearance of a near ground potential in its base electrode due to the feedback path from the collector electrode 247 of transistor T2' and 25 through resistor 249. (The initial non-conductive state of transistor T2' is due to the positive or ground potential on the horn bus when all variables are normal.) The transistor T1' is actually not necessary to the operation of the circuit and is present primarily for standardizing on a printed circuit card which may be used for a variety of different circuit arrangements as, for example, that shown in FIG. 1. As indicated in a description of FIG. 3, the provision of "and" gate circuit 184 controlling operation of the circuit makes it unnecessary to utilize a 35 bistable circuit to control the horn H.

When the manually operable acknowledgement switch 14 is depressed and the bistable circuit 4' is reset causing the closing of "and" gate 184 indicated by the conduction of transistor T8, ground potential is fed to the horn bus 40 and thence to the base electrode of transistor T2' to render the same non-conductive. The non-conductive state of transistor T2' will result in the de-energization of the horn H.

The collector electrode 247 is coupled through load 45 resistors 264 and 265 to a low voltage, low power transistor T3' forming part of a circuit 12' which is identical to the circuit 12 associated with the similarly identified transistor in FIG. 1. Thus, when the transistor T2' is initially in a non-conductive state, a negative voltage is coupled to the base electrode 142' of transistor T3' to render the same conductive. In a manner previously described, this effects a non-conductive state in the series connected high voltage power transistors T4' and T5' which prevents energization of the horn H. When the transistor T2' becomes conductive, the potential coupled to the base electrode of the transistor T3' will be near ground potential to invert the states of conduction of the transistors T3', T4' and T5' to effect energization of the horn 11.

The flasher circuit 195 is shown in FIG. 5 and it includes a pair of transistors T10 and T11 arranged to form a multivibrator circuit having a pulse repetition rate, for example, of in the order of one cycle a second. The multivibrator circuit includes a resistor 275 connected between the collector electrode of the transistor T10 and a line 277 coupled to the negative voltage bus 28 through a voltage dropping resistor 279. A resistor 281 extends from the collector electrode of the transistor T11 to the line 277. The emitter electrodes of both of 70 the transistors T10 and T11 are connected directly to the ground bus 34. The base electrode of the transistor T10 is coupled through a resistor 284 to the line 277 and the base electrode of transistor T11 is connected through a resistor 286 to the line 277. A capacitor 287 is cou- 75 circuit 4'. 14

pled between the collector electrode of transistor T10 and the base electrode of transistor T11. Similarly, a capacitor 288 is coupled from the collector electrode of the transistor T11 to the base electrode of transistor T10. The capacitors 288 and 287 in conjunction with associated resistors form timing networks which establish the pulse repetition rate of the multivibrator circuit.

The output of the multivibrator circuit is taken from the collector electrode of the transistor T10. A resistor 290 is accordingly coupled between the collector electrode of transistor T10 and the base electrode of a transistor T9. A resistor 292 is connected between the base electrode of the transistor T9 and the ground bus 34. biasing resistor 294 is connected between the line 277 and the emitter electrode of transistor T9. A biasing diode 296 is connected between the emitter electrode of the latter transistor and the ground bus 34. The voltage at the collector electrode of the multivibrator transistor T10 varies between ground and negative potential. It is apparent that when this potential is at ground, the transistor T9 whose base electrode receives biasing voltage from the collector electrode of transistor T10 will be in a non-conductive state. When the voltage coupled from the latter collector electrode is negative, this will result in the conduction of transistor T9 whose load circuit extends to the aforementioned flasher bus 193. The flasher bus, in turn, as above indicated extends through the various control circuits of the annunciator system to the negative voltage bus 28.

The flexibility of the annunciator system of FIGS. 3 through 5 is so substantial that it may readily be converted to an annunciator system providing an optional manual reset. As above indicated, a manual reset type of operation is one wherein a visual indication is maintained on the lamp L even after acknowledgement until depression of a manually operable reset switch. Refer now to FIG. 7 which illustrates a minor modification of the circuit of FIGS. 3 through 5 necessary to provide not only a selection of lock-in and non-lock-in operation as the latter circuit but also a selection of manual reset and automatic reset operation. This modification includes the addition of a common reset bus 300 connected through a normally open reset pushbutton switch 16 to the negative voltage bus 28. The only additional change required is the addition of a manual reset select switch 302 having two ganged levels 302a and 302b. The switch level 302a has a movable contact 304 connected to the upper terminal of the capacitor 212 associated with the reset input terminal 78 of the bistable circuit 4. The movable contact is adapted to make selective contact with two stationary contacts Nos. 1 and 2. The contact No. 1 is connected to the flasher bus 193 and is engaged by the movable contact 304 during automatic reset operation of the circuit. In such case, the annunciator circuit operates identical to that described in connection with the annunciator system of FIGS. 3 through 5. When the movable contact 304 is connected to stationary contact No. 2, the circuit is adjusted for manual reset operation wherein the flasher circuit is decoupled from the capacitor 212 and the associated circuit.

The second switch level 302b is interposed between the resistor 211 and the negative voltage bus 28 and the reset bus 300. The second level 302b has movable contact 306 engagable with stationary contacts Nos. 1 and 2. For manual reset operation, movable contact 306 makes engagement with contact No. 2 which in turn is connected to the reset bus 300. Contact No. 1 is connected to the negative voltage bus 28 so that when the movable contact 306 connects with this terminal the operation of the system is identical to that previously described in connection with the annunciator system of FIGS. 3 through 5. During manual reset operation, the lock-in control switch 206 must be connected to its contact No. 2 which extends through the rectifier 213 to the output 199 of the bistable

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It will be recalled that reset of the first bistable circuit 4 requires first of all that the associated variable return to normal and that a reset signal be fed to the control terminal 78 thereof. This reset signal in the exemplary circuit described is a negative pulse. When the manual reset switch 302 is in the position No. 2 as illustrated and the switch 206 is also in position for lock-in operation, a negative pulse can be generated by momentarily operating the manual reset switch 16 to couple the negative potential of the negative bus 28 through resistor 211 to the capacitor 212. Prior to acknowledgement, it will be recalled that the voltage at the output 199 of the bistable circuit 4' is at ground or a relatively positive potential. This potential is coupled through rectifier 213 and the switch 206 to the upper plate of the capacitor 212 to 15 discharge and maintain discharged the capacitor 212. The discharge of the capacitor 212, as previously indicated, will result in the generation of the positive pulse which has no effect on the bistable circuit 4 due to the blocking effect of rectifier 218. After acknowledgement, however, the potential at the output 199 of the bistable circuit 4' becomes negative, which negative potential is blocked by the rectifier 213. Then, operation of manual reset switch 16 will be effective to couple the negative voltage to the capacitor 212 to effect the charging thereof, resulting in generation of a negative pulse which resets the bistable circuit 4.

The various aspects of applicant's invention have thus provided a highly unique and advantageous selection of standard annunciator systems. Most preferably, the 30 static annunciator systems are transistorized systems capable of operating from a relatively high direct current voltage despite the low voltage ratings of the transistors. Moreover, due to the particular circuit logic involved and the circuit connections for carrying out this logic, an 35 extremely flexible and reliable static annunciator results, even in the presence of fairly substantial distributed capacitances in the line connecting the various field contacts to their associated control circuits.

It should be understood that numerous modifications 40 may be made of the various specific forms of the invention disclosed without deviating from the broader aspects of the invention.

What I claim as new and desire to protect by Letters Patent of the United States is:

1. In an annunciator circuit for monitoring a number of variables and including for each variable alarm means for providing an alert indication, and variable responsive means having normal and abnormal conditions when the associated variable is respectively normal and abnormal, 50 the improvement comprising a separate control circuit responsive to each variable responsive means, means for controlling the associated alarm means, each control circuit including: a first bistable circuit having a first input terminal for receiving a control voltage of a given polarity 55 for setting the bistable circuit and a second input terminal for receiving a control voltage of a given polarity which resets the bistable circuit, means responsive to the setting and resetting of said bistable circuit for respectively energizing and de-energizing said alarm means, a source of 60 said control voltage for setting such first bistable circuit, means connecting said source of control voltage continuously to said first input terminal when the condition responsive means is in its abnormal condition, and a series circuit of a capacitor and a resistor connected across a 65 source of direct current voltage, and means coupling the voltage developed across said resistor means to said second input of said bistable circuit and including rectifier means limiting the voltage coupled thereto a polarity which will reset the bistable control circuit; and a common 70 pulse bus and means for continuously pulsating said pulse bus with a voltage of a polarity which will discharge said capacitor in each control circuit, each of said capacitors normally recharging in the intervals between said pulses

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sistor of a polarity to pass through said associated rectifier means and reset the associated first bistable circuit if it is set, when the control voltage applied to the first input terminal thereof is removed.

2. In an annunciator circuit for monitoring a number of variables and including for each variable alarm means for providing an alert indication, variable responsive means having normal and abnormal conditions when the associated variable is respectively normal and abnormal, and manually operable reset switch means, the improvement comprising a separate control circuit responsive to each variable responsive means and said reset switch means for controlling the associated alarm means, each control circuit including: a first bistable circuit having a first input terminal for receiving a control voltage of a given polarity for setting the bistable circuit and a second input terminal for receiving a control voltage of a given polarity which resets the bistable circuit, means responsive to the setting and resetting of said bistable circuit for respectively energizing and de-energizing said alarm means, a source of said control voltage for setting such first bistable circuit, means connecting said source of control voltage continuously to said first input terminal when the condition responsive means is in its abnormal condition, and a series circuit of a capacitor and a resistor connected across a source of direct current voltage, means coupling the voltage developed across said resistor means to said second input of said bistable circuit and including rectifier means limiting the voltage coupled thereto a polarity which will reset the bistable control circuit, a common pulse bus and means for continuously pulsating said pulse bus with a voltage of a polarity which will discharge said capacitor in each control circuit, each of said capacitors normally recharging in the intervals between said pulses and the charge current generating pulses across said resistor of a polarity to pass through said associated rectifier means and reset the associated first bistable circuit if it is set, when the control voltage applied to the first input terminal thereof is removed, each control circuit further including a second bistable circuit having input terminal means for setting and resetting the same and a reset inhibit output connected to said capacitor in the associated control circuit for keeping the same discharged when the second bistable circuit is set and allowing the charge and discharge thereof when the second bistable circuit is reset, and a common bus connected through said manually operable reset switch means to a source of reset voltage for said second bistable circuits and feeding said reset voltage to the second bistable circuits of said control circuits to reset the same when the latter switch means is operated.

3. In an annunciator circuit for monitoring a number of variables and including for each variable alarm means for providing an alert indication, variable responsive means having normal and abnormal conditions when the associated variable is respectively normal and abnormal, and manually operable reset switch means, the improvement comprising a separate control circuit responsive to each variable responsive means and said reset switch means for controlling the associated alarm means, each control circuit including: a first bistable circuit having a first input terminal for receiving a control voltage of a given polarity for setting the bistable circuit and a second input terminal for receiving a control voltage of a given polarity which resets the bistable circuit, means responsive to the setting and resetting of said bistable circuit for respectively energizing and de-energizing said alarm means, a source of said control voltage for setting such first bistable circuit, means connecting said source of control voltage continuously to said first input terminal when the condition responsive means is in its abnormal condition, a series circuit of a capacitor and a resistor connected across a source of direct current voltage, means coupling and the charge current generating pulses across said re- 75 the voltage developed across said resistor means to said

second input of said bistable circuit and including rectifier means limiting the voltage coupled thereto a polarity which will reset the bistable control circuit; a common pulse bus and means for continuously pulsating said pulse bus with a voltage of a polarity which will discharge said capacitor in each control circuit, each of said capacitors normally recharging in the intervals between said pulses and the charge current generating pulses across said resistor of a polarity to pass through said associated rectifier means and reset the associated first bistable circuit 10 if it is set, when the control voltage applied to the first input terminal thereof is removed; each control circuit further including a second bistable circuit having input terminal means for setting and resetting the same and a reset inhibit output connected to said capacitor in the 15 associated control circuit for keeping the same discharged when the second bistable circuit is set and allowing the charge and discharge thereof when the second bistable circuit is reset; a lock-in select switch for selectively coupling and uncoupling the reset inhibit output of said second bistable circuit to and from said capacitor to provide lock-in or non-lock-in operation; and a common bus connected through said manually operable reset switch means to a source of reset voltage for said second bistable circuits and feeding said reset voltage to the second bistable 25 circuits of said control circuits to reset the same when the latter switch means is operated.

4. In an annunciator circuit including visual alarm means, variable responsive means having normal and abnormal conditions when the associated variable is respectively normal and abnormal, a source of high direct current voltage, and manually operable acknowledgment switch means, the improvement comprising: a bistable transistor control circuit responsive to said variable responsive means by providing one output condition when 35 the associated variable is normal and another output condition when the associated variable is abnormal, a second control circuit responsive to the output conditions of said bistable control circuit for controlling the energization of said alarm means, said bistable control circuit comprising: a pair of relatively low voltage transistor elements, said second control circuit comprising at least one relatively high voltage transistor element, each of said transistor elements having control and load terminals and designed for operation with an applied voltage which is less 45 than the value of the output of said source of direct current voltage, load resistor means connected in series between one of the load terminals of each of said low voltage transistor elements of said bistable control circuit and said source of direct current voltage, feedback resistor 50 means connected between the load terminal of each of said low voltage transistor control elements nearest said load resistor means and the control terminal of the other of same, control circuit resistor means connected between the control terminal of each of said low voltage transistor 55 control element and the terminal of said source of direct current voltage which is remote from said load resistor means, each of said load resistor means and the associated feedback and control circuit resistor means providing a voltage divider network to supply the proper relative low 60 voltage conditions across the load terminals of the associated low current transistor element, means connecting said alarm light means in series between one of the load terminals of the high voltage transistor element and said source of direct current voltage, shunt resistor means connected between the load terminals of said high voltage transistor element and providing in conjunction with said alarm light means the proper relative low voltage conditions across the load terminals of said high voltage transistor element and a dim light indication when the associated variable is normal, means responsive to the output condition of said bistable control circuit indicating an abnormal variable for periodically feeding at a

said high voltage transistor element for effecting periodically a high conductive condition thereof to provide a flashing light indication on said alarm light means, and means responsive to momentary operation of said manually operable acknowledgement means for providing steady voltage conditions on the control terminal of the high voltage transistor element for continuously providing a high conductive state therein to provide a steady light indication on the associated alarm light means.

5. In an annunciator system for monitoring the condition of a number of variables, said system including visual alarm means and variable responsive means for each variable having normal and abnormal conditions when the associated variable is respectively normal and abnormal, a common audible alarm means, a common source of signal pulses occurring at a visible flashing rate, and commonly manually-operable acknowledgement switch means, the improvement comprising an electrical control circuit for each variable responsive to the associated variable responsive means and said common acknowledgement switch means for controlling said visual and audible alarm means, each control circuit comprising a first bistable unit having two states of operation, a second bistable unit having two states of operation, a first output controlled by said second bistable unit and at which a gate-opening signal continuously appears only as long as the bistable unit is in one of its states of operation and a second output controlled by said second bistable unit at which a gate-opening signal continuously appears only as long as said second bistable unit is in its other state of operation, a first "and" gate having first and second control inputs for energizing the associated visual alarm means when gate-opening signals are simultaneously fed thereto, said pulses from said common source of pulses being operable as gate-opening pulses for said first "and" gate, a second "and" gate having a first and second control input for energizing said common audible alarm means when gate-opening signals are simultaneously fed thereto, means responsive to the operation of the associated variable responsive means for feeding a set signal to said first bistable unit which signal sets the same, means into one of its states of operation for continuously feeding a gate-opening signal to the second control input of said first and second "and" gates only as long as said first bistable unit remains set, means coupling the gate-opening signal at said first output controlled by said second bistable unit to the first control input initially to energize said common audible alarm means, a double "or" input connection coupled to the first control input means of said first "and" gate and including a first input section extending from said common source of signal pulses which provide gate-opening signals at a visible flashing rate, to effect the visible flashing of said visual alarm means when said first bistable unit is initially set, and a second input section extending from said second output controlled by said second bistable unit which provides a continuous gate-opening signal when the latter bistable unit is in said one operating state, to provide a steady light indication on said visual alarm means after acknowledgement. means responsive to the operation of said manually operable acknowledgement means for operating said second bistable unit from said other to said one operating state whereby to provide a steady light indication on said visual alarm means and to silence said audible alarm means as the gate-opening signals disappear from said first output controlled by said second bistable unit, and means for resetting the first bistable unit after the associated variable responsive means returns to its normal condition.

transistor element and a dim light indication when the associated variable is normal, means responsive to the output condition of said bistable control circuit indicating an abnormal variable for periodically feeding at a visible flashing rate a voltage to the control terminal of 75 associated variable is respectively normal and abnormal,

and manually operable reset switch means, the improvement comprising a separate control circuit responsive to each variable responsive means and said reset switch means for controlling the associated alarm means, each control circuit including: a first bistable circuit having 5 a first input terminal for receiving a control voltage of a given polarity for setting the bistable circuit and a second input terminal for receiving a control voltage of a given polarity which resets the bistable circuit, means responsive to the setting and resetting of said bistable cir- 10 cuit for respectively energizing and de-energizing said alarm means, a source of said control voltage for setting such first bistable circuit, means connecting said source of control voltage continuously to said first input terminal when the condition responsive means is in its abnormal 15 condition, and a series circuit of a capacitor and a resistor connected across a source of direct current voltage, means coupling the voltage developed across said resistor means to said second input of said bistable circuit and including rectifier means limiting the voltage coupled thereto 20 to a polarity which will reset the bistable control circuit, a common pulse bus and means for continuously pulsating said pulse bus with a voltage of a polarity which will discharge said capacitor in each control circuit, each of said capacitors normally recharging in the intervals 25 edgement switch means. between said pulses and the charge current generating pulses across said resistor of a polarity to pass through said associated rectifier means and reset the associated first bistable circuit if it is set when the control voltage applied to the first input terminal thereof is removed; and 30 each control circuit further including lock-in control means connected to said capacitor for keeping said capacitor discharged until operation of said reset switch means, whereupon the capacitor is free to charge and discharge until the associated variable returns to normal 35 and then becomes abnormal again.

7. In an annunciator system for monitoring the condition of a number of variables, said system including visual alarm means and variable responsive means for each variable, having abnormal and normal conditions 40 when the associated variable is respectively normal and abnormal, a common source of signal pulses occurring at a visible flashing rate, and common manually operable acknowledgement switch means, the improvement comprising an electrical control circuit for each variable re- 45 sponsive to the associated variable responsive means and said common acknowledgement switch means for controlling said visual alarm means, each control circuit comprising: a first bistable unit having separate set and reset control input means, a second bistable unit having 50 control input means for setting and resetting the same, a first output at which a gate-opening signal continuously appears only as long as the bistable unit is set, a second output at which a reset inhibit signal continuously appears only as long as said second bistable unit is reset, a first "and" gate having first and second control inputs for energizing the associated visual alarm means when gate-opening signals are simultaneously fed thereto, said pulses from said common source of pulses acting as gate-opening pulses, said first control means responsive 60 to the operation of the associated variable responsive means for feeding a continuous set signal to the set control input means of said first bistable unit which signal sets the same and prevents resetting thereof until removal of the set signal from the latter input means, 65 means responsive to the setting of said first bistable unit for momentarily feeding a set pulse to the second bistable unit for setting the same and for continuously feeding a gate-opening to the second control input of said first set, a double "or" input connection coupled to the first control input means of said first "and" gate and including a first input section extending from said common source of signal pulses which provide gate-opening signals at

visual alarm means when said first bistable unit is initially set, and a second input section extending from said second output of said second bistable unit which provides a continuous gate-opening signal when the latter bistable unit is reset, to provide a steady light indication on said visual alarm means after acknowledgement, means responsive to the operation of said manually operable acknowledgement means for feeding a reset signal to said second bistable unit to reset the same whereby to provide a steady light indication on said visual alarm means as the gate-opening signals disappear from said first output of said second bistable unit, a reset circuit for said first bistable unit coupled to the reset control input means of said first bistable unit, said reset circuit being coupled to said common source of pulses which act as reset pulses which normally continuously prepare said first bistable unit for a reset operation which is effected when the associated variable returns to normal, and means connecting said second output of said second bistable unit to which said reset inhibit signal appears when the bistable unit is set, for inhibiting the coupling of the latter reset pulses to the reset control input means of said first bistable unit, to provide lock-in operation until the second bistable circuit is reset by said acknowl-

8. In an annunciator system for monitoring the condition of a number of variables, said system including visual alarm means and variable responsive means for each variable having abnormal and normal conditions when the associated varible is respectively normal and abnormal, a common source of signal pulses occurring at a visible flashing rate, and a common manually operable acknowledgement switch means, the improvement comprising an electrical control circuit for each variable responsive to the associated variable responsive means and said common acknowledgement switch means for controlling said visual alarm means, each control circuit comprising: a first bistable unit having separate set and reset control input means, a second bistable unit having control input means for setting and resetting the same, a first output at which a gate-opening signal continuously appears only as long as the bistable unit is set, a second output at which a reset inhibit signal continuously appears only as long as said second bistable unit is reset, a first "and" gate having first and second control inputs for energizing the associated visual alarm means when gate-opening signals are simultaneously fed thereto, said pulses from said common source of pulses acting as gate-opening pulses, said first control means responsive to the operation of the associated variable responsive means for feeding a continuous set signal to the set control input means of said first bistable unit which signal sets the same and prevents resetting thereof until removal of the set signal from the latter input means, means responsive to the setting of said first bistable unit for momentarily feeding a set pulse to the second bistable unit for setting the same and for continuously feeding a gate-opening to the second control input of said first "and" gates as long as said first bistable unit remains set, a double "or" input connection coupled to the first control input means of said first "and" gate and including a first input section extending from said common source of signal pulses which provide gate-opening signals at a visible flashing rate, to effect the visible flashing of said visual alarm means when said first bistable unit is initially set, and a second input section extending from said second output of said second bistable unit which provides a continuous gate-opening signal when the latter bistable unit is reset, to provide a steady light "and" gates as long as said first bistable unit remains 70 indication on said visual alarm means after acknowledgement, means responsive to the operation of said manually operable acknowledgement means for feeding a reset signal to said second bistable unit to reset the same whereby to provide a steady light indication on said a visible flashing rate, to effect the visible flashing of said 75 visual alarm means as the gate-opening signals disappear

from said first output of said second bistable unit, a reset circuit for said first bistable unit coupled to the reset control input means of said first bistable unit, said reset circuit being coupled to said common source of pulses which act as reset pulses which normally continuously prepare said first bistable unit for a reset operation which is effected when the associated variable returns to normal, means connecting said second output of said second bistable unit to which said reset inhibit signal appears when the bistable unit is set, for inhibiting the coupling of the latter reset pulses to the reset control input means of said first bistable unit, to provide lock-in operation until the second bistable circuit is reset by said acknowledgement switch means, and manually operable switch means for selectively connecting and disconnecting the

second output of said second bistable unit to provide selectively for lock-in or non-lock-in operation.

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