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(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: MULTIPLEXED AMPLIFIER WITH REDUCED GLITCHING

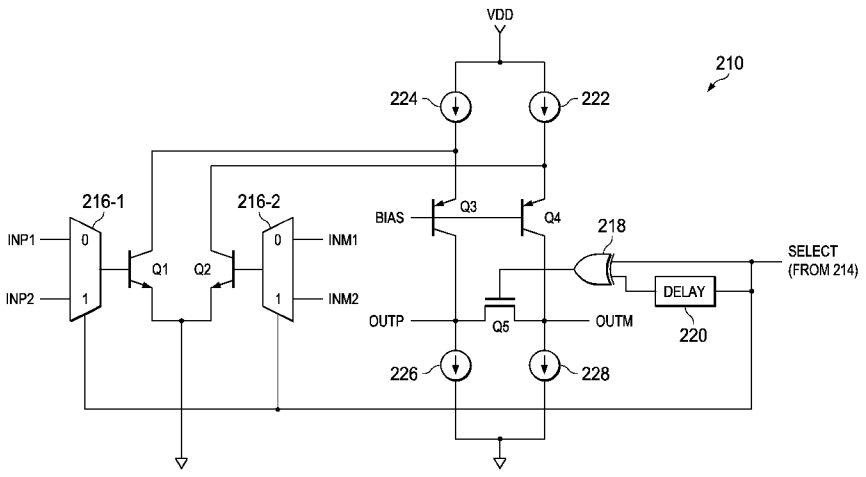

FIG. 2C

(57) Abstract: A first multiplexer (216-1) is coupled to a first input terminal (INP1/INP2) and a second multiplexer (216-2) is coupled to a second input terminal (INM1/INM2) of a folded cascode differential amplifier (210) which includes transistors (Q1 through Q4) and current sources (222-228). Switching between differential input signals (INP1/INM1) and (INP2/INM2) is controlled through a select signal SELECT provided by a controller (214). A reset mechanism includes a switch (Q5) coupled between output terminals (OUTP, OUTM) of amplifier (210) and controlled by a pulse generator (XOR gate 218 and delay circuit 220). On a rising or falling edge of the select signal SELECT, a pulse is provided to activate the switch (Q5) so as to briefly short the output terminals (OUTP, OUTM). This avoids glitching and results in faster settling times.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

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MULTIPLEXED AMPLIFIER WITH REDUCED GLITCHING

[0001] The invention relates generally to amplifiers and, more particularly, to residue amplifiers.

BACKGROUND

[0002] Referring to FIG. 1A of the drawings, reference numeral 100 generally designates a conventional analog-to-digital converter (ADC) 100. ADC 100 generally comprises several stages 102-1 to 102-N, an ADC 106 (which is typically a flash ADC), and a digital output circuit 104. The stages 102-1 to 102-N are generally coupled in series with one another in a sequence, where the first stage 102-1 receives the analog input signal and where each of the subsequent stages 102-2 to 102-N receives a residue signal from the previous stage 102-1 to 102-(N-1), respectively. ADC 106 is coupled to the last stage 102-N (receiving its residue signal). Based on its input signal (either a residue signal or the analog input signal), stages 102-1 to 102-N and ADC 106 are able to resolve a portion of the analog input signal, which is provided to digital output circuit 104. Digital output circuit 104 can then perform error correction or other digital processing to generate the digital output signal DOUT.

[0003] Turning now to FIGS. 1B and 1C, stages 102-1 to 102-N can be seen in greater detail (which are referred to hereinafter as stage 102 for the sake of simplicity). Stage 102 generally comprises a track-and-hold (T/H) circuit 108 (i.e., T/H amplifier), ADC 110, digital-to-analog converter (DAC) 112, adder 114, and a residue amplifier 116. In operation, the T/H circuit 110 enters a track phase T during the logic high state of the clock signal CLK and a hold phase H during the logic low state of the clock signal CLK. During the track phase T, the T/H circuit samples its analog input signal SIN (which may be the analog input signal AIN or the residue signal from the previous stage). During the hold phase H, the sampled signal is provided to ADC 110 and adder 114. The ADC 110 resolves a portion of the signal SIN, providing the resolved bits to digital output circuit 104 and DAC 112. DAC 112 converts the resolved bits to an analog signal which is provided to adder 114. Adder 114 determines the difference between the sampled signal and the analog signal from DAC, which is amplified by amplifier 116 and output as a residue signal ROUT.

[0004] There are some drawbacks to ADC 100. In particular, the residue amplifiers 116 for each stage 102-1 to 102-N are operating at less than 50% duty cycle, which consumes an excess amount of power. Therefore, it is desirable to have a reside amplifier that consumes less power.

[0005] Some examples of other conventions circuits are given in U.S. Patent Nos. 3,877,023; 5,180,932; 6,218,887; and 6,489,845.

SUMMARY

[0006] An example embodiment of the invention, accordingly, provides an apparatus. The apparatus comprises an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second input terminal; a first multiplexer that is coupled to the first input terminal of the amplifier; a second multiplexer that is coupled to the second input terminal of the amplifier; a switch that is coupled between the first and second output terminals of the amplifier; a pulse generator that is coupled to the switch so as to control the switch; and a controller that is coupled to the first multiplexer, the second multiplexer, and pulse generator, wherein the controller provides a select signal to each of the first and second multiplexers, and wherein the controller activates the pulse generator when the first and second multiplexers are switched.

[0007] In accordance with an example embodiment of the invention, the pulse generator further comprises: a logic circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch; and a delay circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch.

[0008] In accordance with an example embodiment of the invention, the logic circuit further comprises a XOR gate.

[0009] In accordance with an example embodiment of the invention, the amplifier further comprises: a first transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the first transistor is coupled to the first multiplexer; a second transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the second transistor is coupled to the second multiplexer, and wherein the first passive electrode of the second transistor is coupled to the first passive electrode of the first transistor; a first current source that is coupled to the second passive electrode of the first transistor; a second current source that is coupled to the second passive

electrode of the second transistor; a first bias transistor that is coupled between the first currents source and the first output terminal; and a second bias transistor that is coupled between the second current source and the second output terminal.

[0010] In accordance with an example embodiment of the invention, the first and second transistors are NPN transistors.

[0011] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises data converter circuitry; a first multiplexer that is coupled to the data converter circuitry; a second multiplexer that is coupled to the data converter circuitry; an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second input terminal, wherein the first multiplexer that is coupled to the first input terminal of the amplifier, and wherein the second multiplexer that is coupled to the second input terminal of the amplifier; a switch that is coupled between the first and second output terminals of the amplifier; a pulse generator that is coupled to the switch so as to control the switch; and a controller that is coupled to the first multiplexer, the second multiplexer, and pulse generator, wherein the controller provides a select signal to each of the first and second multiplexers, and wherein the controller activates the pulse generator when the first and second multiplexers are switched.

[0012] In accordance with an example embodiment of the invention, the data converter circuitry further comprises: a first track-and-hold (T/H) circuit; a second T/H circuit; a first analog-to-digital converter (ADC) that is coupled to the first T/H circuit; a second ADC that is coupled to the second T/H circuit; a first digital-to-analog converter (DAC) that is coupled to the first ADC; a second DAC that is coupled to the second ADC; a first adder that is coupled to the first DAC, the first T/H circuit, and the first multiplexer, wherein the first adder determines the difference between the outputs of the first T/H circuit and the first DAC; and a second adder that is coupled to the second DAC, the second T/H circuit, and the second multiplexer, wherein the second adder determines the difference between the outputs of the second T/H circuit and the second DAC.

[0013] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a plurality of stages that are coupled in series with one another in a sequence, wherein each stage receives an analog input signal or a residue signal from the previous stage, and wherein each stage includes: data converter circuitry; a first

multiplexer that is coupled to the data converter circuitry; a second multiplexer that is coupled to the data converter circuitry; an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second input terminal, wherein the first multiplexer that is coupled to the first input terminal of the amplifier, and wherein the second multiplexer that is coupled to the second input terminal of the amplifier; a switch that is coupled between the first and second output terminals of the amplifier; a pulse generator that is coupled to the switch so as to control the switch; and a controller that is coupled to the first multiplexer, the second multiplexer, and pulse generator, wherein the controller provides a select signal to each of the first and second multiplexers, and wherein the controller activates the pulse generator when the first and second multiplexers are switched; an ADC that is coupled to the last stage of the sequence; and a digital output circuit that is coupled to the ADC and the data converter circuit for each stage.

[0014] The foregoing has outlined rather broadly the features and technical advantages of the invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Example embodiments are described with reference to accompanying drawings, wherein:

[0016] FIGS. 1A and 1B are circuit diagrams for an example of a conventional ADC;

[0017] FIG. 1C is a timing diagram for the ADC of FIGS. 1A and 1B;

[0018] FIGS. 2A and 2B are circuit diagrams for an example of an ADC in accordance with an example embodiment of the invention; and

[0019] FIG. 2C is a circuit diagram of an example of a residue amplifier of FIG. 2B.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] FIG. 2A illustrates an example ADC 200 in accordance with principles of the invention. ADC 200 has the same general functionality as ADC 100. However, a difference

exists in the pipeline; namely, stages 102-1 to 102-N have been replaced by stages 202-1 to 202-N.

[0021] In FIG. 2B, stages 202-1 to 203-N (hereinafter 202) can be seen in greater detail. In operation, T/H circuit 203-1 and 203-2 are coupled to receive an analog input signal IN (which is either the analog input signal AIN or a residue signal from the previous stage). Since these T/H circuits 203-1 and 203-2 are arranged in parallel with one another, T/H circuits 203-1 and 203-2 can be timed so as to sample on generally non-overlapping logic stages or phases of a clock signal. T/H circuits 203-1 and 203-2 are respectively coupled to ADC 204-1 and 204-2, and ADCs 204-1 and 204-2, DACs 206-1 and 206-2, adders 208-1 and 208-2, and residue amplifier 210 can then perform analog processing to resolve sampled signals for digital output circuit 104 and to generate a residue signal ROUT.

[0022] Here, each of the data converter circuits (which respectively include ADCs 204-1 or 204-2, DAC 206-1 or 206-2, and adder 208-1 or 208-2) benefit from the use of a single amplifier. A reason is that duty cycle of an amplifier (for each data converter circuit) would be less than 50%, which would consume an excessive amount of power. Therefore, amplifier 210 can be time multiplexed by controller 214 to process signals from each of the data converter circuits or data paths.

[0023] Turning to FIG. 2C, residue amplifier 210 can be seen in greater detail. In this example, a folded cascode differential amplifier (which generally comprises NPN transistors Q1 through Q4 and current sources 222, 224, 226, and 228) that is biased by a bias voltage BIAS is employed. Coupled to the input terminals of this amplifier are multiplexers 216-1 and 216-2. The switching between differential input signals INP1/INM1 and INP2/INM2 (which are provided by adders 208-1 and 208-2, respectively) are controlled through the select signal SELECT (which is provided by the controller 214). Additionally, multiplexers (not shown) that are coupled to the output terminals of this amplifier (so as to receive output signals OUTP and OUTM) to direct the correct input and output signals to the amplifier at the correct instants in time for processing.

[0024] When multiplexers 216-1 and 216-2 are switched, however, the amplifier (which generally comprises NPN transistors Q1 through Q4 and current sources 222, 224, 226, and 228) exhibits erratic behavior at the switching instant. This erratic behavior is referred to as a glitch, and if not addressed, the glitch can consume significant amounts of the amplifier's available

settling time or even lead to the amplifier output or interior nodes operating at voltages outside their desired ranges. In other words, this glitch can degrade performance. To combat this problem, a reset mechanism is provided at the output terminals of the amplifier. The resent mechanism generally comprises a switch Q5 that is coupled between the output terminals of the amplifier and controlled by a pulse generator (which generally comprises an XOR gate and a delay circuit). Thus, on a rising or falling edge of the select signal SELECT, a pulse is provided to switch Q5 (which activates the switch Q5) so as to briefly short the output terminals of the amplifier together. Thus, glitching can be avoided, which results in faster settling times.

[0025] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments and other embodiments implemented within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second input terminal;

a first multiplexer that is coupled to the first input terminal of the amplifier;

a second multiplexer that is coupled to the second input terminal of the amplifier;

a switch that is coupled between the first and second output terminals of the amplifier;

a pulse generator that is coupled to the switch so as to control the switch; and

a controller that is coupled to the first multiplexer, the second multiplexer, and pulse generator, wherein the controller provides a select signal to each of the first and second multiplexers, and wherein the controller activates the pulse generator when the first and second multiplexers are switched.

2. The apparatus of Claim 1, wherein the pulse generator further comprises:

a logic circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch; and

a delay circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch.

3. The apparatus of Claim 2, wherein the logic circuit further comprises a XOR gate.

4. The apparatus of Claim 3, wherein the amplifier further comprises:

a first transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the first transistor is coupled to the first multiplexer;

a second transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the second transistor is coupled to the second multiplexer, and wherein the first passive electrode of the second transistor is coupled to the first passive electrode of the first transistor;

a first current source that is coupled to the second passive electrode of the first transistor;

a second current source that is coupled to the second passive electrode of the second transistor;

a first bias transistor that is coupled between the first currents source and the first output terminal; and

a second bias transistor that is coupled between the second current source and the second output terminal.

5. The apparatus of Claim 4, wherein the first and second transistors are NPN transistors.

6. An apparatus comprising:

data converter circuitry;

a first multiplexer that is coupled to the data converter circuitry;

a second multiplexer that is coupled to the data converter circuitry;

an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second input terminal, wherein the first multiplexer that is coupled to the first input terminal of the amplifier, and wherein the second multiplexer that is coupled to the second input terminal of the amplifier;

a switch that is coupled between the first and second output terminals of the amplifier;

a pulse generator that is coupled to the switch so as to control the switch; and

a controller that is coupled to the first multiplexer, the second multiplexer, and pulse generator, wherein the controller provides a select signal to each of the first and second multiplexers, and wherein the controller activates the pulse generator when the first and second multiplexers are switched.

7. The apparatus of Claim 6, wherein the pulse generator further comprises:

a logic circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch; and

a delay circuit that is coupled to the controller so as to receive the select signal and that is coupled to the switch.

8. The apparatus of Claim 7, wherein the logic circuit further comprises a XOR gate.

9. The apparatus of Claim 8, wherein the amplifier further comprises:

a first transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the first transistor is coupled to the first multiplexer;

a second transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the control electrode of the second transistor is coupled to the second multiplexer, and wherein the first passive electrode of the second transistor is coupled to the first passive electrode of the first transistor;

a first current source that is coupled to the second passive electrode of the first transistor;

a second current source that is coupled to the second passive electrode of the second transistor;

a first bias transistor that is coupled between the first currents source and the first output terminal; and

a second bias transistor that is coupled between the second current source and the second output terminal.

10. The apparatus of Claim 9, wherein the first and second transistors are NPN transistors.

11. The apparatus of Claim 8, wherein the data converter circuitry further comprises:

a first track-and-hold (T/H) circuit;

a second T/H circuit;

a first analog-to-digital converter (ADC) that is coupled to the first T/H circuit;

a second ADC that is coupled to the second T/H circuit;

a first digital-to-analog converter (DAC) that is coupled to the first ADC;

a second DAC that is coupled to the second ADC;

a first adder that is coupled to the first DAC, the first T/H circuit, and the first multiplexer, wherein the first adder determines the difference between the outputs of the first T/H circuit and the first DAC; and

a second adder that is coupled to the second DAC, the second T/H circuit, and the second multiplexer, wherein the second adder determines the difference between the outputs of the second T/H circuit and the second DAC.

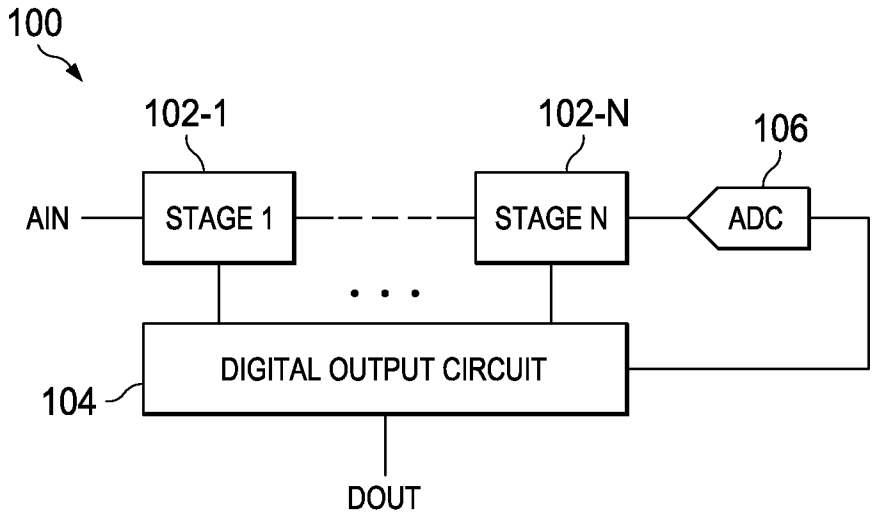

FIG. 1A
(PRIOR ART)

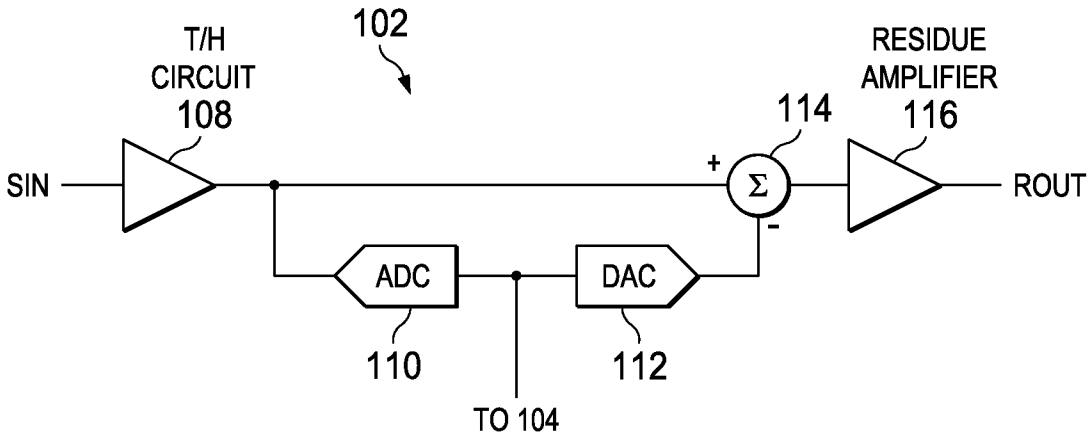

FIG. 1B
(PRIOR ART)

FIG. 1C
(PRIOR ART)

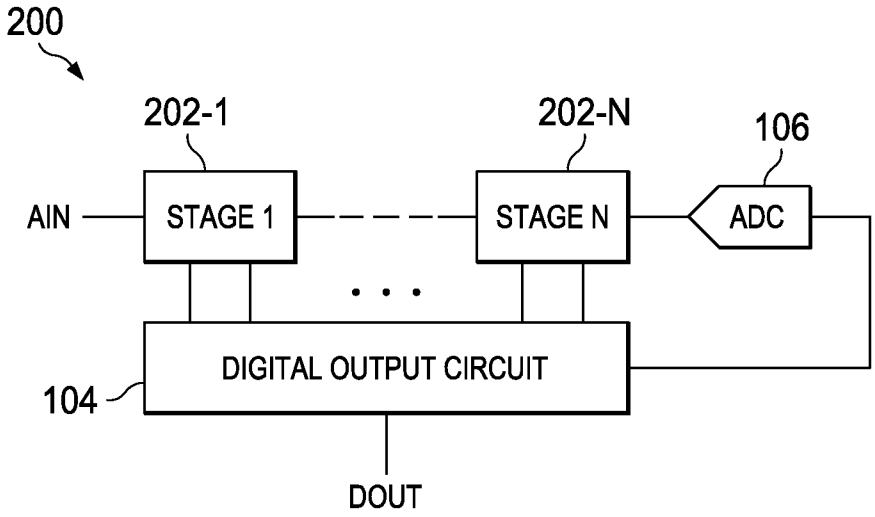
200
202-1
202-N
106
AIN
STAGE 1
STAGE N
ADC
DIGITAL OUTPUT CIRCUIT
104
DOUT

FIG. 2A

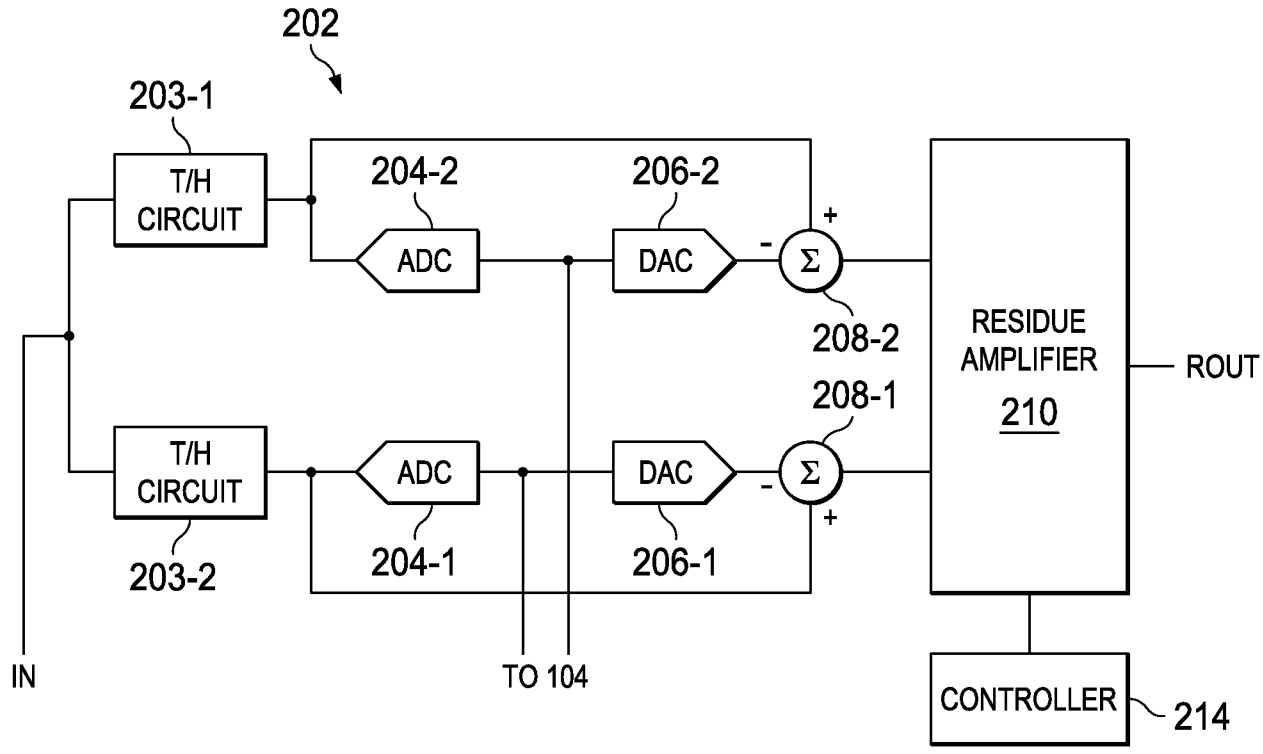
202
203-1
T/H CIRCUIT
204-2
206-2
ADC
DAC
Σ
208-2
208-1
RESIDUE AMPLIFIER
210
ROUT
T/H CIRCUIT
ADC
DAC
Σ
203-2
204-1
206-1
IN
TO 104
CONTROLLER
214

FIG. 2B

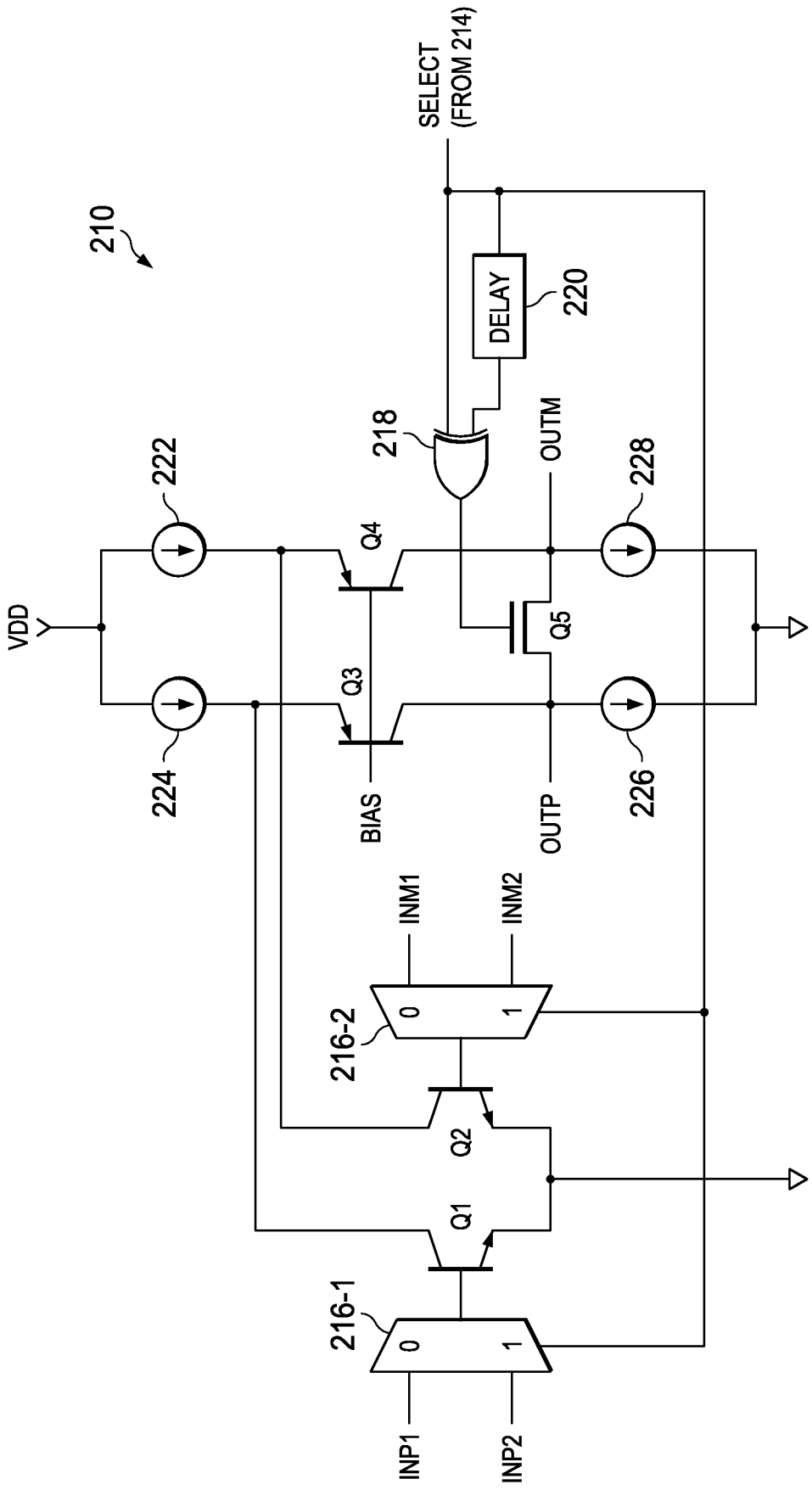
SELECT
(FROM 214)
210
DELAY
220
218
OUTM
222
228
Q4
VDD
Q5
Q3
224
226
BIAS
OUTP
INM1
INM2
216-2
0
1
Q2
Q1
216-1
0
1
INP1
INP2

FIG. 2C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051411

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/45(2006.01)i, H03K 17/62(2006.01)i, H03M 1/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 3/45; H03F 1/56; H03M 1/00; H01P 9/00; H03M 1/14; H03M 1/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:pipeline ADC, residue amplifier, folded cascode differential amplifier, multiplexer, glitch, pulse generator, XOR gate, delay

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 05530444 A (TICE, THOMAS E. et al.) 25 June 1996 See abstract, claims 1, 5-6,9,11-12, 14-16 and figures 2,5,8,13-14	1-11
A	J.H. et al. `A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification`, In: IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 4, APRIL 2009, pp. 1057-1066. See abstract, figures 6-7 and corresponding detailed description.	1-11
A	B.M. et al. `A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification`, In: IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 12, DECEMBER 2003, pp. 2040-2050. See abstract, figures 6,9,13 and corresponding detailed description.	1-11
A	B.S.P. et al. `A 10b 100MS/s 25.2mW 0.18μm CMOS ADC with various circuit sharing techniques `, In: 2009 International SoC Design Conference, 22-24 Nov. 2009, pp. 329-332. See abstract, figures 1-2 and corresponding detailed description.	1-11
A	US 05867053 A (ENGLES, BRUCE E. et al.) 02 February 1999 See abstract, claim 1 and figures 2-5	1-11

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search	Date of mailing of the international search report
16 JANUARY 2012 (16.01.2012)	**17 JANUARY 2012 (17.01.2012)**

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Facsimile No. 82-42-472-7140

Authorized officer
Kang Hyun Il
Telephone No. 82-42-481-8268

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051411

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6323791 B1 (MURDEN, FRANK et al.) 27 November 2001 See abstract, claims 1,5 and figures 2-3	1-11
A	US 2009-0243907 A1 (NAZEMI ALI et al.) 01 October 2009 See abstract, claim 1 and figure 3	1-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/051411

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 05530444 A	25.06.1996	WO 96-21271 A1	11.07.1996
US 05867053 A	02.02.1999	None	
US 6323791 B1	27.11.2001	None	
US 2009-0243907 A1	01.10.2009	EP 1941690 A2	09.07.2008
		EP 1972054 A2	24.09.2008
		US 2007-0133719 A1	14.06.2007
		US 2007-0133722 A1	14.06.2007
		US 2007-0176814 A1	02.08.2007
		US 2008-0240325 A1	02.10.2008
		US 2009-0096647 A1	16.04.2009
		US 2009-0185613 A1	23.07.2009
		US 2011-0058596 A1	10.03.2011
		US 2011-0081152 A1	07.04.2011
		US 7515084 B1	07.04.2009
		US 7576676 B2	18.08.2009
		US 7750835 B1	06.07.2010
		US 7778320 B2	17.08.2010
		US 7808417 B2	05.10.2010
		US 7852913 B2	14.12.2010
		WO 2007-041601 A2	12.04.2007
		WO 2007-041601 A3	12.04.2007
		WO 2007-092067 A2	16.08.2007
		WO 2007-092067 A3	16.08.2007