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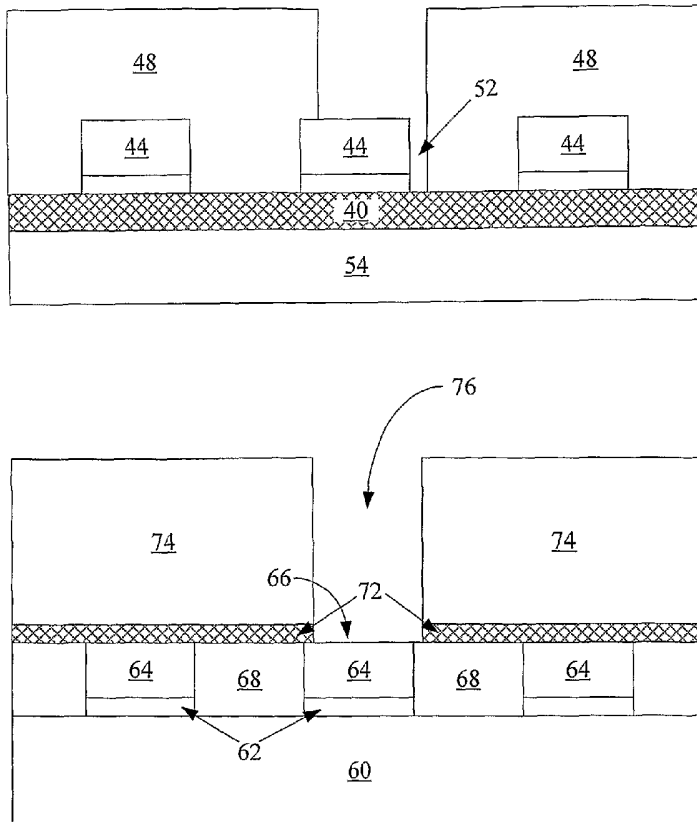
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(54) Title: METHOD FOR REDUCING DIELECTRIC OVERETCH WHEN MAKING CONTACT TO CONDUCTIVE FEAT-
TURES



(57) Abstract: In a first preferred embodiment of the present invention, conductive features (44) are formed on a first dielectric etch stop layer (40), and a second dielectric material (48) is deposited over and between the conductive features. A via etch to the conductive features which is selective between the first and second dielectrics will stop on the dielectric etch stop layer, limiting overetch. In a second embodiment, a plurality of conductive features (64) is formed in a subtractive pattern and etch process, filled with a dielectric fill (68), and then a surface formed coexposing the conductive features and dielectric fill. A dielectric etch stop layer (72) is deposited on the surface, then a third dielectric (74) covers the dielectric etch stop layer. When a contact (76) is etched through the third dielectric, this selective etch stops on the dielectric etch stop layer. A second etch makes contact to the conductive features.

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B. FIELDS SEARCHED

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 472 308 B1 (MEHTA SUNIL D) 29 October 2002 (2002-10-29)	1-3, 5, 6, 14-16, 18, 19, 21, 23-27, 30
Y	the whole document	7, 13, 17, 31-43
X	WO 99/16118 A (ADVANCED MICRO DEVICES, INC) 1 April 1999 (1999-04-01)	1, 4, 5, 8-10, 12
Y	pages 11, 12; figures 4-7	7, 13, 17, 31-43
Y	US 2005/014322 A1 (HERNER S. BRAD ET AL) 20 January 2005 (2005-01-20) cited in the application the whole document	7, 13, 17, 31-43
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 6 072 237 A (JANG ET AL) 6 June 2000 (2000-06-06) column 5; figures 5-8 -----	1, 4, 5, 8-12

INTERNATIONAL SEARCH REPORT

Information on patent family members

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