Oct. 30, 1973 R. L. TREADWAY Re. 27,804

TRANSISTOR-TRANSISTOR LOGIC CIRCUITS HAVING IMPROVED VOLTAGE TRANSFER CHARACTERISTIC

Original Filed Feb. 28, 1967



Fig.1

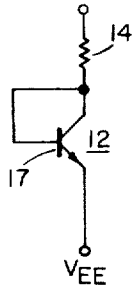


Fig.2

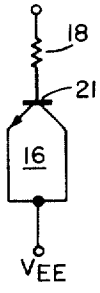


Fig.3

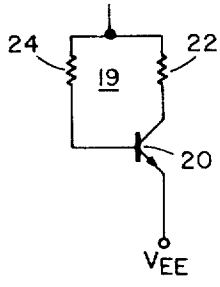


Fig.4

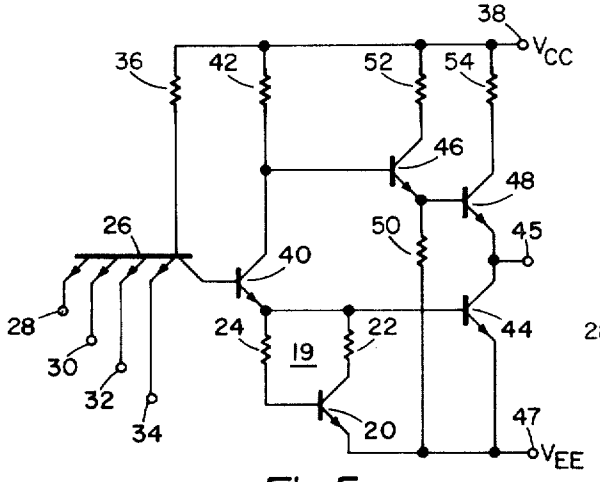


Fig.5

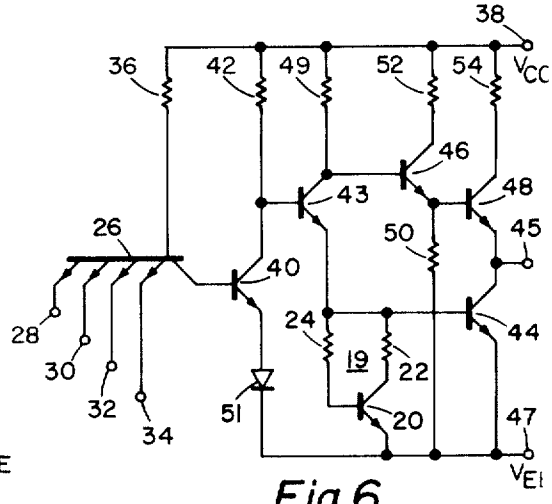


Fig.6

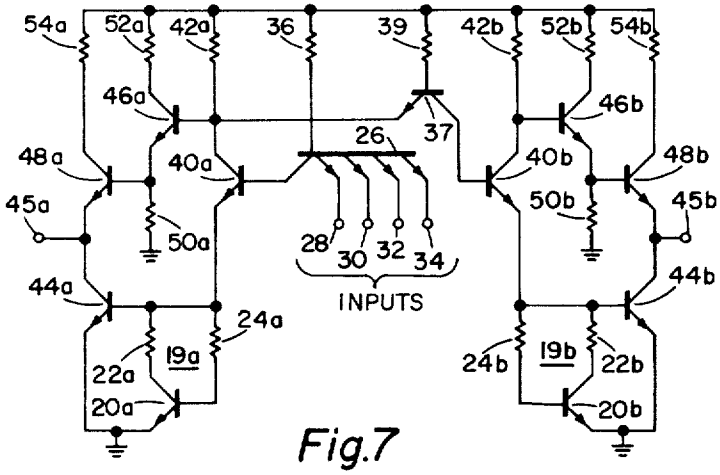


Fig.7

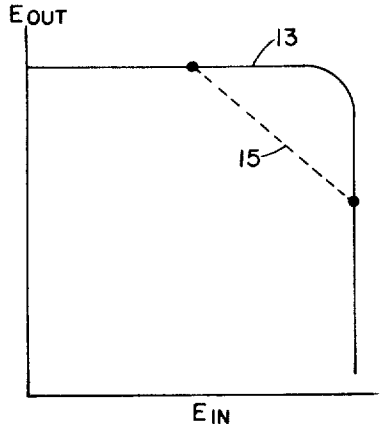


Fig.8

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United States Patent Office

Re. 27,804
Reissued Oct. 30, 1973

27,804

TRANSISTOR-TRANSISTOR LOGIC CIRCUITS HAVING IMPROVED VOLTAGE TRANSFER CHARACTERISTICS

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Original No. 3,555,294, dated Jan. 12, 1971, Ser. No. 619,379, Feb. 28, 1967. Application for reissue Jan. 21, 1971, Ser. No. 108,522

Int. Cl. H03k 3/33

U.S. Cl. 307—300 13 Claims

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

ABSTRACT OF THE DISCLOSURE

Transistor-transistor logic (TTL) circuitry having a bypass network connected to the output device of the circuitry for providing turn off drive for the output device. The bypass network includes a resistor connected in series with at least one PN junction, and such PN junction is within either a simple diode or a transistor. The bypass network prevents undesirable spiking in the output signal of the TTL logic circuitry.

This invention relates generally to high speed logic circuitry and more particularly to high speed transistor-transistor logic (TTL or T^2L) circuits having an improved discharge or pull down circuit for the T^2L circuit output device which is switched into and out of conduction. The terms "bypass," "pull down" and "discharge" will be used interchangeably hereinafter with reference to the network through which turn off drive current flows when the output device turns off.

BACKGROUND OF THE INVENTION

Known prior art T^2L of TTL logic circuits include one or more interstage current drive transistors directly cascaded between an output semiconductor device, such as a transistor, and a source of binary input logic signals. The output device is typically either in saturation or is turned off, depending upon the binary logic signal condition at the input of the T^2L circuit. When binary logic signals above a predetermined level are concurrently applied to multiple input electrodes of an input transistor of the T^2L circuit, the output transistor receives a turn on drive current and is driven into saturation.

The output terminal of the T^2L circuit is commonly connected to the collector of an output transistor, and for switching operation the potential on this collector is at one of two distinct levels of logic. When the output transistor is conducting in saturation, the collector thereof is at a potential equal to the collector-to-emitter saturation voltage of the output transistor, $V_{CE(SAT)}$, and using positive logic the circuit output terminal will be at a binary ZERO level. When the output transistor is turned off and the collector voltage of the output transistor increases, the level at the output terminal will rise from a binary ZERO level to a binary ONE level when the output transistor is completely turned off.

The time required for the output transistor to turn off and hence the overall switching speed of the logic circuit depends in large measure on the time required for the base charge to be removed or "pulled out" of the base of the output transistor. In the past, the discharging of the base region of the output transistor was accomplished using a so-called "pull down" resistor which was commonly connected between the base region of the output transistor and some point of reference potential. Thus, when it was desired to turn off the output transistor, the conductive path through the pull down resistor provided good turn off drive necessary to remove the base charge from the output transistor and terminate conduction therein.

While it is desirable to have a good turn off drive for the output transistor in order to maintain a desired switching speed for the T^2L circuit, there is a major disadvantage in using only a pull down resistor connected between the base region of the output transistor and a point of reference potential for discharging the output transistor. This disadvantage may be attributed to the fact that current will begin to flow in the pull down resistor prior to the time that the input signals applied to the T^2L circuit reach a level sufficiently high to drive the output transistor into saturation and switch the circuit output terminal from one to the other of its two levels of digital logic. This current flow in the pull down resistor produces a corresponding unwanted reduction in the DC output voltage level at the circuit output terminal in the absence of a proper binary signal condition at the input of the circuit. Thus, when extraneous noise signals are coupled to the prior art T^2L circuit having only a pull down resistor to discharge the output device, corresponding unwanted fluctuations in the output voltage level will be produced when current flows in the pull down resistor.

SUMMARY OF THE INVENTION

An object of this invention is to provide a transistor-transistor logic (T^2L) circuit having an improved input voltage versus output voltage transfer characteristic.

Another object of this invention is to provide a new and improved T^2L logic circuit having a high degree of noise immunity.

Another object of this invention is to provide a T^2L logic circuit which may be constructed using all NPN transistors in a monolithic integrated circuit including an improved discharge or pull down circuit for the output device which insures good turn off drive for the output device.

The present invention features a T^2L logic circuit having a new and novel bypass network connected between the output device of the circuit and a point of reference potential. This bypass network provides good turn off drive for the output device and prevents spiking in the output signals for input voltages which are not sufficiently high to drive the output device into saturation.

Another feature of this invention is the provision of a T^2L digital logic circuit wherein the bypass pull down network for the output device includes either a combination of a resistor and a diode or a combination of resistors and a transistor serially connected between the output device and a point of reference potential. The diode portion of the bypass network can be constructed using either a simple PN diode or a diode formed by connecting two electrodes of a transistor together, and the PN junction in the bypass network insures that discharge current will not flow therein until it is desired to turn on the output device.

Briefly described, the TTL logic circuitry according to this invention includes an input transistor for receiving one or more binary input logic signals, an output transistor which is switched into and out of saturation, and an inverting or current drive transistor connected between the input and output transistors for providing turn on drive current for the output transistor when binary logic signals above a predetermined logical level are concurrently applied to the input transistor. An improved bypass pull down network is connected between the output transistor and a point of reference potential

and includes at least one PN junction connected to the output transistor and in series with a resistor for providing a discharge path and turn off drive for the output transistor when the latter turns off. Current will not flow in the above-described bypass network until the output transistor turns on and off, insuring that input signals below a certain logical level do not produce corresponding spiking in the output voltage of the TTL logic circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIGS. 1 through 4 illustrate four different types of bypass networks which are used in the novel T^2L circuits according to this invention;

FIG. 5 is a T^2L NAND logic gate according to this invention;

FIG. 6 is a T^2L AND logic gate according to this invention;

FIG. 7 is a combination AND/NAND T^2L logic circuit according to this invention which combines the features of the circuits shown in FIGS. 5 and 6 to perform the dual AND/NAND logic function; and

FIG. 8 is a transfer characteristic of input voltage versus output voltage for the circuits shown in FIGS. 5 through 7, and the dotted line portion of the transfer characteristic in FIG. 8 represents a portion of the voltage transfer characteristic of the above-described prior art T^2L logic circuits.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawing in more detail, there are shown in FIGS. 1 though 4 four types of bypass networks which may be used in any of the logic circuits in FIGS. 5 through 7 in order to impart to these logic circuits an improved voltage transfer characteristic which will be described in more detail below with reference to FIG. 8. The transistor bypass network **19** in FIG. 4 is used in each of the logic circuits shown in FIGS. 5 through 7, but the diode bypass networks in FIGS. 1 through 3 can be substituted for the transistor bypass network **19** in FIG. 4 in accordance with the novel teachings of this invention.

The diode bypass network in FIG. 1 consists of resistor **10** and diode **11** which are adpated to be connected between the base region of the output device **44** in FIGS. 5 through 7 and a point of reference potential V_{EE}. The diode bypass network in FIG. 2 is also adapted to be connected between the base region of the output device **44** and a point of reference potential V_{EE}, and the bypass network in FIG. 2 differs from that shown in FIG. 1 in that the diode action is provided by a transistor-diode **12**, the collector and base electrodes of which are connected together. The diode bypass network **16** shown in FIG. 3 which may be used to replace the bypass networks in FIGS. 1 and 2 also includes a transistor-diode **21** which is connected in series with a resistor **18**. The emitter and collector electrodes of transistor-diode **21** are connected together at a point of reference potential V_{EE}.

The transistor bypass network **19** shown in FIG. 4 will be described hereinafter with reference to the logic circuits in FIGS. 5 through 7 and with reference to the voltage transfer characteristic **13** shown in FIG. 8. However, it will be appreciated by those skilled in the art that the diode bypass networks in FIGS. 1 to 3 may be substituted for the transistor bypass network **19** in FIG. 4 without departing from the scope of this invention.

The T^2L logic circuit in FIG. 5 includes a multiple emitter input transistor **26** having input terminals **28, 30, 32** and **34** which are connectable to sources of binary logic signals. A current drive transistor **40** has its base region connected directly to the collector region of the input transistor **26**, and the transistor **40** is referred to as a current drive transistor since it furnishes the base drive for the output transistor **44** to which it is connected. The logic circuit of FIG. 5 also includes a second output transistor **48** connected in push-pull with the one output transistor **44**, and a second current drive transistor **46** is connected between the collector of transistor **40** and the base of the second output transistor **48**. Transistor **46** provides base drive to the output transistor **48** when the collector of transistor **40** swings from a low to a high potential.

Collector load resistors **42, 52** and **54** are connected to the collectors of transistors **40, 50** and **48** respectively to establish the desired current levels for proper circuit operation, and sources of collector and emitter potential V_{CC} and V_{EE} are connected respectively to the voltage supply terminals **38** and **47**. As previously mentioned, the transistor bypass network **19** is connected directly between the base of output transistor **44** and a point **47** of reference potential V_{EE} which, in this case, is ground potential. The individual circuit components of the logic circuits in FIGS. 5, 6 and 7 will not be described further except with respect to circuit operation, and the reference numerals used in FIG. 5 are also used in FIGS. 6 and 7 to denote corresponding circuit components which produce identical functions within the three digital logic circuits shown.

OPERATION

In order to fully appreciate and understand the novel features of the bypass networks in FIGS. 1 to 4 and particularly the transistor bypass network **19** in each of the circuits in FIGS. 5 through 7, assume initially that network **19** in FIG. 5 is replaced by a single pull down resistor (not shown) connected between the base of the output transistor **44** and ground potential V_{EE}. Using positive logic in the absence of an "all ONE" binary input signal condition at terminals **28, 30, 32** and **34** the output transistor **44** is turned off and the output transistor **48** is conducting current through output terminal **45** to an external load (not shown). Assume now that the binary signals applied to the terminals **28, 30, 32** and **34** of the input transistor **26** all swing sufficiently high to partially reverse bias the multiple emitter-base junctions of the input transistor **26** and force current across the base-collector junction of transistor **26** and into the base of current drive transistor **40**. Current will flow through the above-described pull down resistor and this current is approximately equal to the base-emitter voltage V_{BE} or transistor **40** minus the offset voltage V_{OFFSET} of transistor **26** plus the input voltage E_{IN} divided by the value of the pull down resistor. The voltage drop across the pull down resistor prior to the time that the output transistor **44** turns on or off is reflected through the serially connected emitter-base regions of transistors **46** and **48** and seen at the output terminal **45**.

The decrease in output voltage E_{OUT} at output terminal **45** with an increasing input voltage E_{IN} is illustrated in FIG. 8, and the dotted portion **15** of the circuit voltage transfer characteristic E_{IN} vs. E_0 is produced by current flowing in the single pull down resistor of the prior art. As will be seen from the following description, the portion **15** of the voltage transfer characteristic is replaced by portion **13** in FIG. 8 in accordance with the teachings of this invention.

Consider now the T^2L logic circuit according to the present invention wherein the single pull down resistor of the prior art logic circuit has been replaced by one of the bypass networks shown in FIGS. 1 to 4. The diode bypass or pull down network of FIG. 1 includes a resistor **10** connected in series with diode **11**, and this series diode bypass network can be used to replace the transistor bypass network **19** which is used in the logic circuits in FIGS. 5 to 7. The transistor bypass network **19** of FIG. 4 is preferred over those shown in FIGS. 1 to 3, but any of the bypass networks in FIGS. 1 to 3 may be used to replace the network **19** and obtain satisfactory circuit operation. Since the offset voltage of the diode **11**

is in the order of .6 or .7 volt, approximately the same as the base-emitter offset voltage V_{BE} of the output transistor **44**, the diode bypass network appears as an infinite impedance during voltage buildup at the base of the output transistor **44**. When the base voltage at the output transistor **44** exceeds the V_{BE} of the transistor, emitter current will flow in the transistor **44** as it is biased into saturation. At this time current will flow into the bypass network, and the value of the pull down current is approximately equal to that drawn by the previous straight pull down resistor. When a binary input signal at any one of the input terminals **28**, **30**, **32** or **34** of the input transistor **26** falls to a binary ZERO level, the base drive is removed from transistor **40** and the output transistor **44** begins to turn off. The diode bypass network in FIG. 1 will provide the turn off drive for the output transistor **44**, and discharge current will flow from the base of output transistor **44** through resistor **10** and diode **11** to ground.

The diode bypass networks **12** and **16** in FIGS. 2 and 3 are alternative connections which may be used in the logic circuits shown in FIGS. 5 through 7, and these bypass networks use the transistors **17** and **21** with two electrodes thereof tied together to provide the diode action as in a normal PN diode.

When the current drive transistor **40** begins to turn off, the voltage at the base of a second current drive transistor **46** rises and turns on transistors **46** and **48** when it reaches a value sufficient to overcome the 2 V_{BE} offset voltage of the transistors **46** and **48**. Thus, transistor **48** drives an output load (not shown) connected to the output terminal **45** when any one of the inputs to the input terminals **28**, **30**, **32** and **34** swings to a binary ZERO logical level. When all inputs which are applied to input transistor **26** again go high, transistors **46** and **48** are turned off and transistor **44** is again driven into saturation, receiving its collector current from an external load connected to the output terminal **45**.

The logic circuit shown in FIG. 6 differs from that shown in FIG. 5 in that a reinverting transistor **43**, a collector load resistor **49** and a diode **51** have been added to the circuit components in FIG. 5. The addition of these three components to the circuit shown in FIG. 5 insures that the non-inverting AND logic function is provided by the logic circuit in FIG. 6. When transistor **40** in FIG. 6 is driven into conduction, the voltage at the base of the reinverting transistor **43** is insufficient to turn the latter transistor on, and the voltage at the base of current drive transistor **46** is sufficiently high to bias transistors **46** and **48** conducting. The output transistor **44** is turned off and the logical level at the output terminal **45** is high or at a binary ONE level. When one of the binary inputs to the input transistor **26** swings low, transistor **40** turns off and transistor **43** is turned on to apply base drive to the output transistor **44** as did the current drive transistor **40** in FIG. 5.

With regard to the logic circuit shown in FIG. 6 consider a prior art non-inverting AND logic circuit similar to FIG. 6 but having only a single pull down resistor connected to the base of the output transistor **44** instead of the diode bypass network **19**. With transistor **40** conducting, the voltage at the emitter of transistor **43** would be equal to the V_{BE} of diode **51** plus the saturation voltage $V_{CE(SAT)}$ of the transistor **40** minus the V_{BE} of the transistor **43**. The resultant voltage $V_{CE(SAT)}$ across the prior art pull down resistor draws a small emitter current from transistor **43**. With the transistor **43** conducting slightly and its current gain approximately equal to one, the collector current of transistor **43** will be substantially equal to the emitter current thereof if the collector resistor **49** is approximately equal in value to the pull down resistor. Therefore, with transistor **43** conducting slightly, the base voltage at the current drive transistor **46** will be $V_{CC}-V_{CE(SAT)}$, establishing the DC output level at terminal **45** at a value equal to $V_{CE(SAT)}$ lower than it is when the bypass network of this invention is used. By using the bypass network **19** in FIG. 6 instead of a single pull down resistor, the voltage level $V_{CE(SAT)}$ at the base of transistor **44** when transistor **44** is turned off is insufficient to bias the pull down transistor **20** into conduction. Thus, no current flows from the transistor **43** in FIG. 6 when all inputs to the terminals **28**, **30**, **32** and **34** are high or at a logical ONE level.

The dual AND/NAND circuit of FIG. 7 combines the novel features described above with reference to FIGS. 5 and 6 and includes a pair of diode bypass networks **19a** and **19b** which function identically to the bypass networks **19** shown in FIGS. 5 and 6. Identical reference characters in FIGS. 5 through 7 have been used to denote corresponding circuit components, and the subscripts "a" and "b" have been used to differentiate the corresponding components of the two bypass networks shown in FIG. 7. Accordingly, each circuit component in FIG. 7 will not be separately identified since such separate identification is not necessary to understand the operation of this circuit. It will be apparent to those skilled in the art that the left hand portion of the logic circuit in FIG. 7 in which the subscript "a" is used performs the inverting NAND function and the right hand portion of the logic circuit shown in FIG. 7 in which the subscript "b" is used performs the non-inverting AND function.

When all of the inputs to transistor **26** are high, the emitter of transistor **37** is low and the current drive transistor **40b** is turned off. With transistor **40b** turned off the output terminal **45b** is high at a logical ONE level. When any one of the inputs to the input transistor **26** goes low, the emitter of transistor **37** swings high and base drive is applied to transistor **40b** from the collector of transistor **37**, turning on the output transistor **44b** and pulling the output terminal **45b** to a binary ZERO level ($V_{CE(SAT)}$ of the output transistor **44b**).

The left hand portion of the dual gate in FIG. 7 performs the NAND function in a manner identical to that of the NAND gate in FIG. 5 in response to changes in binary levels at the input terminals **28**, **30**, **32** and **34**.

The following table is given by way of illustration and includes component values for the three circuits in FIGS. 5 to 7 which have been constructed in accordance with the principles of this invention and which have been successfully operated.

TABLE

		Valve
Resistors:		
R22	ohms	500
R22a	do	500
22b	do	500
24	do	250
24a	do	250
24b	do	250
36	do	2,400
39	do	2,400
42	do	800
42a	do	800
42b	do	800
50	do	3,500
50a	do	3,500
50b	do	3,500
52	do	180
52a	do	180
52b	do	180
54	do	90
54a	do	90
54b	do	90
Voltage supplies:		
V_{EE}	volts	5
V_{CC}	do	5

It will be observed that a first resistor **22** in the collector circuits of the turn off drive transistors **20** in FIGS. 5–7 is 500 ohms, a resistance value which is approximately twice that of the resistor **24**. Since the base-to-

emitter voltage V_{BE} of turn off drive transistor **20** is approximately twice that of the collector-to-emitter voltage V_{CE} the currents flowing into resistors **22** and **24** respectively will be approximately equal with the resistance imbalance described above. The above selection of resistance values for the resistors **22** and **24** provides a good turn off drive for the output transistor **44.**

I claim:

1. In a logic circuit having an input transistor for receiving one or more binary logic signals, an output transistor, and a current drive transistor connected between the input transistor and the output transistor for providing turn on drive current for the output transistor when binary logic signals concurrently applied to the input transistor reach a predetermined logical level, the improvement comprising discharge circuit means including

(a) a turn off drive transistor having an emitter, a base and a collector,

(b) a first resistor connected between said collector of said turn off drive transistor and the base of the output transistor,

(c) a second resistor connected between the base of said turn off drive transistor and the base of the output transistor, and

(d) means connecting the emitter of said turn off drive transistor to a point of reference potential, said turn off drive transistor and said first and second resistors providing a discharge path from the output transistor when the latter is turned off.

2. The circuit according to claim **1** wherein the resistance value of said first resistor is approximately twice that of said second resistor in order that the currents flowing through said first and second resistors to said turn off drive transistor will be approximately equal.

3. A transistor-transistor logic circuit including in combination:

(a) an input transistor having a base, a collector and a plurality of emitters connected to receive binary logic signals,

(b) one output transistor having an emitter, a base and a collector,

(c) one current drive transistor having an emitter, a base and a collector with the base-emitter path thereof connected between the collector of said input transistor and the base of said one output transistor, said one current drive transistor providing a turn on drive current for said one output transistor when binary logic signals concurrently applied to the emitters of the input transistor reach a predetermined logical level,

(d) resistance means connected between a voltage supply terminal and respective ones of said input transistor, said one current drive transistor, and said one output transistor for biasing same and biasing said one output transistor and said one current drive transistor nonconducting in the absence of binary logic signals at a predetermined logic level concurrently applied to the emitter of said input transistor, and

(e) discharge circuit means including a transistor having its base and collector regions resistively connected to the base of said one output transistor and its emitter connected to a point of reference potential.

4. A circuit according to claim **3** which further includes:

(a) a second output transistor connected in push-pull with said one output transistor, and

(b) a second current drive transistor coupled to said voltage supply terminal and connected between said one current drive transistor and said second output transistor for providing turn on drive current for said second output transistor when said one output transistor turns off.

5. The circuit according to claim **4** wherein said discharge circuit means includes:

(a) a turn off drive transistor having an emitter region, a base region and a collector region, the emitter region connected to said point of reference potential,

(b) a first resistor connected between the collector region of said turn off drive transistor and the base of said one output transistor, and

(c) a second resistor connected between the base region of said turn off drive transistor and the base of said one output transistor, said first and second resistors providing a discharge path from the base of said one output transistor and through said turn off drive transistor for rapidly removing the charge from said one output transistor when the latter is turned off.

6. The circuit according to claim **5** wherein said first resistor is substantially larger than said second resistor.

7. The circuit according to claim **6** wherein the resistance value of said first resistor is approximately twice that of said second resistor in order that the currents flowing through said first and second resistors to said turn off drive transistor will be approximately equal.

8. In a circuit configuration employing a first transistor having base, emitter and collector electrodes and means for biasing said first transistor into conduction and means for turning off said first transistor, a circuit means for said first transistor which improves the transfer characteristics and the turn off characteristics of said first transistor comprising:

a second semiconductor device having a PN junction which exhibits an offset voltage approximately the same as the base-emitter offset voltage V_{be} of the first transistor and said device being poled for carrying current simultaneously with said first transistor, and

current limiting means in series connection with said second semiconductor device for providing turn on current for said P-N junction while said first transistor is biased into conduction and in combination with said P-N junction providing a temporary infinite impedance during turn on of said first transistor and for providing a current discharge path for current stored in said base region of said first transistor, when said turn off means turns off said first transistor.

9. In a circuit configuration employing a first transistor having base emitter and collector electrodes and means for biasing said first transistor into conduction and means for turning off said first transistor, a discharge circuit means therefor for improving the turn off characteristics of said first transistor comprising:

second transistor means having base, emitter and collector electrodes,

first current limiting means intermediate said collector electrode of said second transistor and said base electrode of said first transistor,

second current limiting means intermediate said base electrode of said second transistor and said base electrode of said first transistor, and

means connecting the emitter electrode of said second transistor means to a reference potential, whereby said second transistor means and said current limiting means provide a discharge path from said base electrode of said first transistor when said first transistor is turned off by said turn off means.

10. In a circuit configuration employing a first transistor having base, emitter and collector electrodes and means for biasing said first transistor into conduction including a reference potential applied to its emitter electrode and a forward biasing current source applied to said base electrode of said first transistor and means for turning off said first transistor by electrically removing said current source, circuit means therefor for improving the characteristics of said first transistor comprising,

second transistor means having base, emitter and collector electrodes, first current limiting means intermediate said base electrode of said second transistor and said base electrode of said first transistor for providing a forward biasing current path for said second transistor,

second current limiting means intermediate said collector electrode of said second transistor and said base electrode of said transistor, and

means connecting said emitter electrode of said second transistor to said reference potential, whereby said second transistor and said first and second current limiting means provide a discharge path from said base electrode of said first transistor when said first transistor is turned off by said turn off means.

11. In a circuit configuration employing at least a reference potential and a forward biasing current source and means for turning off said forward biasing current source, the combination,

a first transistor having base, emitter and collector electrodes wherein said first transistor has its emitter electrode connected to said reference potential and said base electrode being responsive to said forward biasing current source,

a discharge circuit means for improving the turn off characteristics of said first transistor including,

second transistor means having base, emitter and collector electrodes,

first current limiting means intermediate said base electrode of said second transistor and said base electrode of said first transistor for providing a forward biasing current path for said second transistor,

second current limiting means intermediate said collector electrode of said second transistor and said base electrode of said first transistor, and

means connecting said emitter electrode of said second transistor to said reference potential source, whereby said second transistor and said first and second impedance means provide a discharge path from said base electrode of said first transistor when said first transistor is turned off by said turn off means.

12. In a circuit configuration employing a first transistor having base, emitter and collector electrodes and means for biasing said first transistor into conduction including a reference potential source applied to its emitter electrode and a forward biasing current source applied to said base electrode of said first transistor and means for turning off said transistor by electrically disengaging said current source, a discharge circuit means therefor for improving the turn off characteristics of said first transistor comprising,

second transistor means having base, emitter and collector electrodes,

a first resistor intermediate said base electrode of said second transistor and said base electrode of said first transistor for providing forward a biasing current path for said second transistor,

a second resistor intermediate said collector electrode

of said second transistor and said base electrode of said first transistor, and

means connecting said emitter electrode of said second transistor to said reference potential, whereby said second transistor and the first and second impedance means provide a discharge path from said base electrode of said first transistor when said first transistor is turned off by said turn off means.

13. In a circuit configuration employing a first transistor having base, emitter and collector electrodes and means for biasing said first transistor into conduction including a reference potential source applied to its emitter electrode and a forward biasing current source connected to said base electrode of said first transistor and means for turning on said first transistor by electrically activating said current source, circuit means therefor for improving the transfer characteristics of said first transistor comprising,

second transistor means having base, emitter and collector electrodes,

first current limiting means intermediate said base electrode of said second transistor and said first electrode of said first transistor for providing a forward biasing current path for said second transistor,

second current limiting means intermediate said collector electrode of said second transistor and said base electrode of said first transistor, and

means connecting said emitter electrode of said second transistor to said reference potential source, whereby said second transistor and said first and second current limiting means provide a temporary infinite impedance during turn on of said first transistor when said first transistor is turned on by said turn on means.

References Cited

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U.S. Cl. X.R.

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