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CA 2740629 A1 2010/06/03

(21) 2 740 629

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(86) Date de dépôt PCT/PCT Filing Date: 2009/09/22
(87) Date publication PCT/PCT Publication Date: 2010/06/03
(85) Entrée phase nationale/National Entry: 2011/04/14
(86) N° demande PCT/PCT Application No.: US 2009/057793
(87) N° publication PCT/PCT Publication No.: 2010/062449
(30) Priorité/Priority: 2008/10/28 (US12/259,492)

(51) Cl.Int./Int.Cl. *H05B 37/02* (2006.01), *H05B 41/36* (2006.01), *H05B 41/392* (2006.01)

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(54) Titre : CIRCUIT UNIFIE 0-10V ET INTERFACE DE GRADATION DALI
(54) Title: UNIFIED 0-10V AND DALI DIMMING INTERFACE CIRCUIT

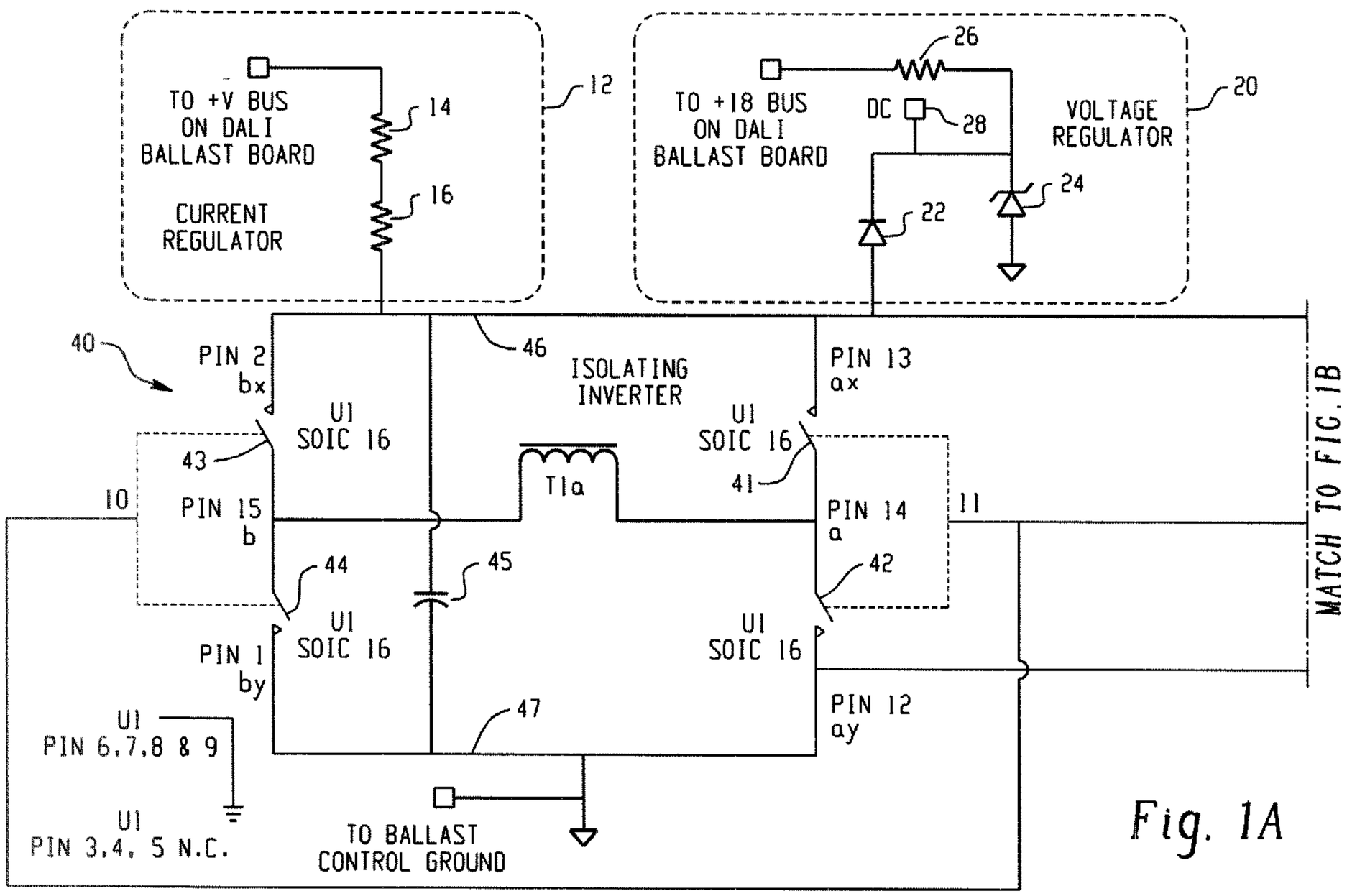

Fig. 1A

(57) Abrégé/Abstract:
Systems and methods are disclosed that facilitate switching a lamp ballast between DALI and analog control states as a function of control state information stored prior to the ballast being powered of and control information received by an interface circuit for the ballast circuit. A depolarization circuit is coupled to the interface circuit and ensures consistent polarity across a rectifier circuit regardless of the polarity of two control wires coupled to a miswiring protection circuit in the interface circuit. In this manner, a single interface circuit provides dual 0-10V analog and DALI control for dimming a lighting device regardless of whether a wall-mounted controller coupled to the interface circuit is an analog or a DALI type controller, thereby mitigating a need to switch out a ballast circuit coupled to the lighting devise when changing between DALI and analog type controllers.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 June 2010 (03.06.2010)

PCT

(10) International Publication Number
WO 2010/062449 A3

(51) **International Patent Classification**:
H05B 37/02 (2006.01) ***H05B 41/392*** (2006.01)
H05B 41/36 (2006.01)

(21) **International Application Number**:
PCT/US2009/057793

(22) **International Filing Date**:
22 September 2009 (22.09.2009)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
12/259,492 28 October 2008 (28.10.2008) US

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) Title: UNIFIED 0-10V AND DALI DIMMING INTERFACE CIRCUIT

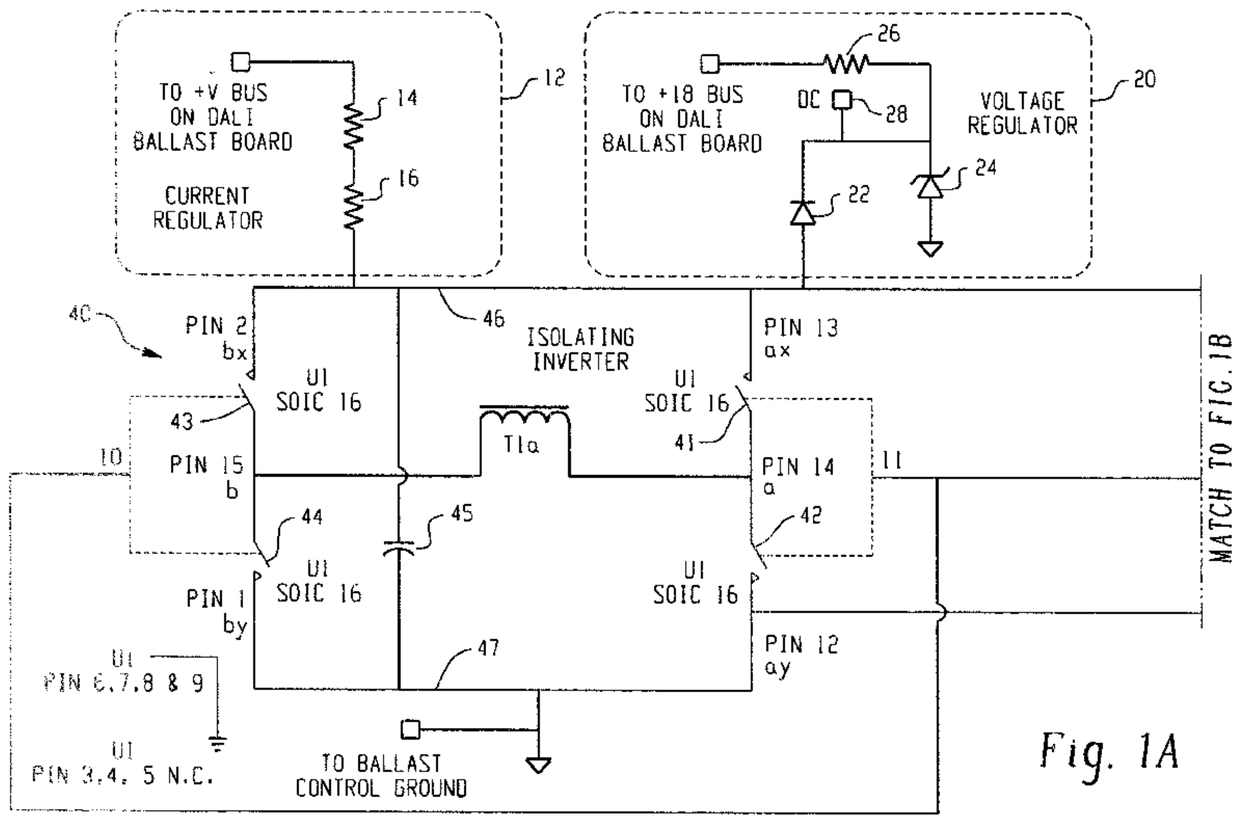

Fig. 1A

(57) Abstract: Systems and methods are disclosed that facilitate switching a lamp ballast between DALI and analog control states as a function of control state information stored prior to the ballast being powered of and control information received by an interface circuit for the ballast circuit. A depolarization circuit is coupled to the interface circuit and ensures consistent polarity across a rectifier circuit regardless of the polarity of two control wires coupled to a miswiring protection circuit in the interface circuit. In this manner, a single interface circuit provides dual 0-10V analog and DALI control for dimming a lighting device regardless of whether a wall-mounted controller coupled to the interface circuit is an analog or a DALI type controller, thereby mitigating a need to switch out a ballast circuit coupled to the lighting devise when changing between DALI and analog type controllers.

WO 2010/062449 A3

WO 2010/062449 A3

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
26 August 2010

UNIFIED 0-10V AND DALI DIMMING INTERFACE CIRCUIT

BACKGROUND OF THE INVENTION

[0001] The present application is directed to electronic interface circuits. It finds particular application in conjunction with digital addressable lighting interface (DALI) circuits and 0-10V dimming interface circuits, and will be described with the particular reference thereto.

[0002] Classical 0-10V dimming interface circuits employ a 0-10V control signal to dim a lighting device over a practical range of output power. Light level is determined by an analog voltage level set by a user in the range of 0-10V. Such circuits have a positive-negative polarity that must be adhered to in order for the system to function properly. The interface circuit is required to provide a controlled current that is electrically isolated from the electronics of the lighting device so that passive control components such as contacts and potentiometers may be used to dim the lighting device.

[0003] Other interface circuits allow lighting devices to be dimmed using the DALI standard protocol. Such circuits are generally not polarized, allowing the control wires to be interchanged. Light level is controlled by digital messages that are passed to a DALI control bus, at up to 22V according to the standard.

[0004] Attempts to depolarize a 0-10V power supply interface have thus far included using a synchronous rectifier bridge that requires continuous commutation and a diode bridge in the depolarizing circuit.

[0005] The following contemplates new methods and apparatuses that overcome the above referenced problems and others.

BRIEF DESCRIPTION OF THE INVENTION

[0006] According to an aspect, a dual-control analog and DALI interface circuit comprises an isolating inverter circuit that is coupled to a current regulator and a voltage regulator, and a microcontroller that is coupled to the isolating inverter circuit, the

current regulator, and the voltage regulator. The interface circuit further comprises a depolarizing circuit that ensures a desired polarity at a rectifier circuit that is inductively coupled to the isolating inverter circuit..

[0007] According to another aspect, a method of providing dual 0-10V analog and DALI control of a ballast circuit for dimming a lighting device comprises powering ON the ballast circuit, reading control state information stored in memory and describing a control state of the ballast circuit prior to entering an OFF state, and determining whether the ballast circuit was in a DALI control state prior to entering the OFF state. The method further comprises employing received DALI commands to control the ballast circuit if the ballast circuit was in a DALI control state prior to entering the OFF state, and employing received analog control commands to control the ballast circuit if the ballast circuit was in an analog control state prior to entering the OFF state.

[0008] According to yet another aspect, a computer-readable medium stores computer-executable instructions for execution by a processor, the instructions including reading, upon powering ON a lighting device ballast circuit, control state information stored in memory and describing a control state of the ballast circuit prior to entering an OFF state, and determining whether the ballast circuit was in a DALI control state prior to entering the OFF state. The instructions further include employing received DALI commands to control the ballast circuit if the ballast circuit was in a DALI control state prior to entering the OFF state, and employing received analog control commands to control the ballast circuit if the ballast circuit was in an analog control state prior to entering the OFF state. Additionally, the computer-readable medium stores instructions for monitoring incoming control signals for DALI control commands when the ballast is in the analog control state, updating the control state information in the memory to indicate that the ballast circuit is in the DALI control state upon detection of the valid DALI control command. Furthermore, the computer-readable medium stores instructions for monitoring incoming control signals for analog control commands when the ballast is in the DALI control state, and updating the control state information in the memory to indicate that the ballast circuit is in the analog control state upon detection of the analog control command.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGURE 1A and 1B illustrate the interface circuit or ballast, which includes a current regulator comprising a pair of resistors in series between a positive voltage bus on a DALI ballast board and an isolating inverter in the interface circuit.

[0010] FIGURE 2 illustrates a portion of the interface circuit that includes an isolation transformer, a rectifier circuit, and a depolarization circuit.

[0011] FIGURE 3 illustrates a miswiring protection circuit (MPC), which is part of the 0-10V-DALI interface circuit.

[0012] FIGURE 4 illustrates a method of providing dual 0-10V and DALI control for a lighting device (e.g., a discharge lamp or the like), such as may be employed using the circuitry described with regard to Figs. 1A-3 and in accordance with various aspects described herein.

DETAILED DESCRIPTION OF THE INVENTION

[0013] With reference to FIGURES 1A-3, a dual mode interface circuit, or ballast circuit, 10 is illustrated that facilitates using either or both or a 0-10V control signal and DALI control signals to control dimming of a single lamp. The interface circuit 10 includes a depolarizing circuit 110 (Fig. 2) that allows a 0-10V interface to be used in a non-polarized fashion. Like a DALI control circuit, the leads of the 0-10V interface may be interchanged without affecting circuit performance. That is, the depolarizing circuit 140 permits two control wires to be applied from the circuit 10 to a lamp or other device regardless of the polarity thereof. The interface 10 also includes a miswiring protection circuit 140 (Fig. 3) that prevents the ballast 10 from being damaged due to accidental connection of the control wires to mains or other high-voltage wiring. That is, the miswiring protection circuit protects the interface circuit should the control wires be inadvertently wired to the mains during installation. The miswiring protection circuit is configured such that it ensures that the ballast circuit operates regardless of the wiring of

two interchangeable control wires coupled to the miswiring protection circuit and to a control device.

[0014] In this manner the interface circuit 10 provides a fast, electrically isolated interface that allows AC and/or DC signals to be received by a microcontroller that regulates a parameter of the device to which it is coupled, such as luminosity of a lighting device. For instance, the interface circuit 10 permits data to be transmitted from the microcontroller to the control wires, as required by DALI standards, as well as permits low-level current to pass through an isolation barrier to the control leads, as required by 0-10V dimming standards. Only two control wires need be applied to the lighting device (e.g., discharge lamp, incandescent lamp, high-intensity discharge lamp, fluorescent lamp, etc.), and the lighting device is not sensitive to the polarity of the control wires regardless of which control method (e.g., 0-10V or DALI) is employed. In the case of 0-10V dimming, the interface circuit provides a low-level current supply to the control wires to provide passive dimming control. In the case of DALI dimming, the control interface allows the lighting device to receive and transmit coded DALI packets per the IEC standard over the same two control wires used for 0-10V dimming. In both cases, the control wires are electrically isolated from mains that supply the lighting device with power.

[0015] The dual 0-10V-DALI ballast circuit 10 permits a lighting device to be employed, for instance, in analog 0-10V mode for an unspecified time period (e.g., weeks, months, years, etc.). If and when a wall-mounted analog control unit is replaced with a DALI controller, the change is sensed and the ballast continues working, without requiring an operator to change out the ballast coupled to the lighting device (e.g., in a ceiling or other relatively inaccessible place). Another advantage resides in the ability of a purchaser (e.g., a construction company or the like) to purchase large numbers of the ballast circuits without knowing a priori whether analog or DALI controllers will be used therewith. That is, a purchaser may purchase a number of the ballasts and then employ analog, DALI, or both control mechanisms to control lighting devices coupled to the ballasts.

[0016] Another advantage resides in the mitigation of a need for a retailer or manufacturer to maintain separate inventories of DALI and analog ballasts, because the dual-mode ballast 10 can operate in either mode. Moreover the dual modality of the circuit 10 can be adjusted to perform with analog and any suitable digital control logic, and is not limited to DALI control.

[0017] Accordingly, FIGURE 1A and 1B illustrate the interface circuit 10, which includes a current regulator 12 comprising a pair of resistors 14, 16 in series between a positive voltage bus on a DALI ballast board and an isolating inverter 40 in the interface circuit 10. In one example, the resistors 14, 16 are 1MΩ resistors. In another example, a single 2MΩ resistor is used in place of the two 1MΩ resistors. It will be appreciated that the resistor foregoing resistor values, as well as any other component values presented herein, are provided for illustrative purposes only, and that the herein-described embodiments are not limited to the provided component values, but rather may comprise any suitable component values to achieve the desired circuit features and/or functionality.

[0018] A voltage regulator 20 is coupled to the isolating inverter portion 40 of the circuit and to the positive voltage bus on the DALI ballast. The voltage regulator 20 includes a clamping diode 22 that is coupled to the isolating inverter 40. The diode 22 and the Zener diode 24 are coupled to a resistor 26 and a regulated DC output supply voltage 28. The Zener diode is further coupled to a signal ground. In one example, the resistor 26 is a 3.3kΩ resistor. In another example, the DC supply output 28 is a 5V supply voltage. In yet another example the diode 22 is a 1N4148 diode.

[0019] The isolating inverter 40 includes a transformer winding T1a (e.g., 20mH or the like) that is couple to an integrated circuit U1, such as a 16-pin small-outline integrated circuit (SOIC). In one example, the integrated circuit U1 is a CD4053 chip. The winding T1a is coupled to the microchip U1 at one end to pin 14 and at the other end to pin 15. Pin 14 is coupled to pin 13 via a switch 41 and to pin 12 via switch 42. Pin 15 is coupled to pin 1 via a switch 43 and to pin 2 via a switch 44. Switches 41 and 42 are further coupled to pin 11 of the chip U1, and switches 43 and 44 are connected to pin 10 thereof. Pin 10 is also coupled to pin 11. Pins 3, 4, and 5 are not connected, and pins 6,

7, 8, and 9 are coupled to earth ground. A capacitor 45 is provided across the isolating inverter 40, and is coupled at one end to pins 2 and 13 via a bus 46, and at the other end to pins 1 and 12 via a bus 47. In one example, the capacitor 45 is a 2.2nF capacitor. In another example, the capacitor has a cutoff frequency of approximately 12kHz. However, it will be appreciated that the capacitor may have any suitable capacitance that permits a DALI signal to pass. The bus 47 is coupled to a ballast control ground (not shown), as well as to signal ground.

[0020] The interface circuit 10 further includes a divide-by-8 counter (DB8C) 50, that is coupled to the chip U1 and to a microcontroller chip 60. In one embodiment, the BD8C 50 is a SOIC 16-pin chip, such as a MC14018B or the like, and the microcontroller 60 is a programmable intelligent computer (PIC), such as a 20-pin SOIC (e.g., a PIC16F690 or the like). Pins 1 and 11 of the DB8C are coupled to each other, to pin 11 of the chip U1, as well as to pin 10 of the chip U1. Pins 8, 10, and 15 of the DB8C are coupled to pin 12 of the chip U1.

[0021] Pin 1 of the microcontroller 60 and pin 16 of the DB8C 50 are coupled to each other, to a DC source 62 (e.g., in one embodiment, the source 62 is the regulated supply voltage output 28 from the voltage regulator 20), and to a capacitor 64. In one example, the DC source is a 5V DC source. The capacitor 64 is coupled across pin 1 (Vdd) and pin 20 (Vss) of the microcontroller 60, as well as to a signal ground. In one example, the capacitor 64 is a 0.1μF capacitor.

[0022] Pin 3 (RA3) of the microcontroller 60 is coupled to pin 14 of the DB8C 50. Pin 5 (P1A) of the microcontroller 60 is coupled to a pulse width modulation (PWM) component in a ballast power regulation control circuit (not shown). Pin 6 (RC4) transmits to node B, which is coupled to a miswiring protection circuit described in greater detail with regard to Fig. 3. Pin 8 (RC6) is coupled to a resistor 66, which in turn is coupled to a node A. Node A is coupled to the miswiring protection circuit, which is described in greater detail with regard to Fig. 3. In one example, the resistor 66 is a 10kΩ resistor.

[0023] Pin 14 (AN6) of the microcontroller 60 receives a 0-10 V input and is coupled to pin 18 (AN1) of the microcontroller 60 and to the bus 46 of the isolating inverter 40.

Pin 15 (AN5) is coupled to a lamp ballast circuit and receives a lamp failure signal in the event that a lamp failure occurs. The remaining pins (pins 2, 4, 7, 9, 10, 11, 12, 13, 16, 17, and 19) of the microcontroller are not connected.

[0024] FIGURE 2 illustrates a portion 80 of the interface circuit 10 that includes an isolation transformer T1b, a rectifier circuit 90, and a depolarization circuit 110. The isolation transformer T1b is inductively coupled to the transformer winding T1a of Fig. 1A, and is coupled to the rectifier circuit 90. That is, the isolating transformer T1b is coupled at a first end between diodes 92 and 94, and at a second end between diodes 96 and 98. A capacitor 100 is coupled to diodes 92 and 96 at a first end, and to diodes 94 and 98 at a second end. The capacitor 100 is further coupled to a negative terminal 101 of the depolarizing circuit 110. The diodes 92 and 94 are coupled to a positive terminal 102 of the depolarizing circuit 110. In one example, the diodes 92, 94, 96, 98 are 1N4148 diodes, and the capacitor is a 2.2nF capacitor.

[0025] The depolarizing circuit 110 includes an integrated circuit U3. In one example the integrated circuit U3 is a CD4053 chip. The integrated circuit U3 comprises a plurality of switches that are selectively engaged to ensure that the polarity across the terminals 101 and 102 remain constant, which ensures proper operation of the rectifier circuit (and thus the ballast 10) regardless of the configuration of two control leads or wires coupled to the miswiring protection circuit (Fig. 3).

[0026] Pin 2 of the chip U3 is coupled to the positive terminal 102 and to a switch 112. Pin 2 is further coupled to pin 13 of the chip U3, which in turn is coupled to a switch 114. Pin 10 of the chip U3 is coupled to switches 112 and 114.

[0027] Pin 1 of the chip U3 is coupled to the negative terminal 101, to a switch 116, and to pin 12 of the chip U3. Pin 12 is coupled to a switch 118. Pins 1 and 12 are also coupled to earth ground. Pin 11 of the chip U3 is coupled to both switch 116 and switch 118.

[0028] Pin 14 of the chip U3 is coupled to switches 114 and 118, as well as to a terminal C1 that is coupled to the miswiring protection circuit 140 (Fig. 3). Pin 15 of the chip U3 is coupled to switch 112 and switch 116, as well as to terminal C2 of the

miswiring protection circuit 140 (Fig. 3). Pin 15 of the chip U3 is further coupled to a resistor 120, which is in turn coupled to pin 1 of a comparator 122. Pins 3, 4, and 5 of the chip U3 are not connected, and pins 6, 7, 8, and 9 are connected to earth ground.

[0029] In one example, the comparator 122 is a LM397 voltage comparator. Pin 2 of the comparator 122 is coupled to earth ground. Pin 3 of the comparator 122 is coupled to a resistor 124, which in turn is coupled to pin 14 of the chip U3. Pin 4 of the comparator 122 is coupled to pins 10 and 11 of the chip U3. Pin 5 of the comparator 122 is coupled to a resistor 126, which in turn is coupled to a voltage source or terminal 128. According to an example, the resistors 120 and 124 are 150kΩ resistors, the resistor 126 is a 100kΩ resistor, and the voltage source 128 is a 19V source.

[0030] Still referring to Figure 2, an isolated power supply circuit 130 is illustrated, which drives the switches of chip U3. The circuit 130 includes a transformer winding T1c, which is inductively coupled to windings T1b and T1a (Fig. 1A) A first end of the winding T1c is coupled to capacitor 131, which in turn is coupled to the anode of diode 132 and to the cathode of diode 133. The cathode of diode 132 is coupled to a capacitor 134, to a cathode of a Zener diode 135, and to a terminal 136. A second end of the transformer winding T1c is coupled to the anode of diode 133, the capacitor 134, and the anode of Zener diode 135. In one example the capacitor 131 is a 0.01nF capacitor, and the capacitor 134 is a 10μF capacitor. In another example, the diodes 132, 133 are 1N4148 diodes, and the Zener diode is a 19V Zener diode. In another example, the terminal 136 is a 19V terminal.

[0031] FIGURE 3 illustrates a miswiring protection circuit (MPC) 140, which is part of the 0-10V-DALI interface circuit 10. The MPC 140 includes an 8-pin SOIC phototransistor 142, which has a light-emitting diode (LED) 144 that is coupled pin 1 of the phototransistor 142, which in turn is coupled to node A (e.g., resistor 66 of Fig. 1B). The LED 144 is further coupled to pin 2 of the phototransistor 142, which is coupled to node B (e.g., pin 6 of the microcontroller 60 of Fig. 1B). Pin 5 of the phototransistor 142 is coupled to an emitter of a transistor 146, and to a first end of a resistor 148 that is coupled to earth ground at a second end. In one example the resistor 148 is a 100kΩ resistor. Pin 6 of the phototransistor 142 is coupled to a resistor 150, which in turn is

coupled to a voltage source 152. In one example, the resistor 150 is a 100kΩ resistor, and the voltage source 152 is 19V source.

[0032] Pin 5 is additionally coupled to a gate of a first metal-oxide-semiconductor field-effect transistor (MOSFET) 154 and to a gate of a second MOSFET 156. The second end of the resistor 148 is coupled to the source of each MOSFET 154, 156. The drain of MOSFET 154 is coupled to a resistor 158 (e.g., a 910Ω resistor or the like), while the drain of the MOSFET 156 is coupled to a positive temperature coefficient (PTC) thermistor 160 (e.g., 500Ω or the like), which in turn is coupled to a first control wire 161. The drain of the MOSFET 156 and the thermister 160 are additionally coupled to a first Zener diode 162 in a dual Zener diode component 164, and to terminal C1, which is coupled to pin 15 of the chip U3 (Fig. 2).

[0033] The resistor 158 is coupled to a second Zener diode 166 in the dual Zener diode component 164, and a terminal C2, which is coupled to pin 14 of the chip U3 (Fig. 2). The resistor 158, the second Zener diode 166, and the terminal C2 are further coupled to a second control wire 167. In one example, the Zener diodes 162, 166 are 18V Zener diodes.

[0034] A pair of dual Schottky diode components 168, 174 is coupled across terminals C1 and C1. For instance, a first dual Schottky diode component 168 comprises a Schottky diode 170 having an anode connected between the terminal C1 and the thermistor 160, and to a cathode of a Schottky diode 172. The cathode of the Schottky diode 170 is coupled to a cathode of a Schottky diode 176 in the second dual Schottky diode component 174. The anode of Schottky diode 176 is coupled to the cathode of Schottky diode 178, which in turn are coupled to a bus between terminal C2 and the second control wire 167. The anodes of diodes 172 and 178 are coupled to earth ground, and the cathodes of diodes 170 and 176 are coupled to a voltage terminal (e.g., 19V or the like).

[0035] FIGURE 4 illustrates a method of providing dual 0-10V and DALI control for a lighting device (e.g., a discharge lamp or the like), such as may be employed using the circuitry described with regard to Figs. 1A-3 and in accordance with various aspects described herein. The very first time a ballast is powered up at a customer site, it is

considered to be in 0-10V control mode. Under this assumption, if the ballast is on a 0-10V controller, it will work immediately. If the ballast is on a DALI controller, it will be fully on (e.g., in a brightest state). On the first appearance of a legal DALI message, the ballast will revert to a DALI mode of operation. The state of the ballast (DALI or 0-10V) can be recorded in non-volatile memory (not shown), so that following a power interruption, the ballast will return to operation in the proper state. Since it is not a normal condition for DALI ballasts to be turned on/off using the mains, it is also acceptable to go straight to 0-10V control mode following a power-up. Using the algorithm of Figure 4, it is possible to switch a powered-ON ballast between 0-10V operation and DALI operation at will, by swapping controllers and issuing reasonably simple control requests with them. If power is cycled, the ballast retains its previous state in an electrically programmable read-only memory (EPROM).

[0036] Accordingly, at 220, the ballast is powered up. At 222, a determination is made regarding whether the ballast was in DALI mode prior to powering off. The determination can be made by reading most recent stored state of the ballast control from a memory or computer-readable medium employed to store the control state of the ballast. If it is determined that the ballast was in DALI mode prior to powering off, then the method proceeds to 230, where the ballast is controlled (e.g., dimmed and/or brightened) according to received DALI messages, while monitoring for A/D signals that might indicate a switch to 0-10V control mode.

[0037] If it is determined that the ballast was not in DALI mode prior to shutting down, then at 224, the ballast is controlled using A/D signals (e.g., in 0-10V control mode) while monitoring for incoming DALI messages that might indicate a switch to DALI mode. At 226, a determination is made regarding whether a DALI message has been detected. If no DALI message has been detected, the method reverts to 224 for continued 0-10V control of the ballast.

[0038] If a DALI message is detected at 226, then at 228 the ballast is recognized as being in DALI control mode, and the memory is updated to reflect the state of the ballast control. At 230, the ballast is controlled in DALI mode while monitoring for A/D signals that indicate a switch to 0-10V mode. At 232, a determination is made regarding

whether a monitored or detected A/D voltage is less than a predetermined threshold voltage V1 for a predetermined time period T1. In one embodiment, the predetermined threshold voltage is approximately 9V, and the predetermined time period is approximately 20ms. If the detected A/D voltage is not below V1 for at least T1, then the ballast is still in DALI mode and the method reverts to 230 for continued operation in DALI control mode. If the detected A/D voltage is below V1 for at least the time period T1, then the detected voltage is inconsistent with a valid DALI message, the ballast is determined to be in 0-10V control mode, and the memory is updated to reflect that the ballast is in 0-10V control mode. The method then reverts to 224 for 0-10V control while monitoring for DALI messages.

[0039] It will be appreciated that one or more computer-executable algorithms for performing the method of Figure 4 is stored to persistent memory 300 associated with and/or integral to a device employing the ballast or interface circuit 10. For instance, the method may be stored as a series of computer-executable instructions that are recalled form the memory 300 and executed by a processor 302.

[0040] According to an example, the ballast may be powered up and checked for 0-10V and DALI function at a factory site. When the ballast uses its EPROM to save its state during factory testing, the state is simply reset to 0-10V mode during a last functional test.

[0041] In another example, by monitoring the A/D signal or the digital inputs during operation, the signal patterns that indicate a switch between 0-10V and DALI need not be restricted to "legal" 0-10V or DALI commands. The ballast may check for frequencies, patterns, or extended digital bursts that are not part of the normal 0-10V or DALI control "language."

[0042] In the case of high intensity discharge (HID) lamps, the digital ballast can have a delay (e.g., 15 minutes or some other predetermined delay) added between power-up and an initial dimming command (whether it be DALI or 0-10V).

[0043] It is to be appreciated that the foregoing example(s) is/are provided for illustrative purposes and that the subject innovation is not limited to the specific values

or ranges of values presented therein. Rather, the subject innovation may employ or otherwise comprise any suitable values or ranges of values, as will be appreciated by those of skill in the art.

[0044] The invention has been described with reference to the preferred embodiments. Obviously, modifications and alterations will occur to others upon reading and understanding the preceding detailed description. It is intended that the invention be construed as including all such modifications and alterations.

WHAT IS CLAIMED IS:

1. A dual-control analog and DALI interface circuit, comprising:

an isolating inverter circuit that is coupled to a current regulator and a voltage regulator;

microcontroller that is coupled to the isolating inverter circuit, the current regulator, and the voltage regulator; and

a depolarizing circuit that ensures a desired polarity at a rectifier circuit that is inductively coupled to the isolating inverter circuit.

2. The interface circuit as set forth in claim 1, further including a miswiring protection circuit that ensures that the interface circuit operates regardless of the wiring of two interchangeable control wires coupled to the miswiring protection circuit and to a control device.

3. The interface circuit as set forth in claim 1, wherein the depolarization circuit includes a plurality of switches that are selectively engaged depending on a detected configuration of the two control wires to ensure that a polarity across the rectifier circuit remains constant.

4. The interface circuit as set forth in claim 3, further comprising an isolated power supply circuit that drives the plurality of switches.

5. The interface circuit as set forth in claim 4, wherein the isolated power supply circuit is inductively coupled to the rectifier circuit.

6. The interface circuit as set forth in claim 3, wherein the depolarization circuit comprises a comparator that detects a polarity of the two interchangeable control wires and selectively engages the plurality of switches to maintain the constant polarity across the rectifier circuit.

7. The interface circuit as set forth in claim 1, wherein the rectifier circuit is inductively coupled to the isolating inverter circuit.

8. The interface circuit as set forth in claim 1, coupled to a power regulation control circuit of a ballast for a discharge lamp.

9. The interface circuit as set forth in claim 1, further comprising a capacitor in the isolating inverter circuit having a cutoff frequency of approximately 12kHz or greater that permits passage of a DALI signal.

10. A method of providing dual 0-10V analog and DALI control of a ballast circuit for dimming a lighting device, comprising:

powering ON the ballast circuit;

reading control state information stored in memory and describing a control state of the ballast circuit prior to entering an OFF state;

determining whether the ballast circuit was in a DALI control state prior to entering the OFF state;

employing received DALI commands to control the ballast circuit if the ballast circuit was in a DALI control state prior to entering the OFF state; and

employing received analog control commands to control the ballast circuit if the ballast circuit was in an analog control state prior to entering the OFF state.

11. The method as set forth in claim 10, further comprising monitoring incoming control signals for DALI control commands when the ballast is in the analog control state.

12. The method as set forth in claim 11, further comprising detecting a valid incoming DALI control command.

13. The method as set forth in claim 12, further comprising updating the control state information in the memory to indicate that the ballast circuit is in the DALI control state upon detection of the valid DALI control command.

14. The method as set forth in claim 10, further comprising monitoring incoming control signals for analog control commands when the ballast is in the DALI control state.

15. The method as set forth in claim 14, further comprising detecting an incoming analog control command.

16. The method as set forth in claim 15, further comprising updating the control state information in the memory to indicate that the ballast circuit is in the analog control state upon detection of the analog control command.

17. The method as set forth in claim 15, wherein detecting an incoming analog control command comprises:

comparing an analog voltage associated with an incoming control command to a predetermined threshold voltage V1;

determining whether the analog voltage is less than the predetermined threshold voltage V1 for a predetermined time period T1; and

identifying the incoming control command as an analog control command if the analog voltage is less than the predetermined threshold voltage V1 for at least the predetermined time period T1.

18. The method as set forth in claim 17, wherein the predetermined threshold voltage V1 is approximately 9 volts.

19. The method as set forth in claim 17, wherein the predetermined time period approximately 20ms.

20. A computer-readable medium having stored thereon computer-executable instructions for execution by a processor, the instructions including:

reading, upon powering ON a lighting device ballast circuit, control state information stored in memory and describing a control state of the ballast circuit prior to entering an OFF state;

determining whether the ballast circuit was in a DALI control state prior to entering the OFF state;

employing received DALI commands to control the ballast circuit if the ballast circuit was in a DALI control state prior to entering the OFF state;

employing received analog control commands to control the ballast circuit if the ballast circuit was in an analog control state prior to entering the OFF state;

monitoring incoming control signals for DALI control commands when the ballast is in the analog control state;

updating the control state information in the memory to indicate that the ballast circuit is in the DALI control state upon detection of the valid DALI control command;

monitoring incoming control signals for analog control commands when the ballast is in the DALI control state; and

updating the control state information in the memory to indicate that the ballast circuit is in the analog control state upon detection of the analog control command.

21. The computer-readable medium of claim 20, further including stored instructions for detecting an analog control command when the ballast circuit is in DALI control mode, the instructions including

comparing an analog voltage associated with an incoming control command to a predetermined threshold voltage V1;

determining whether the analog voltage is less than the predetermined threshold voltage V1 for a predetermined time period T1; and

identifying the incoming control command as an analog control command if the analog voltage is less than the predetermined threshold voltage V1 for at least the predetermined time period T1.

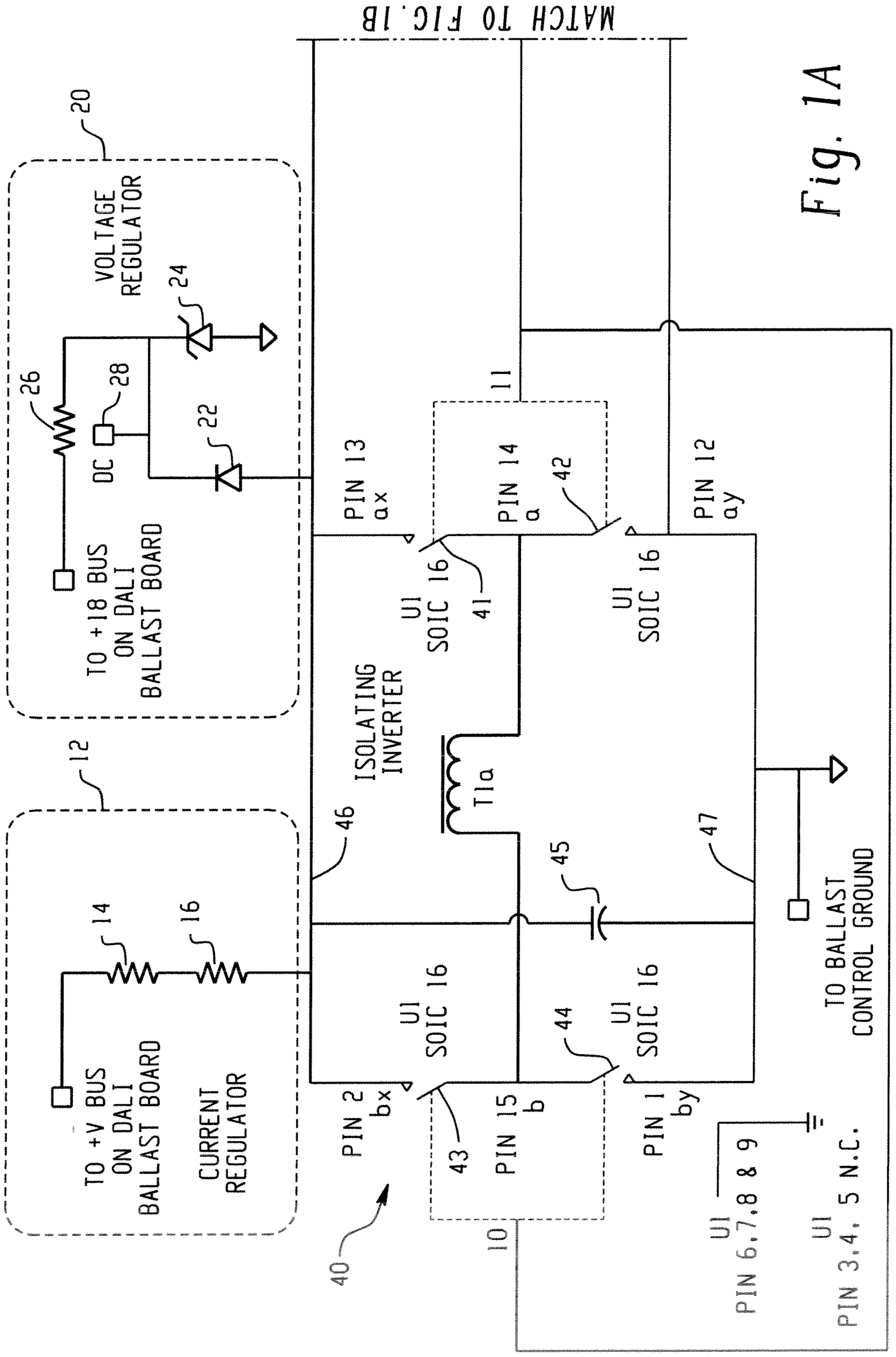
MATCH TO FIG. 1B
20
VOLTAGE REGULATOR
24
26
28
DC
22
TO +18 BUS ON DALI BALLAST BOARD
12
14
16
TO +V BUS ON DALI BALLAST BOARD
CURRENT REGULATOR
11
PIN 13 ax
PIN 14 a
42
PIN 12 ay
U1 SOIC 16
41
ISOLATING INVERTER
T1a
46
45
47
PIN 2 bx
PIN 15 b
PIN 1 by
43
44
40
10
TO BALLAST CONTROL GROUND
U1 PIN 6,7,8 & 9
U1 PIN 3,4, 5 N.C.

Fig. 1A

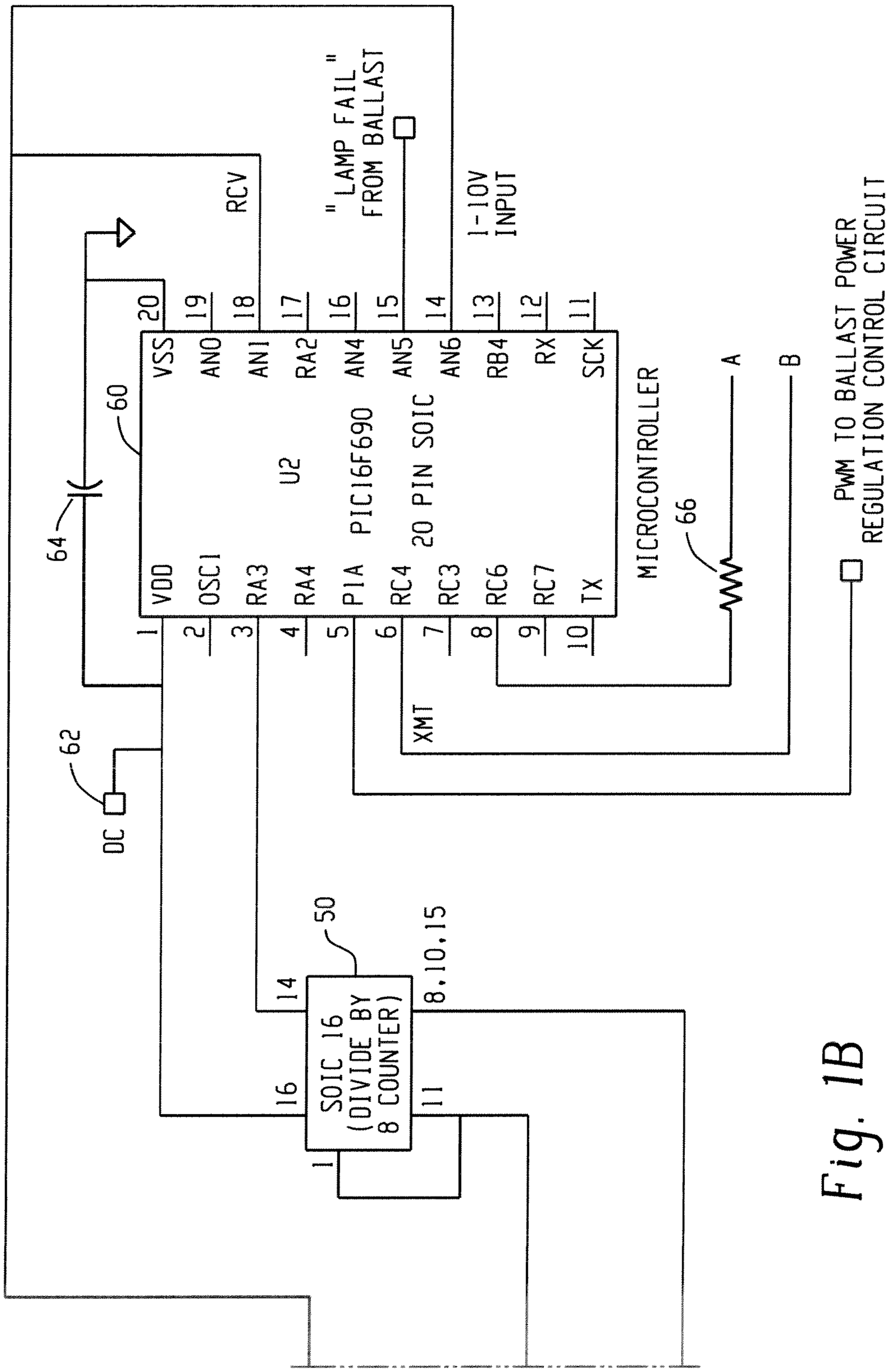
MATCH TO FIG. 1A
SOIC 16 (DIVIDE BY 8 COUNTER)
50
14
16
1
11
8,10,15
62
DC
64
60
U2
PIC16F690
20 PIN SOIC
MICROCONTROLLER
VDD
OSC1
RA3
RA4
P1A
RC4
RC3
RC6
RC7
TX
VSS
AN0
AN1
RA2
AN4
AN5
AN6
RB4
RX
SCK
RCV
XMT
"LAMP FAIL" FROM BALLAST
1-10V INPUT
66
A
B
PWM TO BALLAST POWER REGULATION CONTROL CIRCUIT

Fig. 1B

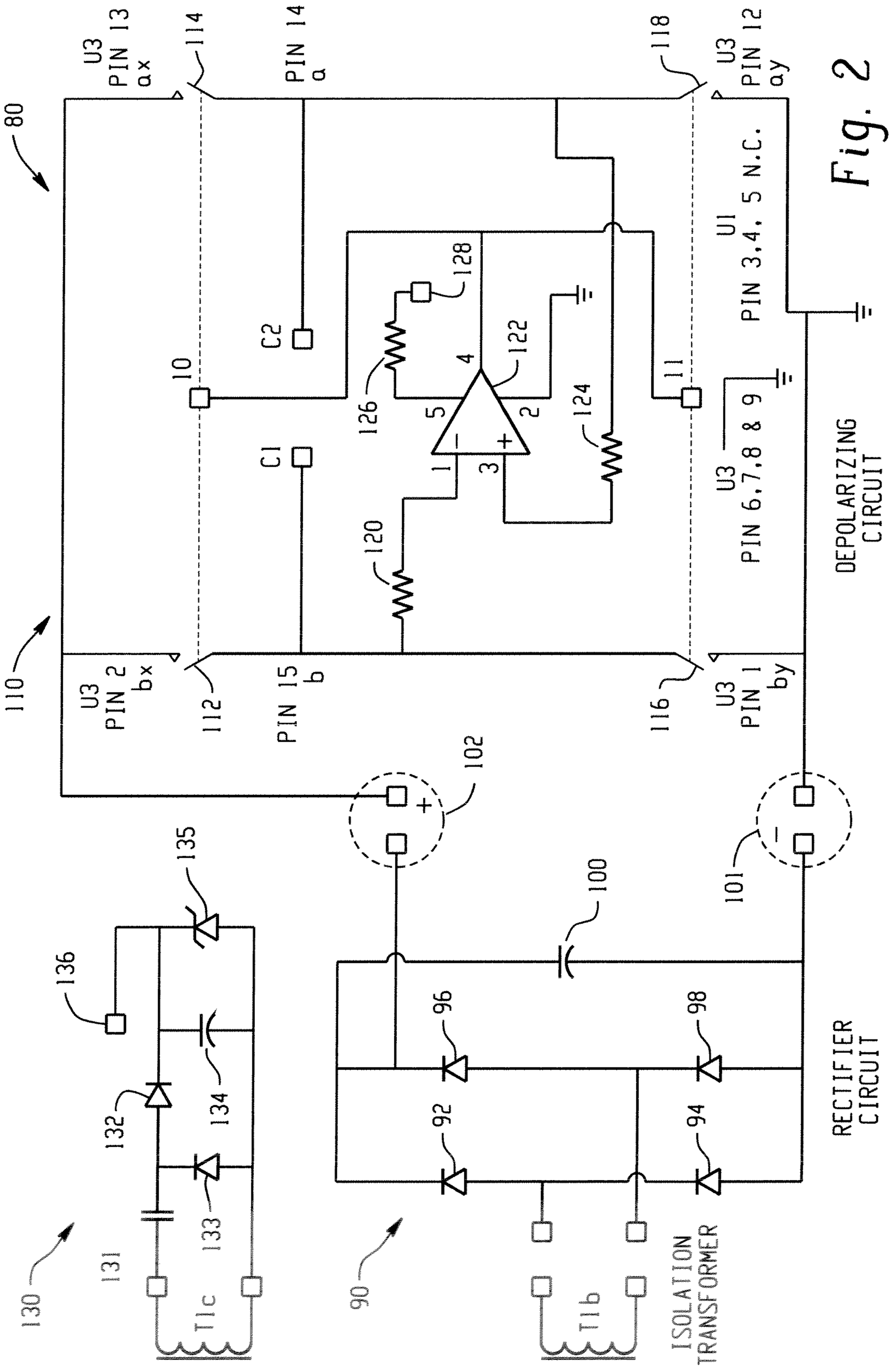
80
U3 PIN 13 ax
114
PIN 14 a
118
U3 PIN 12 ay
C2
128
10
126
122
4
5
2
11
124
C1
1
3
120
U1 PIN 3,4, 5 N.C.
U3 PIN 6,7,8 & 9
DEPOLARIZING CIRCUIT
110
U3 PIN 2 bx
112
PIN 15 b
116
U3 PIN 1 by
102
135
101
100
136
96
98
132
134
92
94
RECTIFIER CIRCUIT
130
131
133
T1c
90
T1b
ISOLATION TRANSFORMER

Fig. 2

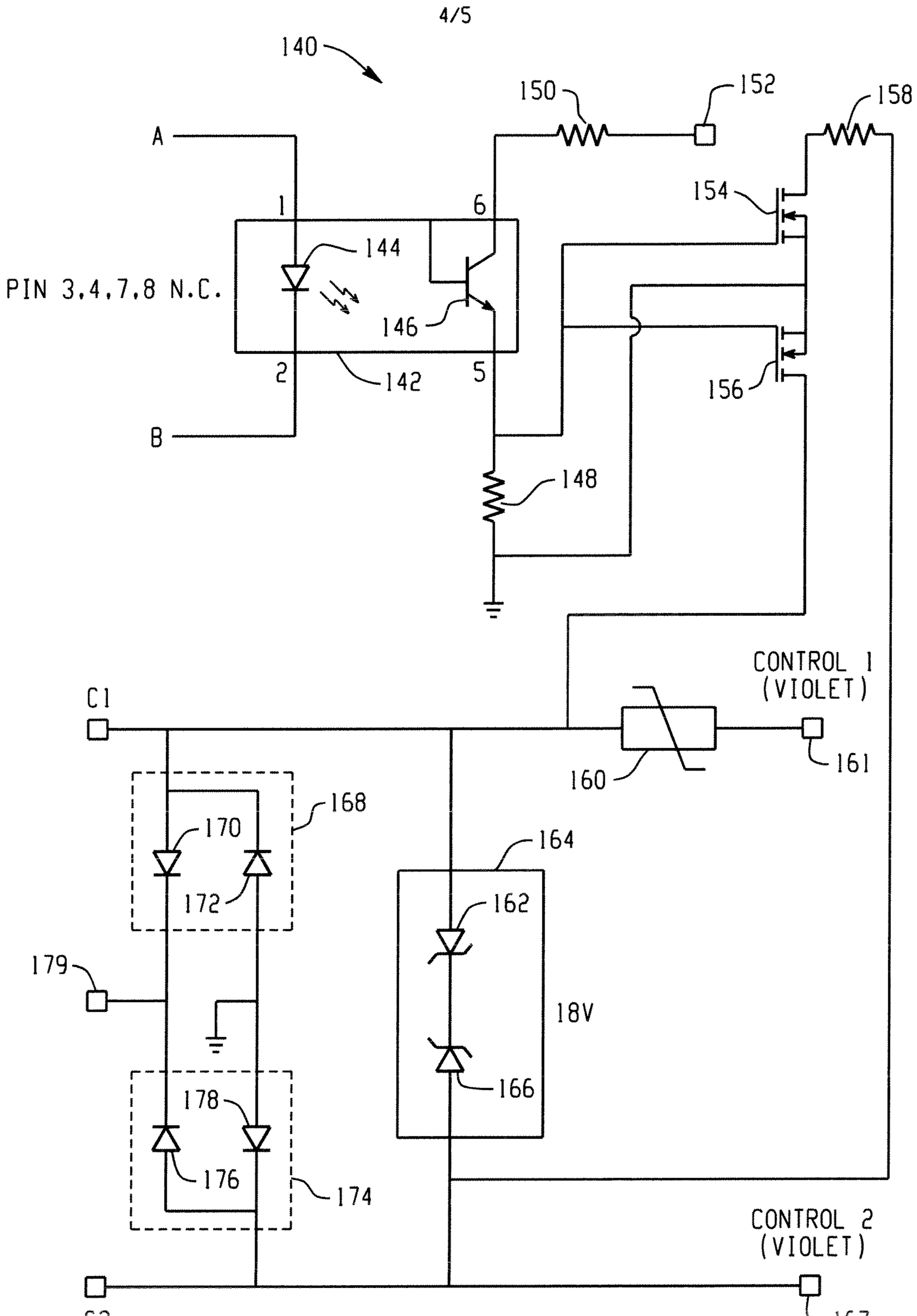
140
150
152
158
A
1
6
154
PIN 3,4,7,8 N.C.
144
146
2
142
5
156
B
148
CONTROL 1
(VIOLET)
C1
160
161
168
170
164
172
162
179
18V
178
166
176
174
CONTROL 2
(VIOLET)
C2
167
MISWIRING PROTECTION CIRCUIT

Fig. 3

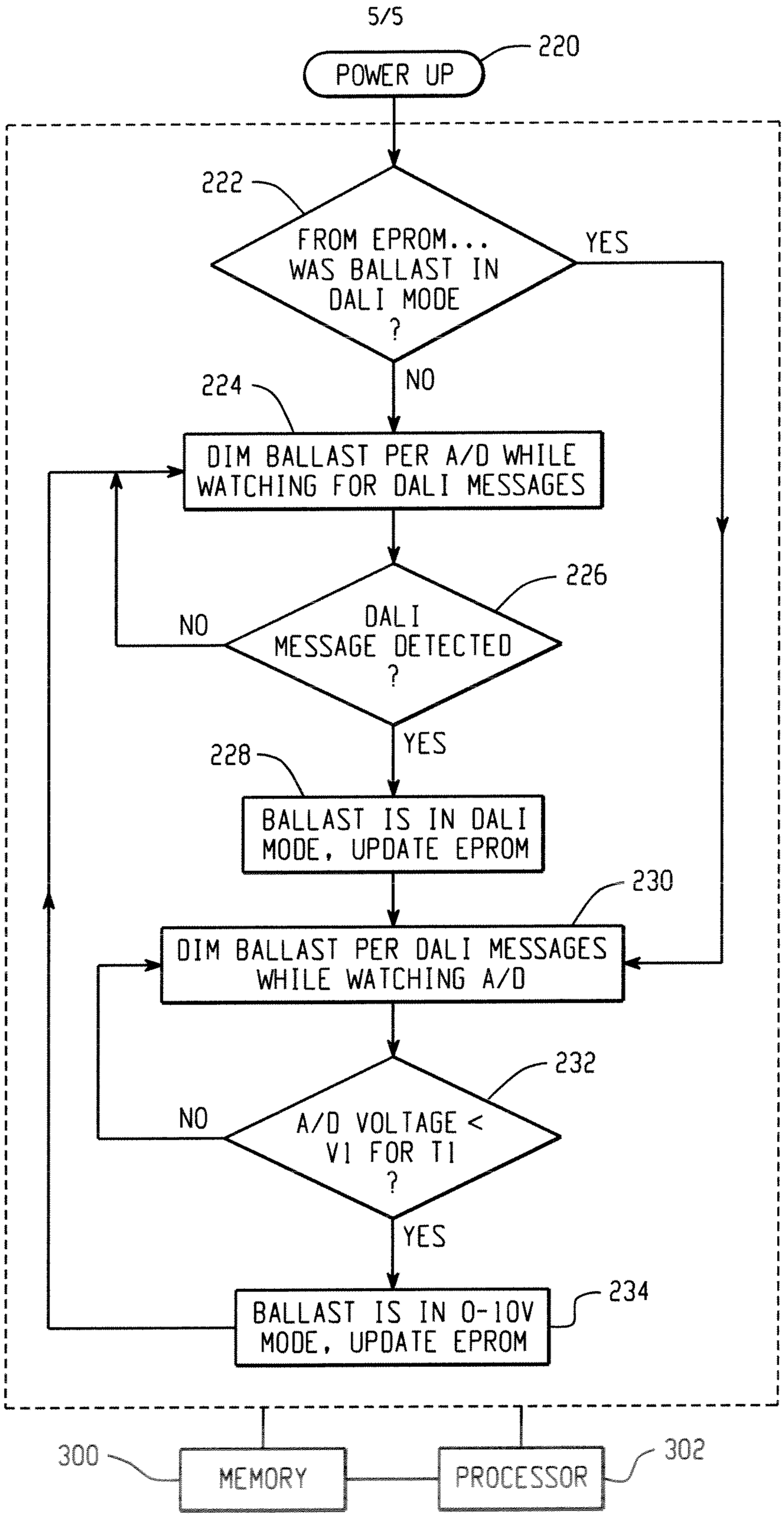
POWER UP
220
222
FROM EPROM... WAS BALLAST IN DALI MODE ?
YES
NO
224
DIM BALLAST PER A/D WHILE WATCHING FOR DALI MESSAGES
226
DALI MESSAGE DETECTED ?
NO
YES
228
BALLAST IS IN DALI MODE, UPDATE EPROM
230
DIM BALLAST PER DALI MESSAGES WHILE WATCHING A/D
232
A/D VOLTAGE < V1 FOR T1 ?
NO
YES
234
BALLAST IS IN 0-10V MODE, UPDATE EPROM
300
MEMORY
PROCESSOR
302

Fig. 4

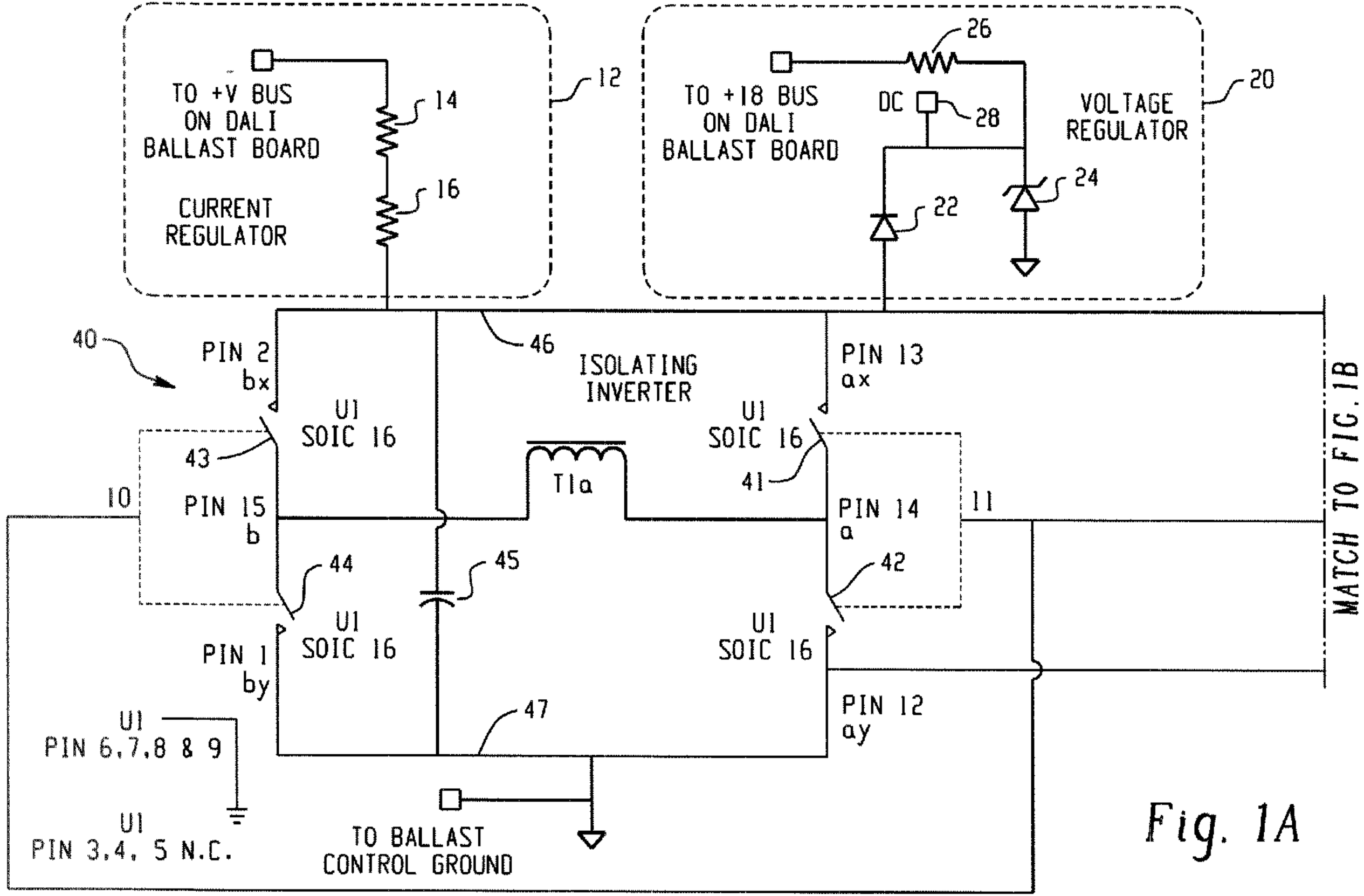
TO +V BUS
ON DALI
BALLAST BOARD
CURRENT
REGULATOR
12
14
16
TO +18 BUS
ON DALI
BALLAST BOARD
26
DC
28
VOLTAGE
REGULATOR
20
22
24
40
PIN 2
bx
U1
SOIC 16
43
46
ISOLATING
INVERTER
PIN 13
ax
U1
SOIC 16
41
T1a
10
PIN 15
b
PIN 14
a
11
44
45
42
U1
SOIC 16
PIN 1
by
U1
SOIC 16
U1
PIN 6,7,8 & 9
47
PIN 12
ay
U1
PIN 3,4, 5 N.C.
TO BALLAST
CONTROL GROUND
MATCH TO FIG. 1B

Fig. 1A