

Jan. 6, 1970

R. J. BRIDGES ET AL

3,487,606

FREQUENCY AND DURATION CONTROL FOR ELECTRODE RAPPERS

Filed April 10, 1968

3 Sheets-Sheet 1

FIG. 1

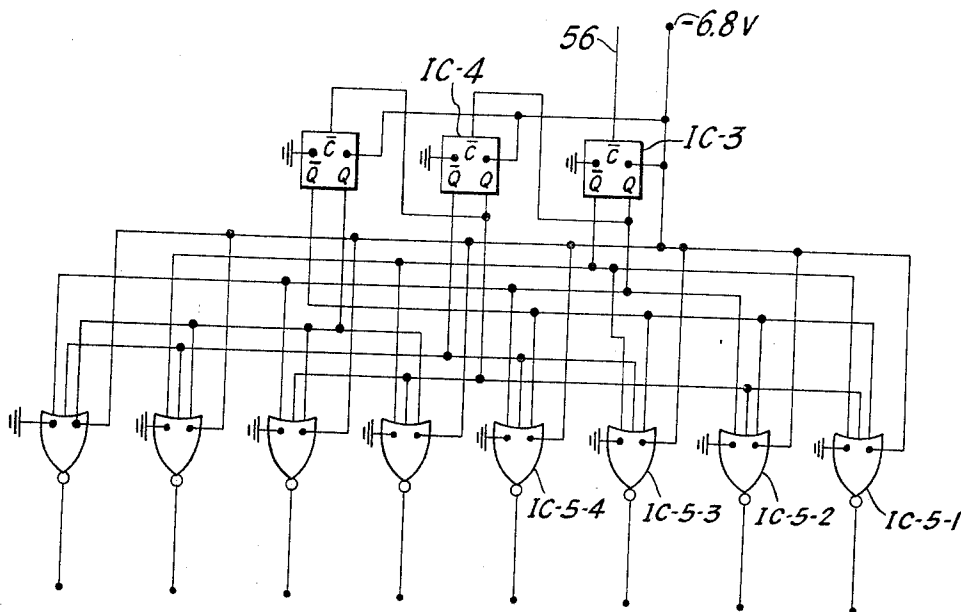
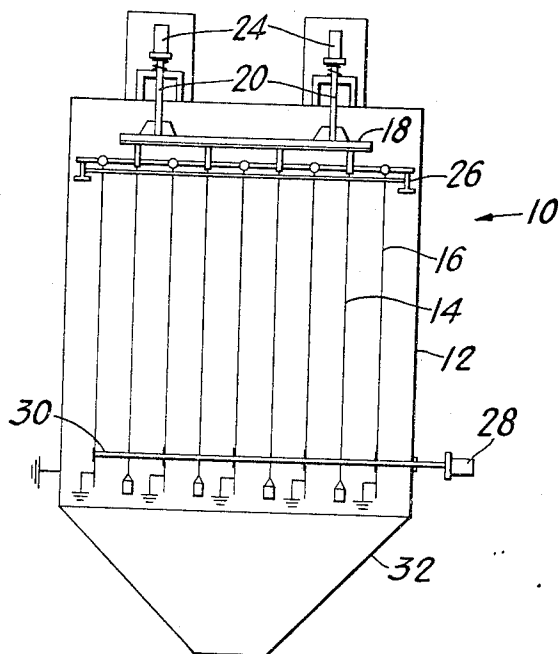


FIG. 4

INVENTORS
RICHARD J. BRIDGES &
PAUL D. HARPER
BY *Bayle C. Dent*
their Attorney

Jan. 6, 1970

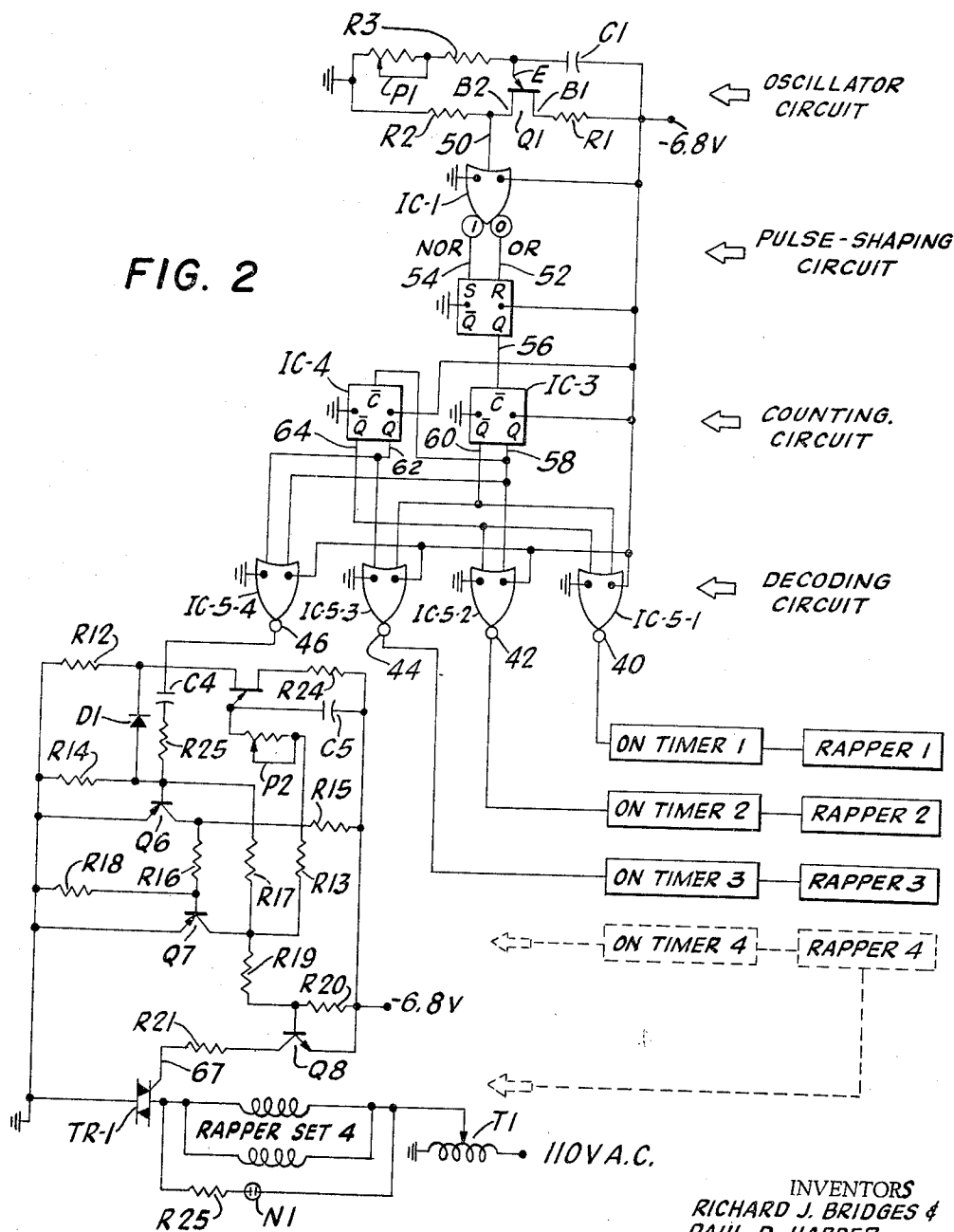
R. J. BRIDGES ET AL

3,487,606

FREQUENCY AND DURATION CONTROL FOR ELECTRODE RAPPERS

Filed April 10, 1968

3 Sheets-Sheet 2



INVENTORS
 RICHARD J. BRIDGES &
 PAUL D. HARPER
 BY *Ray C. Dent*
 their Attorney

Jan. 6, 1970

R. J. BRIDGES ET AL

3,487,606

FREQUENCY AND DURATION CONTROL FOR ELECTRODE RAPPERS

Filed April 10, 1968

3 Sheets-Sheet 3

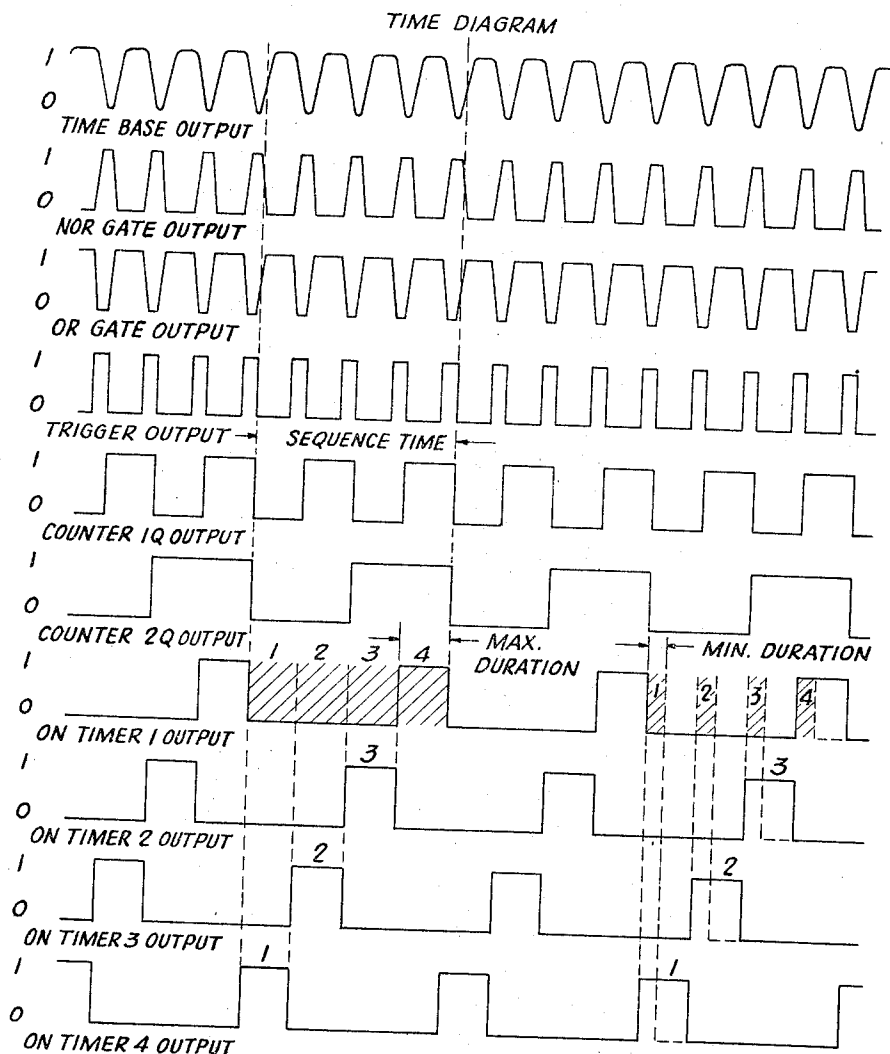


FIG. 3

INVENTORS
RICHARD J. BRIDGES &
PAUL D. HARPER
BY
Boyer C. Dent
their attorney

1

2

3,487,606

FREQUENCY AND DURATION CONTROL FOR ELECTRODE RAPPERS

Richard J. Bridges and Paul D. Harper, Baltimore, Md., assignors to Koppers Company, Inc., a corporation of Delaware

Filed Apr. 10, 1968, Ser. No. 720,416

Int. Cl. B03c 3/74

U.S. Cl. 55—13

21 Claims

ABSTRACT OF THE DISCLOSURE

A solid-state electronic control independently regulates the frequency at which sets of rappers vibrating the electrodes of an electrostatic precipitator are energized and the duration of such energization. A pre-settable sequence timer having a timing circuit produces sequential output pulses at a pre-selected frequency, and a divider network divides the selected frequency into a selected number of equal time bases. The sum of these bases equals the length of the selected frequency. A variable-duration timer network regulates the duration of rapping of the various rapper sets from zero to a maximum time no longer than the selected time base or sequence time so that the duration of rapping of one rapper set does not overlap with the duration of rapping of another set. If desired, the control can include an intensity control for regulating the magnitude of rapper vibration.

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates generally to gas separation and more particularly to rapping means for cleaning the electrodes in an electrostatic precipitator.

Description of the prior art

In a conventional electrostatic precipitator, a particle-laden gas stream is directed through lanes formed by a number of vertically suspended collector electrode plates spaced a short distance apart. A number of discharge electrode wires are suspended along the center of the path of travel of the gas between the collector plates. High voltage applied to the discharge wires forms a corona discharge field between the wires and the plates which ionizes the gas flowing through the fields. The ionization causes the dust particles to become charged and thus attracted to the collector plates. As the particles build up on the plates, they must be removed to maintain efficient collection of the particles on the plates. The conventional way of removing the collected particles is to vibrate or rap the plates.

As the art of electrostatic precipitation developed, it was found that rapping all the collector plates at one time reduced collection efficiency because all the particles fell into collection hoppers at one time causing re-entrainment throughout the precipitator. Eventually, controls were developed which energized selected ones of the plate rappers at intervals and for selected lengths of time to confine re-entrainment to small areas throughout the precipitator. These controls have primarily utilized cam switches, relays, and the like to regulate the sequence at which selected ones of the rappers were energized and to regulate the duration of such energization.

Some of the shortcomings of these heretofore known controls are that they are subject to wear since they contain moving parts such as cams, gears, movable contacts, and the like. They are subject to malfunction from dirt, extremes of temperature and humidity, and the duration of energization of the rappers cannot be adjusted independently of the frequency at which selected rappers

are operated. Thus, as the frequency of energization is lengthened, the longer the sets of rappers will operate. This is not always desirable in a precipitator. For example, under light dust-load conditions, it may be preferable to have a long sequence time between energization of the rapping sets while having a short duration of actual rapping. In order to change the relationship, the controls must be physically dis-assembled and re-arranged. This is both difficult and time-consuming which makes adjustment impractical where the dust-load conditions of the precipitator change frequently.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a control for regulating the frequency and duration of energization for sets of rappers with both the frequency and duration being independently adjustable over wide ranges. These and other objects and novel features are accomplished by providing a solid-state electronic control comprising a sequence timer for producing a time-base output pulse of a selected frequency which is then divided by a divider network into a preselected number of equal time-length pulses which are used to initiate energization of the rappers through an adjustable on-timer network. A timer regulates the length of time that the rappers are energized from zero time up to the maximum time length of the initiating pulse. The control functions sequentially so that following energization of the last set of rappers to be energized, the first set is again energized, and so on.

Being a solid-state device, the control is extremely reliable since it is unaffected by dust, humidity and the like. Life expectancy is increased since there are no moving parts to wear out. Since the duration of energization is independently adjustable with respect to the frequency of energization, it is possible to obtain optimum rapping to suit dust-load conditions within the precipitator.

The above objects and novel features of the invention will appear more fully from the following detailed description when the same is read in connection with the accompanying drawings. It is to be expressly understood, however, that the drawings are not intended as a definition of the invention but are for the purpose of illustration only.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings wherein like parts are marked alike:

FIGURE 1 is a schematic illustration of a portion of a typical electrostatic precipitator having conventional electrode rappers;

FIGURE 2 is an electrical diagram illustrating an embodiment of the rapper control of the present invention;

FIGURE 3 is a time diagram illustrating the voltage waveforms developed by various portions of the rapper control of FIG. 2; and

FIGURE 4 is an electrical diagram illustrating the simple manner in which the control of FIG. 2 may be used to control the operation of a plurality of rapper sets.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The control herein is used for regulating the frequency and duration of rapping of a plurality of rappers usually found in an electrostatic precipitator. When constructed in accordance with this invention, the control can be adjusted to provide sequential energization for sets of rappers at preselected intervals or sequence time within its design limits. A further adjustment is provided to regulate the duration of energization for each set of rappers as they become energized. If desired, the

control may include an intensity control for regulating the magnitude of rapper vibration.

Referring now to FIG. 1, there is illustrated an electrostatic precipitator generally designated by numeral 10. An outer shell 12 directs the flow of particle-laden gases past discharge electrodes 14 and collector electrodes 16. The discharge electrodes are supported by structural members 18 which are themselves supported by hanger rods 20 extending into insulators 22 which electrically isolate the rods from the shell 12 and the collector electrodes 16.

The discharge electrodes 14 are supplied with high voltage electric current by means of a conventional system (not shown). A suitable system, for example, is illustrated in Thomas et al. Patent No. 2,961,577.

As the particle-laden gas passes through shell 12, the particles are charged in the ionization field between the discharge electrode wires 14 and collector plates 16. The charged particles migrate toward the flat surfaces of plates 16 and collect thereon. These collected particles must be removed periodically to maintain efficient collection.

A rapping source 24 is connected to the hanger rod 20 so that vibrations generated by the rappers 24 are transmitted to the electrodes 14 through the structural members 18. A suitable rapper is shown and described in John W. Pennington Patent No. 3,030,753. Briefly, these rappers generate vibrations from a hammer which is reciprocated by pneumatic pressure. The pressure is supplied when an electric solenoid is energized by a control circuit such as, for example, the control of the present invention.

The collector electrodes 16 are supported by structural members 26 which are an integral part of shell 12. Electrodes 16 are also rapped by a rapping source 28, similar to rappers 24, connected to the electrodes 16 by a rod 30. Thus, when the rappers are energized, the electrodes are vibrated thereby dislodging accumulated dust particles which fall into a hopper 32 from which they are periodically removed.

As viewed in FIG. 1, the particle-laden gas is flowing between the lanes formed by collector plates 16 and away from the observer. The lanes may be several feet long so that several rappers 24 may be positioned along the lanes one behind the other. Rappers 28 will be similarly positioned. Thus, it can be seen that if all the rappers along a lane are energized at one time, re-entrainment of dust particles will occur along the entire length of the lane. Accordingly, it is preferable to energize only the two rappers 24 in lateral alignment at the same time to reduce re-entrainment of the collected particles. The downstream pairs of rappers are rapped in sequence.

To further reduce re-entrainment, it is preferable to rap the collector plates 16 at different times when the electrode wires 14. Accordingly, a pair of rappers 28 may be connected to form a set, the pair or set is energized at the same time. The control herein can be connected to energize a first set of rappers 24 and then a first set of rappers 28 and then a second or different set of rappers 24 and so on. The control to be described is shown with four outputs for controlling the energization of four sets of rappers as just described.

The control shown in FIG. 2 is provided with four outputs 40, 42, 44, and 46 which operate in sequence at a frequency which can be easily varied. The frequency is divided into four equal time segments; one segment for each output. Each output is connected respectively to rapper sets 1, 2, 3, and 4 through an on-timer network. The on-timer network includes an adjustment to reduce the time length of each segment from its maximum length of one-fourth the frequency. Thus, the frequency or interval of rapping occurrences can be preselected and the duration of rapping can also be controlled. Since the two adjustments act independently of one another, energization of the rappers can be controlled to suit conditions within the precipitator.

The preferred construction of the control of the present invention includes an adjustable oscillator for producing

an output pulse at a selected time interval or frequency, a wave shaper for modifying the voltage characteristics of the oscillator output pulse, a trigger for further modifying the output pulse of the wave shaper, a pair of counters for modifying the time length of the trigger pulses, and a decoder for producing four sequential output pulses for driving four on-time circuits which in turn control the energization of four rapper sets. An added feature provides an intensity control for regulating the magnitude of rapper vibration. The portion of the circuit preceding the on-timers can be generally classed as a sequence timer.

The drawing of FIG. 2 is a composite of a solid-state logic diagram and an ordinary electrical schematic showing wiring connections and the like. To simplify the explanation, both the construction and operation of the control will be described concurrently.

Referring now to FIG. 2, the sequence timer is an internally timed device which provides signal pulses to each on-timer network in sequence at a preselected frequency. The first portion of the sequence timer is an oscillator circuit which produces pulses at a preselected frequency. The oscillator circuit consists of a unijunction transistor Q1, a capacitor C1, resistors R1, R2 and R3, and a potentiometer P1. The series combination of resistor R3, potentiometer P1, and capacitor C1 form an R-C timing network.

A common power supply voltage of minus 6.8 volts is advantageously used throughout the control since this voltage is compatible with easily available logic elements such as flip-flops and NOR gates. The supply voltage (V) is applied across the R3, P1, and C1 combination at time=0. The emitter voltage (VE), of transistor Q1, will be equal to voltage (V) at time=0. For time greater than 0, the voltage across capacitor C1 will increase in the conventional manner. Thus, the emitter voltage (VE) of transistor Q1 will begin decreasing toward ground. As the emitter voltage reaches a fraction of the supply voltage, as determined by the characteristics of transistor Q1, the resistance of the base 1 to the emitter junction of Q1 will decrease rapidly from its previously high value to a relatively low value. This causes the charge on capacitor C1 to dissipate rapidly through the base 1-emitter junction of Q1 and resistor R1. Resistor R1 is included in the circuit to limit this surge of current below a damaging value in the base 1-emitter junction of transistor Q1. Since the base 1-base 2 junction of Q1 is effectively resistive, when the resistance of base 1 decreases rapidly, the circuit formed by the base 1-base 2 resistance of Q1 and resistors R1 and R2 changes its total resistance quickly. This causes a voltage pulse to form across resistor R2 because of the increased current flowing from resistor R1 through transistor Q1 to resistor R2. When the voltage across capacitor C1 decreases to a small value, the base 1-emitter junction of Q1 reverts back to a large resistance and, because of a diode-like effect in the emitter region of the transistor, the emitter current becomes very small. At this time, the capacitor C1 again begins charging through resistor R3 and potentiometer P1 and the cycle is repeated. The cycle time depends entirely on the values of capacitor C1, resistor R3 and potentiometer P1. One skilled in the art can easily select these values to give a pulse frequency which, in the preferred embodiment may range from 24 pulses per minute to 2 pulses per minute. The potentiometer P1 can be easily adjusted to produce the pulse frequency desired within the designed range, and if desired a dial can be provided with potentiometer P1 to indicate the pulse rate.

The output voltage pulses from the oscillator circuit just described will appear on line 50 and will resemble the pulses shown in FIG. 3 and labeled time base output.

The pulses in line 50 are fed to the wave shaping circuit which shapes the pulse into a suitable form to trigger the counters preceding the decoder. The wave shaper comprises two integrated circuits IC-1 and IC-2. IC-1 is a

5

NOR-OR logic gate and IC-2 is a set-reset logic flip-flop. Gate IC-1 with both NOR and OR outputs is needed because the flip-flop IC-2 requires two inputs to provide the proper trigger pulse characteristics to drive the decoder. Gate IC-1 can be dispensed with if a different type of frequency generator is used which provides two outputs similar to the outputs of gate IC-1.

For a full description of the characteristics of the gate IC-1 and flip-flop IC-2, reference may be made to Bulletin DS-9046 R1 published in October, 1966 by Motorola Semiconductor Products, Inc., Box 955, Phoenix, Arizona 85001. This Bulletin describes the MECL series of digital integrated circuits which can be satisfactorily used in the present control.

Gate IC-1 has two input logic states designated "0" and "1." Gate IC-1 may have several inputs depending on the configuration used by the particular IC manufacturer. Any inputs except the one used are connected to a "0" logic level to isolate them from external noise. The truth table for IC-1 is as follows:

Input	Outputs	
	Nor	or
0-----	1	0
1-----	0	1

The OR output assumes the same logic level as the input while the NOR output assumes the complement. IC-2 requires two complementary inputs. It functions best when these inputs are matched with respect to time and logic level. IC-1 performs the pulse-shaping function required to establish the matched complementary inputs to IC-2.

Resistor R2 in the oscillator is biased such that the voltage across it during the charging cycle of capacitor C1 represents a logical "1." The NOR output 52 and the OR output 54 of IC-1 are logical "0" and "1" respectively. When transistor Q1 fires and capacitor C1 begins to discharge, the voltage across resistor R2 assumes a value corresponding to a logical "0." When this occurs, the NOR and OR outputs of IC-1 switch in a complementary manner to their logical opposites, i.e. "1" and "0" respectively.

The NOR and OR voltage outputs of gate IC-1 will appear in lines 54 and 52 similar to the pulses shown in FIG. 3 and labeled NOR gate output and OR gate output.

IC-2 is an R-5 flip-flop with a truth table as follows:

Inputs		Outputs	
R	S	Q ^{N+1}	$\overline{Q}^{N+1}$
0	1	1	0
1	0	0	1
0	0	Q ^N	$\overline{Q}^N$
1	1	N.D.	N.D.

where Q^{N+1} refers to the logic state occurring at the output after the input has been applied.

Since the R-S inputs from IC-1 are always complementary, the last two conditions in the truth table for IC-2 can be disregarded. The NOR output 54 of gate IC-1 is connected to the Set-input of flip-flop IC-2 and the OR output 52 is connected to the Reset-input of IC-2.

During the charging cycle of capacitor C1 in the oscillator, the Q output 56 of IC-2 remains in a logical "0" state. When transistor Q1 fires, the pulse developed across resistor R2 causes gate IC-1 and flip-flop IC-2 to change states so that the Q output 56 assumes a logical "1" state. After capacitor C1 discharges, Q output 56 switches back to a logical "0" state where it remains until the next pulse occurs. Due to the inherent regenerative switching action of IC-2, it provides an extremely fast rise time pulse at its outputs. This fast rise time is necessary for the positive, unambiguous triggering of the succeeding stages of the circuit. Thus, the oscillator and wave shaping circuits produce a sequence of pulses of predetermined

6

shape on the output 56 of IC-2 of which the sequence time may be varied by the setting of potentiometer P1. The pulses on output line 56 will resemble those shown in FIG. 3 and labeled trigger output.

The next portion of the sequence timer is a sequencing circuit including two counters IC-3 and IC-4 which divide the triggering pulse series frequency on line 56 into a number (N) of shorter pulse series which contains pulses of equal time duration. N represents the number of sets of rappers to be energized in sequence, for example, four sets as shown in FIG. 2. Since four sets are to be energized, there must be four outputs from a decoder (to be subsequently described). The decoder is driven by two flip-flops, IC-3 and IC-4, which form the counter circuit. Thus, if each N output is to fire at a frequency of f firings per minute, for example 15, then the oscillator must produce a frequency of N×f (4×15) firings per minute.

The sequencing circuit comprises a pair of counters IC-3 and IC-4 which count the timing circuit pulses on line 56 and then produce a different binary number for each pulse. The N(4) different binary numbers are then converted into N(4) different outputs by a decoder including N(4) logic gates. Each output 58, 60, 62, and 64 of the counters remains at logical "0" until the counter produces the proper binary number and then the output changes from a logical "0" to a logical "1." When another timing pulse occurs, the logical "1" changes back to logical "0" and another of the four outputs changes from "0" to "1." Thus, the sequencing circuit will produce N different sequenced outputs, for example, four outputs as shown in FIG. 2. The circuit automatically shifts back to the first output 58 after the last output pulse on line 64 and the sequence repeats itself.

The counters are two A.C. coupled J-K flip-flops IC-3 and IC-4 operating in a clocked mode. The Q and $\overline{Q}$ outputs are normally in logical "1" and Logical "0" states respectively, when a "0" to "1" transition occurs at the input $\overline{C}$, the Q and $\overline{Q}$ outputs change to their complementary states. For a "1" to "0" transition, the outputs Q and $\overline{Q}$ do not change. The number of flip-flops needed to count N binary numbers can be calculated as follows: $2^{n-1} < N \leq 2^n$.

For example, if N=, 8=2ⁿ, then n=3 flip-flops needed. If N is not equal to an integer exponent of 2, the number of flip-flops needed will produce more than N counts. In this event, only N counts are utilized and the remaining outputs are not used. The sequencing circuit must be constructed so that it returns to the first count after the last count has occurred. For example, if N=6, 2²<6<2³, and n= 3 again, two of the outputs will not be used since three flip-flops can produce eight binary outputs. However, if all the possible counts N for a number of flip-flops n are used, the counter will automatically return to the first count after the last count has occurred.

FIG. 2 illustrates a four-count sequence timer and FIG. 4 illustrates an eight-count sequence counter. Referring to FIG. 2 for the moment, two J-K flip-flops are necessary to obtain four-count output because 2ⁿ=4 or n=2. The Q output 58 of IC-3 is connected to the clock input $\overline{C}$ of the second flip-flop IC-4 to get the correct count. The number of digits in binary numbers is equal to the number of flip-flops. For flip-flops IC-3 and IC-4, the following truth table applies:

Clock pulse	IC-3		IC-4	
	Q	$\overline{Q}$	Q	$\overline{Q}$
0-----	1	0	1	0
1-----	0	1	1	0
2-----	1	0	0	1
3-----	0	1	0	1
4-----	1	0	1	0

There are four distinct two-digit numbers: 11, 01, 10, and 00 from the Q outputs. The $\overline{Q}$ numbers are complements of the Q numbers.

The decoder portion of the circuit shown in FIG. 2 is used to convert the binary outputs of counters IC-3 and IC-4 to a decimal output for driving the rapper sets in sequence through the on-timer circuits. The decoder includes one NOR gate for each rapper set, for example, IC-5-1, IC-5-2, IC-5-3, and IC-5-4 as shown in FIG. 2 for a system having four rapper sets. These NOR gates are connected to the flip-flops IC-3 and IC-4 so that each pulse will cause only one gate at a time to change states. The number of inputs to each gate is determined by the length of the numbers. For example, if four gates outputs are required, two counters are required so the number of gate inputs is two (FIG. 2). If eight gate outputs are required, three counters are required so the number of gate inputs is three (FIG. 4).

Referring to the following truth table for a NOR gate, the only time this gate has a "1" output is when all inputs are at logical "0."

Inputs	NOR outputs
0	0
0	1
1	0
1	1

The same holds true for gates IC-5-1 through IC-5-4. Thus, in the table, the "0" digits in any number are connected to the inputs of the gate assigned to that number. For example, the first gate IC-5-1 is connected to the $\bar{Q}$ outputs of IC-3 and IC-4; the second gate IC-5-2 is connected to the $\bar{Q}$ output of IC-4 and to the Q output of IC-3 and so on. Thus, as the counters form the different binary numbers, one decoder gate at a time will have a "1" output; the remaining outputs will be "0."

By following the foregoing procedures, it is possible to obtain any number of counts desired.

Referring now to the time diagram of FIG. 3, the trigger output pulses on line 56 are of square-wave configuration. This shape is obtained because the flip-flop IC-2 changes state only when input voltage from gate IC-1 reaches a selected magnitude. Thereupon, the output voltage from IC-2 rises immediately to its upper limit where it will remain until IC-1 again changes state because of reduced magnitude input voltage.

The flip-flop IC-3 is designed to change state once from each trigger pulse from IC-2. Thus, the output pulse in line 58 from IC-3 changes from "0" to "1" in response to a first input pulse and from "1" to "0" in response to a second input pulse from IC-2. Accordingly, there is one output pulse in line 58 for each two input pulses in line 56. The output 60 from line IC-3 is merely the complement of output 58. The input to IC-4 is from the Q output 58 of IC-3; thus, IC-4 changes state once from each two pulses from output 58. Accordingly, IC-4 produces one output pulse from each four trigger pulses from output 56 of IC-2. Output 64 is merely the complement of output 62 of IC-4. These pulses are illustrated in FIG. 3 and labeled counter 1 output and counter 2 output.

The changes in state of IC-3 occur only on one side of the input pulse from IC-2 because of the input coupling design of the flip-flop. In the preferred embodiment, the change occurs on the downside of the input pulse because the system operates from a negative power supply. IC-4 operates in the same manner.

By coupling the outputs from IC-3 and IC-4 to the NOR gates IC-5-1 through IC-5-4 as outlined above, the outputs 40, 42, 44, and 46 of the gates will operate in sequence. The sequence shown in FIG. 3, labeled on-timer outputs, represents the inputs from NOR gates IC-5-1 through IC-5-4 to the on-timers as well as the outputs of the on-timers when no adjustment of the on-timer has been made to reduce the on-time. The dotted line projections and cross-hatching on the left side of FIG. 3 illustrate that the sum of the individual NOR gate output times equals the total sequence time.

If it were not desirable to be able to vary the duration that each rapper remained on, the outputs 40, 42, 44 and 46 could be coupled directly to the rapper sets without additional circuitry. Thus, if the frequency were lengthened by adjusting potentiometer P1, each rapper set would remain energized for a longer period, i.e., for one-fourth the frequency. However, as previously explained, this is not desirable. Accordingly, the outputs from the NOR gates are used to drive an on-timer circuit which in turn drives the rapper sets.

FIG. 2 illustrates in detail only one on-timer network since all are identical. To show the relationship of the on-timer, which is illustrated in detail, in the system, it is also indicated by dotted line blocks. The remaining on-timers appear as blocks appropriately labeled.

The on-timer network determines the length of time that the rapper sets are energized for rapping after the sequence timer provides the signal for rapping to begin. The dotted line projections and cross-hatching on the right of FIG. 3 indicates that the minimum time, during which rapping can occur, approaches zero.

The on-timer network includes three fundamental portions: a timing circuit which determines on-time; a bistable flip-flop which changes state when a signal from the sequence timer occurs and changes state again when the timing circuit provides a signal indicating that the selected time has elapsed; and, a power amplifying stage which provides the desired power output from the on-timer.

Referring to FIG. 2, transistors Q6 and Q7 along with resistors R14, R15, R16, R17, R18, R19, and R20, form the bistable flip-flop. C4 and R25 form the coupling network which carries the signal from the sequence timer to the flip-flop. Transistor Q8 along with resistors R19, R20, and R21 form the power amplifying circuit. Unijunction transistor Q5, along with base resistors R24 and R12, timing capacitor C5, timing resistor R13, and timing potentiometer P2 form the timing circuit.

When the on-timer is in the off state, the flip-flop circuit is biased such that Q6 is in a saturated mode and Q7 is biased off (non-conducting). When Q7 is off, the current through R19 and R20 is very small and the voltage drop across these resistors is small. Two conditions exist when the flip-flop is in this state. First, the base to emitter voltage of Q8 is small and insufficient to cause Q8 to conduct. Thus, no current flows to the output 67 of the on-timer. Secondly, the collector-emitter voltage of Q7 is approximately the power supply voltage. V. The C5-R13-P2 series combination thus has a small voltage across it and C5 remains effectively discharged.

The signal from the sequence timer through C4 and R25 is such that it drives Q6 off. Resistor R12 is biased such that the voltage developed across R12 is less than the base-emitter junction voltage of Q6 when Q6 is not in saturation. Thus, the voltage across R12 will cause diode D1 to be back biased so that Q6 remains out of saturation. The collector voltage of Q6 rises sharply, biasing Q7 on through R16 and R18. The collector voltage of Q7 drops to a small value, biasing Q6 off through R17 and R16 through regenerative action. Also, current flows through R19 and R20, biasing Q8 such that it saturates, providing output current through R21. As the collector of Q7 drops to a small voltage with respect ground, the C5-R13-P2 combination sees almost all the supply voltage. C5 begins to charge along an exponential R-C charging curve. When the voltage on C5 reaches a fraction of the voltage across C5-R13-P2 determined by Q5, Q5 will "fire" and a pulse will form across R12. The operation is much the same as the oscillator circuit in the sequence timer. The pulse across R12 is coupled through D1 to the base of Q6, turning it on and taking Q7 and Q8 out of saturation. Most of the charge on C5 is dissipated through current limiting resistor R24. The remaining charge dissipates through R13 and P2 when

the collector voltage of Q7 becomes approximately equal to the supply voltage. This represents one on-time cycle. The circuit will remain in the off state until another signal from the sequence timer occurs.

If for some reason the pulse across R12 does not saturate Q6 and turn Q7 and Q8 off, the signal from the sequence timer which occurs when the sequence timer switches to the next on-timer will cause Q6 to saturate. This signal is the change in voltage which occurs when the sequence timer switches from a logical "1" to logical "0." However, if Q6 is already saturated, this signal will have no effect on the on-timer. Thus, a safety feature is provided to prevent the rapper sets and associated circuitry from sticking "on" for extended periods of time, causing possible damage. This also prevents overlapping of rapper sets if the on-times are set longer than the period of the sequence.

A triac switch TR-1 is driven by the on-timer network for switching current through the rappers to ground and off at a signal from the on-timer. (Triac is the designation for a silicon gate-controlled A.C. switch such as, for example, R.C.A. No. 40576, 15 amp, described in R.C.A. File No. 300 published in October, 1967). The on-timer provides a direct-current signal which causes the triac TR-1 to conduct current from a 110 v. A.C. transformer T-1 through the rappers of the set to ground thereby energizing each rapper. The advantage of using the triac TR-1 is that it has the current capability, along with extended life inherent in its solid-state design, needed to operate a set of rappers.

Transformer T-1 may be of the variable type so that by varying its output, the intensity of the rapping vibrations can be selected for optimum performance.

A neon indicator N-1 and a complementary resistor R-25 are placed in parallel with the rapper set to indicate, at a remote location for example, that the rapper set is operating.

The foregoing describes the construction and operation of a solid-state electronic control system for regulating the frequency and duration of rapping the electrodes in an electrostatic precipitator. Both frequency and duration are independently and easily adjustable by merely turning adjustment screws on potentiometers P1 and P2 respectively. The capability of independent adjustment is extremely advantageous since it enables an operator to select the mode of rapping best suited for conditions within the precipitator. The control is reliable since it does not include moving parts normally subject to wear nor other parts which would be affected by humidity, dust, temperature and the like. Another advantage is that the control can be adapted for automatic operation in response to conditions within the precipitator. For example, the potentiometer P1 in the oscillator circuit can be replaced by a transistor circuit so that the emitter voltage of the transistor varies in response to a control signal from within the precipitator to change the frequency at which pulses are produced by the oscillator. The control signal can be a signal, for example, from the current supply to the electrodes, it being understood that the current supplied usually varies in proportion to the dust loading of the precipitator.

The potentiometer P2 can likewise be modified to respond to a control signal for varying the on-times of the rappers.

Thus, the invention having been described in its best embodiment and mode of operation, that which is desired to be claimed by Letters Patent is:

1. An electrostatic precipitator for removing particles from a gas comprising:
 - discharge electrodes for applying an electrostatic charge to said particles,
 - collecting electrodes for receiving said particles,
 - rappers operable upon energization for vibrating said collector electrodes for removing the collected particles from said collecting electrode, and

a solid-state electronic control for energizing said rappers, said control including means for varying the sequence of energization of said rappers.

2. The apparatus of claim 1 wherein said control also includes means for regulating the duration of energization of said rappers.

3. The apparatus of claim 2 wherein said control includes further means for independently varying the means for regulating the sequence of energization and the means for regulating the duration of energization.

4. An electrostatic precipitator for removing particles from a gas comprising:

- a plurality of discharge electrodes for applying an electrostatic charge to said particles,
- a plurality of collecting electrodes for receiving said particles,
- a plurality of sets of rappers operable upon energization for vibrating associate collecting electrodes for removing collected particles therefrom, and
- an electronic control for energizing selected sets of said rappers, said control including means for varying the sequence of energization of said sets of rappers.

5. The apparatus of claim 4 wherein said control includes means for varying the duration of said energization.

6. An electrostatic precipitator having electrodes therein and including a control system for rapping of said electrodes comprising:

- a plurality of rappers adapted for vibrating engagement with said electrodes;
- a pulse generating circuit for producing first pulses at a selected frequency;
- a counting circuit driven by said first pulses for dividing said first pulses into a pre-selected number of second pulses; and
- a decoder circuit driven by said second pulses for sequencing said second pulses; and energizing said rappers sequentially by said second pulses, whereby said rappers vibrate said electrodes in sequence.

7. The control system of claim 6, and in addition:

- a pulse-shaping circuit driven by said first pulses for producing shaped pulses having first and second logic levels.

8. The control system of claim 6, and in addition:

- an on-timer circuit driven by said second pulses and connected to said rappers for regulating the duration of energization of said rappers.

9. The control system of claim 6 wherein said pulse generating circuit includes a first adjusting means for varying the frequency at which said first pulses are produced.

10. The control system of claim 8 wherein said on-timer circuit includes a second adjusting means for varying the duration of said second pulses,

- whereby the length of time that said rappers are vibrated is controlled by said on-timer circuit.

11. The control system of claim 6, and in addition:

- a switching circuit operable in response to said second pulses for connecting a current supply to said rappers during the time length of said second pulses.

12. The control system of claim 6, and in addition:

- a variable-intensity control in the current supply circuit for said rappers for regulating the magnitude of vibration of said rappers.

13. An electrostatic precipitator having electrodes, rappers therefor, and an electronic logic control for regulating the frequency and duration of rapper energization comprising:

- an oscillator circuit for producing a series of first pulses at a selected frequency;
- a pulse shaping circuit driven by said first pulses for producing a series of second pulses having first and second logic levels;
- a counting circuit operative in response to said first and second logic levels of said second pulses for

dividing said second pulses into a preselected number of third pulses having first and second logic levels; a decoder circuit operative in response to said first and second logic levels of said third pulses for producing a series of fourth pulses having first and second logic levels, said fourth pulses being arranged to follow one another in timed sequence along a separate channel for each such pulse; and

an on-timer circuit having corresponding channels for connecting said fourth pulses to respective ones of said rappers for the energization thereof,

said on-timer circuit having control means for regulating the duration of energization of said rappers.

14. The control of claim 13 wherein said oscillator circuit includes a first adjusting means for varying the frequency at which said first pulses are produced.

15. The control of claim 14 wherein said on-timer circuit includes a second adjusting means for varying the duration of said fourth pulses to regulate the on-time of said rappers, said second adjusting means operative independently of said first adjusting means.

16. The control of claim 15 wherein said counting circuit includes first and second counters of which the first is responsive to said second pulses for producing a first series of complementary sets of said third pulses and said second counter is responsive to a series of one of said sets of complementary pulses for producing a second series of complementary sets of said third pulses, said decoder circuit being responsive to said first and second series of complementary sets of third pulses.

17. The control of claim 16 including means for regulating the intensity of said energization.

18. An electrostatic precipitator having electrodes, rappers therefor, and an electronic logic control for regulating the frequency and duration of energization for a plurality of rappers in an electrostatic precipitator, comprising:

an oscillator circuit for producing a series of voltage pulses at a selected frequency and including a potentiometer for varying the frequency of said voltage pulses;

a pulse-shaping circuit driven by said voltage pulses for producing a series of binary pulses, said pulse-shaping circuit including a binary flip-flop driven by a NOR gate having dual outputs;

a counting circuit operative in response to said series of binary pulses for dividing each of said binary pulses into a preselected number of equal time-length binary pulses, said counting circuit including at least first and second clocked flip-flops each having dual outputs for said equal time-length binary pulses;

a decoder circuit operative in response to said equal time-length binary pulses for placing the same in timed sequence along a separate channel for each of said pulses;

said decoder circuit including binary gates having at least two inputs and one output; and

an on-timer circuit for each of said separate channels and responsive to pulses thereon, said on-timer circuit including a potentiometer for regulating the duration of said equal time-length binary pulses,

a solid-state switch for completing a current path for a current supply to each of said rappers, each of said switches connected to corresponding ones of said on-timer circuits and made conductive during the duration of said regulated equal time-length binary pulses from said on-timer circuits, said current path being completed during the duration of said conduction, whereby said rappers are energized for a selected time period.

19. A method for maintaining the efficiency of an electrostatic precipitator by periodically energizing the rappers of said electrostatic precipitator, comprising:

producing a series of voltage pulses at a selected frequency;

converting said voltage pulses to a series of corresponding binary pulses;

dividing each of said binary pulses into a preselected number of equal time-length binary pulses;

placing said equal time-length binary pulses in sequence along a separate path for each of said pulses; and

connecting each of said separate paths with corresponding ones of said plurality of rappers, whereby each of said rappers is energized in sequence for the duration of said equal time-length binary pulses.

20. The method of claim 19 wherein each of said separate paths includes a timing circuit, and in addition: adjusting said timing circuit to regulate the duration of said equal time-length binary pulses, whereby the energization time for said rappers is controllable.

21. The method of claim 19, and in addition: varying the frequency of said series of voltage pulses, whereby said rappers are energized at varying intervals of time.

References Cited

UNITED STATES PATENTS

2,854,089	9/1958	White et al.	55—112
2,858,900	11/1958	Foley	55—112
2,922,085	1/1960	Drenning et al.	55—112 X
2,978,065	4/1961	Berg	55—105
3,030,753	4/1962	Pennington	55—112

FOREIGN PATENTS

591,169 1/1960 Canada.

DENNIS E. TALBERT, JR., Primary Examiner

U.S. Cl. X.R.

55—112, 139