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(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON (PUBL) [SE/SE]; S-164 83 Stockholm (SE).

(72) Inventors: ANDERSSON, Kristoffer; Doktor Forselius gata 18, S-413 26 Göteborg (SE). BAO, Mingquan; Citrusgatan 27, S-426 54 Västra Frölunda (SE).

(74) Agent: ALTHOFF, Fredrik; Ericsson AB Patent Unit GL, S-417 56 Göteborg (SE).

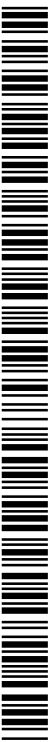
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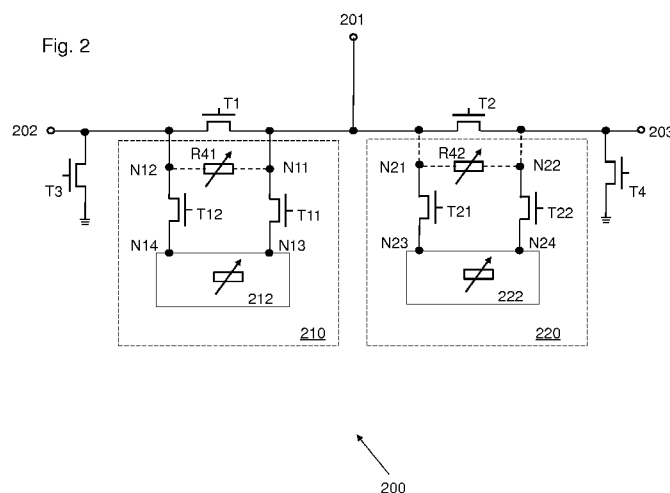
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(54) Title: A SWITCH CIRCUITRY WITH INTEGRATED ATTENUATOR



(57) Abstract: A switch circuitry (200) comprises a first port (201), a second port (202) and a third port (203). The switch circuitry (200) further comprises a first switch transistor (T1) coupled between the first port (201) and the second port (202); a second switch transistor (T2) coupled between the first port (201) and the third port (203); a third switch transistor (T3) coupled between the second port (202) and a ground node; and a fourth switch transistor (T4) coupled between the third port (203) and the ground node. The switch circuitry (200) further comprises a first switch and attenuator unit (210) having a first node (N11) and second node (N12). The first node (N11) is coupled to the first port (201) and the second node (N12) is coupled to the second port (202), and thereby is in parallel with the first switch transistor (T1). The first switch and attenuator unit (210) comprises an impedance network (212). The first and second terminals (N13, N14) of the impedance network (212) are coupled to the first and second nodes (N11, N12) of the first switch and attenuator unit (210) via respective switch transistors (T11, T12).

A SWITCH CIRCUITRY WITH INTEGRATED ATTENUATOR

TECHNICAL FIELD

Embodiments herein relate to a switch circuitry. In particular, they relate to a switch
5 circuitry with integrated attenuator employed in a front-end device of a communication
system.

BACKGROUND

The front-end device of a pulsed radar system or a time division duplex communication
10 system, usually comprises a transmit branch and a receive branch. The transmit branch
generally comprises driver amplifiers, digital step attenuators, power amplifiers and filters.
The receive branch generally comprises low noise amplifiers and filters. Two transmit/receive
switches are used to select the branch depending on whether the front-end receives or
transmits signals.

15 The performance of a wireless communication device in, e.g. the radar or
communication system, is heavily dependent on transmitted output power, power added
efficiency in transmit mode and noise figure in receiving mode. In order to minimize noise
figure and maximize power added efficiency, the transmit/receive switch in the front-end
device is a critical component. The transmit/receive switch must be designed to both
20 withstand high output power while providing low-loss.

Attenuators are circuits used to control amplitude of a signal either continuously or in
steps. When the signal is controlled digitally in steps by an attenuator, the attenuator is
referred as a digital step attenuator. In a front-end device design, digital step attenuators may
be needed to control the amplitude of received and/or transmitted signals. A major problem
25 associated with digital step attenuators is undesired insertion loss. In particular, for
broadband step attenuators, the undesired insertion loss may reach 3 dB which is probably
higher than the desired attenuation of, for instance, 0.5 dB only. This insertion loss must be
compensated for by increasing the gain in the driver amplifier and/or in the power amplifier,
at the cost of increased circuit area and increased power consumption.

30 To improve the performance of a front-end device in a communication system, the
design of transmit/receive switches and step attenuators needs to be improved.

SUMMARY

Therefore, it is an object of embodiments herein to provide a transmit/receive switch and step attenuator with improved performance for a front-end device in a communication system.

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According to one aspect of embodiments herein, the object is achieved by a switch circuitry comprising a first port, a second port and a third port.

The switch circuitry further comprises a first switch transistor coupled between the first port and the second port; a second switch transistor coupled between the first port and the third port; a third switch transistor coupled between the second port and a ground node; and a fourth switch transistor coupled between the third port and the ground node.

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The switch circuitry further comprises a first switch and attenuator unit having a first node and second node. The first node is coupled to the first port and the second node is coupled to the second port. Thus the first switch and attenuator unit is in parallel with the first switch transistor.

15

The first switch and attenuator unit further comprises an impedance network. The first and second terminals of the impedance network are coupled to the first and second nodes of the first switch and attenuator unit via respective switch transistors.

20

The switch circuitry according to embodiments herein integrates a digital step attenuator, i.e. the first switch and attenuator unit, into the transmit/receive switches, i.e. the first and/or second switches, by paralleling the first switch and attenuator unit with the first switch transistor. In this way, a series switch transistor in the digital step attenuator is omitted, thus the undesired insertion loss of the digital step attenuator due to the series switch transistor is mitigated. Since the first switch and attenuator unit comprises an impedance network which may be switched in to the transmit and/or receive branch, or switched out from the transmit and/or receive branch by two switch transistors, different attenuation levels may be provided.

25

Thus, embodiments herein provide an integrated switch and step attenuator circuitry with improved performance on e.g. insertion loss, attenuation levels etc.

30

BRIEF DESCRIPTION OF THE DRAWINGS

Examples of embodiments herein are described in more detail with reference to attached drawings in which:

35

Figure 1 shows schematic views of (a) a transmit/receive switch, (b) a T-type step attenuator, (c) a Pi-type step attenuator, and (d) a transmit/receive switch cascade with step attenuators according to prior art.

5 Figure 2 is a schematic block view illustrating a switch circuitry according to embodiments herein.

Figure 3 shows schematic views illustrating (a) a T-type impedance network and (b) a Pi-type impedance network according to embodiments herein.

10 Figure 4 is a block diagram illustrating a wireless communication device in which embodiments herein may be implemented.

DETAILED DESCRIPTION

As part of developing embodiments herein, some problems related to prior art will first be identified and discussed.

15

Broadband transmit/receive switches are typically implemented as shunt-series switches as shown in **Figure 1 (a)**. The transmit/receive switch in Figure 1 (a) has one input port, denoted as **Common**, and two output ports, denoted as **Port 1** and **Port 2**. Port 1 is switched to the Common port by turning on transistors Tb and turning off transistors Ta, while keeping Port 2 isolated by switching off transistor Tc and turning on transistor Td. The main switching action is provided by the series transistors Tb and Tc, while the shunt transistors Ta and Td provide isolation. The on-resistance of the series transistors Tb and Tc determines the insertion loss, low on-resistance means low insertion loss. However in order to achieve low on-resistance, the transistor size needs to be large hence increasing the off state capacitance of the transistor. The large off state capacitance will degrade the isolation when the transistor is switched off. Hence there is a tradeoff between the insertion loss and isolation. There is a similar tradeoff also for the shunt transistors but that may be mitigated by absorbing the off-state capacitance in a matching network.

30 Digital step attenuators are typically implemented using either a T- or Pi-topology as shown in Figure 1 (b) and (c).

In Figure 1(b), switching transistors Ta and Tb are used to switch between high attenuation, i.e. Ta is on, Tb is off, and low attenuation i.e. Ta is off and Tb is on. In Figure 1(c), switching transistors Ta, Tb and Tc are used to switch between high attenuation, i.e. Ta and Tb are on, Tc is off, and low attenuation i.e. Ta and Tb are off and Tc is on.

35

The series switching transistor, i.e. Tb in Figure 1 (b), Tc in Figure 1 (c), is used to bypass series elements of a resistive attenuator network, i.e. R1 and R2 in Figure 1 (b), R1 in Figure 1 (c). The shunt switching transistors, i.e. Ta in Figure 1 (b), Ta and Tb in Figure 1 (c), are used to isolate shunt resistors, i.e. R3 in Figure 1(b), R2 and R3 in Figure 1(c).

5 Similar to the transmit/receive switch, the insertion loss of the step attenuator at low attenuation state is dominated by the on resistance of the series switching transistor. In addition to the tradeoff between the isolation and insertion loss, the step attenuator needs to have a large ratio between the on resistance of the series switching transistor and the resistance of the series resistors. Hence it is difficult to design step attenuators having low
10 insertion loss at the low attenuation state and having high attenuation at the high attenuation state.

In a conventional front-end device in a radar or wireless communication system, the digital step attenuator(s) is in cascade with the transmit/receive switch. For example, as
15 shown in Figure 1 (d), transmit/receive switch SW is cascaded with a first digital step attenuator DA1 and a second digital step attenuator DA2.

It can be seen that both the transmit/receive switch SW and the step attenuator DA1/DA2 employs a series switching transistor. The series switching transistors Tc in the digital step attenuator DA1 is in series with the series switching transistors T1. The series
20 switching transistors Tc in the digital step attenuator DA2 is in series with the series switching transistors T2 in the transmit/receive switch SW. As discussed above, the on resistance of the series switching transistor Tc in the step attenuators DA1 and DA2 will cause insertion loss at low attenuation state.

25 To solve this problem, according embodiments herein, the series switching transistors Tc in the digital step attenuators DA1 and DA2 are combined with the series switching transistors T1 and T2 in the transmit/receive switch SW. In other words, the series switching transistors Tc in the digital step attenuators DA1 and DA2 are removed or omitted. Instead, the series switching transistors T1 and T2 in transmit/receive switch SW are re-used in the
30 step attenuator. By combining the series switching transistors for the transmit/receive switch and step attenuator, an integrated switch and attenuator circuitry is configured as shown in **Figure 2**, denoted as a **switch circuitry 200**.

According to embodiments herein, the switch circuitry 200 comprises a **first port 201**, a **second port 202** and a **third port 203**.

35 The switch circuitry 200 further comprises a **first switch transistor T1** coupled between the first port 201 and the second port 202; a **second switch transistor T2** coupled

between the first port 201 and the third port 203; a **third switch transistor T3** coupled between the second port 202 and a ground node; and a **fourth switch transistor T4** coupled between the third port 203 and the ground node.

The switch circuitry 200 further comprises a **first switch and attenuator unit 210** having a **first node N11** and **second node N12**. The first node N11 is coupled to the first port 201 and the second node N12 is coupled to the second port 202. Thus the first switch and attenuator unit 210 is in parallel with the first switch transistor T1.

According to some embodiments, the first switch and attenuator unit 210 comprises an impedance network 212. The first and second terminals N13, N14 of the impedance network 212 are coupled to the first and second nodes N11, N12 of the first switch and attenuator unit 210 via respective switch transistors T11, T12.

According to some embodiments, the switch circuitry 200 further comprises a **second switch and attenuator unit 220** having a **first node N21** and **second node N22**. The first node N21 is coupled to the first port 201 and the second node N22 is coupled to the third port 203. Thus the second switch and attenuator unit 220 is in parallel with the second switch transistor T2. The dotted line connections of the second switch and attenuator unit 222 to the second switch transistor T2 means that the second switch and attenuator unit 222 is optional.

According to some embodiments, the second switch and attenuator unit 220 may have similar structure as the first switch and attenuator unit 210. The second switch and attenuator unit 220 comprises an **impedance network 222**. The first and second terminals N23, N24 of the impedance network 222 are coupled to the first and second nodes N21, N22 of the second switch and attenuator unit 220 via respective switch transistors T21, T22.

According to some embodiments, the impedance network 212, 222 may comprise a **PI-type impedance network 214**, as shown in **Figure 3 (a)**. The PI-type impedance network 214 comprises a **first impedance R1** coupled between the first terminal N1 and the second terminal N2 of the impedance network 214, a **second impedance R2** coupled between the second terminal N2 and the ground node, and a **third impedance R3** coupled between the first terminal N1 and the ground node.

According to some embodiments, the impedance network 212, 222 may comprise a **T-type impedance network 216**, as shown in **Figure 3 (b)**. The T-type impedance network 216 comprises a first impedance R1 connected in series with a second impedance R2 and coupled between the first terminal N1 and the second terminal N2 of the impedance network;

and a third impedance R3 coupled between the ground node and a middle node N0 formed by the connection of the first impedance R1 and second impedance R2.

According to some embodiments, the first and second switch and attenuator units 210, 220 may further comprise a **fourth impedance R41, R42**. The fourth impedance R41 is connected between the first node N11 and second node N12 of the first switch and attenuator unit 210. The fourth impedance R42 is connected between the first node N21 and second node N22 of the second switch and attenuator unit 220. The dotted line connections of the fourth impedance R41, R42 to the first node N11, N21 and second node N12, N22 as shown in Figure 2 means that the fourth impedance R41, R42 is optional. The fourth impedance R41, R42 may be a variable resistor, or a variable resistor connected in series or in parallel with inductors or capacitors.

According to some embodiments, the impedance network 212, 222 may be a variable resistance network, and the impedances R1, R2, R3 comprised in the impedance network 212, 222 are variable resistors.

According to some embodiments, the impedance network 212, 222 may be a variable impedance network, and the impedances R1, R2, R3 comprised in the impedance network 212, 222 are variable resistors connected in series or in parallel with inductors or capacitors.

As shown in Figure 2, the switch and attenuator unit 210, 220 may be incorporated into one or both branches i.e. in transmit branch and/or receive branch. The shunt switch transistors T11, T12, T21, T22 are used to engage an attenuator, i.e. the Pi-type or T-type impedance network 212, 222 to the transmit/receive switch T1/T2. As discussed above, the fourth impedance R41, R42 is optional and in most practical implementations it may be omitted. However, for relative high attenuation, e.g. 10 dB or higher, the fourth impedance R41, R42 may be included with a resistance value of about 70 Ohms or larger in a system with 50 Ohm input/output impedance.

When the switch and attenuator unit 210, 220 is incorporated into one branch, this branch may be configured to have four operating modes: isolated, low loss, X dB attenuation and Y dB attenuation. The amount of attenuation, X dB and Y dB, may be controlled by selecting impedances R1, R2, R3, and R41. The Y dB attenuation mode is an extra mode that provides less attenuation than X dB. As mentioned above, the impedances R1, R2, R3, and R41 may comprise a resistor connected in series or in parallel with an inductor or

capacitor. The reactive component, i.e. the inductor and capacitor are used to reduce the influence of parasitic capacitances and improve impedance matching.

The table below shows a mapping between the operating modes and the switch transistor states, i.e. either on or off. The table is valid for the case where the switch and attenuator unit 210 is incorporated in one branch between Port 201 and Port 202, e.g. the transmit branch TX and no switch and attenuator unit 220 in the receive branch RX between Port 201 and Port 203.

Transistor	RX	TX (0 dB)	TX (X dB)	TX (Y dB)
T1	Off	On	Off	On
T2	On	Off	Off	Off
T3	On	Off	Off	Off
T4	Off	On	On	On
T11	Off	Off	On	On
T12	Off	Off	On	On

To illustrate the performance of the integrated switch and step attenuator circuitry 200 according to embodiments herein, simulations have been done for the switch circuitry 200, where any reactive tuning components are not included. The simulated switch circuitry comprises 4x100 um Field-Effect Transistors (FETs) as the series switch transistors T1 and T2 and 2x100 um FETs as the shunt switch transistors T11 and T12. The isolation transistors T3 and T4 are two 2x100 um FETs in parallel. The attenuation resistors are set as R41=open circuit, i.e. is omitted, R2=R3=98 Ohm, and R1=7 Ohm.

The simulation results show that the insertion loss at 4GHz for the transmit branch is -1.6dB for 0-dB attenuation mode, -4.7dB for 3-dB attenuation mode, and -8.4dB for 8-dB attenuation mode. The insertion loss for the receive mode is -1.5dB. Thus, the degradation in the insertion loss due to the switch and attenuator unit 210 is only 0.1dB which is negligible. The simulation results also show that the isolation between the transmit TX and receive RX branch is not hampered by adding the switch and attenuator unit 210.

To summarise the discussions above, integration of a digital step attenuator with the transmit/receive switch as implemented in the switch circuitry 200 has several advantages. The foremost advantage is that the undesired insertion loss associated with the digital step attenuator is completely mitigated, since the insertion loss of the step attenuator is absorbed by the transmit/receive switch and the insertion loss is set only by the transmit/receive

switch. The second advantage is that due to the integration, the size of the front-end device module or circuitry, DC power consumption can be greatly reduced. As a results, high gain, high power, highly efficient and low noise front-ends may be designed by employing the switch circuitry 200 according to embodiments herein.

5

The switch circuitry 200 according to embodiments herein may be employed in various communication devices. **Figure 4** shows a block diagram of a **communication device 400**, which may be, e.g. a user equipment or a mobile device and/or a base station. The communication device 400 may comprise other units, where a **transceiver 430** comprising a **receiver 410** and a **transmitter 420** and a **processing unit 440** are shown. The switch circuitry 200 is coupled between the receiver 410 and transmitter 420. The processing unit 440 may interact with the switch circuitry 200 for different attenuation settings or operating modes.

10
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Those skilled in the art will understand that although switch transistors in the switch circuitry 200 as shown in Figure 2 are Field-Effect Transistors (FET), any other types of transistors, e.g. Metal–Oxide–Semiconductor FET (MOSFET), Junction FET (JFET), Bipolar Junction Transistors (BJT), High-Electron-Mobility Transistor (HEMT), Heterojunction Bipolar Transistor (HBT), PIN diode, i.e. diode with wide, undoped Intrinsic semiconductor region between a P-type semiconductor and an N-type semiconductor region, etc. may be comprised in the switch circuitry 200. When using the word "comprise" or "comprising" it shall be interpreted as non- limiting, i.e. meaning "consist at least of".

20
25

The embodiments herein are not limited to the above described preferred embodiments. Various alternatives, modifications and equivalents may be used. Therefore, the above embodiments should not be taken as limiting the scope of the invention, which is defined by the appending claims.

CLAIMS

1. A switch circuitry (200) comprising:
 - a first port (201), a second port (202) and a third port (203);
 - 5 a first switch transistor (T1) coupled between the first port (201) and the second port (202);
 - a second switch transistor (T2) coupled between the first port (201) and the third port (203);
 - a third switch transistor (T3) coupled between the second port (202) and a
 - 10 ground node;
 - a fourth switch transistor (T4) coupled between the third port (203) and the ground node; and
 - a first switch and attenuator unit (210) having a first node (N11) and second node (N12), wherein the first node (N11) is coupled to the first port (201) and the second
 - 15 node (N12) is coupled to the second port (202), and thereby is in parallel with the first switch transistor (T1), wherein the first switch and attenuator unit (210) comprises an impedance network (212), and wherein a first and second terminals (N13, N14) of the impedance network (212) are coupled to the first and second nodes (N11, N12) of the first switch and attenuator unit (210) via respective switch transistors (T11, T12).
 - 20
2. The switch circuitry (200) according to claim 1, further comprising a second switch and attenuator unit (220) having a first node (N21) and second node (N22), wherein the
- 25 first node (N21) is coupled the first port (201) and the second node (N22) is coupled to the third port (203), and thereby is in parallel with the second switch transistor (T2), and wherein the second switch and attenuator unit (220) comprises an impedance network (222), and wherein a first and a second terminals (N23, N24) of the impedance network (222) are coupled to the first and second nodes (N21, N22) of the second switch and attenuator unit (220) via respective switch transistors (T21, T22).
- 30
3. The switch circuitry (100) according to any one of claims 1-2, wherein the impedance network (212, 222) comprises a PI-type impedance network (214), and the PI-type impedance network (214) comprises a first impedance (R1) coupled between the first
- 35 terminal (N1) and the second terminal (N2) of the impedance network, a second impedance (R2) coupled between the second terminal (N2) and the ground node, and a third impedance (R3) coupled between the first terminal (N1) and the ground node.

4. The switch circuitry (200) according to any one of claims 1-2, wherein the impedance network (212, 222) comprises a T-type impedance network (216), and wherein the T-type impedance network (216) comprises:
 - a first impedance (R1) connected in series with a second impedance (R2) and
5 coupled between the first terminal (N1) and the second terminal (N2) of the impedance network; and
 - a third impedance (R3) coupled between the ground node and a middle node (N0) formed by the connection of the first impedance (R1) and second impedance (R2).
10
5. The switch circuitry (200) according to any one of claims 1-4, wherein the first and second switch and attenuator units (210, 220) further comprise a fourth impedance (R41, R42), wherein the fourth impedance (R41) in the first switch and attenuator unit (210) is connected between the first node (N11) and second node (N12) of the first
15 switch and attenuator unit 210, the fourth impedance (R42) in the second switch and attenuator unit (220) is connected between the first node (N21) and second node (N22) of the second switch and attenuator unit (220).
6. The switch circuitry (200) according to claim 5, wherein the fourth impedance (R41, R42) is a variable resistor or a variable resistor connected in series or in parallel with
20 inductors or capacitors.
7. The switch circuitry (200) according to any one of claims 1-6, wherein the impedance network (212, 222) is a variable resistance network, and the impedances (R1, R2, R3) comprised in the impedance network (212, 222) are variable resistors.
25
8. The switch circuitry (200) according to any one of claims 1-6, wherein the impedance network (212, 222) is a variable impedance network, and the impedances (R1, R2, R3) comprised in the impedance network (212, 222) are variable resistors connected
30 in series or in parallel with inductors or capacitors.
9. A transceiver (430) comprising a switch circuitry (200) according to any one of claims 1-8.
- 35 10. A communication device (400) comprising a switch circuitry (200) according to any one of claims 1-8.

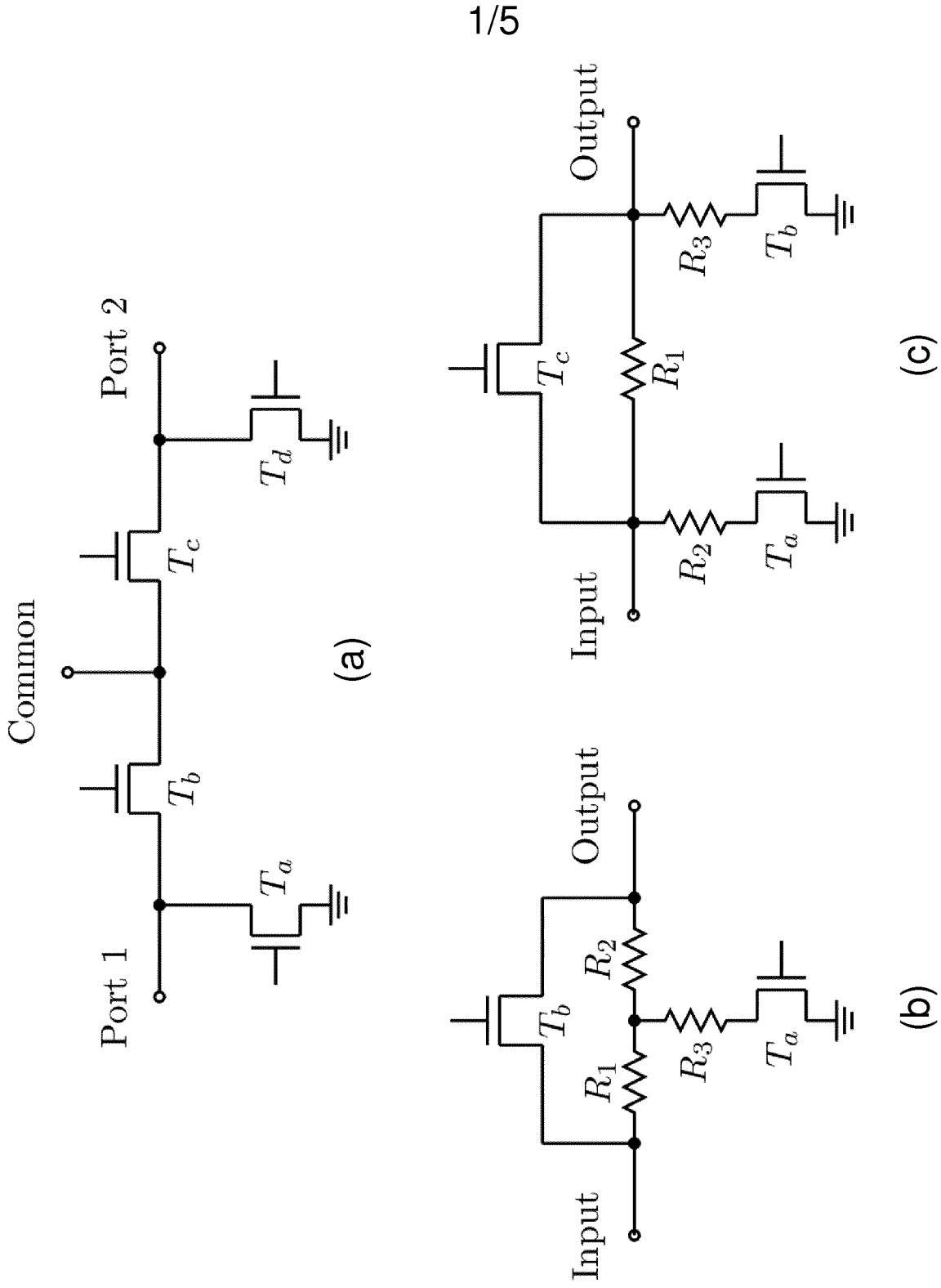
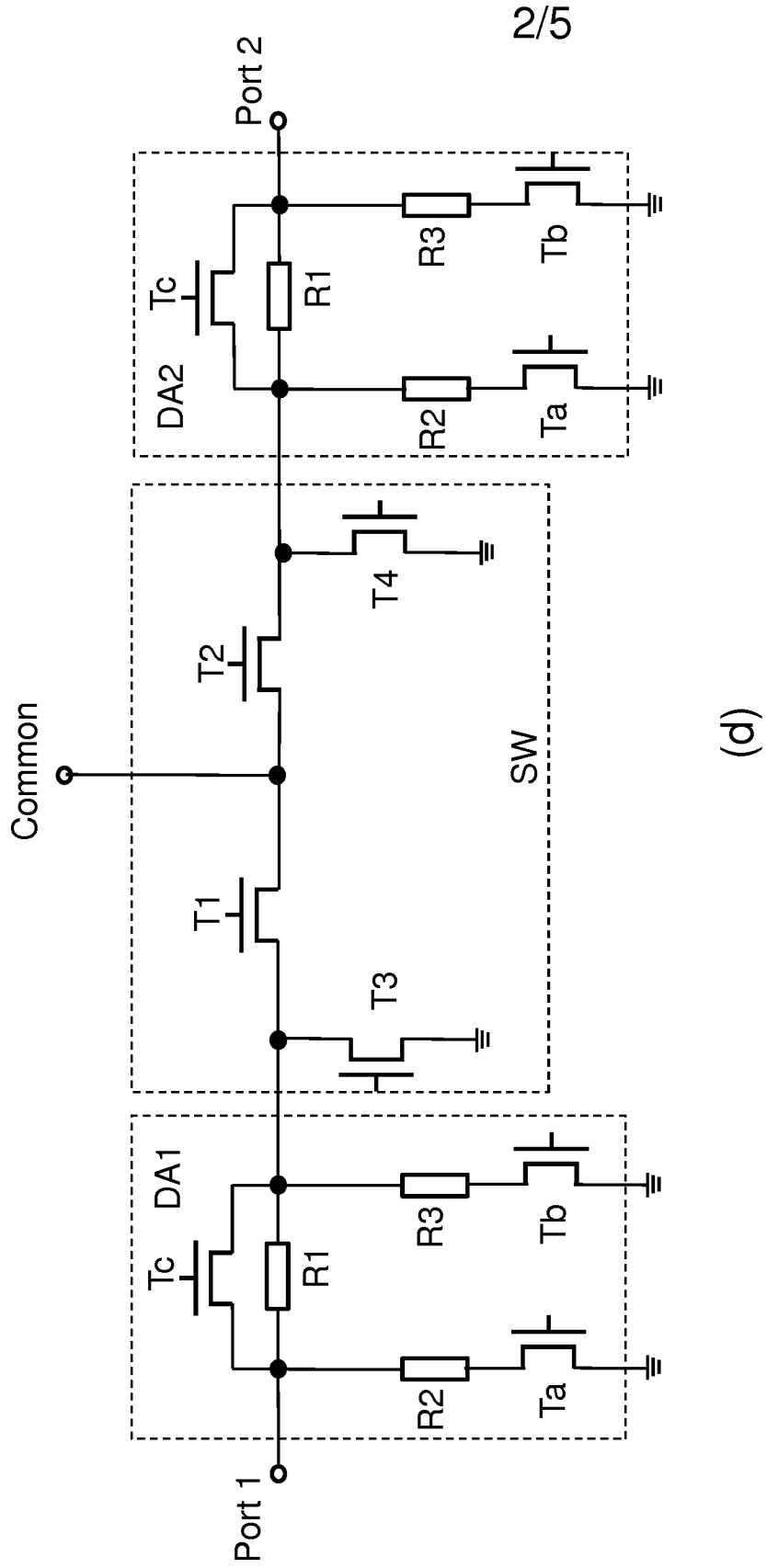


Fig. 1 prior art



(d)

Fig. 1 prior art

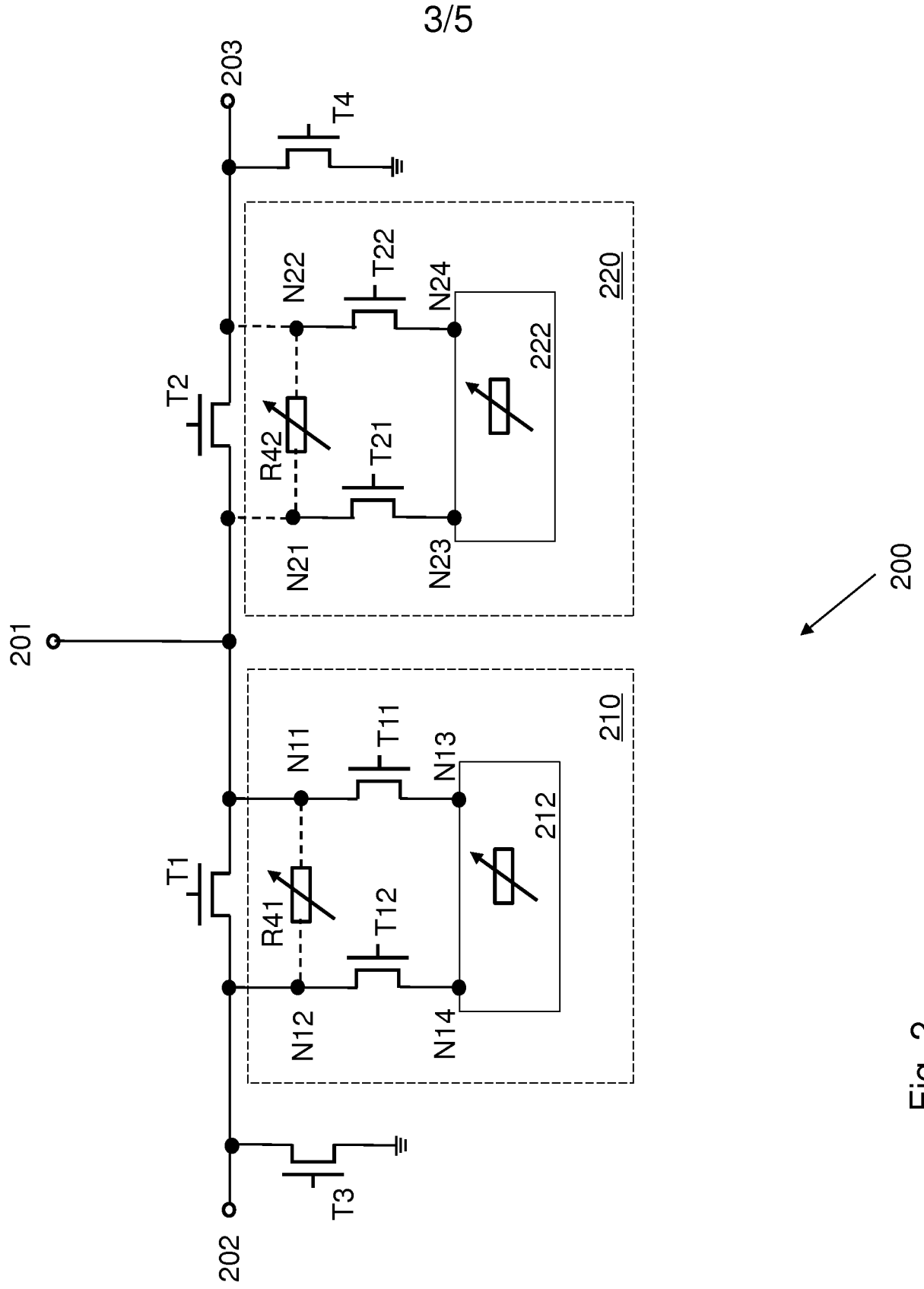


Fig. 2

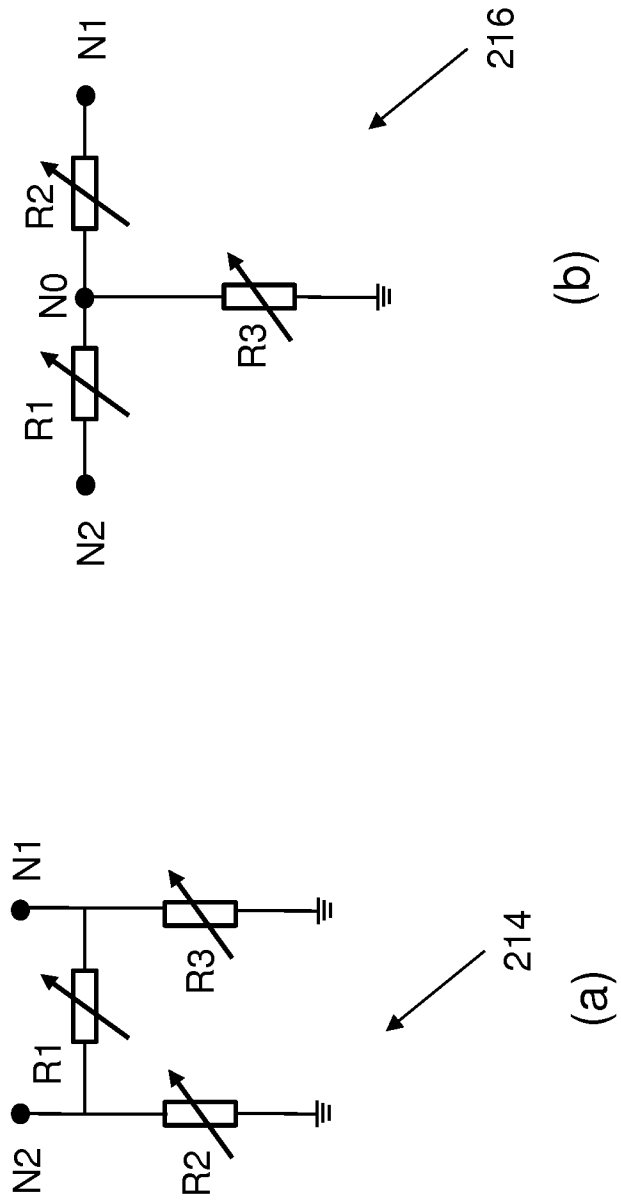


Fig. 3

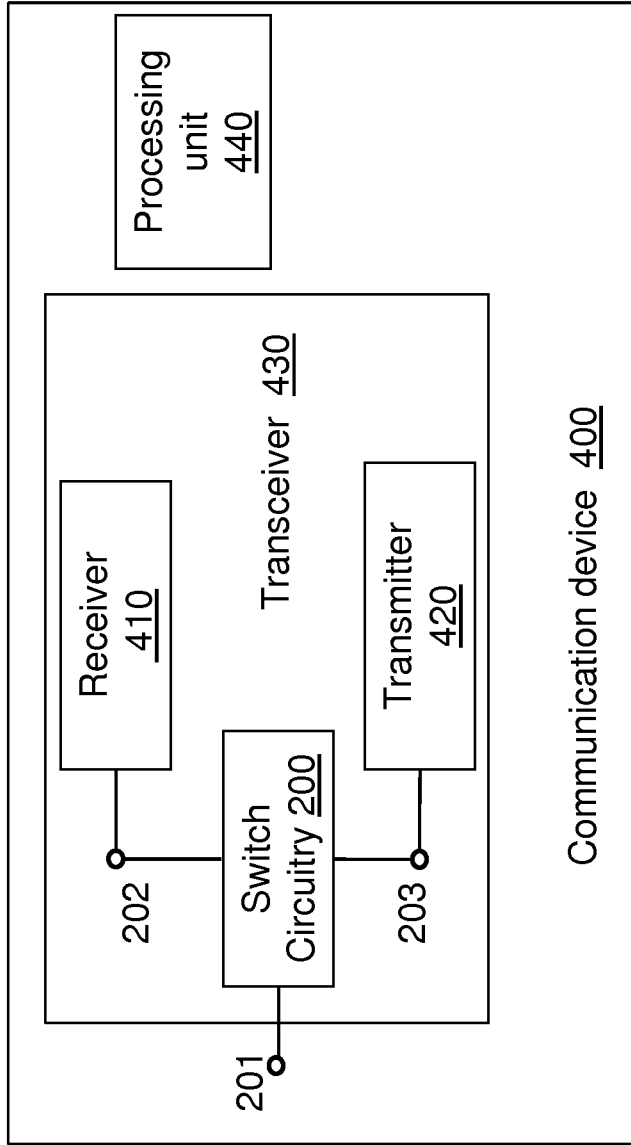


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/056160

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H04B1/48 H01P1/15 H03K17/693
 ADD.
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
 Minimum documentation searched (classification system followed by classification symbols)
 H04B H01P H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 EPO-Internal, COMPENDEX, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 777 530 A (NAKATUKA TADAYOSHI [JP]) 7 July 1998 (1998-07-07) column 1, lines 13-31, 43-46 column 2, line 39 - line 49 column 5, line 53 - column 10, line 63; figures 1-10	1-10
A	----- US 2013/072134 A1 (GOTO SATOSHI [JP] ET AL) 21 March 2013 (2013-03-21) paragraph [0054] - paragraph [0067]; figures 3, 4, 9-16 paragraph [0091] - paragraph [0110]	1-10
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Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search 1 December 2015	Date of mailing of the international search report 09/12/2015
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Patrovsky, Andreas
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2015/056160

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