United States Patent [19]

Hill et al.

[11] **3,835,821**

[45] **Sept. 17, 1974**

[54] **PETROL INJECTION SYSTEMS FOR INTERNAL COMBUSTION ENGINES**

[75] Inventors: **William Frank Hill**, Stafford; **Roger Edward Cattermole**, Leicester, both of England

[73] Assignee: **Joseph Lucas (Industries) Limited**, Birmingham, England

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[21] Appl. No.: **275,825**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 69,614, Sept. 4, 1970, abandoned.

[52] **U.S. Cl.** ..... **123/32 EA**, 123/139 E

[51] **Int. Cl.** **F02b 3/00**

[58] **Field of Search** ..... 123/32 EA, 32 AC

[56] **References Cited**

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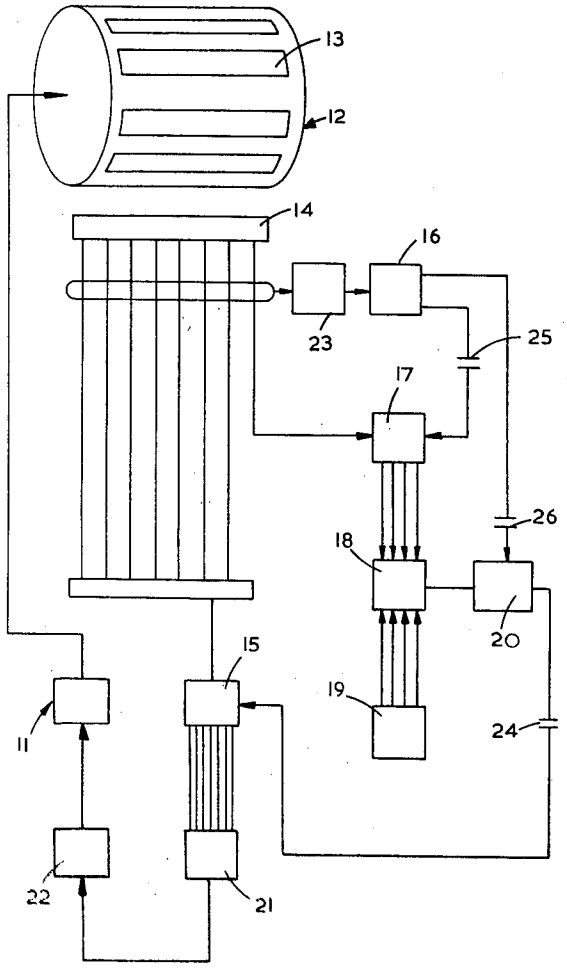
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Primary Examiner—Laurence M. Goodridge
Assistant Examiner—Ronald B. Cox
Attorney, Agent, or Firm—Holman & Stern

[57] **ABSTRACT**

A petrol injection system for an internal combustion engine has a memory device on which are stored a plurality of sets of information, each set containing a number of coded signals and each of the coded signals representing a different fuel requirement. The delivery of fuel is controlled by a control device in which is stored a control signal which is changed from time to time, but is always obtained from the memory device. One significant signal fed to the engine is used to determine from which sets the signal fed to the control device is obtained, and another significant parameter of the engine is used to determine which coded signal from the chosen set is fed from the memory device to the control device.

4 Claims, 7 Drawing Figures



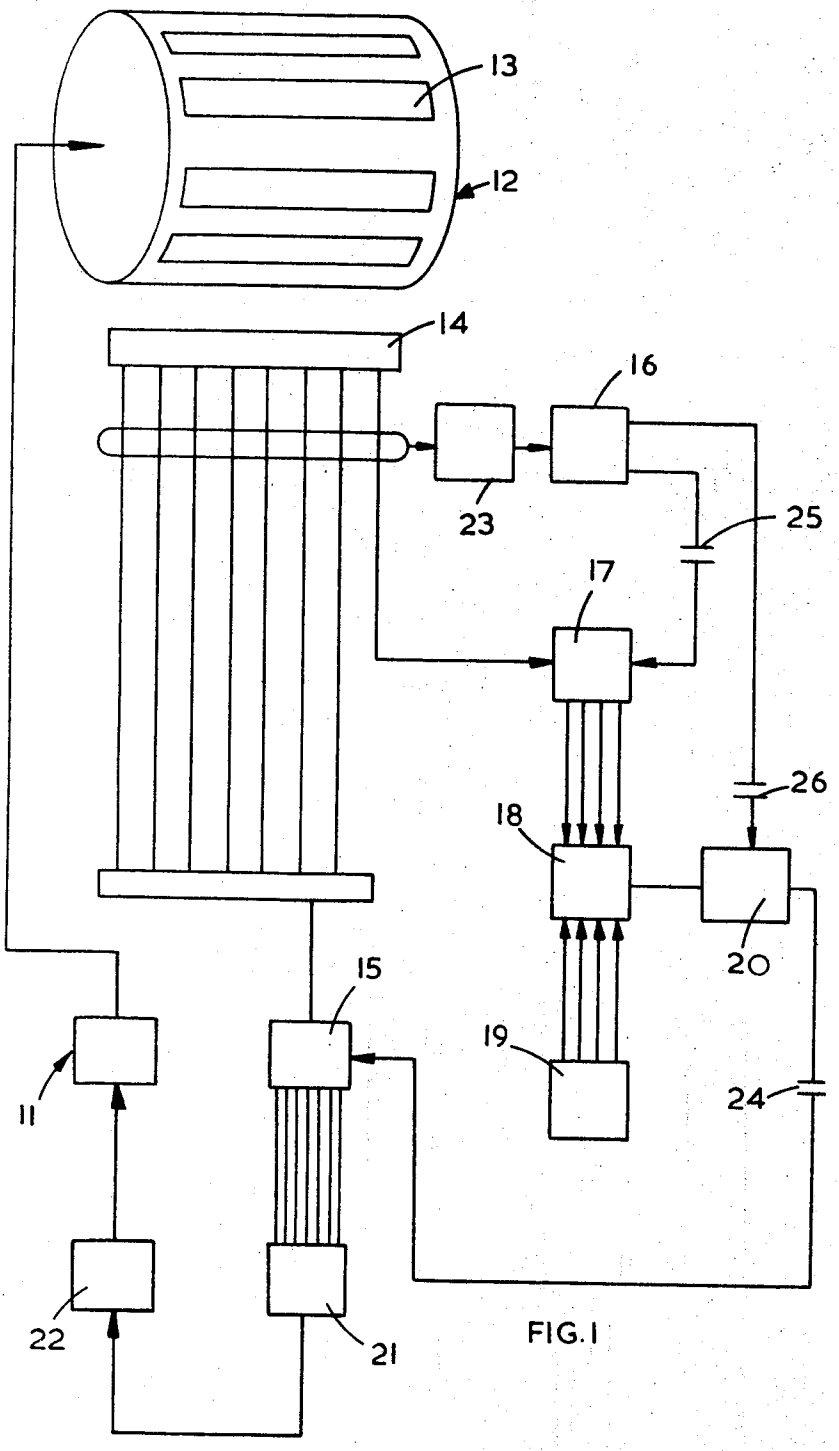


FIG. 1

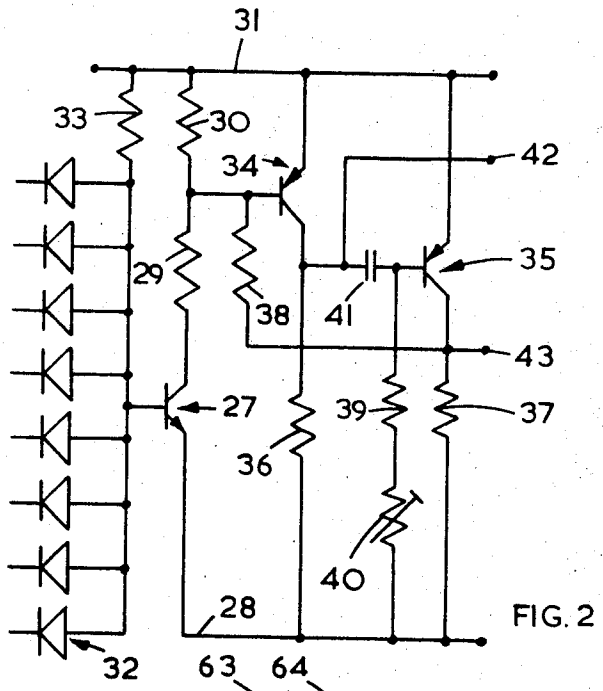

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FIG. 2

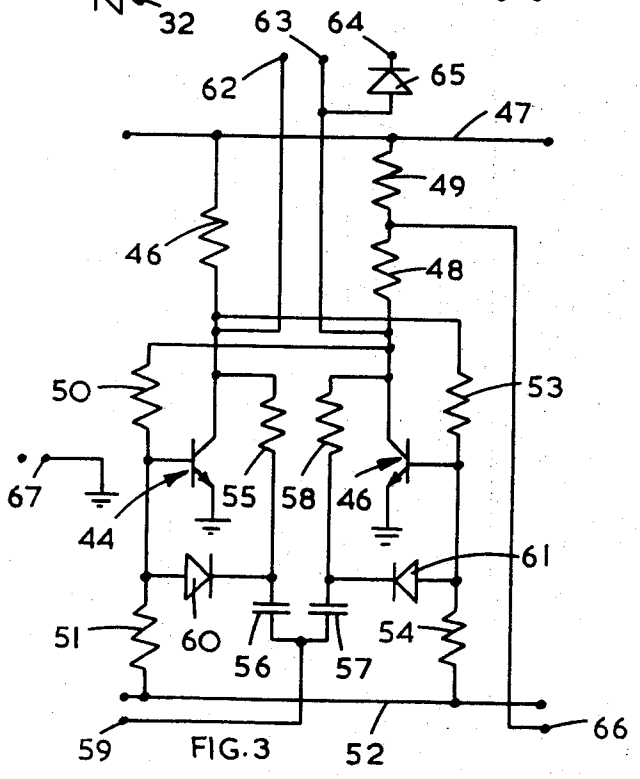

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FIG. 3

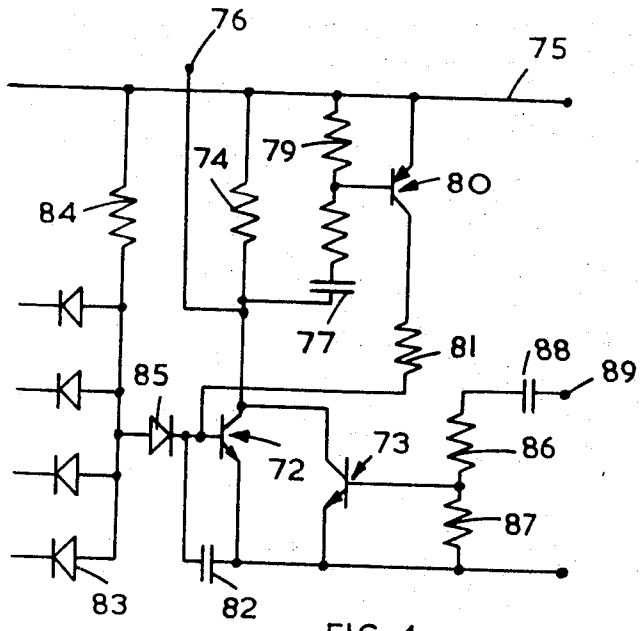

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FIG. 4

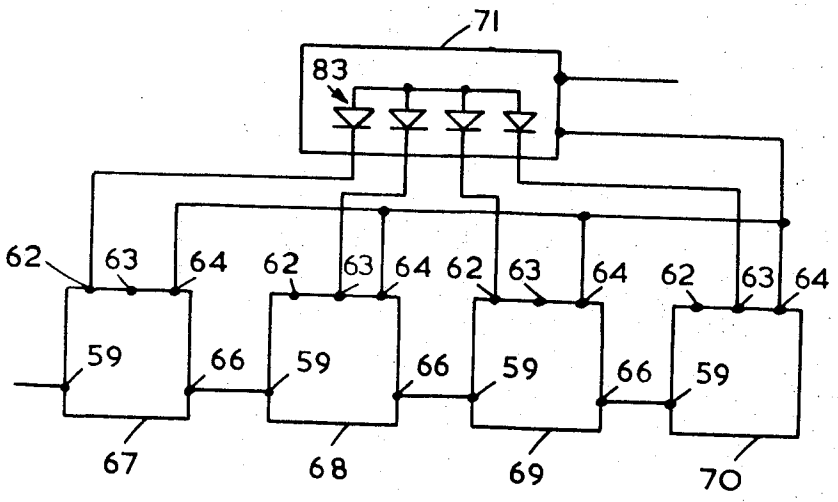

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FIG. 5

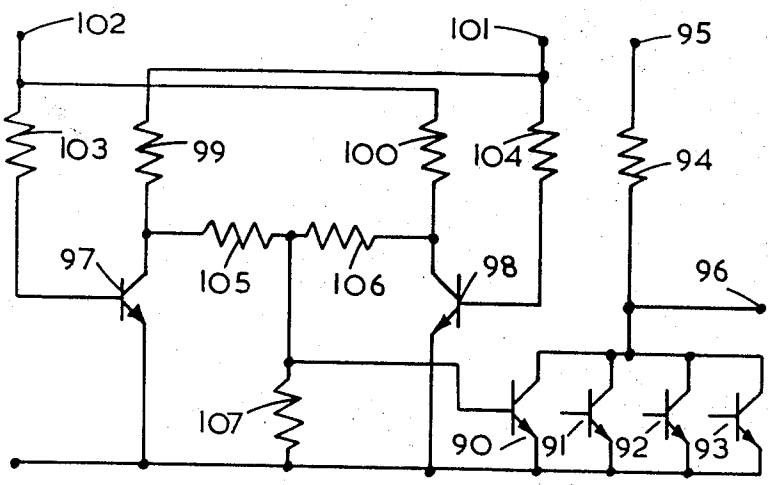

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FIG. 6

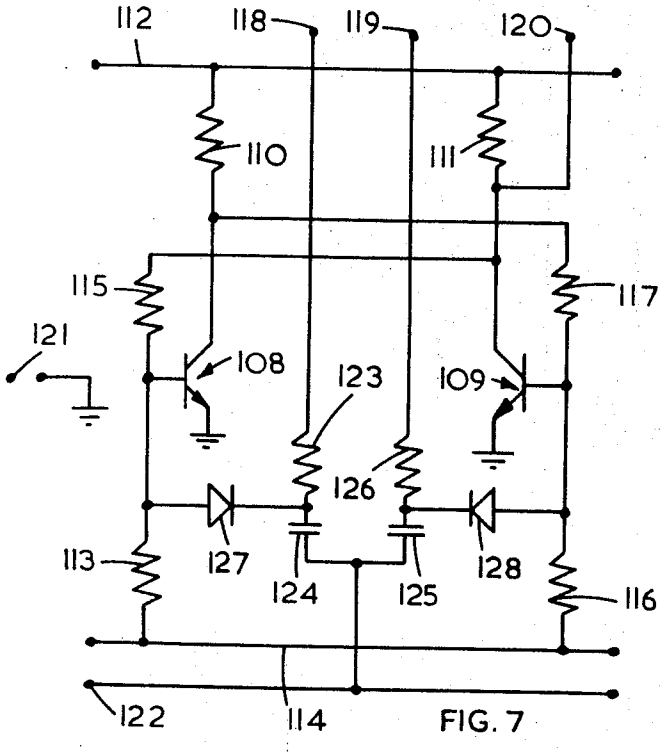

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FIG. 7

PETROL INJECTION SYSTEMS FOR INTERNAL COMBUSTION ENGINES

This invention relates to a petrol injection system for an internal combustion engine and is a Continuation in Part of our application Ser. No. 69,614 filed Sept. 4, 1970, now abandoned.

The ideal quantity of fuel to be injected into an internal combustion engine depends upon the operating conditions of the engine. These may be principally represented for control purposes as engine speed and either throttle opening or the consequent manifold pressure. For convenience, these two parameters, namely speed on one hand and throttle opening or manifold depression on the other hand, are referred to throughout this Specification as significant parameters. The quantity is also affected by engine temperatures and by the immediate past history of engine operation so that it is customery to use temperature signals and signals representing rate of change of throttle opening or of manifold pressure to modify the principal control action. Various means are also known which modify the quantity of fuel to be injected in response to the barometric pressure.

The object of this invention is to provide improved means of determining the quantity of fuel delivered under steady temperature and barometric conditions. However, modification to the quantity of fuel delivered in accordance with variation in temperature and/or pressure and to cater for dynamic conditions of operation can be incorporated in the preferred embodiment, using known means.

A system according to the invention includes a memory device on which are stored a plurality of sets of information, each set containing a number of coded signals representing different fuel requirements, a control device on which is stored a control signal determining the quantity of fuel delivered to the engine, the control signal being obtained from the memory device, means sensitive to one significant parameter for determining from which set the signal fed from the memory device to the control device is obtained, and means sensitive to the other significant parameter for determining which coded signal from the chosen set is fed from the memory device to the control device.

The invention will now be more particularly described with reference to the accompanying drawings wherein:

FIG. 1 illustrates diagrammatically one embodiment of the invention, in which the two significant parameters are engine speed and throttle angle,

FIG. 2 is a circuit diagram illustrating one embodiment of the coincidence detector and the timing pulse generator illustrated diagrammatically in FIG. 1,

FIG. 3 is a circuit diagram of one stage of one embodiment of the binary counter illustrated diagrammatically in FIG. 1,

FIG. 4 is a circuit diagram illustrating a zero re-set circuit which forms part of the binary counter illustrated diagrammatically in FIG. 1,

FIG. 5 shows the connections between the four stages and the zero re-set circuit of the binary counter illustrated diagrammatically in FIG. 1,

FIG. 6 is a circuit diagram of one embodiment of the comparator illustrated diagrammatically in FIG. 1, and

FIG. 7 is a circuit diagram of part of one embodiment of the static register illustrated diagrammatically in FIG. 1.

Referring more particularly to FIG. 1 of the drawings, an engine 11 drives a rotary memory device 12 on which are stored 12 sets of information indicated at 13. Each set 13 of information contains 10 coded signals in the form of eight-bit rows extending across the drum and which are presented in turn to an eight channel reading head 14. The information on the drum could be conveniently in the form of patches which differ from surrounding areas in respect of magnetisation, transparency, reflectivity, protuberance, conductivity or any other parameter conveniently able when used with a suitable reading head, to furnish signals when the drum is rotated. Presence and absence of such a patch in each position of a row may be used to represent a binary "1" and a binary "0" respectively. The first seven bits of the eight bits in each row presented to the reading head 14 are used to define a quantity of fuel to be delivered to the engine 11. The eighth bit in each row provides a control pulse which is detected by the eighth channel of the reading head 14 and fed to a counter 17 to which the eighth channel of the reading head 14 is connected. The first seven channels of the reading head 14 are coupled to a seven channel static register 15 which on receipt of an input pulse from a bistable circuit 20 an output of which is connected to the register 15 through a capacitor 24, reads the seven bits of information present in the first seven channels of the reading head 14. This digital information is fed to a digital-to-analogue converter 21 which is connected to the outputs of the register 15 and which provides a continuous output signal corresponding to the last seven bits of information received by the static register 15 from the head 14. This analogue signal is fed to a fuel supply control device 22 which meters the quantity of fuel injected into the engine.

One of the sets 13 of information on the drum 12 is designated the first set and when the first row of the first set reaches to reading head 14 it provides a unique datum signal to a coincidence detector 23 which operates only when the unique datum signal is produced, and when operated triggers a timing pulse generator 16 to which an output of the detector 23 is connected and which produces an output pulse of fixed duration. The timing pulse generator 16 has two outputs, one of which is connected to the counter 17 through a capacitor 25 and the other of which is connected to the bistable circuit 20 through a capacitor 26. At the start of the output pulse produced by the timing pulse generator 16, the counter 17 is re-set to zero and thereafter counts the control pulses (ie. the eighth bit in each row). The counter 17 counts from zero to $n-1$, where n is the number of rows in each set 13 of information and then starts counting from zero again so that irrespective of which of the 12 sets is being read by the head 14, the counter 17 maintains a count corresponding to the row in that set that is being read by the head 14. In the example quoted, the counter 17 must of course count up to nine, and then reset to zero. The signal in the counter 17 is fed to a comparator 18 which also receives a signal from zero to nine from a throttle angle encoder 19. When the comparator 18 receives corresponding signal from the counter 17 and the throttle angle encoder 19 the comparator 18 provides an output signal to the bistable circuit 20.

It will be appreciated that since the encoder **19** produces an output from zero to nine, depending on the throttle angle, and the counter **17** scans from zero to nine for each set **13** of information, the comparator **18** will provide an input signal to the bistable circuit **20** once for each set **13** passing the head **14,** each of these input signals attempting to re-set the bistable circuit **20.** However, the bistable circuit is only set by the output of the generator **16** after the fixed period of time, following which the next input from the comparator **18** re-sets the bistable circuit, which triggers the register **15** so that the information in the head **14** at the instant when the bistable circuit **20** is re-set is fed to the converter **21** to determine the quantity of fuel to be delivered to the engine **11** until the next time the bistable circuit **20** is reset, at which point the signal in the register **15** will be changed if there has been a change in either of the significant parameters.

Turning now to consider more particularly the reading head **14,** this provides eight bi-valued parallel signal channels as the drum rotates. The first seven channels provide a parallel digital output collectively used to signify quantity of fuel, except that, out of the 2^7 possible combinations, one is reserved as a unique datum signal for signifying drum position. This signal is a full set of binary "1's." This unit may be considered to furnish paraphased output signals for each channel. Alternatively, these signals may be derived locally from single-ended binary signals where necessary. Preferably, the arrangement of the reading head **14** and the patches on the drum is such that the full set of binary "'s" furnished by the eighth channel all commence and finish during the period when the first seven channels are fully operated by their corresponding signals. In this way, the sampling of the first seven channels performed by the eighth channel, surpresses transitional portions of the first seven channels.

The coincidence detector **23** and the timing pulse generator **16** will now be more particularly described with reference to FIG. **2** of the accompanying drawings. The coincidence detector **23** comprises an n-p-n transistor **27** the emitter of which is connected to a zero voltage rail **28** and the collector of which is connected through a pair of series connected resistors **29** and **30** to a positive supply rail **31.** Eight diodes **32** are provided, the cathodes of which are connected respectively to the eight channels of the reading head **14** and the anodes of which are connected on the one hand to the base of the transistor **27** and on the other hand through a resistor **33** to the rail **31.**

The timing pulse generator **16** comprises a pair of p-n-p transistors **34** and **35** the collectors of which are connected to the rail **28** through resistors **36** and **37** respectively and the emitters of which are connected to the rail **31.** The base of the transistor **34** is connected on the one hand to the junction between the resistors **29** and **30** of the detector **23** and on the other hand through a resistor **38** to the collector of the transistor **35** whilst the base of the transistor **35** is connected on the one hand to the rail **28** through a fixed resistor **39** connected in series with a variable resistor **40,** and on the other hand through a capacitor **41** to the collector of the transistor **34.** The collectors of the two transistors **34** and **35** are also respectively connected to a pair of output terminals **42** and **43** of the timing pulse generator **16.**

Let us now assume that the reading head **14** furnishes a positive going output signal on each channel, i.e. a voltage signal which is substantially positive to represent binary "1" and is essentially zero when representing binary "0." Only when a full set of binary "1's" is read by the reading head **14** does resistor **33** pass base current into transistor **27.** However when transistor **27** turns on, conduction in transistor **34** is initiated thereby triggering the monostable flip-flop constituted by the transistors **34** and **35.** Base conduction in transistor **34** is re-generatively sustained through resistor **38** keeping transistor **34** bottomed and transistor **35** cut off while capacitor **41** discharges through resistors **39** and **40.** After a time pre-settable by resistor **40,** conduction in transistor **35** resumes and the circuit re-generatively returns to its prior condition with capacitor **41** rapidly re-charging through resistor **36.** Thus, a quasi-rectangular positive output voltage pulse is produced at terminal **42,** and a complementary signal is furnished at terminal **43.**

The counter **17** will now be more particularly described with reference to FIGS. **3** to **5** and referring first of all to FIG. **3** there is shown therein a single stage of the counter **17.** This stage comprises a pair of n-p-n transistors **44** and **45** the emitters of which are grounded. The collector of the transistor **44** is connected through a resistor **46** to a positive supply rail **47** and the collector of the transistor **45** is connected through a pair of series connected resistors **48** and **49** to the rail **47.** The base of the transistor **44** is connected on the one hand through a resistor **50** to the collector of the transistor **45** and on the other hand through a resistor **51** to a negative supply rail **52.** The base of the transistor **45** is connected on the one hand through a resistor **53** to the collector of the transistor **44** and on the other hand through a resistor **54** to the rail **52.** The collectors of the two transistors **44** and **45** are connected together through a series circuit comprising a resistor **55,** two capacitors **56** and **57** and a further resistor **58,** the junction of the two capacitors **56** and **57** being connected to a terminal **59** of said stage of the binary counter **17.** Moreover, the cathode of a diode **60** is connected to the junction of the resistor **55** and the capacitor **56** whilst the anode of this diode is connected to the junction of the resistors **50** and **51,** and the cathode of the diode **61** is connected to the junction of the resistor **58** and the capacitor **57** whilst the anode of this latter diode is connected to the junction of the resistors **53** and **54.** Finally, the collector of transistor **44** is connected to a terminal **62** of said stage whilst the collector of the transistor is connected on the one hand to a terminal **63** of said stage and on the other hand to a further terminal **64** of said stage through a diode **65.** The junction of the resistors **48** and **49** is connected to a terminal **66** of said stage and a terminal **67** is grounded. The circuit of the aforesaid stage is largely symmetrical, and constitutes a cross-coupled bistable trigger. The condition in which the the transistor **45** conducts is regarded as representing binary "0" and the other state is used to represent binary "1." Since the transistors have their emitters at zero potential, the outputs from their collectors are substantially zero or positive. The output at terminal **63** is at substantially zero volts when the counter stage is in the binary "0" state. A complementary output is provided at terminal **62.** The counter can be triggered from one state to the other by means of sufficiently large and abrupt negative going

voltage transitions at the terminal **59.** If the transistor **44** is non-conducting, its collector potential is high. Consequently a large reverse voltage bias is applied through resistor **55** to the diode **60.** In contrast, the diode **61** has no large reverse bias, since the collector of the transistor **45** is at approximately zero potential. In consequence, the occurrence of a fast negative-going excursion of potential at terminal **59** will turn off transistor **45** at its base, by reason of the signal path through capacitor **57** and diode **61.** Turning off the transistor **45** triggers the circuit into its other stable stage. The relaxation time constant of the resistor **55** and capacitor **56,** as that of its symmetrical counterpart, is chosen to be adequately short compared with the minimum interval between input triggering signals. Consequently, a succession of input triggering signals causes the bistable to trigger successionally to and fro between its two stable states. Positive-going edges at the terminal **59** are ignored by the circuit, since they reverse bias both diodes **60** and **61.** An output is provided at terminal **66** and the voltage excursions provided at this output terminal have approximately half the amplitude of the excursions of the collector. Consequently this output is suitable for driving an input terminal of another similar binary counter unit which input signal is similar to the terminal **59** of the present stage. Terminal **64** is a zero re-set input terminal which is normally maintained at the potential of a positive supply rail. In consequence diode **65** is normally non-conducting. Reducing the potential of the terminal **64** to zero loads down the potential of the collector of the transistor **45** thereby ensuring that the transistor **44** is non-conducting and the transistor **45** is conducting. Returning the potential of terminal **64** to that of the positive supply rail again leaves the binary stage in a state where the transistor **45** is conducting, corresponding to a count of zero. This state will be retained by the counter stage until it is next reversed by an input pulse from terminal **59.**

A chain of binary counter stages formed by linking output terminal **66** to input terminal **59** of the next stage constitutes a straight binary counter, having a capacity of 2^n states, where N is the number of binary stages. The capacity of such a counter may be reduced to a smaller number by adding an automatic zero reset circuit. The counter shown in FIG. **5** comprises four stages **67, 68, 69** and **70** together with a zero reset circuit **71** which is arranged to provide a resetting pulse to terminal **64** of all four binary stages when they achieve the combination of states corresponding to a count of **10.**

The zero reset circuit **71** will now be more particularly described with reference to FIG. **4.** This circuit **71** comprises a pair of n-p-n transistors **72** and **73** the emitters of which are grounded and the collectors of which are connected together and connected through a resistor **74** to a positive supply rail **75.** The collectors of the transistors **72** and **73** are also connected on the one hand to a terminal **76** and on the other hand through a series circuit comprising a capacitor **77** and a pair of resistors **78** and **79** to the rail **75.** The junction of the resistors **78** and **79** is connected to the base of a p-n-p transistor **80** the emitter of which is connected to the rail **75** and the collector of which is connected through a resistor **81** to the base of the transistor **72** which is also connected through a capacitor **82** to ground. Four output diodes **83** are also provided and the anodes of these diodes are connected in parallel connected on the one hand through a resistor **84** to the supply rail **75** and on the other hand to the anode of a diode **85** a cathode of which is connected to the base of the transistor **72.** The base of the transistor **73** is connected to the junction of a pair of resistors **86** and **87,** the other end of the resistor **87** being grounded and the other end of the resistor **86** being connected through a capacitor **88** to an input terminal **89.** Referring to FIG. **5** terminal **76** of the reset circuit **71** is connected in parallel to the four terminals **64** of the four stages and the cathodes of the four diodes **83** are respectively connected to the terminal **62** of the stage **67,** the terminal **63** of the stage **68,** the terminal **62** of the stage **69** and the terminal **63** of the stage **70,** the diodes **83** forming an And gate. The counter **17** is arranged to be reset when it reaches a count of 10 (which in binary form is indicated by 0101) and by reason of the connection between the cathodes of the diodes **83** and the stages **67, 68, 69** and **70** it will be seen that transistor **72** of the zero reset circuit **71** will conduct when the counter reaches a count of 10 and the monostable constituted by transistors **72** and **73** will be triggered causing the potential of terminal **76** to descend temporarily from that of the positive supply rail **75** to approximately zero thereby affording a signal suitable for re-setting the binary counter stages to zero. By suitable design, the duration of this resetting pulse is substantially shorter than the shortest interval between input pulses to the counter. This time is determined by the relaxation time constant associated with capacitor **77.** Capacitor **82** enables the coincidence input signal to transistor **72** to be briefly persistent in order to prevent the possibility of very fast re-setting of one binary stage removing the coincidence from transistor **72** before the re-generation process via transistor **73** is effectively established. The duration of a re-set pulse from terminal **76** is by suitable design adequate to override inter-stage carry signals within the counter. Transistor **73,** normally non-conducting, is also able to trigger the re-set pulse generator, being rendered briefly conducting by a positive-going excursion of potential of the input terminal **89** which is coupled to the base of transistor **73** by a pulse forming differentiating network. This terminal **7** is of course connected through the capacitor **25** through the timing pulse generator **16** and the input terminal **59** of the stage **67** is connected to the eighth channel of the reading head **14.** In operation input terminal **89** receives abrupt positive going excursions from the collector output of transistor **34** of the timing pulse generator **16** thereby causing the counter **17** to be re-set to zero by the leading edge of the timing pulse produced by the generator **16.**

Turning now to the comparator **18** this will now be more particularly described with reference to FIG. **6** of the accompanying drawing. The comparator **18** comprises four n-p-n transistors **90, 91, 92** and **93** the collector emitter junctions of which are connected in parallel with the emitters grounded and the collectors connected through a resistor **94** to a positive voltage supply terminal **95.** An output terminal **96** of the comparator is connected to the junction between the resistor **94** and the collectors of the transistors **90, 91, 92** and **93** and an output signal is received at the terminal **96** only when all the transistors **90, 91, 92** and **93** are turned off. The bases of the transistors are connected to similar circuits only one of which is illustrated connected

to the base of the transistor **90.** Each of these circuits comprises a pair of n-p-n transistors **97** and **98** the emitters of which are grounded. The collectors of the transistors **97** and **98** are connected respectively through resistors **99** and **100** to input terminals **101** and **102** respectively. The base of the transistor **97** is connected through a resistor **103** to the terminal **102** and the base of the transistor **98** is connected through a resistor **104** to the terminal **101.** The collectors of the two transistors **97** and **98** are connected together through a pair of series connected resistors **105** and **106** the junction of which is on the one hand connected through a resistor **107** to ground and on the other hand to the base of the transistor **90.** The input terminals **101** of the four similar circuits are connected to the corresponding signal channels of the inputs from the encoder **19** whilst the four input terminals **102** of the four similar circuits are connected to the corresponding signal channels of the inputs from the counter **17.** Moreover, the output terminal **96** of the comparator is connected to an input of the bistable circuit **20.**

In use, the signal applied to each of the terminals **101** and **102** is bi-valued, being either at approximately zero potential or at a substantial positive potential. The transistor **97** receives base current through resistor **103** from input terminal **102** when the signal applied to this terminal is positive, and a collector supply voltage is applied through resistor **99** from terminal **101** when this is positive. Thus, the collector potential of transistor **97** is approximately zero except when a positive potential on terminal **101** and zero potential on terminal **102** are simultaneously present. A supply voltage to the collector of transistor **97** through resistor **105** from terminal **102** is only present when the latter terminal also makes transistor **97** conducting. In like manner, the collector potential of transistor **98** is substantially positive only when a positive input to terminal **102** co-exists with a zero input to terminal **101.** The transistor **90** receives base current through resistor **105** whenever the collector potential of transistor **97** is substantially positive, and likewise receives current via resistor **106** unless the transistor **98** is bottomed. Thus, transistor **90** will be nonconducting only when both transistors **97** and **98** are bottomed, i.e. when input terminals **101** and **102** are in corresponding state.

Turning now to the static register **15,** this consists of seven bistable circuits of which one is shown in FIG. **7.** This bistable circuit comprises a pair of n-p-n transistors **108** and **109** the emitters of which are grounded and the collectors of which are connected through a pair of resistors **110** and **111** respectively to a positive voltage supply rail **112.** The base of the transistor **108** is connected on the one hand through a resistor **113** to a negative voltage supply rail **114** and on the hand through a resistor **115** to the collector of the transistor **109.** The base of the transistor **109** is connected on the one hand through a resistor **116** to the supply rail **114** and on the other hand through a resistor **117** to the collector of the transistor **108.** Five terminals **118, 119, 120, 121** and **122** are provided, the terminal **121** being grounded and terminal **120** being connected to the collector of the transistor **109.** The terminals **118** and **119** are connected together through a series circuit comprising a resistor **123** a pair of capacitors **124** and **125** and a further resistor **126,** the junction of the two capacitors **124** and **125** being connected to the terminal **122.** Finally, a pair of diodes **127** and **128** are provided, the cathode of the diode **127** being connected to the junction of the resistor **123** and the capacitor **124** and the anode of the diode **127** being connected to the base of the transistor **108,** whilst the cathode of the diode **128** is connected to the junction of the resistor **126** and the capacitor **125** and the anode of the diode **128** is connected to the base of the transistor **109.** Each of the seven bistable circuits receives paraphased d.c. inputs representing one channel of the reading head output and all receive a common read pulse input, a negative going edge derived from the output of the bistable circuit **20.** Each of the seven bistable circuits provide a d.c. output to the digital-to-analogue converter **21.** When the input signifies binary "0," approximately zero potential is applied to input terminal **118** by the reading head output which also applies a substantial positive potential to terminal **119.** In consequence, a negative going excursion of the potential applied to terminal **122** turns off transistor **108** by conduction in diode **127,** whilst diode **128** is blocked by the reverse bias applied through the terminal **119.** This leaves the bistable circuit in the state in which the transistor **109** is conducting, and the output potential at terminal **120** is approximately zero. This state is maintained irrespective of further input at terminal **122** for so long as the d.c. inputs to terminals **118** and **119** remain the same. If these d.c. inputs reverse values, then the bistable will change into its other stable state at the next negative going edge received at terminal **122,** thereby changing over the binary signal presented at output terminal **120.** As aforesaid, the static register **15** consists of seven identical bistable circuits. In operation this set together sample the first seven channels of the output of the reading head **14** present at the instant when an input signal is received at terminal **122** at all the bistable circuits of the register at the instant when the bistable circuit **20** is reset. The register will therefore furnish at its output terminals **120** a signal representing the input to the register **15** at the last previous instant of sampling.

Both the digital-to-analogue converter **21** and the encoder **19** may be of any convenient known form. By way of example, a suitable digital to analogue converter is shown in Page 675 of the book pulse, digital and switching waveforms published in 1965 by McGraw-Hill. A suitable encoder is the Baldwin model **57***a* described in the magazine 'Instruments and Control Systems' for May, 1970.

Going through the operation of the above disclosured circuitry step by step so as to further facilitate understanding thereof, one may initially suppose that the drum **12** performs a complete revolution/cycle of the engine and that the engine has a top speed of just under 6,000 r.p.m. i.e. just under 3,000 (four stroke) cycles/minutes. Accordingly, the drum completes nearly a full revolution at full engine speed in a period of 1/50 *th* second, i.e. 20 mS. The unique datum signal provided by the first row of the first set of digits stored on the drum may conveniently be a full set of eight binary "1's" so that each time this reference row of information passes under the reading head **14** a coincidence signal is detected by the detector **23** and the pulse generator **16** is accordingly triggered to produce a pulse which could conveniently be 20 mS in duration. Hence when the trailing edge of this timing pulse occurs, the drum will have travelled an angular distance past the position in which the datum signal was presented to the

reading head **14,** proportional to the prevailing speed of the engine, a distance which is almost a full revolution when the engine is at a maximum. In consequence, by suitably positioning a given row of information on the memory drum it is possible to arrange that this row appears under the reading head **14** in time coincidence with the trailing edge of the timing pulse whenever the engine is running at a particular speed. For example, a row of information positioned at 180° away from the datum row would arrive at the reading head **14** in time coincidence with the trailing edge of the timing pulses produced by the timing pulse generator **16** when the engine is running at approximately half full speed.

In practice it is necessary to have several rows of information for controlling the fuel supply to the engine for each engine speed, so as to enable a selection to be made depending upon throttle opening, and in the version above described these sets of information are stored on consecutive rows of the drum. The eighth channel of the reading head **14** furnishes a pulse for every row of information on the drum. As the rows of information constituting each such set are presented serially to the reading head **14** it is necessary to include means of selecting the correct row of information and to transfer it to the static register **15** so as to make it continuously available for control purposes until it is next revised. This is accomplished by the arrangement including counter **17** which is re-set to zero at the commencement of the timing pulse, i.e. at the moment when the datum row is under the reading head **14** and thereafter counter pulses furnished by the eighth channel of the reading head **14,** one for each row of the drum information. The capacity of the counter **17** is arranged to be equal to the number of rows in each set of information on the drum hence the state of the counter maintains correspondence with the ordinal position in its set of the row currently presented to the reading head. The digital throttle position encoder **19** furnishes signals to the digital comparator **18** which also receives signals representing the state of the counter **17.** Each signal combination furnished by the throttle angle encoder **19** corresponds to a small range of throttle angles and the corresponding quantity of fuel is represented by the information on the row presented to the reading head **14** when the counter **17** is in a corresponding state to the signal furnished by the throttle angle encoder. In other words the ordinal position in its set of a given row of information on the drum corresponds with a particular state of the counter **17,** and for the corresponding set of signals from the throttle angle encoder furnished by it when the relevant range of throttle angles is obtained. If it is supposed that the engine is rotating at half its full speed then the trailing edge of the timing pulses produced by the timing pulse generator **16** will occur as explained earlier when a portion of the drum about 180° away from the datum row is presented to the reading head **14.** If we suppose that the start of a set of information arrives at the reading head at this instant then we can think of successive rows of this set passing the reading head, with the eighth channel causing the contents of the counter **17** to maintain correspondence until it achieves the state corresponding with the signal combination currently furnished by the throttle angle encoder. Upon arrival of this row of drum information under the receiving head **14,** comparator **18** provides the pulse re-setting bi-stable circuit **20** and causing the information currently presented to the reading head **14** to be transferred to the static register **15** by reason of the pulse furnished to the register **15** from the bi-stable circuit **20** at this moment.

The trailing edge of the delay pulse produced by the timer **16** sets the bi-stable circuit **20,** the re-setting of which provides a shift pulse for accepting digital information from the reading head **14** into the static register **15.**

Clearly, if the fifth row of drum information was specified by the prevailing throttle angle encoder signal combination and the trailing edge of the delay pulse produced by the timing pulse generator **16** occurred when the sixth or later row of particular set is under the reading head **14** then the arrangement described would sample the fifth row of the next set of drum information to arrive at the reading head **14.** The disposition of the sets of information on the drum is preferably arranged so as to minimise the errors thus introduced in representing engine speed. It will be seen that the arrangement described enables a particular row of information selected by the approximate engine speed and throttle opening of the engine to be reproduced in the static register **15** and to be revised if necessary **1** per revolution of the drum. This continually updated digital information is furnished to the digital-to-analogue converter **21** used to control suitable fuel dispensing means at the engine, for example pulse timing means for controlling electro-magnetic switching valves used in known forms of petrol injection.

It should further be appreciated that the information which would be typically found on one information set on the memory drum and the form of the information is as follows. The eighth channel consists of a complete row of binary "1's" and the other seven channels in each row a coded (e.g. binary) representation of a number signifying fuel shot size or quantity.

It will be understood that the number of sets of information on the drum **12,** the number of bits in a row, and the number of rows in a set can all be varied, to suit the accuracy requirements of the system. The encoder **19** must of course have a number of outputs equal to the number of rows in a set. In order to achieve high accuracy with a relatively small memory device it is possible to arrange for the output from the static register **15** to be used as a trimming adjustment to the engine fuel control, which is primarily controlled by a separate system, which may for example, be responsive only to manifold pressure.

In a modification, the number of signals produced by the encoder **19** is equal to the number of sets of information on the drum **12,** and the counter **17** is operated only by the first row in each set, so that the counter **17** indicates the set passing the head **14** at any instant, and re-sets to zero when all the sets have passed the head **14.** When the signals from the counter **17** and encoder **19** are equal, the comparator **18** sets the bi-stable circuit **20** and also starts a timer, which operates for a fixed period at the end of which the bistable circuit **20** is re-set to trigger the register **15.** The fixed period is less than the time taken for a set to pass the head **14** even at maximum engine speed, and it will be seen that the throttle angle will determine which set is selected, and the engine speed will determine which row in the set is utilized.

Other known forms of digital memory device can of course be used in place of the drum **12.**

We claim:

1. A petrol injection system for an internal combustion engine having first and second significant parameters including a digital memory device on which are stored a plurality of sets of information, each set containing a number of digital coded signals representing different fuel requirements, a control device in which is stored a digital control signal determining the quantity of fuel delivered to the engine, the control signal being obtained from said memory device, means responsive to said first significant parameter for determining from which set the digital signal fed from the memory device to the control device is obtained, and means sensitive to said second significant parameter for determining which digital coded signal from the chosen set is fed from the memory device to the control device, each coded signal including a bit of information operating a counter which runs from zero to $(n-1)$ and then re-sets, where n is the number of coded signals in a set, said means sensitive to said second significant paramemter being in the form of an encoder having one of n outputs corresponding to the n readings of the counter, the system including a comparator which compares the outputs of the counter and the encoder and produces an output pulse each time the outputs are equal, so that one output pulse is produced for each set of information passing a given point, and a timing device which is initiated by a signal from one set of information and operated for a fixed period, after which the next output pulse from the comparator causes a signal to be fed from the memory device to the control device to constitute the control signal.

2. A petrol injection system for an internal combustion engine having first and second significant parameters, including a digital memory device on which are stored a plurality of sets of information, each set containing a number of digital coded signals representing different fuel requirements, a control device in which is stored a digital control signal determining the quantity of fuel delivered to the engine, the control signal being obtained from said memory device, means responsive to said first significant parameter for determining from which set the digital signal fed from the memory device to the control device is obtained, and means sensitive to said second significant parameter for determining which digital coded signal from the chosen set is fed from the memory device to the control device, each set of information including a bit of information operating a counter having m readings, said counter running from zero to $(m-1)$ and resetting, said means sensitive to said first significant parameter being in the form of an encoder having one of m outputs corresponding to the m readings of the counter, the system including a comparator which compares the outputs of the counter and the encoder and produces an output pulse when the outputs are equal, the output pulse operating a timer which operates for a fixed period which is less than the time taken for a set to pass a given point even at maximum engine speed, a signal being fed from the memory device to the control device to constitute the control signal at the end of said fixed period.

3. A system as claimed in claim 2 in which the first and second significant parameters are engine speed and throttle opening respectively.

4. A system as claimed in claim 2 in which the first and second significant parameters are engine speed and manifold pressure respectively.

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