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APPARATUS

(57) **Abrégé/Abstract:**

A data processing apparatus includes a microprocessor which processes data and outputs m bits of data simultaneously and a semiconductor chip module. The module has a plurality of memory chips having data width of n bits data formed on each side of a substrate. The apparatus further includes data lines connected to the microprocessor and the memory chips for slicing m bit data into n bit data and providing the sliced n bit data to each memory chip. The data of a data processing apparatus is transmitted by the microprocessor and the memory chips. The microprocessor outputs an address signal to the memory chips. One group of the memory chips outputs data upper n bits to the microprocessor in parallel based on the address signal. The other group of the memory chips outputs data of lower (m-n) bits to the microprocessor in parallel based on the address signal.



ABSTRACT

A data processing apparatus includes a microprocessor which processes data and outputs m bits of data simultaneously and a semiconductor chip module. The module has a plurality of memory chips having data width of n bits data formed on each side of a substrate. The apparatus further includes data lines connected to the microprocessor and the memory chips for slicing m bit data into n bit data and providing the sliced n bit data to each memory chip. The data of a data processing apparatus is transmitted by the microprocessor and the memory chips. The microprocessor outputs an address signal to the memory chips. One group of the memory chips outputs data upper n bits to the microprocessor in parallel based on the address signal. The other group of the memory chips outputs data of lower $(m-n)$ bits to the microprocessor in parallel based on the address signal.

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DATA PROCESSING APPARATUS AND METHOD OF DATA TRANSMISSION OF
DATA PROCESSING APPARATUS

This is a division of co-pending Canadian Patent
5 Application Serial No. 2,061,949, filed on February 27,
1992, now issued.

Technical Field

The present invention relates to a data processing
apparatus and a method of data transmission of a data
10 processing apparatus.

Background Information

It is sought to achieve the miniaturization of an
electronic circuit package, and, more particularly, to an
extra-small computer for use in space exploration.

15 A number of computers are being employed for various
uses and the demand for smaller and lighter computers has
increased. Computers for use in space are required to be
particularly small and light in order to decrease the
launching costs while increasing the payload.

20 As shown by a photograph 1 of "Development of LSI for
Radiation Resistant 16-Bit Microprocessor", pp. 10 - 411,
Goke et al, Collection of Papers at 32nd Space Science and
Technology Federation Lecture Meeting, a space computer can
be built of discrete parts with reliable, resistant-to-
25 environment single chips contained in one package.

There is no serious consideration of decreasing the
size and weight of a computer comprised of discrete parts.

On the other hand, a so-called multiple chip mounting
technique, that is, the technique of mounting a plurality of
30 bare chips on one wiring substrate for use on the ground is
being studied. It has heretofore been arranged that, as
shown in Fig. 3 of "Nikkei Micro Device", pp. 32 - 40,

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December Issue, 1989, a wiring conductor connected to a bonding pad is led out from the bonding pad.

5 Making the wiring density uniform was not considered in this technique. The wiring density around the die bonding pad in particular is extremely high and consequently effective wiring cannot be implemented. The wiring density in the outermost layer causes a bottleneck and the package size is not sufficiently reduced. As the hole connecting the upper and lower layers occupied most of the area on this particular multilayer wiring substrate, the holes account for a large percentage of the area of the outermost layer, particularly around the die bonding pad.

15 With respect to a fault tolerant system, a checking unit for detecting errors and faults and a unit under check are accommodated in one and the same chip to reduce its size, as described in "Trial Manufacture and Evaluation of Fault Tolerant Quartz Oscillation IC", by Tsuchimura et al, Research Material, 24th FTC Study Meeting. With the diffusion of ASICs (Application Specified ICs) in particular, attempts have been made to add an MPU inspection circuit by making an ordinary MPU a core through the ASIC technology.

25 Faults and trouble affecting the whole chip were not taken into consideration in this technique. If the checking unit and the unit under check develop trouble simultaneously, the irregularity may not be detected.

Summary of the Invention

It is an object of the present invention to provide an improved data processing apparatus.

30 It is another object of the present invention to provide an improved method of data transmission of a data processing apparatus.

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In accordance with one aspect of the present invention, there is provided a method of data transmission of a data processing apparatus which comprises a microprocessor having data width of m bits (wherein m is an integer), a plurality
5 of memory chips connected to said microprocessor, said plurality of memory chips being divided into two groups, and each of said groups of memory chips is mounted on different substrate surfaces, said method comprising the steps of: said microprocessor outputting an address signal to said
10 plurality of memory chips; one of said groups of memory chips mounted on one of said substrate surfaces outputting data upper n bits to said microprocessor in parallel based on said address signal; and the other of said groups of memory chips mounted on another of said substrate surfaces
15 outputting data of lower $(m-n)$ bits to said microprocessor in parallel based on said address signal.

In accordance with another aspect of the present invention, there is provided a method of data transmission of a data processing apparatus which comprises a
20 microprocessor having data width of m bits (wherein m is an integer), a plurality of memory chips connected to said microprocessor, each of said memory chips having data width of n bits (wherein n is an integer, and m is an integer times n), and said plurality of memory chips is divided into
25 two groups, wherein each of said groups of memory chips is mounted on a different substrate surface than the other of said groups of memory chips, said method comprising the steps of: said microprocessor outputting an address signal for demanding m bit data to each memory chip; and each of
30 said memory chips outputting a combined total of m bit data to said microprocessor simultaneously based on said address signal.

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In accordance with yet another aspect of the present invention, there is provided a data processing apparatus, comprising: a microprocessor which processes data and outputs m bits of data (wherein m is an integer)

5 simultaneously; a semiconductor chip module including: a substrate, and a plurality of memory chips having data width of n bits data (wherein n is an integer, and m is integer times of n) formed on each side of said substrate; and data lines connected to said microprocessor and said plurality of

10 memory chips for slicing m bit data into n bit data and providing said sliced n bit data to each of said memory chips.

In accordance with still yet another aspect of the present invention, there is provided a method of data

15 transmission for a data processing apparatus which comprises a microprocessor for processing data, a semiconductor chip module including a substrate and a plurality of memory chips having data width of n bit data (wherein n is an integer, and m is an integer times n) formed on each side of said

20 substrate, data lines connected to said microprocessor and said plurality of memory chips for slicing m bit data into n bit data and providing said sliced n bit data to each memory chip, said method comprising the steps of: said microprocessor outputting an address signal and m bit data

25 (wherein m is an integer) simultaneously; and each of said memory chip storing n bit data in parallel based on said address signal.

In accordance with still yet another aspect of the present invention, there is provided a data processing

30 apparatus, comprising: a processor having a data width of m bits; a plurality of memory modules connected to data lines, each of said memory modules comprising: a first group of

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memory chips mounted on one side of said substrate, and a second group of memory chips mounted on another side of said substrate, wherein said first group of memory chips outputting data of upper n bits, and said second group of memory chips outputting data of lower $(m-n)$ bits; and a selection circuit which outputs a selection signal for selecting a memory module from among said plurality of memory modules based on a signal output by said processor, wherein the memory module selected by said selection circuit outputs data of m bits to said processor in parallel based on an address of said processor.

In accordance with still yet another aspect of the present invention, there is provided a data processing apparatus, comprising: a processor having data width of m bits (m is an integer); a memory module comprising: a first group of memory chips mounted on one side of a substrate, and a second group of memory chips mounted on another side of said substrate, wherein said first group of memory chips output data of n bits, and said second group of memory chips output data of $(m-n)$ bits; and a selection circuit which selects a memory chip from among said plurality of memory chips based on a signal output from said processor; wherein said processor write data to memory chip selected by said selected circuit.

In accordance with still yet another aspect of the present invention, there is provided a data processing apparatus, comprising: a processor having data width of m bits (m is an integer); a memory module comprising: first data lines for transmitting data of n bits (n is an integer), second data lines for transmitting data of $(m-n)$ bits, a first group of memory chips connected to said first data lines and mounted on one side of a substrate, a second

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group of memory chips connected to said first data lines and mounted on one side of said substrate, a third group of memory chips connected to said second data lines and mounted on another side of said substrate, and a fourth group of memory chips connected to said second data lines and mounted on another side of said substrate; and wherein said memory module outputs data of m bits to said processor in parallel based on address of said processor.

In accordance with still yet another aspect of the present invention, there is provided a data processing apparatus, comprising: a processor which outputs address and data of m bits; a memory module comprising: first data lines for transmitting data of n bits, second data lines for transmitting data of (m-n) bits, a first group of memory chips mounted on one side of a substrate and connected to said first data lines, a second group of memory chips mounted on one side of said substrate and connected to said first data lines, a third group of memory chips mounted on another side of said substrate and connected to said second data lines, and a fourth group of memory chips mounted on another side of said substrate and connected to said second data lines; a selection circuit which selects two groups of memory chips based on address output from said processor, and wherein said memory module outputs data of m bits to said processor in parallel based on address of said processor.

Brief Description of the Drawings

The present invention taken in conjunction with the invention disclosed in co-pending Canadian Patent Application Serial No. 2,061,949 which was filed on February 27, 1992, now issued, will be disclosed hereinbelow with the aid of the accompanying drawings in which:

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Fig. 1 is an overall structural view of an embodiment of the present invention;

Fig. 2 is a sectional view of a die bonding portion of a wiring substrate according to an embodiment of the present invention;

Fig. 3 is a diagram showing an arrangement of holes in an embodiment of the present invention;

Fig. 4 is a diagram showing the division of a data bus in an embodiment of the present invention;

Fig. 5 is a diagram showing the division of a data bus having a 32 bit width in an embodiment of the present invention;

Fig. 6 is a structural view of an MPU with a checking circuit and a RAM with an error correction code on a wiring substrate in an embodiment of the present invention;

Fig. 7 is a structural view of an MPU with an external ROM on a wiring substrate in an embodiment of the present invention;

Fig. 8 is a circuit diagram of electronic apparatus according to the present invention;

Fig. 9 is a diagram showing packaging of semiconductor chips as shown in Fig. 8 on one side of a wiring substrate;

Fig. 10 is a diagram showing packaging of semiconductor chips as shown in Fig. 8 on the other side of the wiring substrate; and

Fig. 11 (with Fig. 1) is a sectional view of a package in an embodiment of the present invention.

Detailed Description

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Fig. 1 illustrates the inner construction of electronic apparatus embodying the present invention by way of example. In the embodiment shown, MPU 101, RAM 102, ROM 103, FPU (Floating-point Processing Unit) 104, DMAC (Direct Memory Access Controller) 105, and an interface circuit 106 are connected via a bus 100 in a wiring substrate 10. What is particularly noticeable according to this embodiment is that the bus 100 is not led out of the wiring substrate 10, but only an interface line 107 for connection to external devices is led out of the substrate 10.

All semiconductor chips connected to the bus 100 are totally packaged on the wiring substrate 10 according to this embodiment. As the bus 100 is not led out of the substrate 10, the number of signal lines connecting internal and external devices is reduced by a large margin. Accordingly, the number of pins connecting the signal lines inside and outside the wiring substrate 10 decreases and this avoids an obstacle to rendering the wiring substrate smaller and lighter.

Fig. 2 is a sectional view of a die bonding portion of the wiring substrate 10. Wire bonding pads 11 are formed on the substrate 10 and an insulating layer 16 is formed on a wiring conductor 14 for use in leading out the wire bonding pad. A die bonding ground 15 is formed on the insulating layer 16, and a semiconductor chip 20 is bonded thereto by die bonding. A bonding wire 30 is then used for connecting a wire bonding pad 21 on the semiconductor chip 20 to the wire bonding pad 11 on the wiring substrate 10. According to this embodiment, as shown in Fig. 3, holes 13, 13' may be formed in the periphery and inside of the die bonding ground 15, respectively. The hole 13 formed in the periphery of the die bonding ground 15 and the wire hole 13' formed inside the die bonding ground 15 are preferably arranged alternately. As a result, a portion beneath the die bonding ground 15 as the outermost layer that has heretofore been unutilized can be put to practical use as a wiring and a hole region. An area to be occupied by the wiring and hole regions can thus be made

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drastically smaller than the area occupied by the semiconductor chip of the wiring substrate.

Fig. 4 refers to an embodiment wherein signal lines of the data bus 100 connected to the MPU 101 are divided into two groups 100-1 and 100-2. RAMs 102-1 - 102-k and ROMs 103-1 - 103-k connected to the data bus 100-1 are packaged on one side (B side) of the substrate, while RAMs 102-(k + 1) - 102-N, ROMs 103-(k + 1) - 103-N connected to the data bus 100-2 are packaged on the other side (A side) of the substrate, wherein k and N is each an integer. According to this embodiment, it is unnecessary to connect the data bus on the A side to what is on the B side and hence the number of holes in a wide area can be reduced. As a result, an area to be occupied by wiring and hole regions can thus be made drastically smaller than the area occupied by the semiconductor chip of the wiring substrate, so that the apparatus can be made smaller and lighter.

Fig. 5 refers to an embodiment in which the data bus 100 connected to the MPU 101 is 32 bits wide and the data bus connected to the ROM and RAM is 8 bits wide. Data lines D0 - D31 constituting the data bus 100, D0 - D15 are formed into a group of data bus 100-1, and lines D16 - D31 into a group of data bus 100-2. Lines D0 - D7 in the group of data bus 100-1 are connected to the RAM 102-1 and the ROM 103-1, and lines D8 - D15 to the RAM 102-2 and the ROM 103-2. Moreover, lines D16 - D23 in the group of data bus 100-2 are connected to the RAM 102-3 and the ROM 103-3, and lines D24 - D31 to the RAM 102-4 and the ROM 103-4. According to this embodiment, the apparatus can be made smaller and lighter as in the case of the embodiment shown in Fig. 4.

According to the embodiments shown in Figs. 2 to 5, it is also possible to package as many bare chips as possible on the wiring substrate that is limited in size.

Fig. 6 refers to an embodiment wherein the MPU 101, a checking circuit 111 of the MPU 101, and the RAM 102 and an error correction code encoding/decoding circuit 112 are packaged in the form of bare chips on the wiring substrate 10.

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In this case, the bonding wire has been omitted for simplification.

The MPU 101 and the checking circuit 111 are different bare chips and are connected by wire bonding on the wiring substrate 10. Heretofore, various systems have been proposed for the checking circuit 111. There are the following, for instance:

(1) A watch dog timer for resetting the MPU 101 after sensing its operation on an impulse when it is inaccessible within a fixed period of time.

(2) A system having a reference MPU (not shown) within the checking circuit 111 for comparing the output signal of the reference MPU with that of the MPU 101, regarding the reference MPU or the MPU 101 as irregular when nonconformity is found.

In the conventional method of packaging the MPU 101 and the checking circuit 111 separately, the number of packages, the number of wires and the dimensions of the apparatus tend to increase. In the method recently followed for forming the MPU 101 and the checking circuit 111 on the same chip, moreover, a fault involving the whole chip is not completely detectable as even the checking circuit 111 then ceases to function.

According to this embodiment, the MPU 101 with the checking circuit 111 is capable of detecting a fault involving the whole chip without causing the number of packages and that of wires to increase. Therefore, a small lightweight, reliable apparatus can be achieved.

The RAM 102 and the error correction code encoding/decoding circuit 112 are different bare chips and are connected by wire bonding on the wiring substrate 10.

The error correction code adds an error detection/correction redundant bit to the data stored in the memory, thus causing an error to be detected and corrected by making a code-to-code Hamming distance 4 or greater. When the code-to-code Hamming distance is set to 4, 1-bit error correction is possible, but a 2-bit error remains only

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detectable. Consequently, it is called SECDED (Single-Error-Correction, Double-Error Detection). For instance, a 6-bit detection/correction redundant bit needs to be added when SECDED is to be realized for 16-bit data. A detailed description of an error correction code is omitted since the present invention is not concerned therewith.

In the conventional method of packaging the RAM 102 and the error correction code encoding/decoding circuit 112 separately, the number of packages, the number of wires and the dimensions of the apparatus tend to increase. In the method recently followed for forming the RAM 102 and the error correction code encoding/decoding circuit 112 on the same chip, moreover, a fault involving the whole chip is not completely detectable as even the error correction code encoding/decoding circuit 112 then ceases to function.

According to this embodiment, the RAM 102 with the error correction code encoding/decoding circuit 112 is capable of detecting a fault involving the whole chip without causing the number of packages and wires to increase. Therefore, a small lightweight, reliable apparatus can be achieved.

Like other semiconductor elements, the storage element (ROM) storing the program involved is packaged on the same wiring substrate in the form of a bare chip, and, if it is incorporated into the same package, the apparatus can be made drastically smaller and lighter. If the ROM is incorporated into the package, it will require to devise its programming and erasing methods. Use of an EPROM (Electrically Erasable Programmable ROM) will make programming readily possible and make the program erasable. Even when a UVEPROM (Ultra-Violet Erasable Programmable ROM) is used, the program can be executed or erased by providing the apparatus with a window that allows erasing ultra-violet rays to pass therethrough.

When an EPROM is used as space electronic apparatus to be exposed to cosmic rays, the data written by the cosmic rays may be erased. Moreover, an EPROM is not suitable for use in an electronic apparatus to be used over several hundred thousand years, due to the electronic thermal movement.

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Therefore, mask- or fuse-ROMs will have to be used for this purpose.

For program development, the program involved has to be modified and rewritten. For this reason, a mask- or fuse-ROM
5 may not be used efficiently for such program development.

According to the following embodiment of the present invention, the electronic apparatus leads the line connected to the ROM out of the package and makes it possible to operate the ROM outside the package. Consequently, no wire bonding is
10 provided for the ROM in the developing package. By connecting a program externally, that is, its easily erasable EPROM to an external device, any program may be developed by means of a wiring substrate having the same pattern as that proposed in the present description.

15 Fig. 7 refers to an embodiment wherein either the ROM inside the wiring substrate 10 or an external ROM can be used to operate the MPU. The RAM 102 and the ROM 103 are connected to the MPU 101 via the bus 100 in the wiring substrate 10. Moreover, the RAM 102 and the ROM 103 selection signals CS#
20 are formed by an address decoder 107. Although a signal name with a line thereon is provided for each active low signal in Fig. 7, a signal name followed by a '#' mark is employed in this specification for convenience of description. The address decoder 107 decodes higher significant bits in an
25 address signal supplied to the bus 100, and, when the address signal indicates the address of the RAM 102 or the ROM 103, applies the corresponding selection signal CS# to the RAM 102 or the ROM 103. While the selection signal CS# is active, the RAM 102 or the ROM 103 reads or writes the desired address
30 data in accordance with the lower significant bits.

According to this embodiment, a ROM 103 selection signal CS# 108 is also sent out of the wiring substrate 10. Consequently, a ROM 103' outside the wiring substrate 10 in place of the ROM 103 inside the wiring substrate 10 can be
35 used for operation. Moreover, since part of the lower significant bits in the address bus signal is enough for an address line to be connected to the ROM 103', the number of

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leader lines from the wiring substrate 10 is also prevented from increasing. In order to develop a program, it is only necessary to write the program to the ROM 103' outside the wiring substrate 10 without packaging the ROM 103 inside the wiring substrate 10. Hence, efficient program development can be made, as a program is readily written to and erased from the ROM. If a mask- and a fuse-ROM are used as the ROM 103 inside the wiring substrate 10 for an actual apparatus after program development, any fear of erasure of the data in the ROM 103 is eliminated and the apparatus stands to remain in good condition after long use.

Fig. 8 is a circuit diagram embodying the present invention. The MPU 101, RAM 102, ROM 103, FPU 104, DMAC 105, and a gate array 110 in the form of bare chips are mounted on the wiring substrate 10. Although the RAM 102 and the ROM 103 consist of a plurality of chips, depending on the memory capacity and bit width, each of them is indicated as one in Fig. 8 for simplicity. In the gate array 110 are the checking circuit 111 formed with the watch dog timer or the like for detecting the operation of MPU on impulse, the error correction code encoding/decoding circuit 112 for correcting the inversion of data in the RAM 102, the address decoder 107, and the interface circuit 106 with external devices or the like as built-in elements. (These circuits in the gate array are not shown in Fig. 8.) The number of chips can thus be reduced significantly, as the peripheral circuits of the MPU 101 are arranged in such a gate array form.

As the checking circuit 111 and the error correction code encoding/decoding circuit 112 are accommodated on chips different from those for the MPU 101 and RAM 102 with respect to the gate array 110, failure to detect a fault involving the whole chip is avoided.

Although use can be made of various kinds of respective MPU 101, FPU 104, DMAC 105, the illustration of Fig. 8 is based on the assumption that a GMICRO/200 (H32/200) series is employed. Consequently, the names of the various control signal lines are indicated in accordance with the

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specification of the GMICRO/200 (H32/200) series. Since the present invention is not limited to a particular product series, the description of the signal names is irrelevant to the present invention and are omitted; a detailed description of them has been given in a document ('H32/200 Hardware Manual', Hitachi Ltd.). Incidentally, the bit positions of the address and data lines are provided in the form of a bigendian display and the lower significant bits are therefore expressed by small numbers. For instance, A0 of the address line represents the highest significant bit, whereas A29 represents the lowest significant bit.

The bus signal lines led out of the wire substrate 10 according to this embodiment are only as follows: address lines A13 - A29, data lines D0 - D31, address strobes AS1#, AS2#, byte control signals BC0# - BC2#, a read/write switching signal R/W# and a data transfer termination signal DC#. In other words, since only a part of the bus signal lines is led out of the wiring substrate 10, the number of pins affixed to the outside of the package can be reduced so that the package size can be made smaller. If it is decided not to use ROMs outside the wiring substrate 10, all of these bus signal lines need not necessarily be led out. Thus, the number of pins can be reduced.

The address decoder 107 (not shown) in the gate array generates the ROM selection signal ROCS#108, a RAM selection signal RACE0# - RACE3#, and an external element selection signal XCS# by means of the address lines A0 - A12.

The ROM selection signal ROCS#108 on one of these signal lines is connected to the ROM 103 in the wiring substrate 10 and is simultaneously led out of the wiring substrate 10. According to this embodiment, the ROM 103' (not shown) in place of the ROM 103 inside the wiring substrate 10 can be connected to the outside of the wiring substrate 10 and used for operation. Moreover, since a part of the lower significant bits A13 - A29 in the address bus signal is enough for an address line to be connected to the ROM 103', the number of leader lines from the wiring substrate 10 is also

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prevented from increasing. In order to develop a program, it is only needed to write the program to the ROM 103' outside the wiring substrate 10 without packaging the ROM 103 inside the wiring substrate 10. Hence, efficient program development can be achieved, with a program being readily written to and erased from the ROM. If a mask- and a fuse-ROM is used as the ROM 103 inside the wiring substrate 10 for the apparatus after the program development, any risk of erasure of data in the ROM 103 is eliminated and the apparatus can be expected to remain in good condition after long use.

The RACE0# - RACE1# out of the RAM selection signals RACE0# - RACE3# are connected to the RAM 102 inside the wiring substrate 10, whereas the RACE2# - RACE3# are led out of the wiring substrate 10. If the RACE2# - RACE3# are led out of the wiring substrate 10, the byte control signal BC0# - BC2#, the read/write switching signal R/W#, the address lines A13 - A29 and the data lines D0 - D31 are connected to a RAM 102' (not shown) outside the wiring substrate 10, and an increase in the storage capacity can be attained with the combination of the RAM 102 and the RAM 102'.

The external element selection signal XCS# is led out of the wiring substrate 10, and, if the external element selection signal XCS#, the byte control signal BC0# - BC2#, the read/write switching signal R/W#, the address strobes AS1#, AS2#, the data transfer termination signal DC#, the address lines A13 - A29 and the data lines D0 - D31 are connected to an external element (not shown), the system will be improved as the external element becomes usable.

The number of pins may be drastically reduced when the external element is not connected as the RAM selection signals RACE2# - RACE3#, the selection signal XCS#, the byte control signal BC0# - BC2#, the read/write switching signal R/W#, the address strobes AS1#, AS2#, the data transfer termination signal DC#, the address lines A13 - A29 and the data lines D0 - D31 are unnecessary to lead out of the wiring substrate 10 to the RAM 102' outside the wiring substrate 10.

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In addition, the gate array 110 can be allowed to incorporate the interface circuit 106 with external devices. A signal line MIL - 1553B is employed for use in the so-called MIL - 1553B communication standard. Moreover, a communication
5 line CELLCOMCNTR is a communication line for coupling a plurality of computer units, each having the wiring substrate 10. If the number of wiring substrates 10 required is prepared for the communication lines CELLCOMCNTR to be connected together, it will facilitate the construction of a
10 multiprocessor system or a multiplex computer system for fault tolerance.

Figs. 9 and 10 illustrate methods of packaging a wiring substrate 10 embodying the apparatus shown in Fig. 8.

The MPU 101, FPU 104, ROMs 103-1, 103-2 and RAM 102-1,
15 102-2 are mounted on the surface (B side) shown in Fig. 9. The storage element, the ROMs 103-1, 103-2 and the RAMs 102-1, 102-2 connected to the data lines which belong to the bus 100-1 are mounted on this surface, as shown in Fig. 5.

The DMAC 105, the gate array 110, the ROMs 103-3, 103-4
20 and the RAMs 102-3, 102-4 are mounted on the surface (A side) shown in Fig. 10. The storage element, the ROMs 103-3, 103-4 and the RAMs 102-3, 102-4 connected to the data lines which belong to the bus 100-1 are mounted on this surface as shown in Fig. 5.

25 Since the number of wiring layer-to-layer holes can be reduced according to this embodiment, the wiring substrate 10 can be made smaller. Moreover, the concentration of heat and wiring on one side can be avoided by splitting the LSI, MPU 101, FPU 104, DMAC 105 and the gate array 110 into two groups,
30 each having a large chip size and many input-output signal lines, and allotting them to the respective sides. In view of thermal resistance, chemical stability and the like, a ceramic substrate is suitable for use as the wiring substrate 10 when it is employed in space where reliability is required.

35 Fig. 11 illustrates a package embodying the present invention. Ceramic caps 50 are attached to the respective sides of the ceramic wiring substrate 10 to hermetically seal

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the bare chips, such as the MPU 101 mounted thereon. The inside thus hermetically sealed by the caps 50 is kept under a vacuum or is filled with an inactive gas, such as nitrogen, helium or the like. If helium is used, it will conveniently be used for leakage checking when the airtightness of the seal is checked. When it is desired to accommodate a plurality of chips in a single package, the package tends to become large and the volume of air inside the caps 50 also tends to increase. When the ceramic caps 50 are attached to the respective sides of the ceramic wiring substrate 10 before being used to hermetically seal the contents by soldering, the molten solder may be drawn into or jutted out of the caps 50 due to the difference in pressure between the inside and the outside as the solder cools. One of the measures to be taken to prevent the molten solder from being thus drawn into or jutted out of the caps 50, even though the package is large, is to bore ventilating holes 51 into them and to cover the holes 51 with lids 52 or the like after the contents have been hermetically sealed with the inactive gas encapsulated.

According to the present invention, a plurality of semiconductor elements can be accommodated in a single package and the number of signal lines to be led out of the package can be reduced so that the package size is decreased. A small lightweight apparatus is thus made available.

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Claims:

1. A method of data transmission of a data processing apparatus which comprises a microprocessor having data width of m bits (wherein m is an integer), a plurality of memory
5 chips connected to said microprocessor, said plurality of memory chips being divided into two groups, and each of said groups of memory chips is mounted on different substrate surfaces, said method comprising the steps of:

said microprocessor outputting an address signal to
10 said plurality of memory chips;

one of said groups of memory chips mounted on one of said substrate surfaces outputting data upper n bits to said microprocessor in parallel based on said address signal; and

the other of said groups of memory chips mounted on
15 another of said substrate surfaces outputting data of lower (m-n) bits to said microprocessor in parallel based on said address signal.

2. A method of data transmission of a data processing apparatus according to claim 1, wherein said memory chips
20 include random access memory chips.

3. A method of data transmission of a data processing apparatus according to claim 1, wherein said memory chips of said one group are assigned to upper bits of said m bits, and said memory chips of said other group are assigned to
25 lower bits of said m bits.

4. A method of data transmission of a data processing apparatus which comprises a microprocessor having data width of m bits (wherein m is an integer), a plurality of memory chips connected to said microprocessor, each of said memory
30 chips having data width of n bits (wherein n is an integer,

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and m is an integer times n), and said plurality of memory chips is divided into two groups, wherein each of said groups of memory chips is mounted on a different substrate surface than the other of said groups of memory chips, said
5 method comprising the steps of:

said microprocessor outputting an address signal for demanding m bit data to each memory chip; and

each of said memory chips outputting a combined total of m bit data to said microprocessor simultaneously based on
10 said address signal.

5. A method of data transmission of a data processing apparatus according to claim 4, wherein said memory chips include random access memory chips.

6. A method of data transmission of a data processing
15 apparatus according to claim 4, wherein said memory chips of said one group are assigned to upper bits of said m bits, and said memory chips of said other group are assigned to lower bits of said m bits.

7. A data processing apparatus, comprising:
20 a microprocessor which processes data and outputs m bits of data (wherein m is an integer) simultaneously;
a semiconductor chip module including:
a substrate, and
a plurality of memory chips having data width of n
25 bits data (wherein n is an integer, and m is integer times of n) formed on each side of said substrate; and
data lines connected to said microprocessor and said plurality of memory chips for slicing m bit data into n bit data and providing said sliced n bit data to each of said
30 memory chips.

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8. A data processing apparatus according to claim 7, wherein said memory chips include random access memory chips.

9. A data processing apparatus according to claim 7,
5 wherein said memory chips mounted on one side of said substrate are assigned to upper bits of said m bits, and said memory chips mounted on another surface of said substrate are assigned to lower bit of said m bits.

10. A data processing apparatus according to claim 7,
10 wherein said m bit data is stored in said memory chips based on a same address signal.

11. A data processing apparatus according to claim 7, wherein said memory chips are output to said data lines based on a same address signal.

15 12. A method of data transmission for a data processing apparatus which comprises a microprocessor for processing data, a semiconductor chip module including a substrate and a plurality of memory chips having data width of n bit data (wherein n is an integer, and m is an integer
20 times n) formed on each side of said substrate, data lines connected to said microprocessor and said plurality of memory chips for slicing m bit data into n bit data and providing said sliced n bit data to each memory chip, said method comprising the steps of:

25 said microprocessor outputting an address signal and m bit data (wherein m is an integer) simultaneously; and
each of said memory chip storing n bit data in parallel based on said address signal.

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13. A method of data transmission of a data processing apparatus according to claim 12, wherein said memory chips include random access memory chips.

14. A method of data transmission of a data processing apparatus according to claim 12, wherein said memory chips mounted on one side of said substrate are assigned to upper bit of said m bits, and said memory chips mounted on another surface of said substrate are assigned to lower bits of said m bits.

15. A data processing apparatus, comprising:
a processor having a data width of m bits;
a plurality of memory modules connected to data lines, each of said memory modules comprising:
a first group of memory chips mounted on one side of said substrate, and
a second group of memory chips mounted on another side of said substrate,
wherein said first group of memory chips outputting data of upper n bits, and said second group of memory chips outputting data of lower (m-n) bits; and
a selection circuit which outputs a selection signal for selecting a memory module from among said plurality of memory modules based on a signal output by said processor, wherein the memory module selected by said selection circuit outputs data of m bits to said processor in parallel based on an address of said processor.

16. A data processing apparatus according to claim 15, wherein said memory chips include a random access memory.

17. A data processing apparatus according to claim 15, wherein said selection circuit inputs the address signal

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from said processor and outputs said selection signal based on said input address signal.

18. A data processing apparatus, comprising:

5 a processor having data width of m bits (m is an integer);

a memory module comprising:

a first group of memory chips mounted on one side of a substrate, and

10 a second group of memory chips mounted on another side of said substrate,

wherein said first group of memory chips output data of n bits, and said second group of memory chips output data of (m-n) bits; and

15 a selection circuit which selects a memory chip from among said plurality of memory chips based on a signal output from said processor;

wherein said processor write data to memory chip selected by said selected circuit.

20 **19.** A data processing apparatus according to claim 18, wherein said plurality of memory chips write and read data in byte units.

20. A data processing apparatus according to claim 18, wherein said memory module includes said selection circuit.

21. A data processing apparatus, comprising:

25 a processor having data width of m bits (m is an integer);

a memory module comprising:

first data lines for transmitting data of n bits (n is an integer),

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second data lines for transmitting data of (m-n) bits,

a first group of memory chips connected to said first data lines and mounted on one side of a substrate,

5 a second group of memory chips connected to said first data lines and mounted on one side of said substrate,

a third group of memory chips connected to said second data lines and mounted on another side of said substrate, and

10 a fourth group of memory chips connected to said second data lines and mounted on another side of said substrate; and

wherein said memory module outputs data of m bits to said processor in parallel based on address of said processor.

22. A data processing apparatus, comprising:

a processor which outputs address and data of m bits;

a memory module comprising:

20 first data lines for transmitting data of n bits,
second data lines for transmitting data of (m-n) bits,

a first group of memory chips mounted on one side of a substrate and connected to said first data lines,

25 a second group of memory chips mounted on one side of said substrate and connected to said first data lines,

a third group of memory chips mounted on another side of said substrate and connected to said second data lines, and

30 a fourth group of memory chips mounted on another side of said substrate and connected to said second data lines;

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a selection circuit which selects two groups of memory chips based on address output from said processor, and

wherein said memory module outputs data of m bits to said processor in parallel based on address of said

5 processor.

23. A data processing apparatus according to claim 22, wherein said memory module includes said selection circuit.

FIG 1

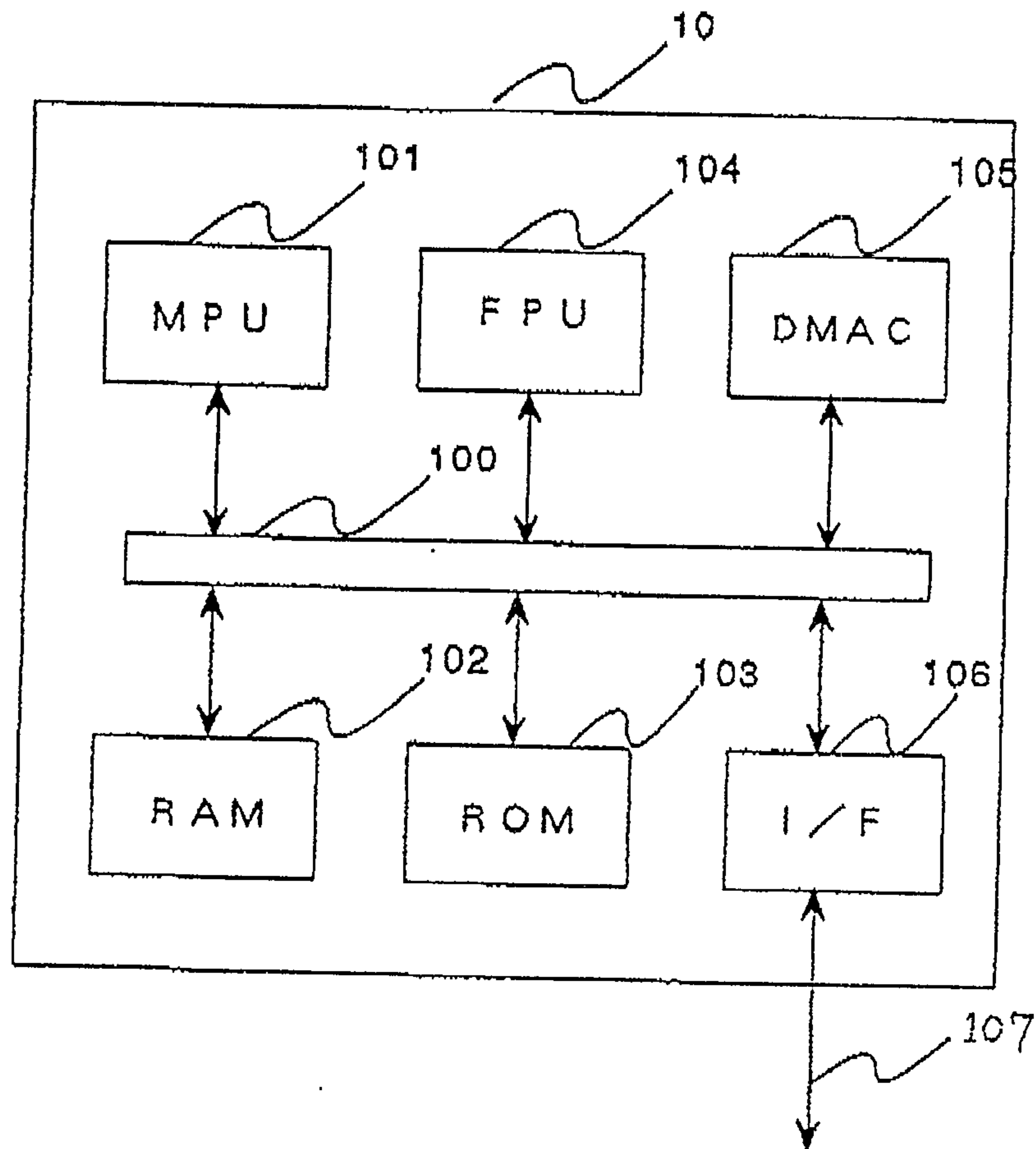


FIG 11

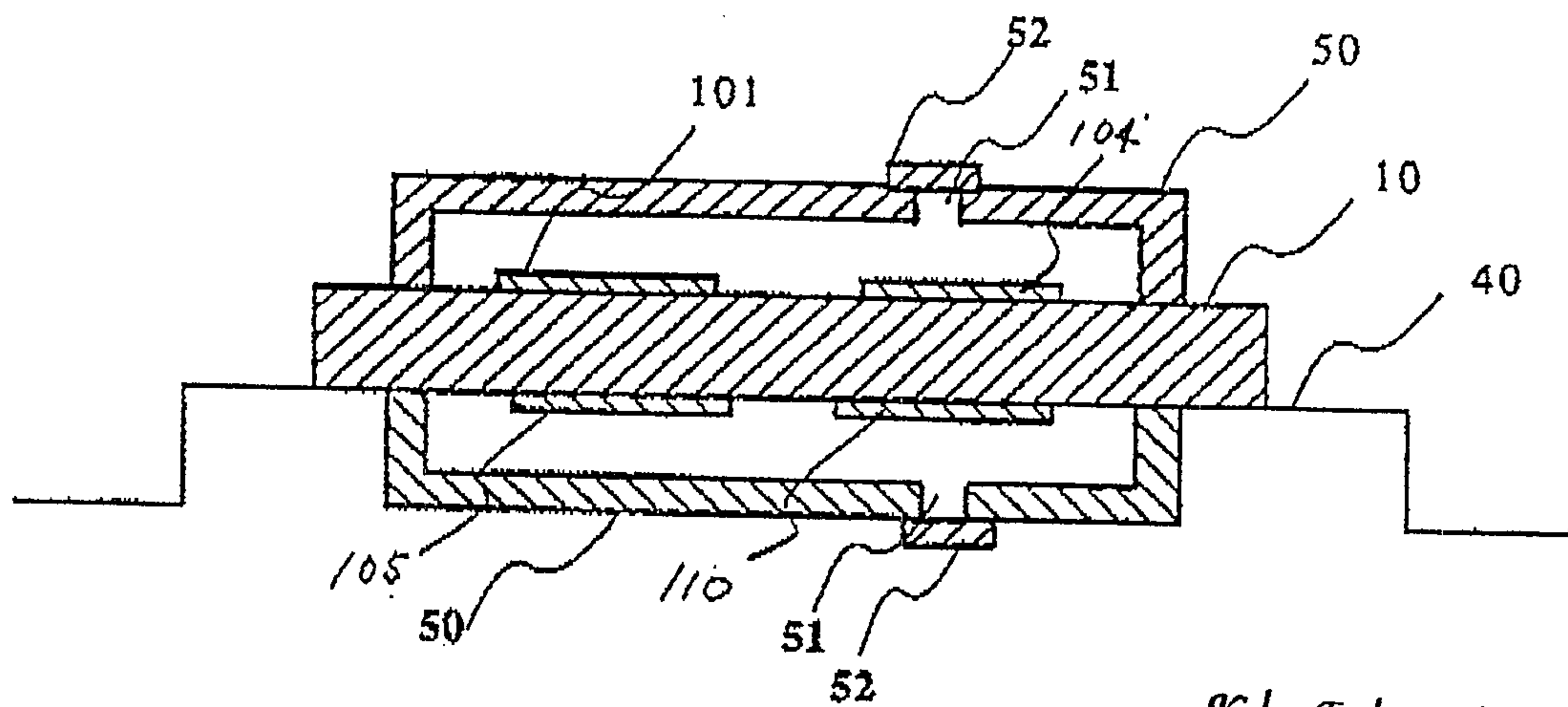
*Kirby, Eades, Gale, Baker*

FIG 2

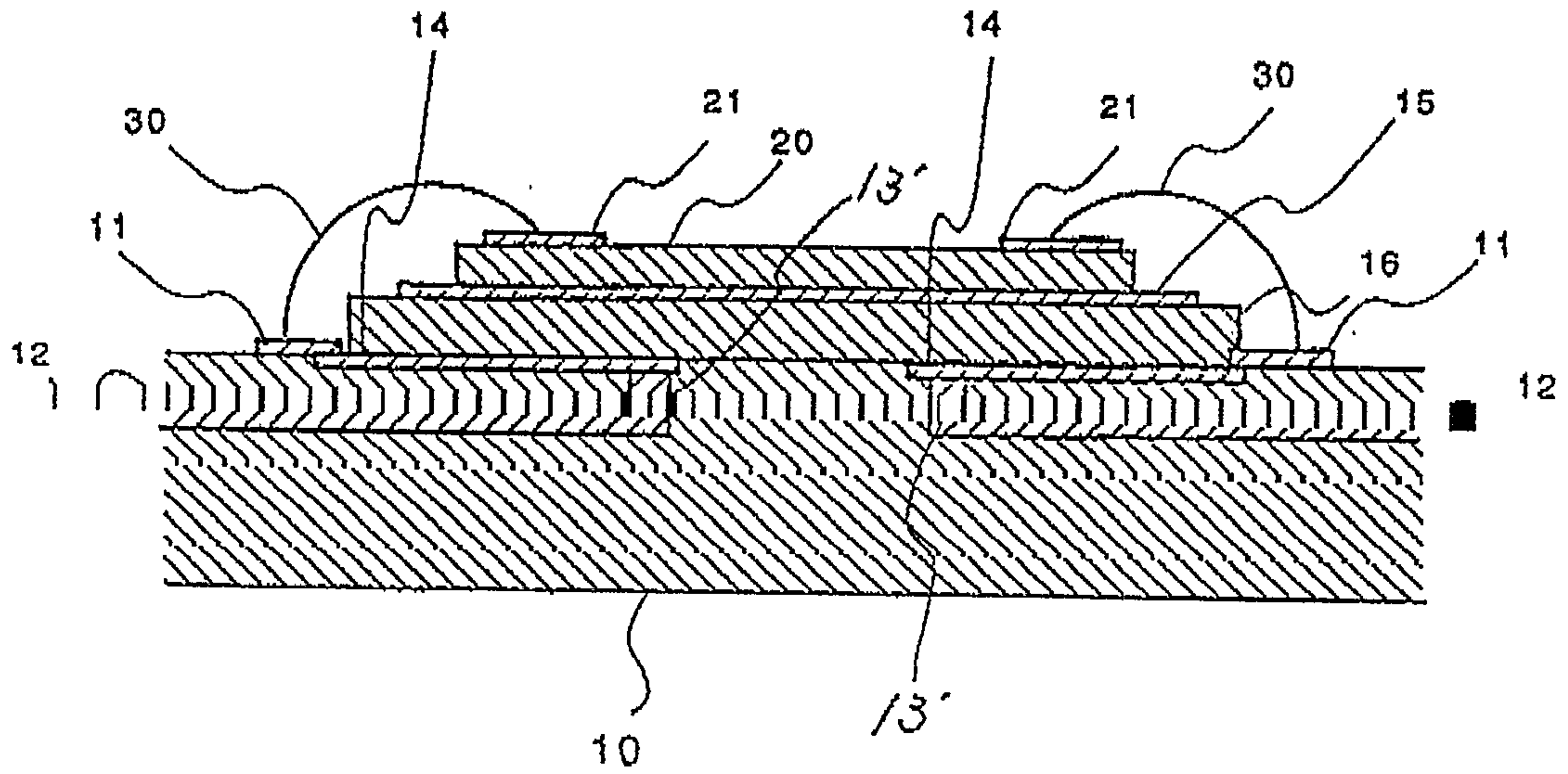


FIG 3

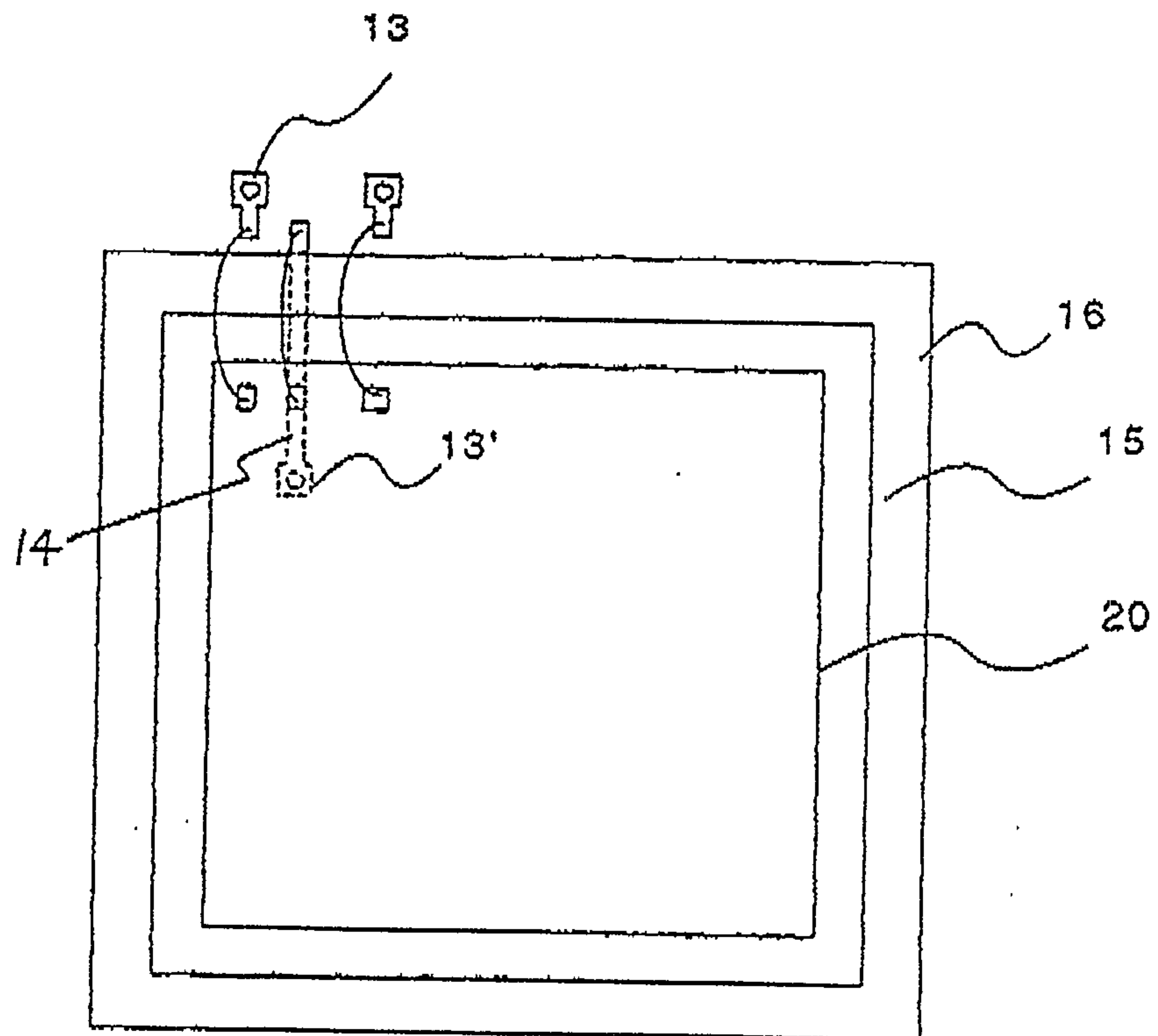


FIG 4

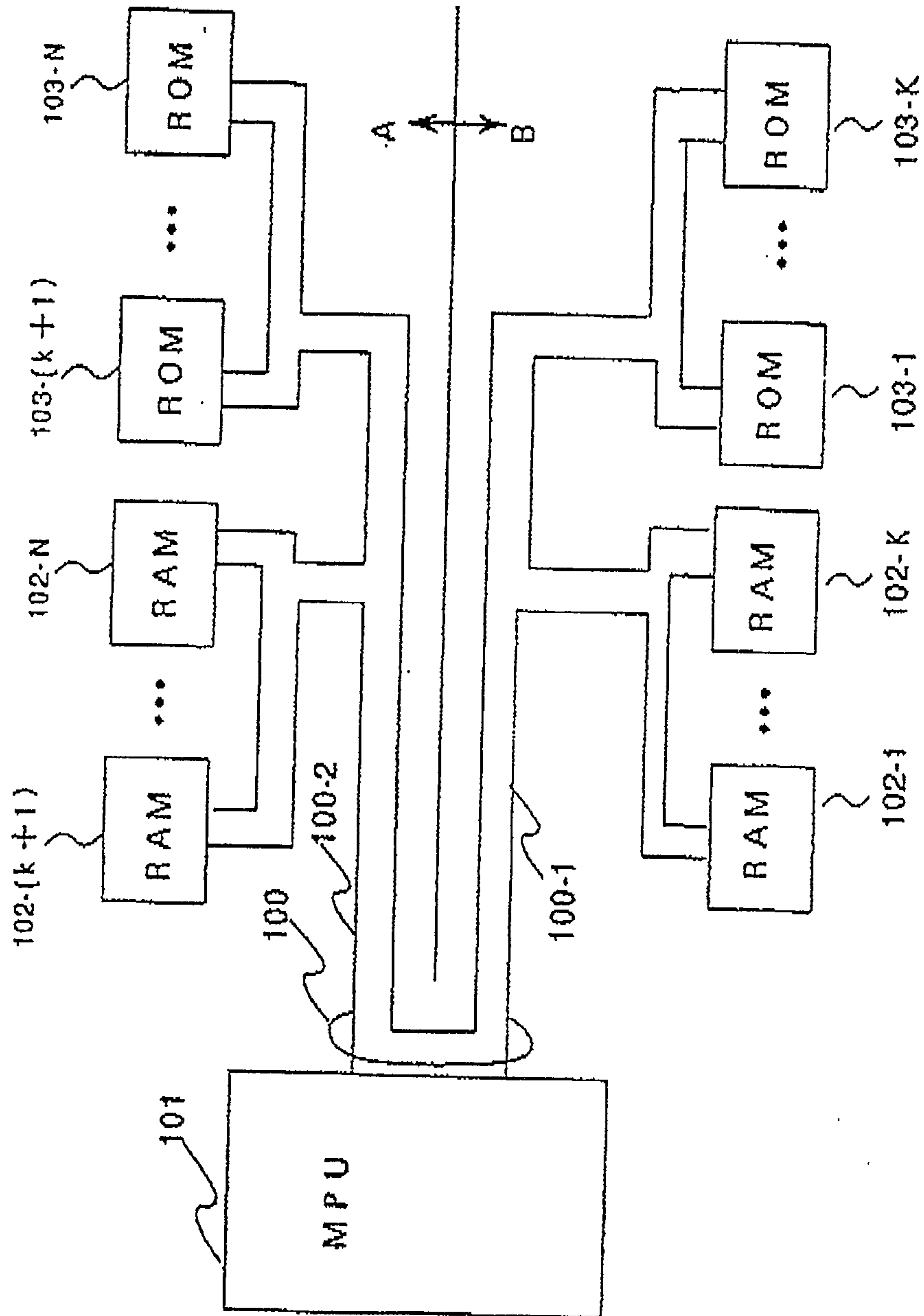


FIG 5

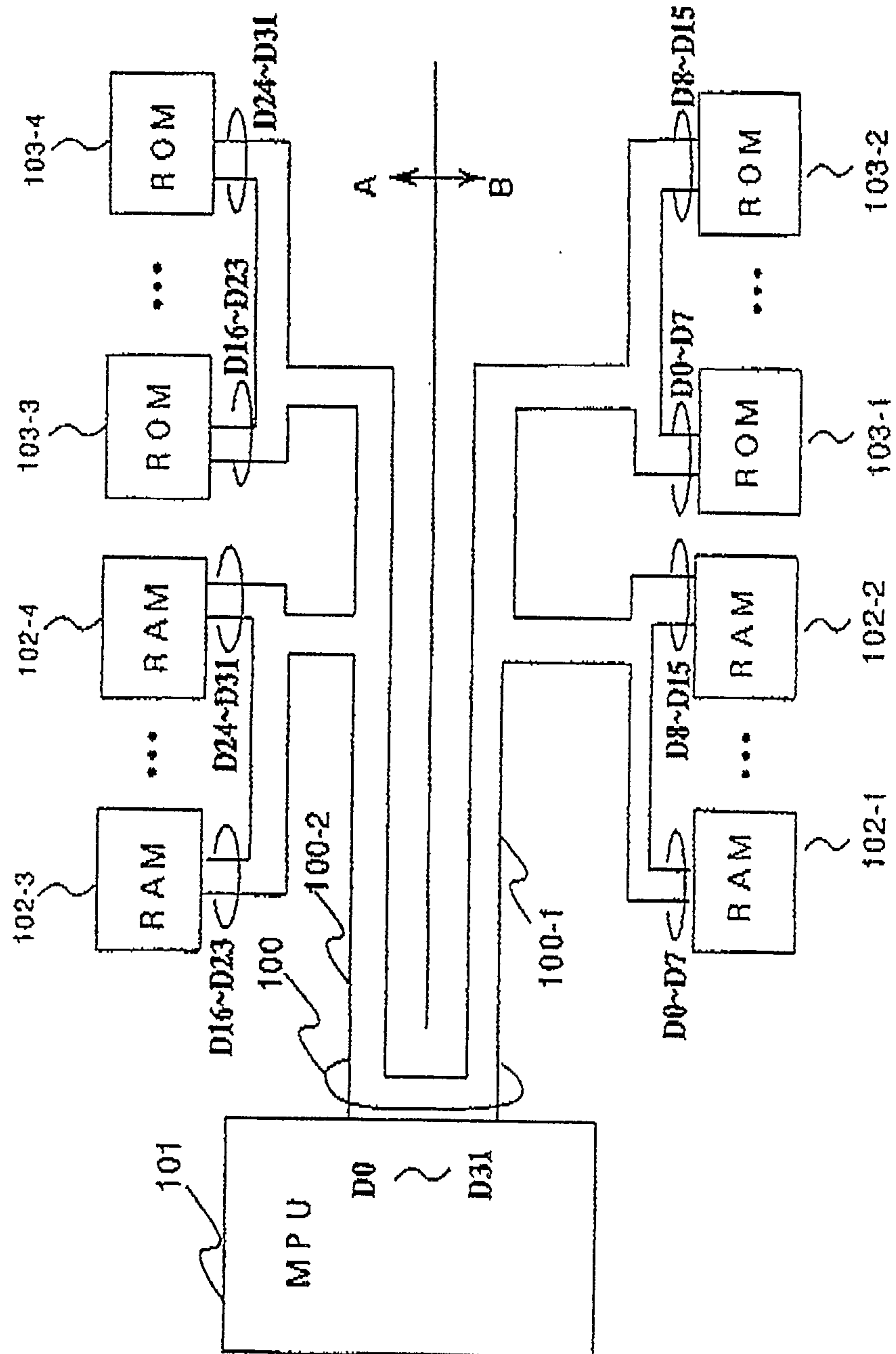


FIG 6

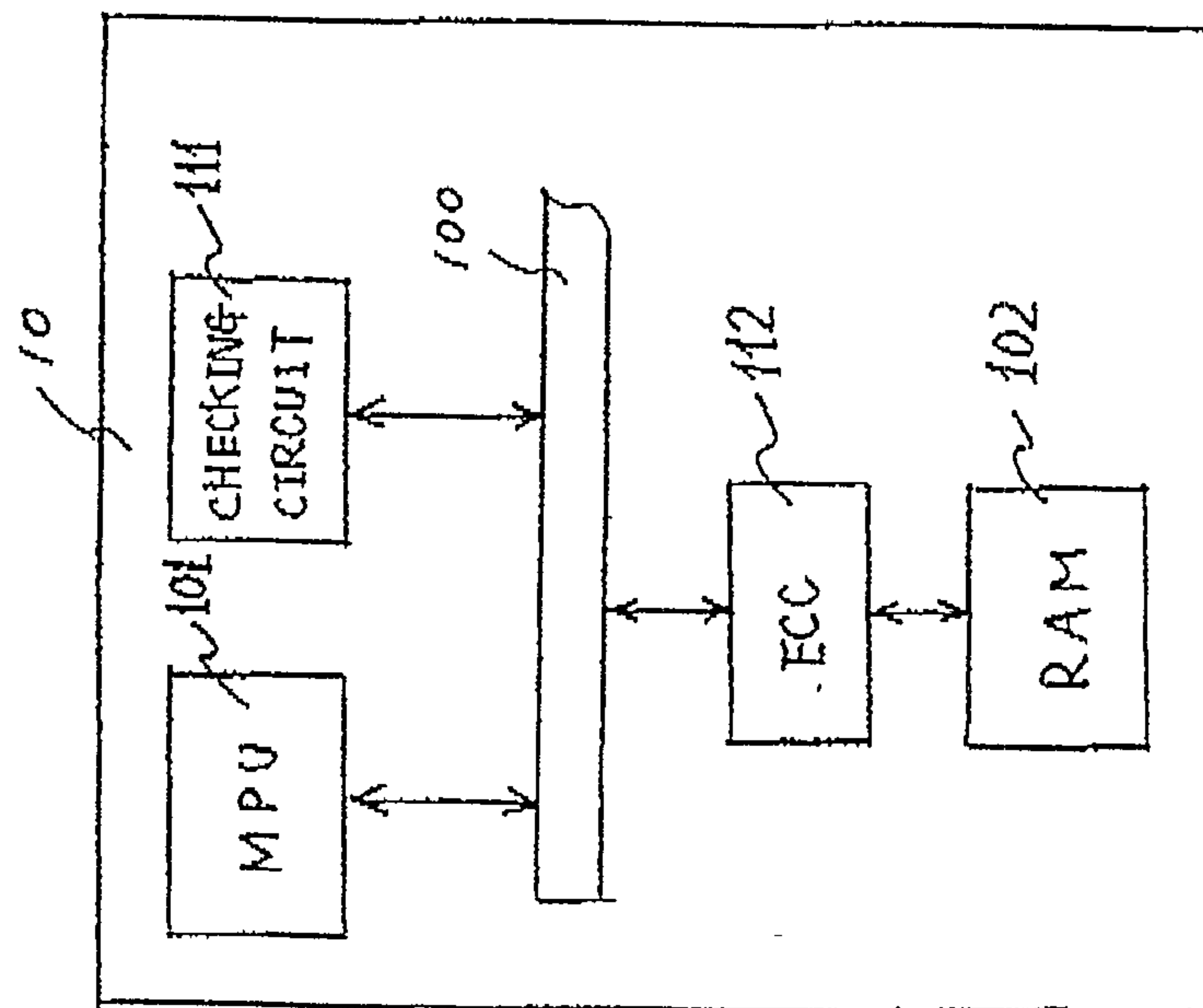


FIG 7

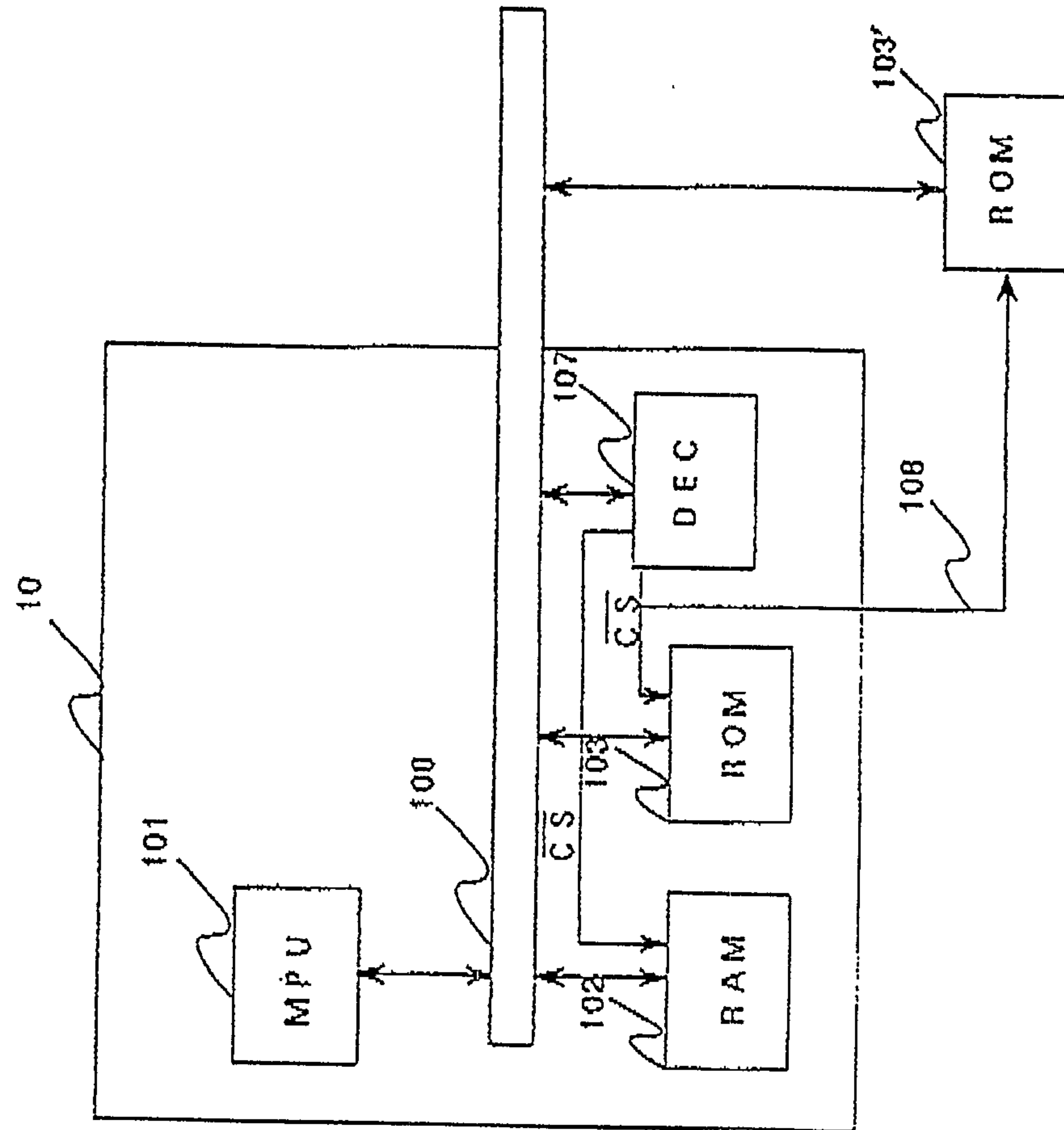


FIG 8

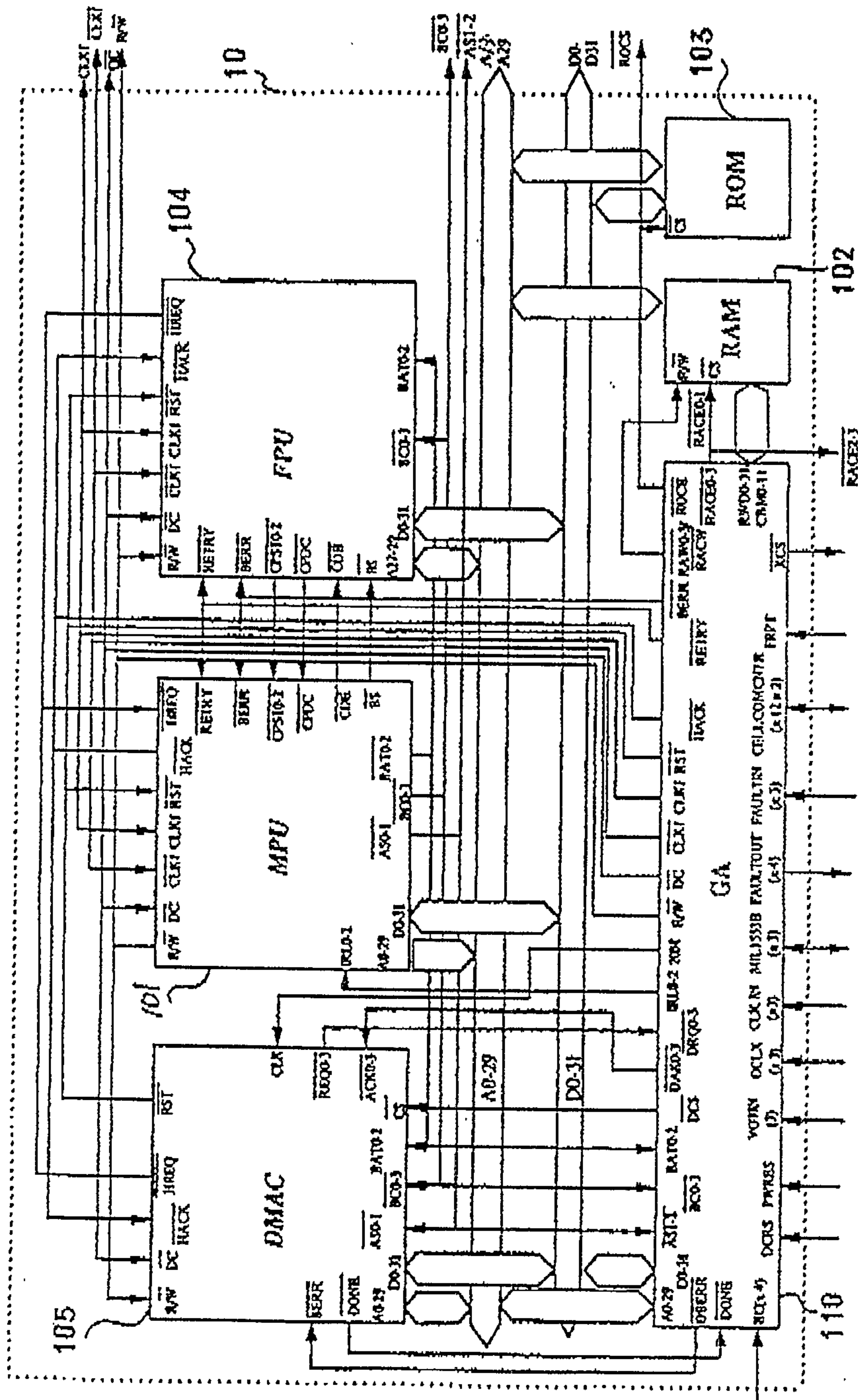


FIG 10

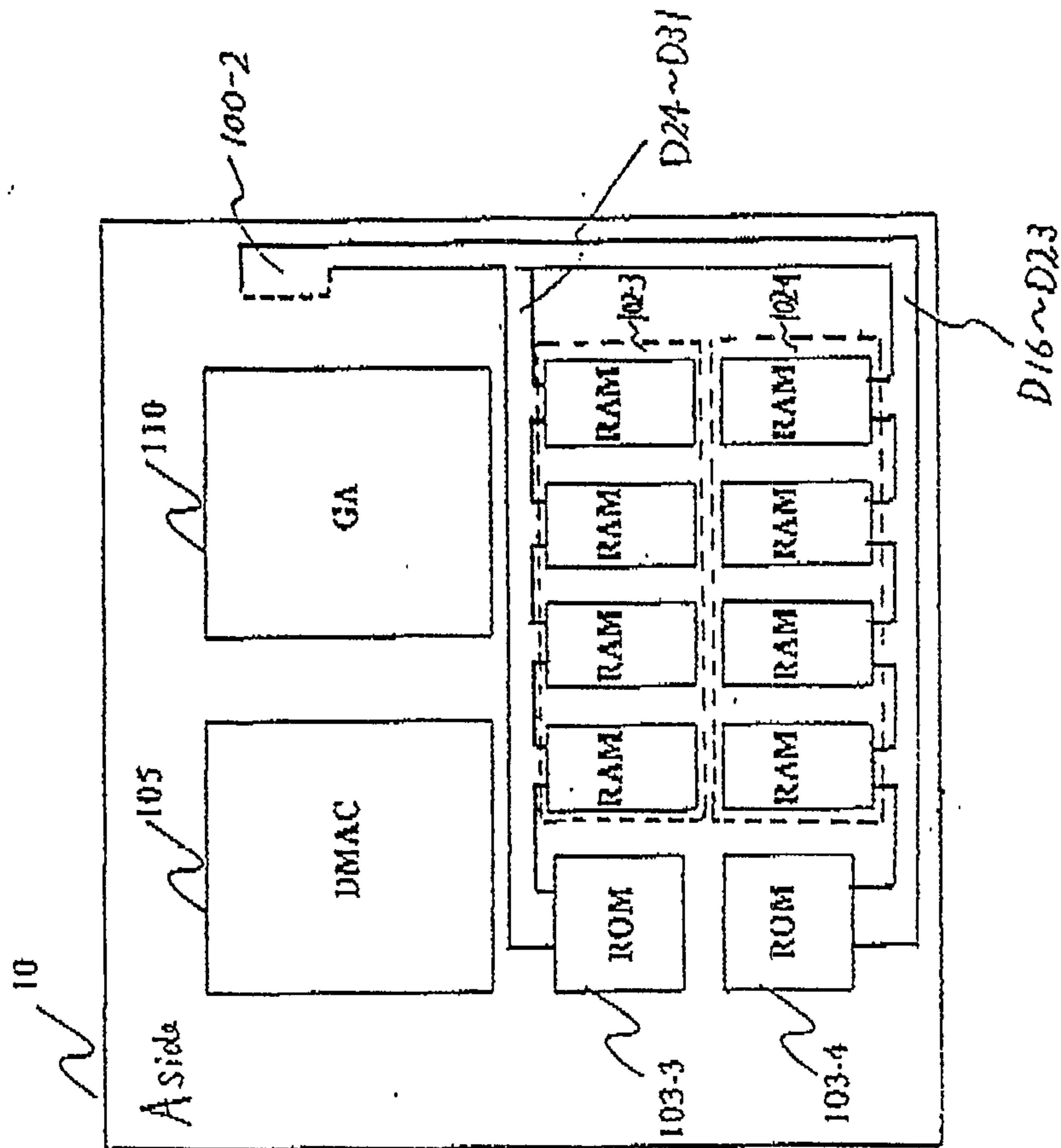
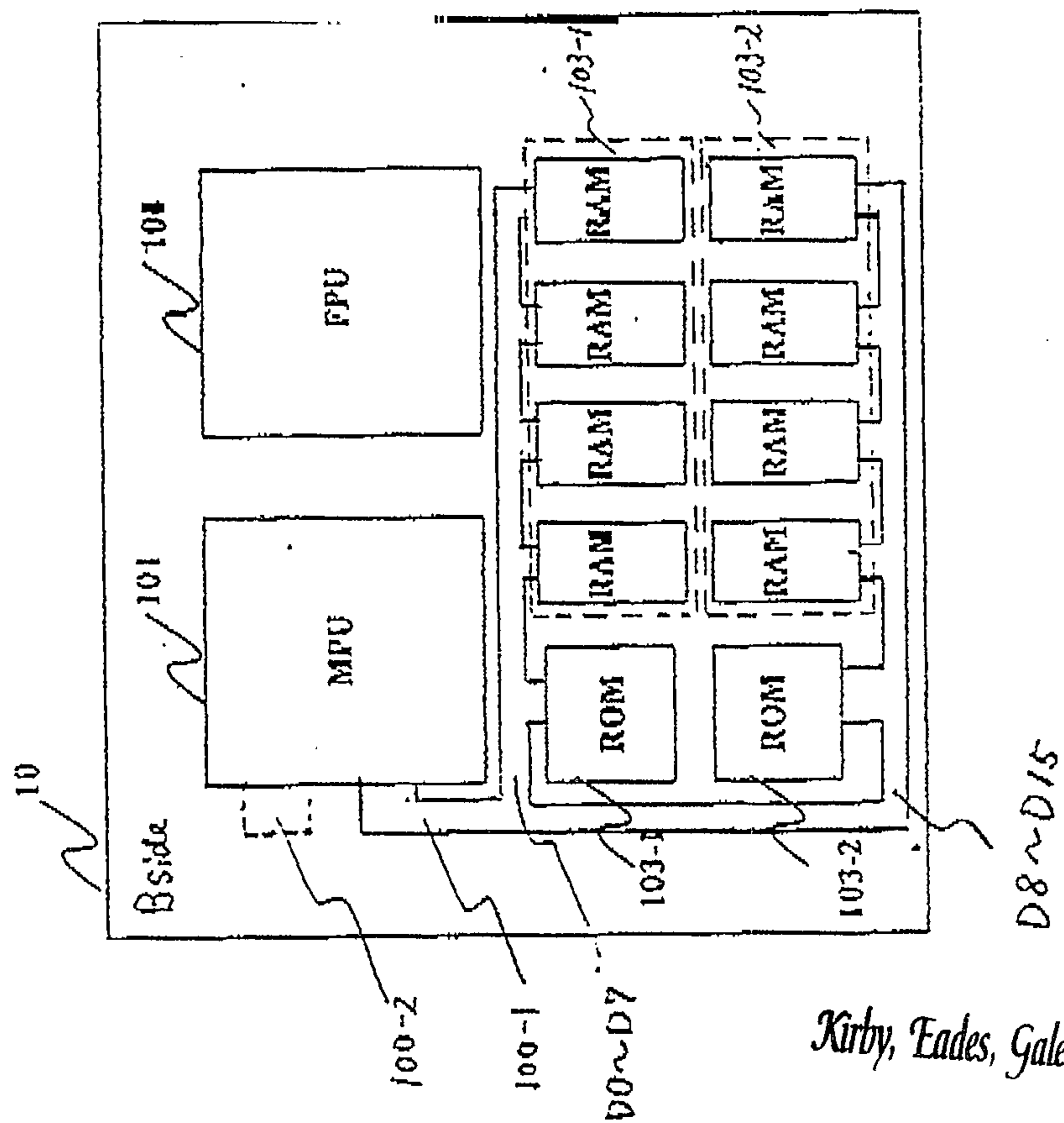


FIG 9



Kirby, Eades, Gale, Baker