(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 933 893 A1

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
21.10.2015 Bulletin 2015/43

(21) Application number: **13862658.5**

(22) Date of filing: **25.11.2013**

(51) Int Cl.:
H02J 3/01 (2006.01) ***H02M 1/12*** (2006.01)
H02M 7/12 (2006.01)

(86) International application number:
PCT/JP2013/081662

(87) International publication number:
WO 2014/091915 (19.06.2014 Gazette 2014/25)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **14.12.2012 JP 2012273744**

(71) Applicant: **Daikin Industries, Ltd.**
Osaka-shi, Osaka 530-8323 (JP)

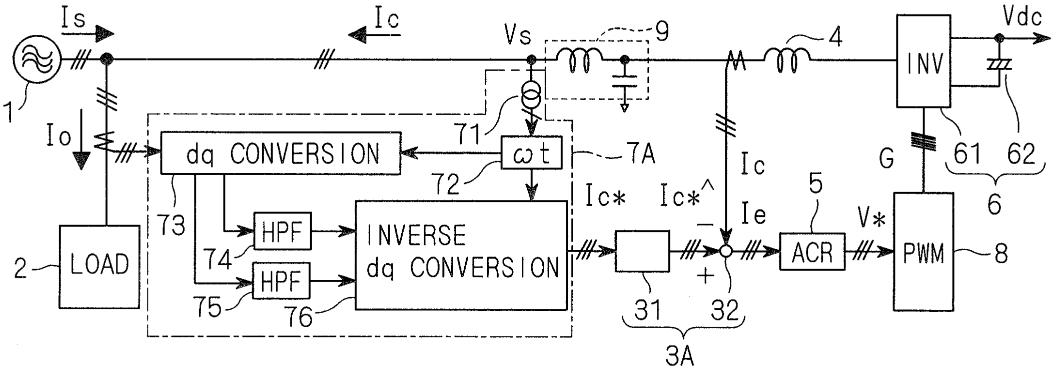
(72) Inventor: **KAWASHIMA, Reiji**
Osaka-shi
Osaka 530-8323 (JP)

(74) Representative: **Hoffmann Eitle**
Patent- und Rechtsanwälte PartmbB
Arabellastraße 30
81925 München (DE)

(54) ACTIVE FILTER CONTROL DEVICE

(57) Provided is technology for improving, in an active filter, impediment to suppression of a harmonic component of power current caused by arithmetic processing performed by a current controller. The current controller (5) performs processing of generating a three-phase voltage command value V* based on output of a difference current generation unit (3A). The current controller (5) achieves the above-mentioned processing, for example, by performing PI (proportional integral) control, so that a delay time ta occurs. If a deviation Ie is obtained from a command value Ic* and compensating current Ic, the time ta causes a difference between the compensating current Ic and the harmonic component, and becomes an impediment to suppression of the harmonic component of the power current Is. However, by the difference current generating unit (3A) obtaining the deviation Ie from the compensating current Ic and a value Ic*^ obtained by leading a phase of the command value Ic* by a phase corresponding to the time ta, the above-mentioned impediment is eliminated or reduced.

F I G. 1



EP 2 933 893 A1

Description

Technical Field

[0001] The present invention relates to technology for controlling an active filter and, in particular, to technology for controlling a parallel active filter.

Background Art

[0002] When load current flows from an AC power supply to a load, a so-called harmonic component is typically generated in the load current. The harmonic component is a well-known problem as it causes so-called harmonic interference, and is thus to be reduced.

[0003] An active filter is proposed as one approach to solving the problem. Particularly a parallel active filter is connected to the AC power supply through an interconnection reactor and passing compensating current to reduce a harmonic component of power current flowing through the AC power supply.

[0004] Specifically, in order to reduce the harmonic component of the power current, processing of passing compensating current of an opposite phase to this through the parallel active filter (or supplying compensating current of the same phase as this from the parallel active filter) is performed.

[0005] The harmonic component of the load current is adopted as a command value of the compensating current, and, based on a deviation of the compensating current therefrom, a current controller operates to control operation of the parallel active filter.

[0006] The parallel active filter is introduced, for example, in Non-patent Document 1 and FIG. 10 of Patent Document 1.

[0007] Further, Patent Documents 2 and 3 are listed as prior art documents disclosing technology related to the present application. Patent Document 2 discloses technology for suppressing overcurrent in the event of accidents, and Patent Document 3 discloses technology for suppressing a time delay of operation of performing rotating coordinate conversion and a delay occurring when current is detected.

Prior Art Documents

Patent Documents

[0008]

Patent Document 1: Japanese Patent No. 3755220
Patent Document 2: Japanese Patent Application Laid-open No. 5-252751
Patent Document 3: Japanese Patent Application Laid-open No. 2008-234298

Non-patent Document

[0009] Non-patent Document 1: Katsuhiro Izumi and four others, "Influence of the Compensation Current Detection Characteristic on the Active Filter Performance", Reports of the Faculty of Engineering, Nagasaki University, Vol. 30, No. 55, pp. 165-169, July 2000

Summary of Invention

Problems to be Solved by the Invention

[0010] The parallel active filter is controlled by the operation of the current controller based on the deviation of current as described above. The current controller, however, is typically configured as a proportional integral controller, and, due to arithmetic processing performed thereby, the compensating current tends to be delayed from the command value thereof. The divergence between the command value and the compensating current is likely to be more noticeable especially when the command value varies more significantly.

[0011] Such a delay caused by the arithmetic processing becomes an impediment to suppression of the harmonic component of the power current. However, Patent Documents 1 and 2 as well as Non-patent Document 1 are silent about such an impediment.

[0012] The present invention has been conceived in view of the above-mentioned standpoint, and aims to provide technology for improving, in the active filter, the impediment to suppression of the harmonic component of the power current caused by the arithmetic processing performed by the current controller.

Means for Solving the Problems

[0013] An active filter control device according to the present invention is a device that controls a parallel active filter (6) connected, through an interconnection reactor (4), to an AC power supply (1) that supplies load current (Io) to a load (2), and outputting compensating current (Ic; Id, Iq).

[0014] The first aspect thereof includes a harmonic component extraction unit (7A; 7B) obtaining a command value (Ic*; Id*, Iq*) of the compensating current from a harmonic component of the load current; a difference current generation unit (3A; 3B) obtaining a deviation (Ie) between the compensating current and a value (Ic*^; Id*^, Iq*^) obtained by leading a phase of the command value by a predetermined phase difference (360° ×ta/Tr); a current controller (5; 10dd, 10qq) generating a control signal (V*; Vid, Viq) based on output of the difference current generation unit; and a driving signal generation circuit (8) generating, based on the control signal, a driving signal (G) driving the parallel active filter.

[0015] The second aspect of the active filter control device according to the present invention is the first aspect, wherein the difference current generation unit (3A;

3B) includes: a delay unit (31) performing processing of delaying the command value (Ic*; Id*, Iq*) by a phase obtained by subtracting the predetermined phase difference (360°×ta/Tr) from a phase for one cycle of the AC power supply (1); and a subtracter (32) obtaining a difference between output (Ic*^; Id*^, Iq*^) of the delay unit and the compensating current (Ic; Id, Iq).

[0016] The third aspect of the active filter control device according to the present invention is any one of the first aspect to the second aspect, wherein the command value (Ic*) is obtained by removing a DC component from the load current (Io) grasped in a rotating coordinate system synchronizing with a phase of the AC power supply (1), and further performing coordinate conversion so as to be grasped in a fixed coordinate system, the compensating current (Ic) is grasped in the fixed coordinate system, and the deviation (Ie) is obtained in the fixed coordinate system.

[0017] The fourth aspect of the active filter control device according to the present invention is any one of the first aspect to the second aspect, wherein the command value (Id*, Iq*) is obtained by removing a DC component from the load current (Io) grasped in a rotating coordinate system synchronizing with a phase of the AC power supply (1), the compensating current (Id, Iq) is grasped in the rotating coordinate system, and the deviation (Ied, Ieq) is obtained in the rotating coordinate system.

[0018] The fifth aspect of the active filter control device according to the present invention is the second aspect, wherein the load (2) is an air conditioner including: an inverter (23); and a compressor (24) controlled by the inverter to compress a refrigerant.

Effects of the Invention

[0019] According to the first aspect of the active filter control device according to the present invention, the phase of the command value of the compensating current is led by the predetermined phase difference to eliminate a delay time in the current controller. The phase difference can be set appropriately in accordance with the delay time.

[0020] According to the second aspect of the active filter control device according to the present invention, the phase of the command value can substantially be led by the delay unit as the command value varies with approximately the same waveform for each cycle of the AC power supply.

[0021] According to the third aspect of the active filter control device according to the present invention, a component, of the load current grasped in the rotating coordinate system, synchronizing with the phase of the AC power supply appears as a DC component. Therefore, by removing the DC component from the load current grasped in the rotating coordinate system, the harmonic component of the load current is obtained as the command value of the compensating current.

[0022] According to the fourth aspect of the active filter control device according to the present invention, the rotating coordinate system can be grasped as a two-phase coordinate system even when the AC power supply is a multi-phase power supply having three or more phases, and thus the configuration of the delay unit can easily be simplified. The cycles of the command value and the compensating current in the rotating coordinate system are shorter than those in the fixed coordinate system, and thus the configuration of the delay unit can easily be simplified when the delay unit is adopted.

[0023] According to the fifth aspect of the active filter control device according to the present invention, the variation of the load is small, and thus the delay unit substantially leads the phase of the command value with high accuracy.

[0024] Objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0025]

[FIG. 1] A block diagram showing the aspect in which the active filter control device is adopted in a first embodiment.

[FIG. 2] A graph showing the effects of the first embodiment.

[FIG. 3] A graph showing the effects of the first embodiment.

[FIG. 4] A graph showing the effects of the first embodiment.

[FIG. 5] A graph showing technology to be compared with the first embodiment.

[FIG. 6] A graph showing the effects of the first embodiment.

[FIG. 7] A block diagram showing the aspect in which the active filter control device is adopted in a second embodiment.

[FIG. 8] A graph showing the effects of the second embodiment.

[FIG. 9] A block diagram showing the technology to be compared with the first embodiment.

[FIG. 10] A graph showing the technology to be compared with the first embodiment.

Description of Embodiments

First Embodiment

[0026] FIG. 1 is a block diagram showing the aspect in which the active filter control device is adopted in the present embodiment. Description is made below by taking a case of adopting three-phase alternating current as an example. However, this number of phases is an example, and there is no need to limit the number of phases to three.

[0027] A three-phase AC power supply 1 supplies three-phase load current Io to a load 2. A parallel active filter 6 is connected to the AC power supply 1 through a three-phase interconnection reactor 4. The parallel active filter 6 outputs three-phase compensating current Ic. Description is made herein on the assumption that a direction in which the compensating current Ic flows from the parallel active filter 6 to the AC power supply 1 is taken as being positive, and the sum of power current Is flowing from the AC power supply 1 and the compensating current Ic is equal to the load current Io.

[0028] Of course, if the direction of the compensating current Ic is taken as being opposite to the direction in the description of the present embodiment, only the polarity sign (positive/negative) of the compensating current Ic changes.

[0029] The parallel active filter 6 includes an inverter 61 and a capacitor 62, for example. The inverter 61 inputs and outputs the compensating current Ic to charge and discharge the capacitor 62 at a DC voltage Vdc. For example, the inverter 61 is a voltage source inverter, three current paths are connected in parallel to the capacitor 62, and two switching elements are provided for each of the current paths.

[0030] The active filter control device includes a harmonic component extraction unit 7A, a difference current generation unit 3A, a current controller 5, and a driving signal generation circuit 8.

[0031] The harmonic component extraction unit 7A obtains a command value Ic* of the compensating current Ic from the harmonic component of the load current Io. Specific configuration is known from Patent Document 3 and other(s), so that description thereof is made only briefly. The harmonic component extraction unit 7A includes a transformer 71, a phase detector 72, a dq converter 73, high-pass filters 74 and 75, and an inverse dq converter 76.

[0032] The transformer 71 detects one phase of a three-phase voltage Vs of the AC power supply 1, and provides it to the phase detector 72. The phase detector 72 transfers the detected phase to the dq converter 73 and the inverse dq converter 76.

[0033] The dq converter 73 performs three-phase/two-phase conversion on the load current Io as detected to obtain d-axis current and q-axis current. The d-axis current and the q-axis current are provided to the inverse dq converter 76, after being removed low-frequency components, particularly DC components, by the high-pass filters 74 and 75. The inverse dq converter 76 performs two-phase/three-phase conversion to generate the command value Ic* of the compensating current Ic. The d axis and the q axis are herein axes in the rotating coordinate system rotating in synchronization with the phase detected by the phase detector 72.

[0034] Components, of the load current Io, synchronizing with the phase of the AC power supply 1 appear as DC components in the d-axis current and the q-axis current. That is to say, the d-axis current and the q-axis current include only DC components in the absence of the harmonic component in the load current Io. The above-mentioned high-pass filters 74 and 75 thus output only the harmonic components of the load current Io, which appear as the d-axis current and the q-axis current. As a result, the command value Ic* represents the harmonic component of the load current Io. Therefore, when the compensating current Ic matches the command value Ic* with no phase shift, the compensating current Ic absorbs the harmonic component of the load current Io, and the harmonic component is not generated in the power current Is.

[0035] The difference current generation unit 3A obtains a deviation Ie between the compensating current Ic and a value Ic*^ obtained by leading a phase of the command value Ic* by a predetermined phase difference, which is described later. The command value Ic* is obtained by removing the DC component from the load current Io grasped in the rotating coordinate system (dq coordinate system) synchronizing with the phase of the AC power supply 1, and further performing coordinate conversion so as to be grasped in the fixed coordinate system. The compensating current Ic and the deviation Ie are also obtained in the fixed coordinate system.

[0036] The current controller 5 performs processing of generating a three-phase voltage command value V* based on the output of the difference current generation unit 3A. The current controller 5 achieves the above-mentioned processing, for example, by performing PI (proportional integral) control.

[0037] The driving signal generation circuit 8 generates, based on the voltage command value V*, a driving signal G driving the parallel active filter 6. The driving signal generation circuit 8 generates the driving signal G, for example, by performing logical operation on results of comparison between the voltage command value V* and a carrier. Therefore, it can be said that the voltage command value V* is a control signal indirectly controlling the parallel active filter 6 through the driving signal G.

[0038] It is desirable to provide a low-pass filter 9 in terms of removing ripples of the compensating current Ic. Only the low-pass filter 9 for one phase is shown herein, but is actually provided for each of three phases.

[0039] Since the current controller 5 generates the voltage command value V* by performing the PI control as described above, a delay time (hereinafter, this delay time is expressed as a time ta) occurs. If the deviation Ie is obtained from the command value Ic* and the compensating current Ic, the time ta causes a difference between the compensating current Ic and the harmonic component, and becomes an impediment to suppression of the harmonic component of the power current Is.

[0040] In the present embodiment, however, the difference current generation unit 3A obtains the deviation Ie from the compensating current Ic and the value Ic*^ obtained by leading the phase of the command value Ic* by a phase corresponding to the time ta to eliminate or reduce the above-mentioned impediment.

[0041] The phase amount φ for the phase leading can be expressed as $\varphi = 360° \times ta/Tr$ by introducing a cycle Tr of the voltage Vs output from the AC power supply 1. The time ta is considered to take a constant value in a steady state. Therefore, the time ta can be estimated in advance through measurement or presumption, and the phase amount φ can also be set in advance appropriately.

[0042] The difference current generation unit 3A includes, for example, a delay unit 31 and a subtracter 32. The delay unit 31 performs processing of providing a delay by a phase obtained by subtracting the phase amount φ from 360 degrees (i.e., a phase for one cycle unit of the voltage Vs). Since the harmonic component cyclically varies at the same cycle as the voltage Vs in the steady state, the delay becomes substantially equivalent to the phase leading by the phase amount φ. The subtracter 32 obtains the deviation Ie as a difference between the output Ic*^ of the delay unit 31 and the compensating current Ic.

[0043] FIGs. 2 to 4 and 6 are graphs showing the effects of the present embodiment. FIG. 5 is a graph showing the technology to be compared with the present embodiment. In FIGs. 2 to 6, various amounts are shown for only one phase. This is because, in a case of adopting a balanced load as the load 2, three phases of the load current Io are balanced, three phases of each of the power current Is and the compensating current Ic are balanced, and three phases of each of these amounts only differ from one another by 120 degrees.

[0044] FIG. 2 shows, downwards from an upper row, waveforms of the load current Io, a value (-Ic) obtained by reversing the polarity of the compensating current Ic, the power current Is, the phase-led command value Ic*^, the compensating current Ic, and the deviation Ie, respectively.

[0045] FIG. 3 shows waveforms of the voltage Vs and its phase θ in an upper row, a waveform of the command value Ic* in a middle row, and a waveform of the phase-led command value Ic*^ in a lower row, respectively. The time ta and the cycle Tr are also shown. It is visually recognized that the command value Ic*^ is led from the command value Ic* by the time ta.

[0046] FIG. 4 shows waveforms of the command value Ic* and the phase-led command value Ic*^ in an upper row and waveforms of the command value Ic* and the compensating current Ic in a lower row. The waveforms are shown in FIG. 4 in an extended time axis, compared to the waveforms shown in FIG. 3. It is visually recognized from the waveforms in the upper row of FIG. 4 that the phase-led command value Ic*^ is led from the command value Ic*, as visually recognized from the middle and lower rows of FIG. 3. It is visually recognized from the waveforms in the lower row of FIG. 4 that the command value Ic* and the compensating current Ic have approximately the same waveform.

[0047] FIG. 5 is a graph showing various amounts obtained when the delay amount in the delay unit 31 is set to 0 (i.e., the phase amount φ is also set to 0). Waveforms of the (not phase-led) command value Ic* and the compensating current Ic are shown in an upper row, a waveform of the deviation Ie is shown in a middle row, and a waveform of the power current Is is shown in a lower row.

[0048] FIG. 6 is a graph showing various amounts obtained when the delay unit 31 provides a delay substantially corresponding to the phase leading by the phase amount φ. Waveforms of the phase-led command value Ic*^ and the compensating current Ic are shown in an upper row, a waveform of the deviation Ie is shown in a middle row, and a waveform of the power current Is is shown in a lower row.

[0049] FIG. 9 shows configuration obtained by omitting the delay unit 31 from FIG. 1 and substantially corresponding to configuration shown in FIG. 1 when the phase amount φ is set to 0. FIG. 10 is a graph showing waveforms of various amounts obtained with the configuration so as to correspond to FIG. 2.

[0050] It is visually recognized from comparison between FIGs. 5 and 6 and comparison between FIGs. 2 and 10 that the deviation Ie is reduced, and the harmonic component of the power current Is is thereby significantly reduced by obtaining the compensating current Ic through control using not the command value Ic but the phase-led command value Ic*^.

[0051] That is to say, it is known that the impediment to suppression of the harmonic component of the power current Is caused by the arithmetic processing performed by the current controller 5 has been improved in the present embodiment.

Second Embodiment

[0052] The impediment to suppression of the harmonic component of the power current Is caused by the arithmetic processing performed by the current controller can also be improved when the command value of the compensating current is grasped in the rotating coordinate system by performing phase leading in a similar manner to the first embodiment.

[0053] FIG. 7 is a block diagram showing the aspect in which the active filter control device is adopted in the present embodiment. In contrast to the configuration shown in the block diagram of FIG. 1 in the first embodiment, the harmonic component extraction unit 7A has been replaced by a harmonic component extraction unit 7B, the difference current generation unit 3A has been replaced by a difference current generation unit 3B, and the current controller 5 has been replaced by a phase voltage command generation unit 10, and a dq converter 11 has been added in the configuration in the present embodiment. Furthermore, more detailed configuration of the load 2 is shown.

[0054] In the example of the present embodiment, the load 2 is an air conditioner including an inverter 23 and a compressor 24 controlled by the inverter 23 to compress a refrigerant (not shown). The load 2 further includes a converter 21 for supplying DC power to the inverter 23, and a capacitor 22 interposed in parallel between the converter 21 and the inverter 23.

[0055] Such a load 2 is desirable as the variation of the load is small, and thus the phase of the command value is substantially led with high accuracy.

[0056] The dq converter 11 performs dq conversion on the compensating current Ic, and outputs d-axis current Id and q-axis current Iq.

[0057] The harmonic component extraction unit 7B has such configuration that the inverse dq conversion unit 76 has been omitted from the harmonic component extraction unit 7A, and a subtracter 77, a voltage controller 78, and an adder 79 have been added. Functions of and mutual connection relationships among the transformer 71, the phase detector 72, the dq converter 73, and the high-pass filters 74 and 75 of the harmonic component extraction unit 7B are the same as those of the harmonic component extraction unit 7A.

[0058] The subtracter 77 obtains a deviation of the DC voltage Vdc supported by the capacitor 62 from the command value Vdc* thereof. The voltage controller 78 performs the PI control on the deviation obtained from the subtracter 77 to obtain a correction value of the d-axis current. The correction value is added to the output of the high-pass filter 74 (for the d-axis current) by the adder 79. As a result, a d-axis current command value Id* is obtained from the adder 79.

[0059] A q-axis current command value Iq* is obtained from the high-pass filter 75 for the q-axis current. It can be said that the d-axis current command value Id* and the q-axis current command value Iq* are the harmonic components of the load current Io considering pulsation of the DC voltage Vdc as grasped in the rotating coordinate system. These can thus be grasped as command values of the d-axis current Id and the q-axis current Iq that are the compensating current Ic grasped in the rotating coordinate system.

[0060] The difference current generation unit 3B includes delay units 31d and 31q, and subtracters 32d and 32q. Like the delay unit 31 shown in the first embodiment, each of the delay units 31 d and 31 q performs processing of providing a delay by a phase obtained by subtracting each of the phase amounts φd and φq from 360 degrees. These phase amounts φd and φq are described later. A phase-led d-axis current command value Id*^ and a phase-led q-axis current command value Iq*^ are respectively obtained from the d-axis current command value Id* and the q-axis current command value Iq* through the delay processing.

[0061] Like the subtracter 32 shown in the first embodiment, the subtracters 32d and 32q respectively output deviations Ied and Ieq. That is to say, the deviation Ied between the phase-led d-axis current command value Id*^ and the d-axis current Id as well as the deviation Ieq between the phase-led q-axis current command value Iq*^ and the q-axis current Iq are respectively obtained from the subtracters 32d and 32q.

[0062] The phase voltage command generation unit 10 includes current controllers 10dd and 10qq. The current controllers 10dd and 10qq respectively performs the PI control on the deviations Ied and Ieq to output voltage command values Vid and Viq. Assuming that delay times td and tq respectively occur through the PI control performed by the current controllers 10dd and 10qq, effects similar to those obtained in the first embodiment can be obtained by setting the above-mentioned phase amounts φd and φq as follows:

$$\varphi d = 360° \times td/Tr,\ \varphi q = 360° \times tq/Tr$$

[0063] Further, FIG. 7 shows the aspect in which configuration (hereinafter, referred to as "non-interference configuration") to avoid so-called interference between current control in the d-axis and current control in the q-axis is adopted, and the voltage command values Vid and Viq are corrected. The non-interference configuration is known technology as disclosed, for example, in Patent Document 2, so that description thereof is made only briefly.

[0064] Specifically, multipliers 10dq and 10qd, a subtracter 10d, and an adder 10q have been additionally provided. The multiplier 10dq multiplies the product ωL of an angular frequency ω (= 2π/Tr) of the AC voltage Vs and inductance L of the interconnection reactor by the d-axis current command value Id*, and provides it to the adder 10q. The multiplier 10qd multiplies the product ωL of the angular frequency ω and the inductance L by the q-axis current command value Iq*, and provides it to the subtracter 10d. The subtracter 10d corrects the voltage command value Vid obtained from the current controller 10dd by subtracting the output of the multiplier 10qd. The adder 10q corrects the voltage command value Viq obtained from the current controller 10qq by adding the output of the multiplier 10dq.

[0065] Note that the (not phase-led) d-axis current command value Id* and q-axis current command value Iq* are respectively provided to the multipliers 10dq and 10qd. This is based on such a standpoint that a delay as in the processing performed by the current controllers 10dd and 10qq does not occur in the processing performed by the multipliers 10dq and 10qd.

[0066] However, the influence of the non-interference configuration is small in the steady state, and the delay occurring in the delay units 31d and 31q does not substantially correspond to the phase leading. From this standpoint, the phase-led d-axis current command value Id*^ and the phase-led q-axis current command value Iq*^ may respectively be provided to the multipliers 10dq and 10qd.

[0067] Note that the multipliers 10dq and 10qd, the subtracter 10d, and the adder 10q can naturally be omitted when interference between the d-axis and the q-axis is not considered.

[0068] In the present embodiment, the driving signal generation circuit 8 generates, based on the voltage command values Vid and Viq for two phases, the driving signal G driving the parallel active filter 6, in contrast to the first embodiment. Therefore, it can also be said that the voltage command values Vid and Viq are control signals indirectly controlling the parallel active filter 6 through the driving signal G as with the voltage command value V* for three phases. Since the configuration of the driving signal generation circuit 8 having this function is well known, description thereof is omitted herein.

[0069] FIG. 8 is a graph showing the effects of the second embodiment, and shows, downwards from an upper row, respective waveforms of the d-axis current Id, the deviation Ied, the q-axis current Iq, the deviation Ieq, and the power current Is in the stated order.

[0070] The d-axis current Id cyclically varies at a cycle Tr/6, which is 1/6 of the cycle Tr of the power current Is, reflecting that the power current Is actually has three phases. The d-axis current Id is approximately sinusoidal. Similarly, the q-axis current Iq also cyclically varies at the cycle Tr/6.

[0071] It is known that the harmonic component is suppressed as the deviations Ied and Ieq are small, and the power current Is is approximately sinusoidal.

[0072] As described so far, it is known that the impediment to suppression of the harmonic component of the power current Is caused by the arithmetic processing performed by the current controllers 10dd and 10qq has been improved in the present embodiment as in the first embodiment.

[0073] As described above, in the present embodiment, the compensating current Ic is grasped as the d-axis current Id and the q-axis current Iq in the rotating coordinate system and the deviations Ied and Ieq are obtained in this rotating coordinate system. Since the rotating coordinate system can be grasped as a two-phase coordinate system even when the AC power supply 1 is a multi-phase power supply having three or more phases, the delay units 31 d and 31 q as well as the current controllers 10dd and 10qq for two phases are sufficient. In the first embodiment, the delay unit 31 and the current controller 5 are actually required for each of three phases.

[0074] Further, in the present embodiment, particularly the fact that the d-axis current Id and the q-axis current Iq cyclically vary at a cycle that is 1/6 of the cycle Tr of the AC voltage Vs brings about other effects. That is to say, the cycles of the command values Id* and Iq* as well as the cycles of the d-axis current Id and the q-axis current Iq as the compensating current in the rotating coordinate system are shorter than the cycles Tr of them (the command value Ic* and the compensating current Ic in the first embodiment) in the fixed coordinate system. This easily simplifies the configuration in which the delay units 31 d and 31 q are adopted.

[0075] Specifically, in a case where FIFO memory is used as the delay unit 31 shown in the first embodiment, for example, parts for the cycle Tr are sequentially stored, and sequentially output with the predetermined delay amount to substantially perform the phase-leading processing. Since the command value Ic* is stored for each of three phases in the example of the first embodiment, memory capacity that is three times larger than the cycle Tr is substantially required.

[0076] On the other hand, in a case where the FIFO memory is used as the delay unit 31d, it suffices that the d-axis current command values Id* for the cycle Tr/6 are sequentially stored, and sequentially output with the predetermined delay amount. The same applies to the delay unit 31q. The required memory capacity is thus 1/3 of the cycle Tr, and can be reduced to 1/9 of that in the first embodiment.

Modifications

[0077] Assume that the number of storage locations of the command value Ic* for one phase in the memory adopted as the delay unit 31 is N. For example, if a control cycle of the current control is 50 μs when Tr = 20 ms (corresponding to a power supply frequency of 50 Hz) is satisfied, it is desirable to satisfy $N \geq 20\text{ms}/50\mu\text{s} = 400$.

[0078] In contrast, when the number of storage locations for the cycle Tr is N, it is desirable that the control cycle be longer than N/Tr. It is also desirable to approximate the phase amount φ by which the phase is led, which should originally be the time ta when converted into time, by k/(N·Tr) by introducing a non-negative integer k. This is because the phase-leading of the command value Ic* can be performed by delaying values for (N-k) data. The same applies to the delay units 31d and 31 q.

[0079] Alternatively, when the above-mentioned integer k for the time ta corresponding to the led phase does not exist, integers k1 and k2 may be determined as shown below by expressing the fractional part of ta/Tr as F[ta/Tr], and a substantially phase-led command value may be obtained through interpolation using the (N-k1)th command value and the (N-k2)th command value. The same applies to the delay units 31 d and 31 q.

$$k1 = ta/Tr - F[ta/Tr],\ k2 = k1 + 1$$

[0080] While the present invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications that have not been described can be devised without departing from the scope of the present invention.

Claims

1. An active filter control device that controls a parallel active filter (6) connected to an AC power supply (1) through an interconnection reactor (4) and outputting compensating current (Ic; Id, Iq), said AC power sup-

ply supplying load current (Io) to a load (2), said active filter control device comprising:

a harmonic component extraction unit (7A; 7B) obtaining a command value (Ic*; Id*, Iq*) of said compensating current from a harmonic component of said load current;
a difference current generation unit (3A; 3B) obtaining a deviation (Ie) between said compensating current and a value (Ic^; Id*^, Iq*^) obtained by leading a phase of said command value by a predetermined phase difference (360°×ta/Tr);
a current controller (5; 10dd, 10qq) generating a control signal (V*; Vid, Viq) based on output of said difference current generation unit; and
a driving signal generation circuit (8) generating, based on said control signal, a driving signal (G) driving said parallel active filter.

2. The active filter control device according to claim 1, wherein
said difference current generation unit (3A; 3B) includes:

a delay unit (31) performing processing of delaying said command value (Ic*; Id*, Iq*) by a phase obtained by subtracting said predetermined phase difference (360°×ta/Tr) from a phase for one cycle of said AC power supply (1); and
a subtracter (32) obtaining a difference between output (Ic*^; Id*^, Iq*^) of said delay unit and said compensating current (Ic; Id, Iq).

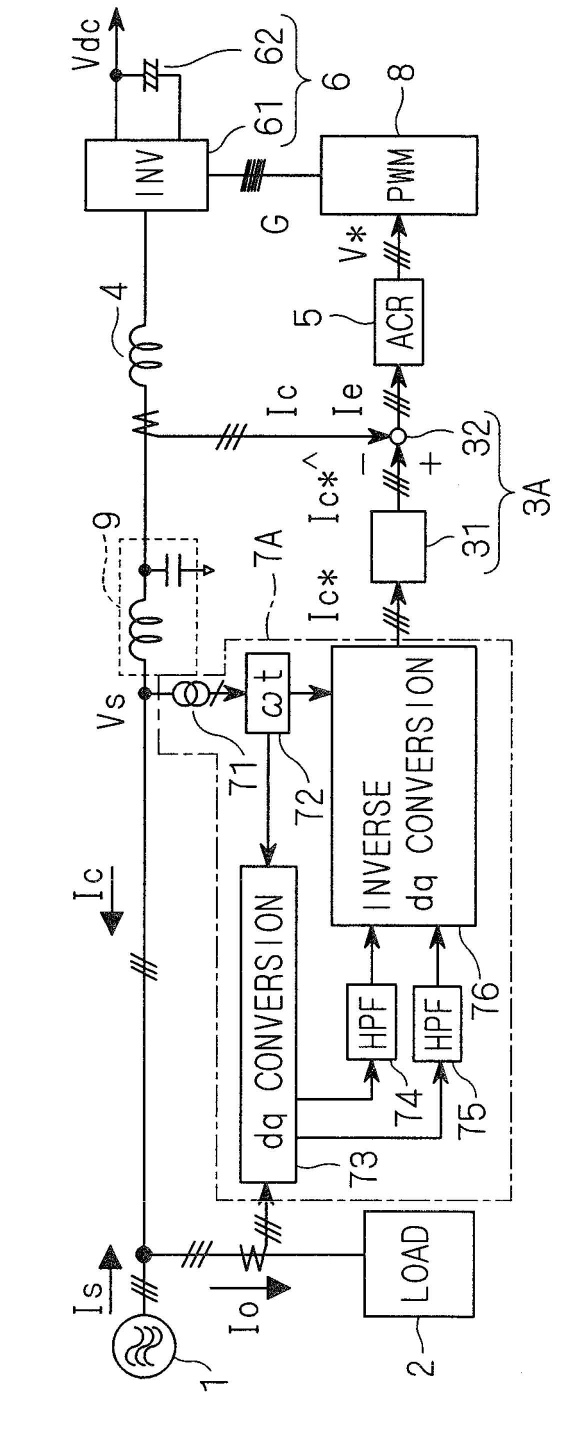
3. The active filter control device according to any one of claims 1 to 2, wherein
said command value (Ic*) is obtained by removing a DC component from said load current (Io) grasped in a rotating coordinate system synchronizing with a phase of said AC power supply (1), and further performing coordinate conversion so as to be grasped in a fixed coordinate system,
said compensating current (Ic) is grasped in said fixed coordinate system, and
said deviation (Ie) is obtained in said fixed coordinate system.

4. The active filter control device according to any one of claims 1 to 2, wherein
said command value (Id*, Iq*) is obtained by removing a DC component from said load current (Io) grasped in a rotating coordinate system synchronizing with a phase of said AC power supply (1),
said compensating current (Id, Iq) is grasped in said rotating coordinate system, and
said deviation (Ied, Ieq) is obtained in said rotating coordinate system.

5. The active filter control device according to claim 2, wherein
said load (2) is an air conditioner including:

an inverter (23); and
a compressor (24) controlled by said inverter to compress a refrigerant.

FIG. 1


Vdc
INV
61
62
6
PWM
8
G
V*
ACR
5
4
Ic
Ie
32
3A
31
Ic*^
Ic*
9
7A
Vs
ωt
71
72
INVERSE dq CONVERSION
dq CONVERSION
HPF
HPF
73
74
75
76
Ic
Is
Io
LOAD
1
2

F I G . 2

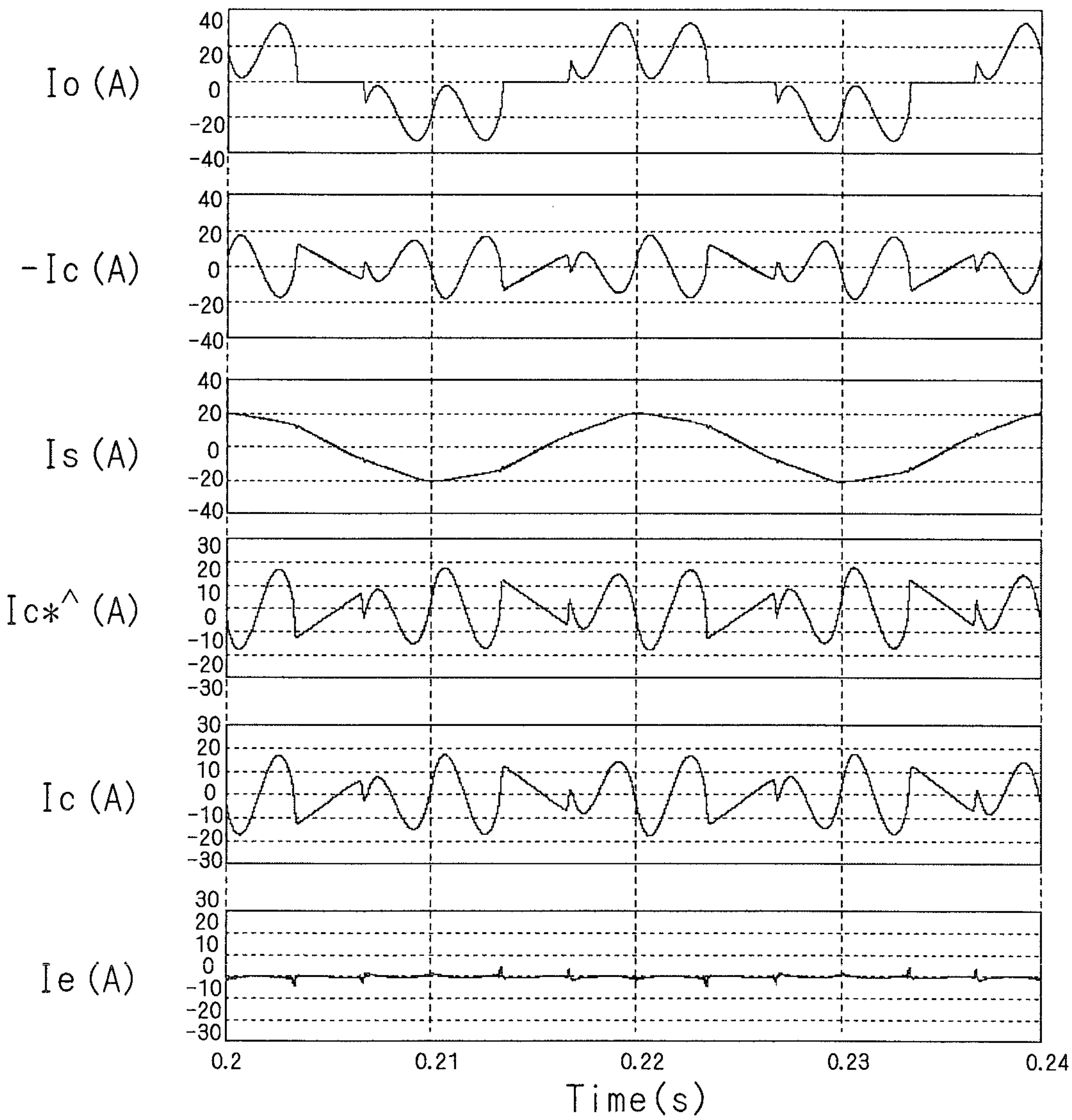

Io (A)
40
20
0
-20
-40
-Ic (A)
40
20
0
-20
-40
Is (A)
40
20
0
-20
-40
Ic*^ (A)
30
20
10
0
-10
-20
-30
Ic (A)
30
20
10
0
-10
-20
-30
Ie (A)
30
20
10
0
-10
-20
-30
0.2
0.21
0.22
0.23
0.24
Time(s)

FIG. 3

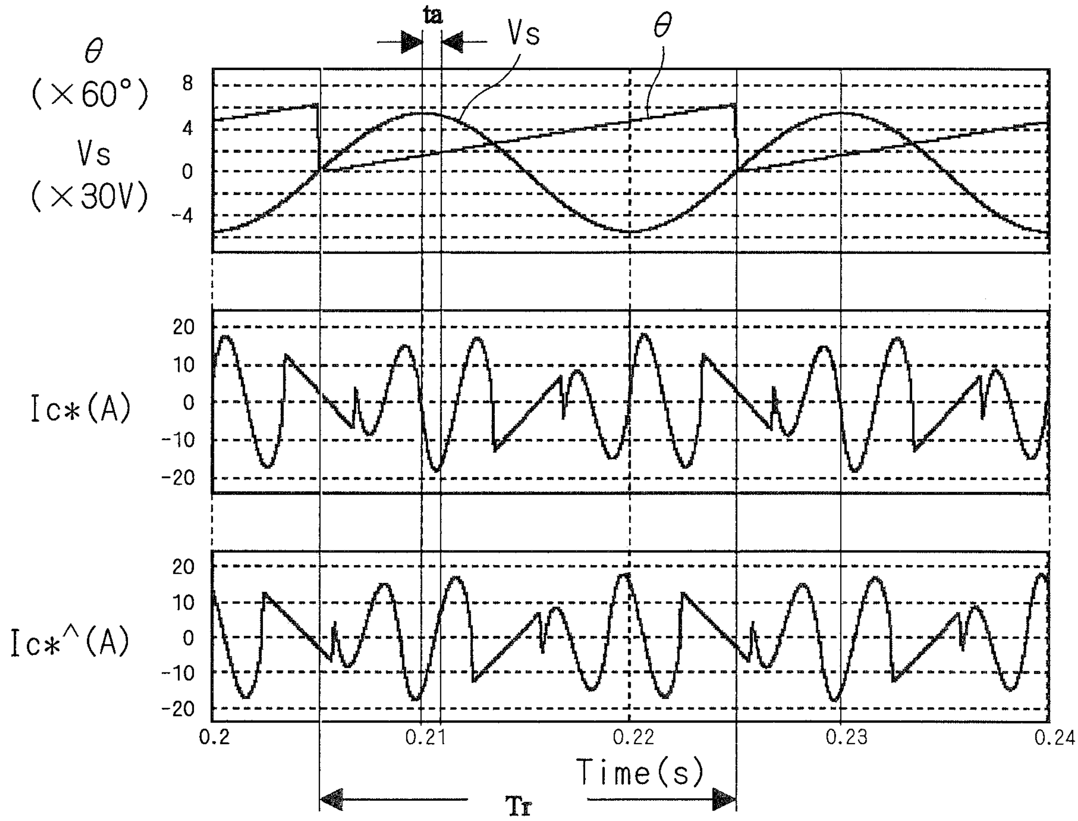
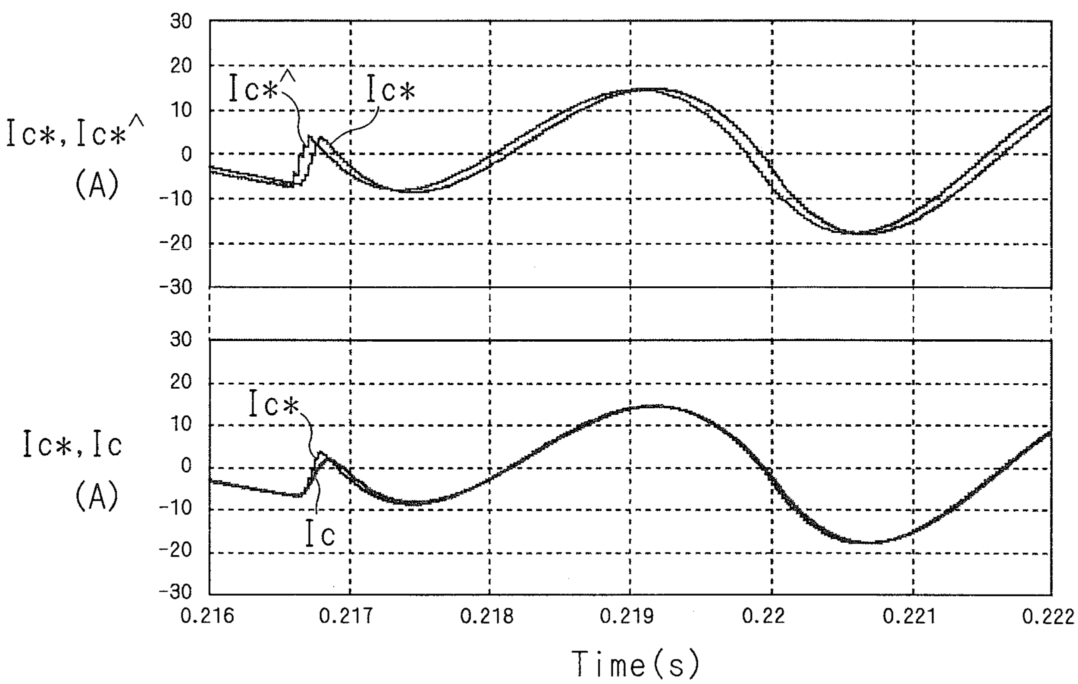
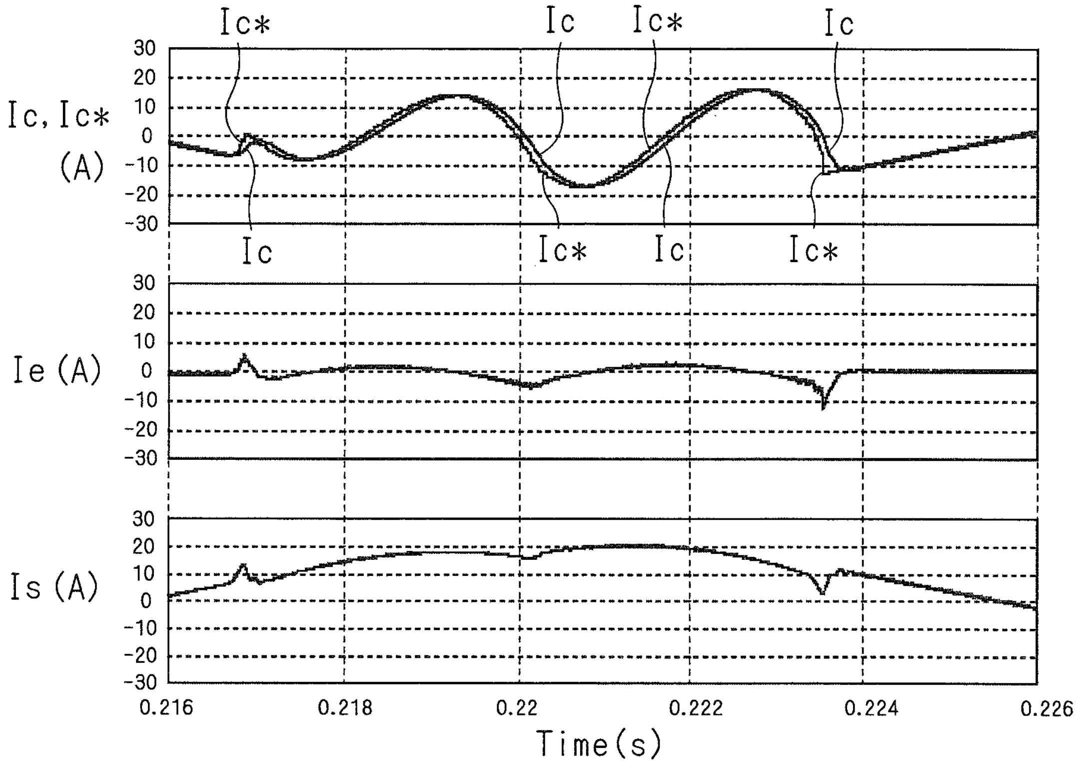

ta
Vs
θ
θ
(×60°)
Vs
(×30V)
8
4
0
-4
Ic*(A)
20
10
0
-10
-20
Ic*^(A)
20
10
0
-10
-20
0.2
0.21
0.22
0.23
0.24
Time(s)
Tr

FIG. 4


Ic*,Ic*^
(A)
30
20
10
0
-10
-20
-30
Ic*^
Ic*
Ic*,Ic
(A)
30
20
10
0
-10
-20
-30
Ic*
Ic
0.216
0.217
0.218
0.219
0.22
0.221
0.222
Time(s)

F I G. 5


Ic*
Ic
Ic*
Ic
Ic, Ic* (A)
Ic
Ic*
Ic
Ic*
30
20
10
0
-10
-20
-30
Ie (A)
Is (A)
0.216
0.218
0.22
0.222
0.224
0.226
Time(s)

F I G. 6

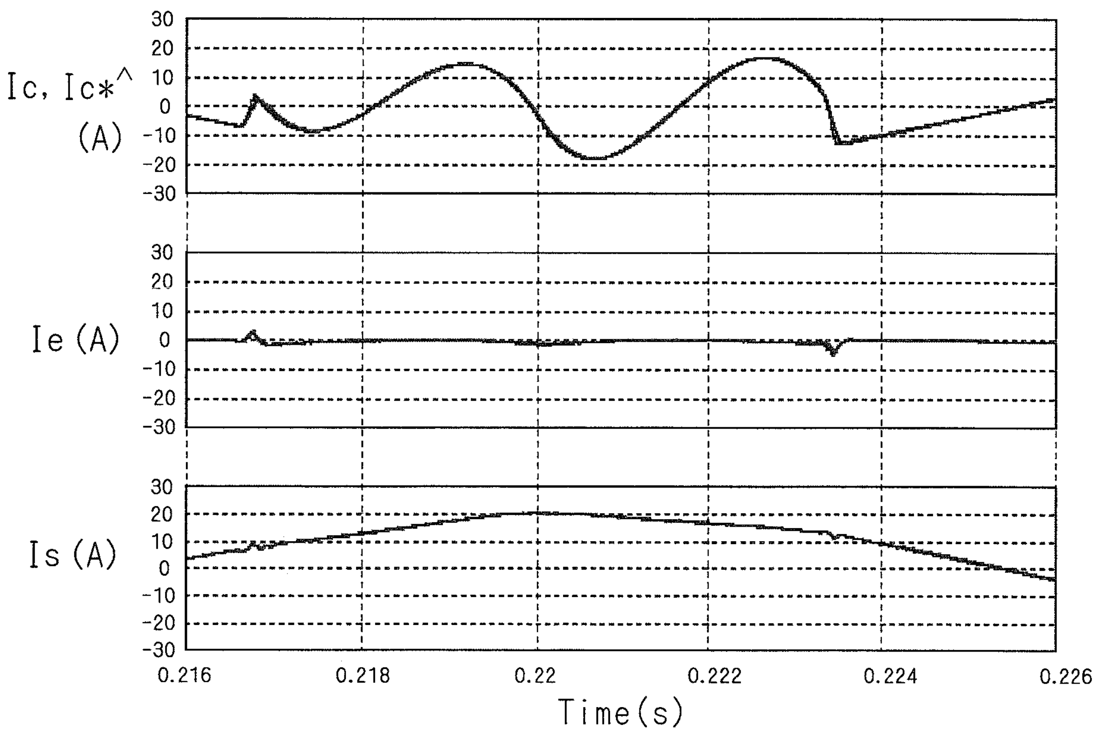
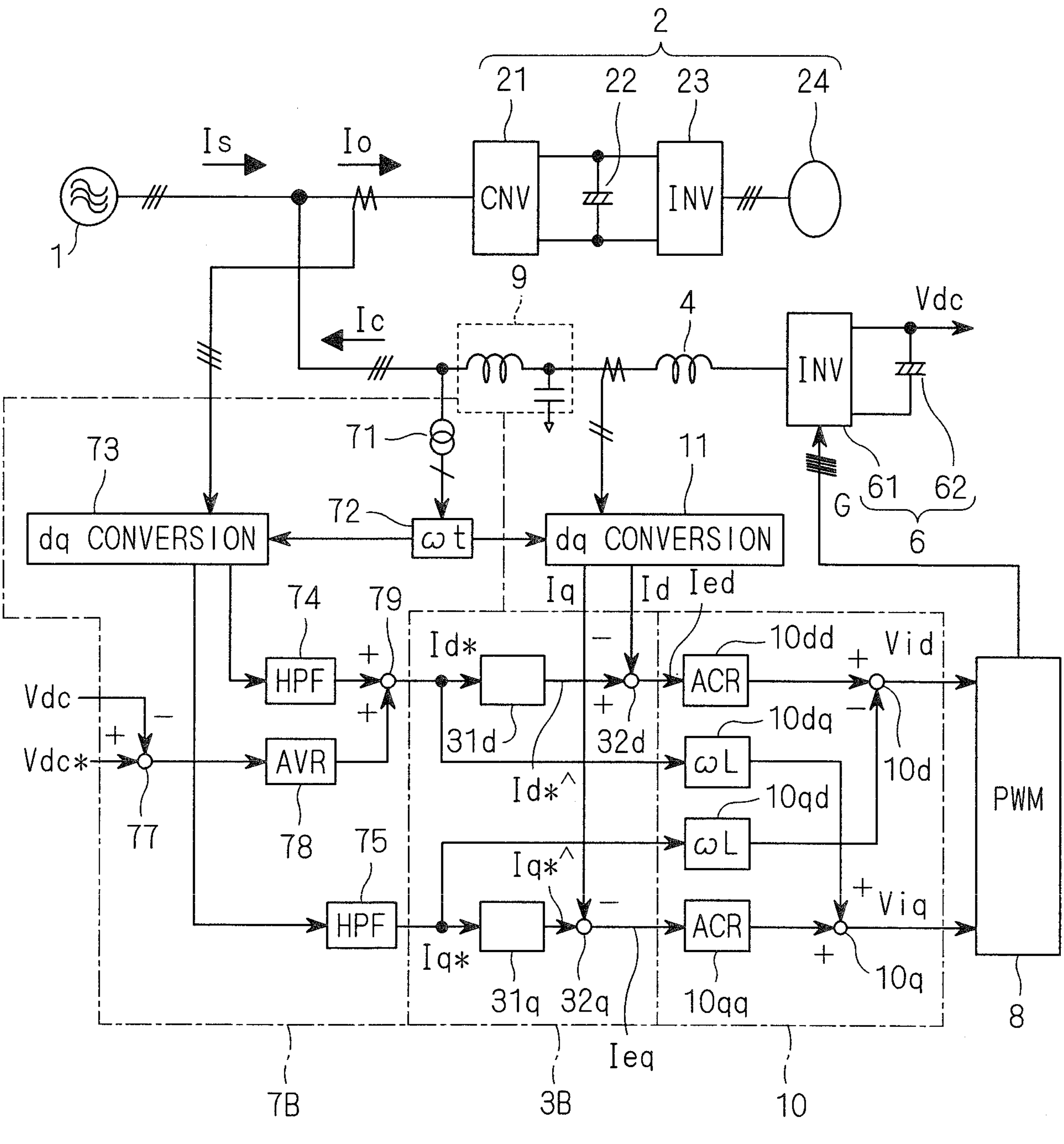

Ic, Ic*^ (A)
30
20
10
0
-10
-20
-30
Ie (A)
Is (A)
0.216
0.218
0.22
0.222
0.224
0.226
Time(s)

FIG. 7


2
21
22
23
24
Is
Io
CNV
INV
1
9
Ic
4
Vdc
INV
71
72
73
11
61
62
G
6
dq CONVERSION
ωt
dq CONVERSION
Iq
Id
Ied
74
79
HPF
AVR
HPF
Id*
Iq*
31d
32d
31q
32q
Id*^
Iq*^
ACR
ωL
ωL
ACR
10dd
10dq
10qd
10qq
Vid
Viq
10d
10q
PWM
8
Vdc
Vdc*
77
78
75
7B
3B
Ieq
10

F I G. 8

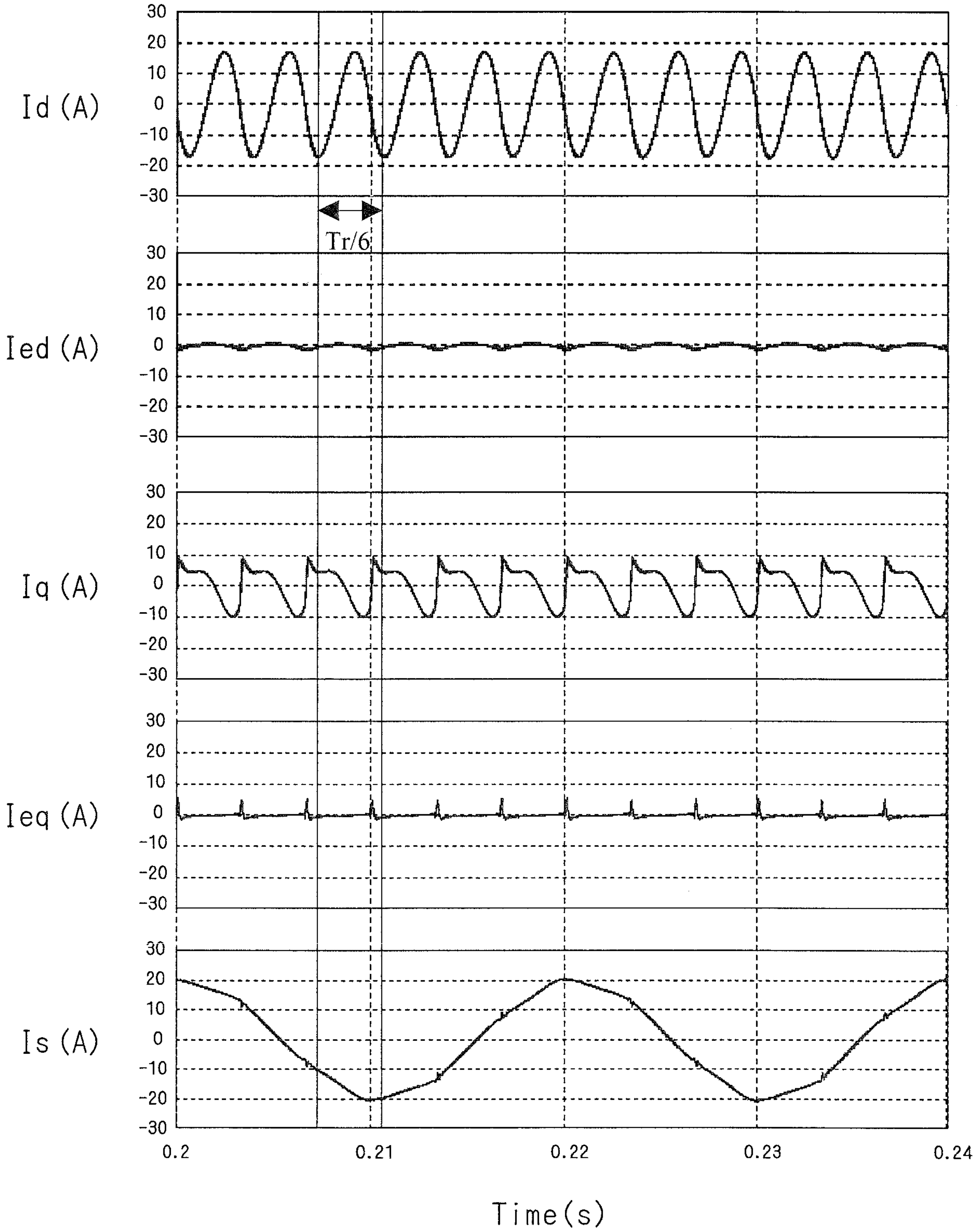
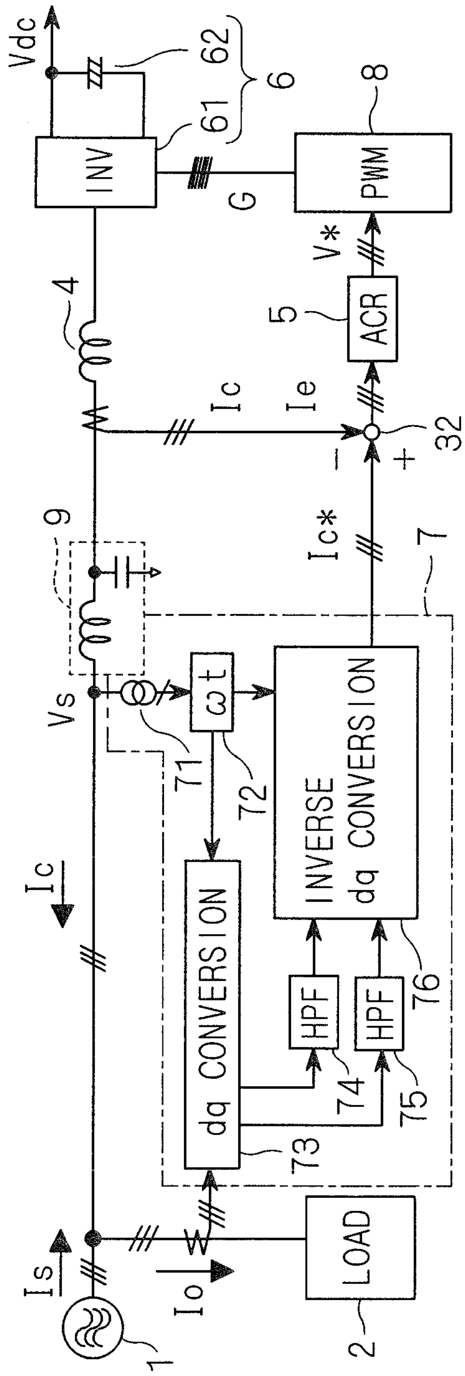
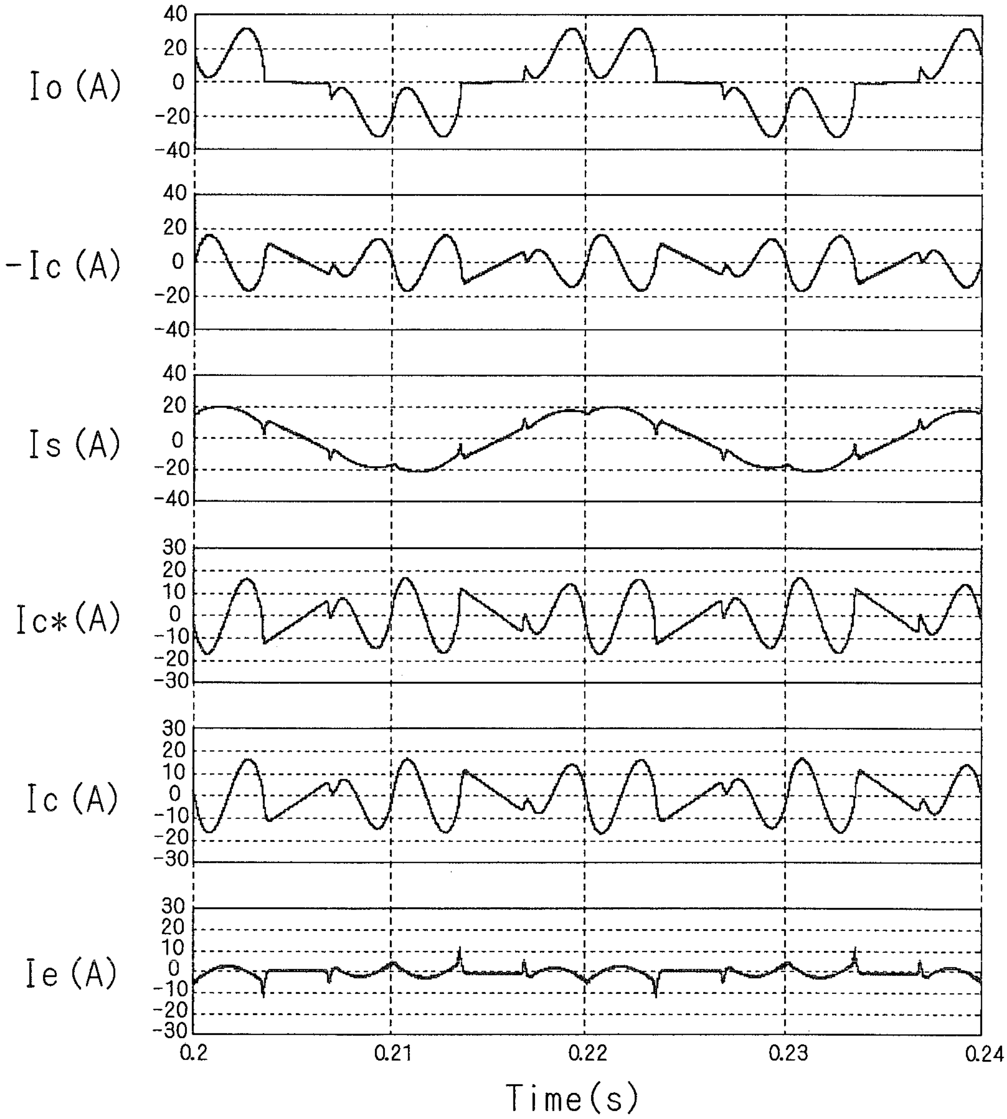

Id (A)
Ied (A)
Iq (A)
Ieq (A)
Is (A)
Tr/6
30
20
10
0
-10
-20
-30
0.2
0.21
0.22
0.23
0.24
Time(s)

FIG. 9


Vdc
62
6
61
INV
G
8
PWM
V*
5
ACR
4
Ic
Ie
32
−
+
9
Ic*
7
Vs
ωt
71
72
INVERSE
dq CONVERSION
Ic
dq CONVERSION
HPF
HPF
76
74
75
73
Is
Io
LOAD
1
2

F I G . 1 0



Io (A)
-Ic (A)
Is (A)
Ic* (A)
Ic (A)
Ie (A)
40
20
0
-20
-40
30
10
-10
-30
0.2
0.21
0.22
0.23
0.24
Time(s)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2013/081662

A. CLASSIFICATION OF SUBJECT MATTER
H02J3/01(2006.01)i, *H02M1/12*(2006.01)i, *H02M7/12*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02J3/01, H02M1/12, H02M7/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2014
Kokai Jitsuyo Shinan Koho	1971-2014	Toroku Jitsuyo Shinan Koho	1994-2014

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 11-318029 A (The Tokyo Electric Power Co., Inc.), 16 November 1999 (16.11.1999), paragraphs [0002] to [0037]; fig. 1, 6, 8 (Family: none)	1-5
A	JP 9-233701 A (Hitachi, Ltd.), 05 September 1997 (05.09.1997), paragraph [0011]; fig. 1 (Family: none)	1-5
A	JP 11-103527 A (The Tokyo Electric Power Co., Inc.), 13 April 1999 (13.04.1999), paragraph [0015]; fig. 1 (Family: none)	3

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 February, 2014 (03.02.14)	10 February, 2014 (10.02.14)

Name and mailing address of the ISA/	Authorized officer
Japanese Patent Office	
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2013/081662

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2003-169481 A (Daikin Industries, Ltd.), 13 June 2003 (13.06.2003), paragraphs [0033] to [0039]; fig. 1 to 5 (Family: none)	5

Form PCT/ISA/210 (continuation of second sheet) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 3755220 B **[0008]**
- JP 5252751 A **[0008]**
- JP 2008234298 A **[0008]**

Non-patent literature cited in the description

- **KATSUHIRO IZUMI.** Influence of the Compensation Current Detection Characteristic on the Active Filter Performance. *Reports of the Faculty of Engineering,* July 2000, vol. 30 (55), 165-169 **[0009]**