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(54) Title: SILICON NITRIDE PROCESS FOR REDUCTION OF THRESHOLD SHIFT

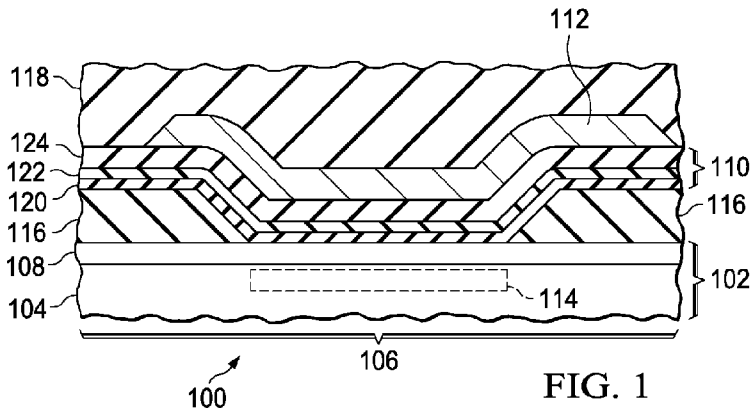

FIG. 1

(57) Abstract: A semiconductor device (100) has a substrate (102) with a semiconductor material (104). The semiconductor device (100) includes a field effect transistor (106) in and on the semiconductor material (104). The field effect transistor (106) has a gate dielectric layer (110) over the semiconductor material (104) of the semiconductor device (100), and a gate (112) over the gate dielectric layer (110). The gate dielectric layer (110) includes a layer of nitrogen-rich silicon nitride (120) immediately over the region for the channel (114), and under the gate (112).

WO 2017/223541 A1

[Continued on next page]

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SILICON NITRIDE PROCESS FOR REDUCTION OF THRESHOLD SHIFT

[0001] This relates generally to semiconductor devices, and more particularly to field effect transistors in semiconductor devices.

BACKGROUND

[0002] A field effect transistor (FET) operates by applying a potential to the gate of the transistor, which changes the density of charge carriers in the channel of the transistor. The threshold potential of the transistor may be understood as the gate potential at which the transistor changes from the off state, in which minimal current flows through the channel, to the on state, in which a pre-defined current flows through the channel. Reliable operation of the transistor depends on the threshold potential remaining constant during the operational lifetime of the transistor. Charges tend to accumulate between the gate and the channel, in the gate dielectric layer, and thus adversely affect the reliability by shifting the threshold potential. Charge accumulation is particularly problematic in gate dielectric layers which include silicon nitride.

SUMMARY

[0003] A semiconductor device includes a FET with a gate dielectric layer over a semiconductor region of the semiconductor device, and a gate over the gate dielectric layer. The gate dielectric layer includes a layer of nitrogen-rich silicon nitride immediately over the semiconductor region, and under the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example semiconductor device.

[0005] FIG. 2A through FIG. 2E are cross sections of the semiconductor device of FIG. 1, depicting stages of an example method of formation.

[0006] FIG. 3 is a flowchart of an example method for forming a semiconductor device including a FET.

[0007] FIG. 4A and FIG. 4B are cross sections of the semiconductor device of FIG. 1, depicting stages of another example method of formation for the N-rich layer.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] The drawings are not drawn to scale. Example embodiments can be practiced without one or more of the specific details or with other methods. In this description, some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with this description.

[0009] A semiconductor device includes a FET with a gate dielectric layer over a region for a channel in a semiconductor region of the semiconductor device, and a gate over the gate dielectric layer. The channel is an inversion layer in the semiconductor region under the gate. If the FET is an enhancement mode device, the channel generally does not exist when the semiconductor device is unpowered and not being operated. If the FET is a depletion mode device, the channel generally exists when the semiconductor device is unpowered and not being operated. For the purpose of improving the readability of this description, the region for the channel will hereinafter be referred to as the channel, even in cases in which the semiconductor device is unpowered and not being operated. The channel may exist for the particular semiconductor device being described only when the semiconductor device is being operated.

[0010] The channel may be developed in a group III-V semiconductor material such as gallium nitride or an alloy semiconductor material of gallium nitride and aluminum nitride. The gate dielectric layer includes a layer of nitrogen-rich silicon nitride that is positioned immediately over the channel, and under the gate. The gate dielectric layer may also include a layer of silicon-rich silicon nitride over the layer of nitrogen-rich silicon nitride, and the gate dielectric layer is positioned under the gate.

[0011] FIG. 1 is a cross section of an example semiconductor device 100. The semiconductor device 100 is developed on a substrate 102 having a semiconductor region 104. The semiconductor device 100 includes a FET 106. The semiconductor region 104 may include group III-V semiconductor material such as gallium nitride or an alloy semiconductor material of gallium nitride and aluminum nitride. Other semiconductor materials, such as other group III-V semiconductors, group II-VI semiconductors or possibly Group IV semiconductors, are within the scope of this example. In versions of this example in which the semiconductor region 104 includes group III-V semiconductor material, an optional stressor layer 108 comprising one or more sub-layers of group III-V material may be formed over the semiconductor region 104. The

stressor layer 108 may be used for inducing piezoelectric stress in the semiconductor region 104, and potentially for other purposes, such as providing isolation between a two-dimensional electron gas in the semiconductor region 104 and a gate 112. The optional stressor layer 108, if present, may be a part of the substrate 102. Similarly, any native oxide layers on the substrate 102, if present, may be developed onto the substrate 102.

[0012] The FET 106 may be a depletion mode device or an enhancement mode device. The FET 106 includes a gate dielectric layer 110 disposed over the substrate 102. The gate 112 is disposed over the gate dielectric layer 110. A channel 114 is located in the semiconductor region 104 under the gate dielectric layer 110. An isolation dielectric layer 116 may be disposed over the substrate 102 outside of the channel 114; lateral boundaries of the isolation dielectric layer 116 may define a lateral area for the channel 114. The gate dielectric layer 110 and the gate 112 may extend partway over the isolation dielectric layer 116, further on a drain side than on a source side, as depicted in FIG. 1, to serve as a field plate adjacent to the channel 114. An interconnect dielectric layer 118 may be disposed over the gate 112 to isolate the gate 112 from other interconnects of the semiconductor device 100 such as source and drain contacts.

[0013] In this example, the gate dielectric layer 110 includes a nitrogen-rich layer of silicon nitride 120, herein after referred to as the N-rich layer 120 disposed immediately over the substrate 102 in the area over the channel 114. A silicon-to-nitrogen atomic ratio of a silicon nitride layer may be characterized by an index of refraction. The index of refraction may be measured at a wavelength of 630 nanometers to 635 nanometers. Stoichiometric silicon nitride may have an example silicon-to-nitrogen atomic ratio of about 0.75, within a margin of less than 1 percent. The N-rich layer 120 may have an index of refraction that is 0.015 to 0.030 less than an index of refraction of stoichiometric silicon nitride material. Such an N-rich layer 120 has been shown to be an effective for reducing charge accumulation. The N-rich layer 120 may be 5 nanometers to 20 nanometers thick, which has been shown to be an effective thickness for reducing charge accumulation. A hydrogen content, expressed in atomic fraction, of the N-rich layer 120 may be less than 10 percent, which may advantageously further reduce charge accumulation.

[0014] The gate dielectric layer 110 may further include an optional silicon rich layer of silicon nitride 122, hereinafter referred to as the Si-rich layer 122, disposed over the N-rich layer 120. The Si-rich layer 122 may have an index of refraction that is 0.025 to 0.040 more than the

index of refraction of the stoichiometric silicon nitride material. The Si-rich layer 122 may be 5 nanometers to 20 nanometers thick, which has been shown to be an effective thickness for further reducing charge accumulation when disposed over the N-rich layer 120. A hydrogen content of the Si-rich layer 122 may also be less than 10 percent.

[0015] The gate dielectric layer 110 may further include an optional threshold adjust dielectric layer 124 disposed over the N-rich layer 120 and over the Si-rich layer 122 if present, to provide a desired threshold potential for the FET 106. The threshold adjust dielectric layer 124 may include stoichiometric silicon nitride, or silicon dioxide, or other dielectric material.

[0016] The FET 106 includes source and drain regions (not shown in FIG. 1) that are positioned on opposite ends of the channel 114. The semiconductor device 100 includes interconnects such as metal contacts and metal lines through the interconnect dielectric layer 118 to provide electrical connections to the gate 112 and the source and drain regions.

[0017] FIG. 2A through FIG. 2E are cross sections of the semiconductor device of FIG. 1, depicting stages of an example method of formation. Referring to FIG. 2A, the isolation dielectric layer 116 is formed over the substrate 102 before forming the gate dielectric layer 110. For example, the isolation dielectric layer 116 may be formed by forming a layer of silicon dioxide over the substrate 102, and then forming an isolation mask over the layer of silicon dioxide to expose the layer of silicon dioxide in the area for the channel 114 of FIG. 1. The layer of silicon dioxide is etched in the area exposed by the isolation mask, and the isolation mask is subsequently removed.

[0018] The semiconductor device 100 is placed in a first low pressure chemical vapor deposition (LPCVD) chamber 126, possibly with a plurality of similar substrates. The semiconductor device 100 is heated to a temperature of 600 °C to 740 °C. Dichlorosilane is flowed into the first LPCVD chamber 126 at a flow rate of 10 standard cubic centimeters per minute (sccm) to 80 sccm, using a first dichlorosilane (DCS) flow controller 128. Ammonia is flowed into the first LPCVD chamber 126 at a flow rate of 6 to 12 times the flow rate of the dichlorosilane, using a first ammonia (NH_3) flow controller 130. A pressure in the first LPCVD chamber 126 is maintained at 100 millitorr to 500 millitorr. The flow rates of the dichlorosilane and the ammonia described in this example apply to 200 millimeter substrates run in a batch of 60 wafers to 150 wafers. The flow rates may be varied for other size substrates and batch loads, while the ratio of the dichlorosilane and ammonia flow rates is maintained. The dichlorosilane

and the ammonia react on the semiconductor device 100 to form the N-rich layer 120. Flows of the dichlorosilane and the ammonia may be continued for a predetermined time to attain a desired thickness of the N-rich layer 120, after which the flows are discontinued. Alternatively, a thickness of the N-rich layer 120 may be monitored to determine an appropriate time to discontinue the flows. Other methods of process control for formation of the N-rich layer 120 are within the scope of this example. In one version of this example, the N-rich layer 120 may maintained in a low pressure ambient substantially free of oxidizing reagents, such as oxygen or nitrous oxide, to prevent oxidation of a top surface of the N-rich layer 120.

[0019] Referring to FIG. 2B, the semiconductor device 100 is placed in a second LPCVD chamber 132, which may be the first LPCVD chamber 126 of FIG. 2A. The semiconductor device 100 is heated to a temperature of 780 °C to 900 °C. Dichlorosilane is flowed into the second LPCVD chamber 132 at a flow rate of 40 sccm to 100 sccm, using a second DCS flow controller 134, which may be the first DCS flow controller 128 of FIG. 2A. Ammonia is flowed into the second LPCVD chamber 132 at a flow rate of 3 to 6 times the flow rate of the dichlorosilane, using a second NH_3 flow controller 136, which may be the first NH_3 controller 130 of FIG. 2A. A pressure in the second LPCVD chamber 132 is maintained at 100 millitorr to 500 millitorr. The dichlorosilane and the ammonia react on the N-rich layer 120 to form the Si-rich layer 122. Flows of the dichlorosilane and the ammonia may be continued for a predetermined time or may be endpointed, as described in reference to FIG. 2A. In one version of this example, the Si-rich layer 122 may maintained in a low pressure ambient substantially free of any oxidizing reagent. Using the same LPCVD chamber 132 for forming the N-rich layer 120 and the Si-rich layer 122 may advantageously reduce process complexity for forming the semiconductor device 100.

[0020] Referring to FIG. 2C, the semiconductor device 100 is placed in a third LPCVD chamber 138, which may be the first LPCVD chamber 126 of FIG. 2A and/or the second LPCVD chamber 132 of FIG. 2B. The semiconductor device 100 is heated to a temperature of 740 °C to 780 °C. Dichlorosilane is flowed into the third LPCVD chamber 138 at a flow rate of 30 sccm to 120 sccm, using a third DCS flow controller 140, which may be the first DCS flow controller 128 of FIG. 2A and/or the second DCS flow controller 134 of FIG. 2B. Ammonia is flowed into the third LPCVD chamber 138 at a flow rate of 8 to 12 times the flow rate of the dichlorosilane, using a third NH_3 flow controller 142, which may be the first NH_3 controller 130

of FIG. 2A and/or the second NH_3 flow controller 136 of FIG. 2B. A pressure in the third LPCVD chamber 138 is maintained at 100 millitorr to 500 millitorr. The dichlorosilane and the ammonia react on the Si-rich layer 122 to form the stoichiometric silicon nitride layer 124. Flows of the dichlorosilane and the ammonia may be continued for a predetermined time or may be endpointed, as described in reference to FIG. 2A. Using the same LPCVD chamber 138 for forming the stoichiometric silicon nitride layer 124 and the N-rich layer 120 and the Si-rich layer 122 may advantageously further reduce process complexity for forming the semiconductor device 100.

[0021] Referring to FIG. 2D, a layer of gate material 144 is formed over the gate dielectric layer 110. The layer of gate material 144 may include sub-layers of different metals, such as to provide adhesion, a desired work function and a desired sheet resistance. For example, the layer of gate material 144 may include titanium, titanium nitride and aluminum. Also, for example, the layer of gate material 144 may be formed by a sputter process, an evaporation process, and/or an atomic layer deposition (ALD) process.

[0022] A gate mask 146 is formed over the layer of gate material 144 which covers an area for the gate 112 of FIG. 1. The gate mask 146 may extend partway over the isolation dielectric layer 116, as depicted in FIG. 2D, to provide the field plate functionality described in reference to FIG. 1. The gate mask 146 may include photoresist, formed by a photolithographic process, and may include anti-reflection material such as an organic bottom anti-reflection coat (BARC).

[0023] Referring to FIG. 2E, gate material of the layer of gate material 144 of FIG. 2D is removed where exposed by the gate mask 146, leaving the gate material under the gate mask 146 to form the gate 112. The gate material may be removed from the layer of gate material 144 by a wet etch process, producing sloped sides on the gate 112 as depicted in FIG. 2E. A wet etch process may have a desired etch selectivity to the gate dielectric layer 110. Alternatively, the gate material may be removed by a plasma etch process such as a reactive ion etch (RIE) process. The gate mask 146 is subsequently removed, such as by an asher process, followed by a wet clean process.

[0024] FIG. 3 is a flowchart of an example method for forming a semiconductor device including a FET. Operation 300 is to provide a semiconductor substrate. The semiconductor substrate may be a wafer with multiple areas for similar semiconductor devices. The semiconductor substrate may include several epitaxial layers to provide a desired channel region

for the FET.

[0025] Operation 302 is to form a nitrogen-rich silicon nitride layer, hereinafter the N-rich layer, of a gate dielectric layer on the semiconductor substrate. The N-rich layer may formed at a lower temperature than a stoichiometric silicon nitride layer. A ratio of a flow rate of a nitrogen-containing reagent to a flow rate of a silicon-containing reagent may be higher than for the stoichiometric silicon nitride layer.

[0026] Optional operation 304 is to form a silicon-rich silicon nitride layer, hereinafter the Si-rich layer, of the gate dielectric layer on the N-rich layer. The Si-rich layer may be formed at a temperature similar to the temperature for forming the stoichiometric silicon nitride layer. A ratio of a flow rate of a nitrogen-containing reagent to a flow rate of a silicon-containing reagent may be lower than for the stoichiometric silicon nitride layer.

[0027] Optional operation 306 is to form a stoichiometric silicon nitride layer of the gate dielectric layer over the N-rich layer, on the Si-rich layer if present. The stoichiometric silicon nitride layer may be formed using the same nitrogen-containing reagent and silicon-containing reagent as used to form the N-rich layer.

[0028] Operation 308 is to form a gate over the gate dielectric layer. The gate may extend past a channel region to provide a field plate functionality.

[0029] FIG. 4A and FIG. 4B are cross sections of the semiconductor device of FIG. 1, depicting stages of another example method of formation for the N-rich layer. Referring to FIG. 4A, the semiconductor device 100 is placed in an ALD chamber 148, possibly with a plurality of similar substrates. The semiconductor device 100 is heated to a temperature of about 375 °C. Tetrachlorosilane is flowed into the first LPCVD chamber, using an ALD tetrachlorosilane flow controller 150, to provide a pressure of about 170 millitorr. Tetrachlorosilane molecules are adsorbed on the semiconductor device 100 to form an adsorbed layer of silicon-containing reagents. Flow of the tetrachlorosilane is discontinued after the adsorbed layer of silicon-containing reagents is formed.

[0030] Referring to FIG. 4B, the semiconductor device 100 is heated to a temperature of about 550 °C in the ALD chamber 148. The ALD chamber 148 may encompass two separate deposition regions, held at different temperatures. Ammonia is flowed into the ALD chamber 148 using an ALD ammonia flow controller 152, to provide a pressure in the ALD chamber 148 of about 300 millitorr. Ammonia molecules adsorb on the semiconductor device 100 and react

with the adsorbed layer of silicon-containing reagents to form a portion of the N-rich layer 120.

[0031] The operations described in reference to FIG. 4A and FIG. 4B are repeated to form the full N-rich layer 120. Depending on a desired thickness of the N-rich layer 120, the operations described in reference to FIG. 4A and FIG. 4B may repeated, such as 30 times to 120 times. After the full N-rich layer 120 is formed, formation of the semiconductor device 100 may proceed, such as described in reference to FIG. 2B through FIG. 2E.

[0032] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate comprising a semiconductor material; and

a field effect transistor (FET) comprising: a gate dielectric layer disposed over the substrate, the gate dielectric layer comprising a nitrogen-rich silicon nitride layer and a silicon nitride layer disposed over the nitrogen-rich silicon nitride layer; and a gate disposed over the gate dielectric layer.

2. The semiconductor device of claim 1, wherein the nitrogen-rich silicon nitride layer is 5 nanometers to 20 nanometers thick.

3. The semiconductor device of claim 1, wherein the nitrogen-rich silicon nitride layer has an index of refraction which is 0.015 to 0.030 less than an index of refraction of a stoichiometric silicon nitride material, wherein the index of refraction is determined at a wavelength of 630 nanometers to 635 nanometers.

4. The semiconductor device of claim 1, wherein the silicon nitride layer comprises a silicon-rich silicon nitride layer positioned on the nitrogen-rich silicon nitride layer.

5. The semiconductor device of claim 4, wherein the silicon-rich silicon nitride layer is 5 nanometers to 20 nanometers thick.

6. The semiconductor device of claim 4, wherein the silicon-rich silicon nitride layer has an index of refraction which is 0.025 to 0.040 greater than an index of refraction of stoichiometric silicon nitride material, wherein the index of refraction is determined at a wavelength of 630 nanometers to 635 nanometers.

7. The semiconductor device of claim 1, wherein the silicon nitride layer comprises a stoichiometric silicon nitride layer positioned on the nitrogen-rich silicon nitride layer, wherein the stoichiometric silicon nitride layer has a silicon-to-nitrogen atomic ratio of about 0.75.

8. The semiconductor device of claim 1, wherein the nitrogen-rich silicon nitride layer has a hydrogen content less than 10 percent in atomic fraction.

9. The semiconductor device of claim 1, wherein the semiconductor material comprises group III-V semiconductor material.

10. The semiconductor device of claim 9, wherein the group III-V semiconductor material comprises gallium and nitrogen.

11. A method, comprising:

providing a substrate of a semiconductor device, the substrate comprising a semiconductor material;

forming a nitrogen-rich silicon nitride layer over the substrate in an area for a FET;

forming a silicon nitride layer over the nitrogen-rich silicon nitride layer; and

forming a gate of the FET over the silicon nitride layer.

12. The method of claim 11, wherein the nitrogen-rich silicon nitride layer is formed by a low pressure chemical vapor deposition (LPCVD) process in a first LPCVD chamber using dichlorosilane and ammonia.

13. The method of claim 12, wherein the ammonia is flowed into the first LPCVD chamber at a flow rate of 6 to 12 times a flow rate of the dichlorosilane during formation of the nitrogen-rich silicon nitride layer.

14. The method of claim 12, wherein a temperature of the substrate in the first LPCVD chamber is 600 °C to 740 °C during formation of the nitrogen-rich silicon nitride layer.

15. The method of claim 11, wherein a thickness of the nitrogen-rich silicon nitride layer is 5 nanometers to 20 nanometers.

16. The method of claim 11, wherein the nitrogen-rich silicon nitride layer has an index of refraction which is 0.015 to 0.030 less than an index of refraction of stoichiometric silicon nitride material, wherein the index of refraction is determined at a wavelength of 630 nanometers to 635 nanometers.

17. The method of claim 11, wherein forming the silicon nitride layer over the nitrogen-rich silicon nitride layer is performed so that the nitrogen-rich silicon nitride layer is maintained in an ambient that is substantially free of any oxidizing reagent after the nitrogen-rich silicon nitride layer is formed until the silicon nitride layer is formed.

18. The method of claim 11, wherein forming the silicon nitride layer over the nitrogen-rich silicon nitride layer comprises forming a silicon-rich silicon nitride layer on the nitrogen-rich silicon nitride layer.

19. The method of claim 18, wherein the silicon-rich silicon nitride layer is formed by an LPCVD process in a second LPCVD chamber using dichlorosilane and ammonia.

20. The method of claim 19, wherein the second LPCVD chamber is the first LPCVD chamber.

21. The method of claim 18, wherein the ammonia is flowed into the second LPCVD chamber at a flow rate of 3 to 6 times a flow rate of the dichlorosilane during formation of the silicon-rich silicon nitride layer.

22. The method of claim 18, wherein a temperature of the substrate in the second LPCVD chamber is 780 °C to 900 °C during formation of the silicon-rich silicon nitride layer.

23. The method of claim 18, wherein a thickness of the silicon-rich silicon nitride layer is 5 nanometers to 20 nanometers.

24. The method of claim 11, wherein the silicon-rich silicon nitride layer has an index of refraction which is 0.025 to 0.040 greater than an index of refraction of stoichiometric silicon nitride material, wherein the index of refraction is determined at a wavelength of 630 nanometers to 635 nanometers.

25. The method of claim 11, wherein forming the silicon nitride layer over the nitrogen-rich silicon nitride layer comprises forming a stoichiometric silicon nitride layer on the nitrogen-rich silicon nitride layer, wherein the stoichiometric silicon nitride layer has a silicon-to-nitrogen atomic ratio of about 0.75.

26. The method of claim 11, wherein the nitrogen-rich silicon nitride layer is formed by an atomic layer deposition (ALD) process in an ALD chamber using tetrachlorosilane and ammonia.

27. The method of claim 26, wherein the ALD process comprises:

heating the substrate to a temperature of about 375 °C in the ALD chamber;

flowing the tetrachlorosilane into the ALD chamber to provide a pressure of about 170 millitorr while the substrate is at the temperature of about 375 °C;

subsequently discontinuing the flow of the tetrachlorosilane into the ALD chamber;

subsequently heating the substrate to a temperature of about 550 °C in the ALD chamber;

flowing the ammonia into the ALD chamber to provide a pressure of about 300 millitorr while the substrate is at the temperature of about 550 °C; and

subsequently discontinuing the flow of the ammonia into the ALD chamber.

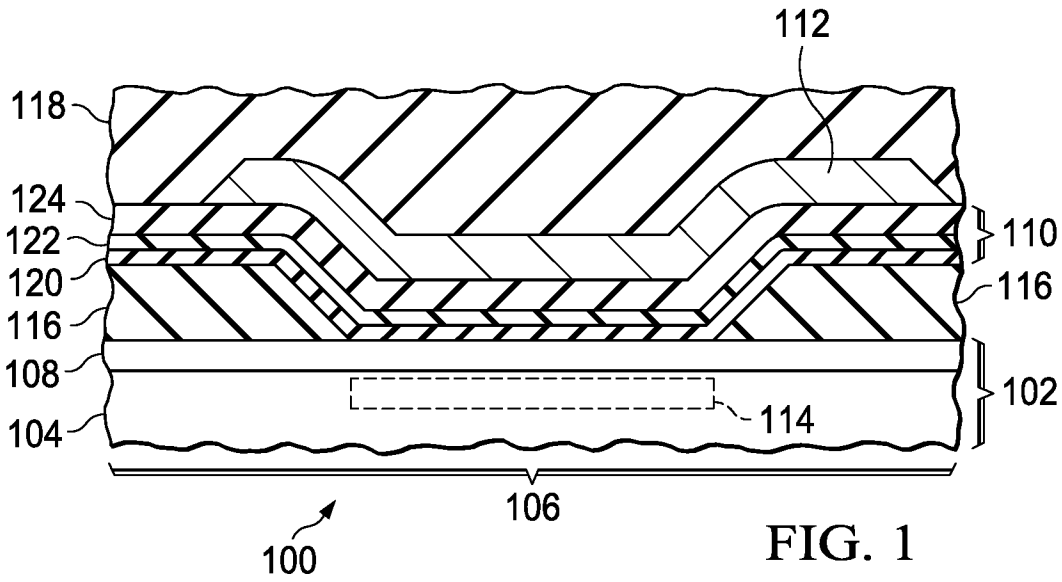
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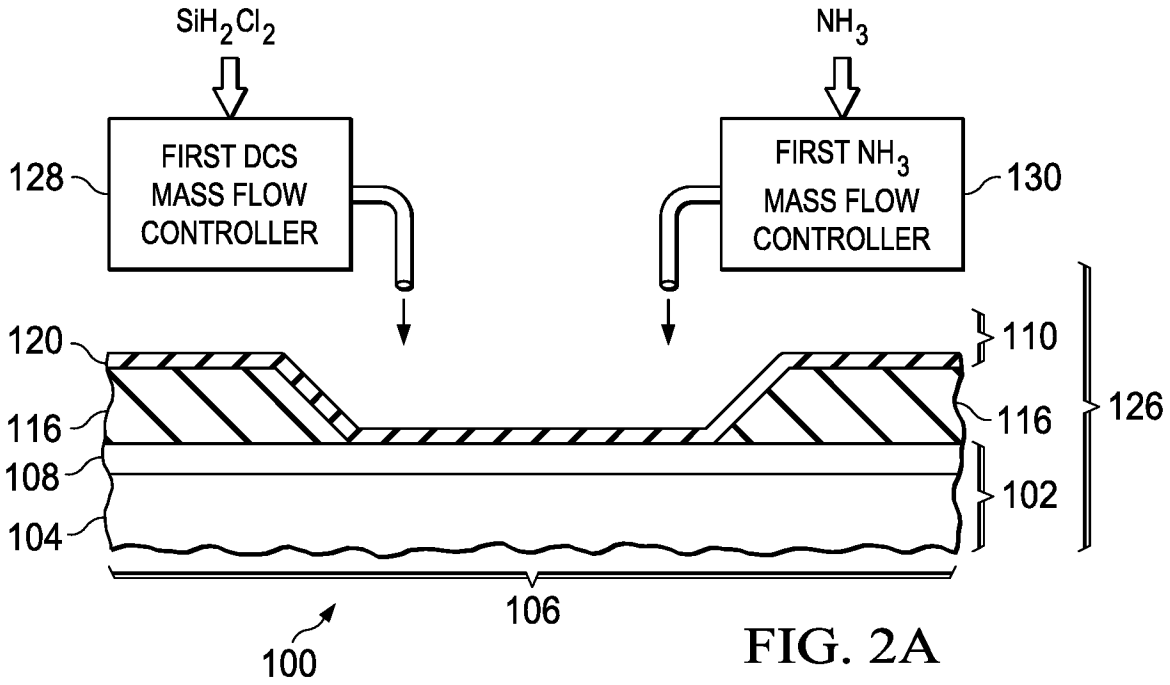
FIG. 1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NH_3
FIRST DCS MASS FLOW CONTROLLER
FIRST NH_3 MASS FLOW CONTROLLER
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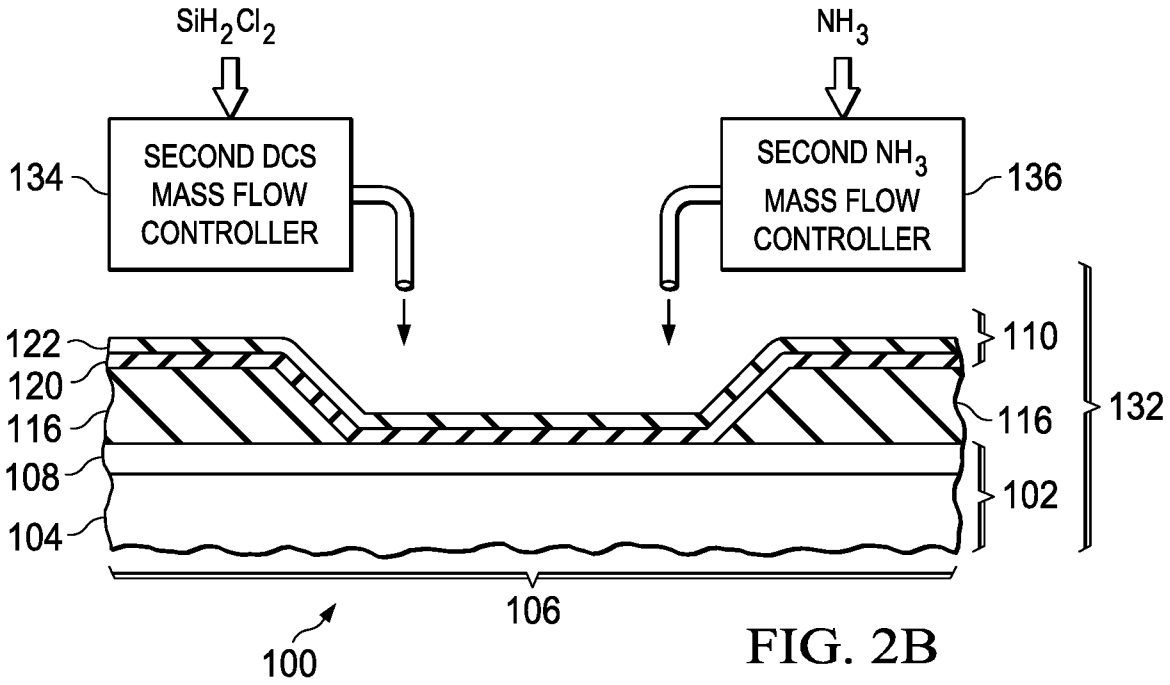
130
120
116
108
104
110
116
102
126
106
100

FIG. 2A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SECOND NH_3 MASS FLOW CONTROLLER
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110
116
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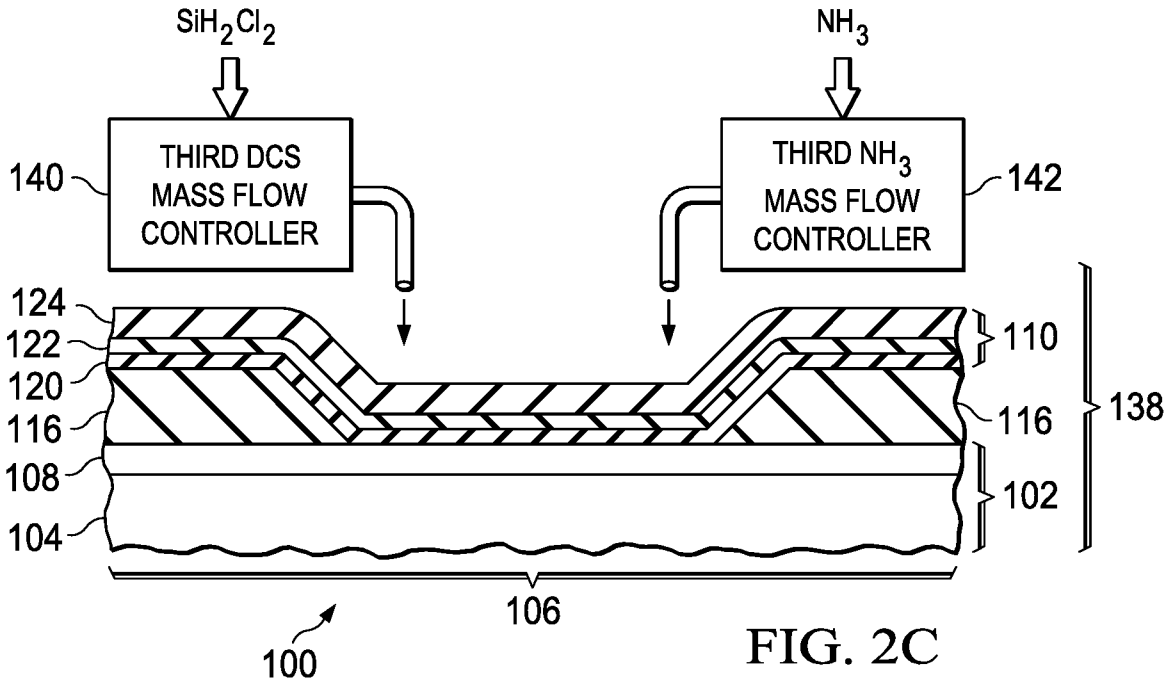
FIG. 2B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THIRD NH_3 MASS FLOW CONTROLLER
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116
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104
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116
102
138
106
100

FIG. 2C

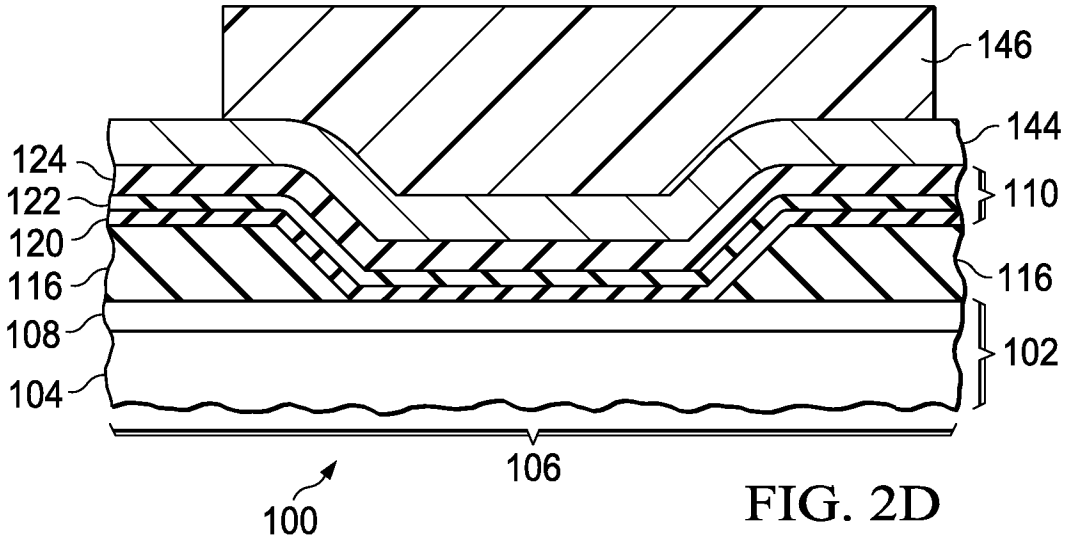

FIG. 2D

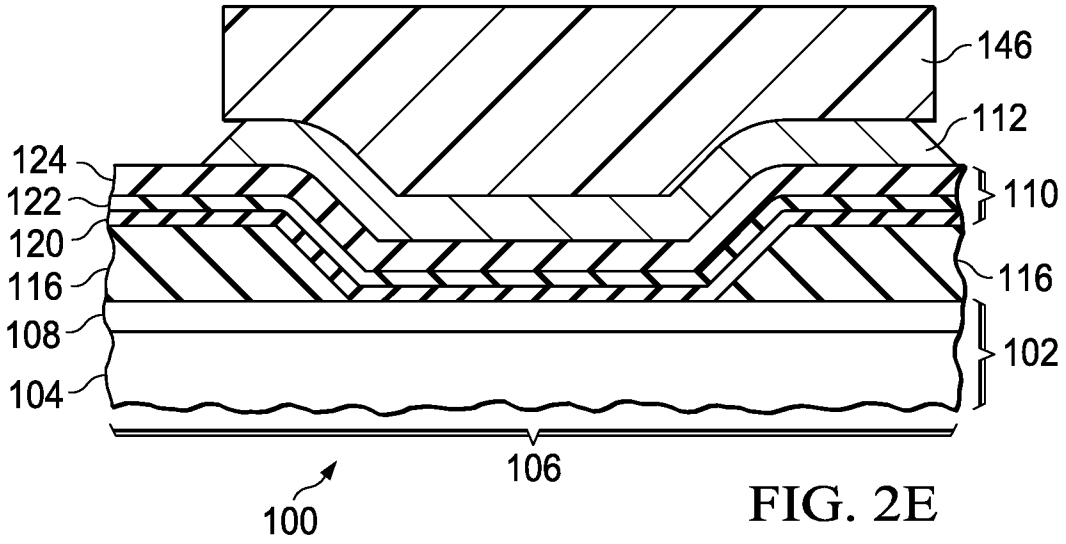

FIG. 2E

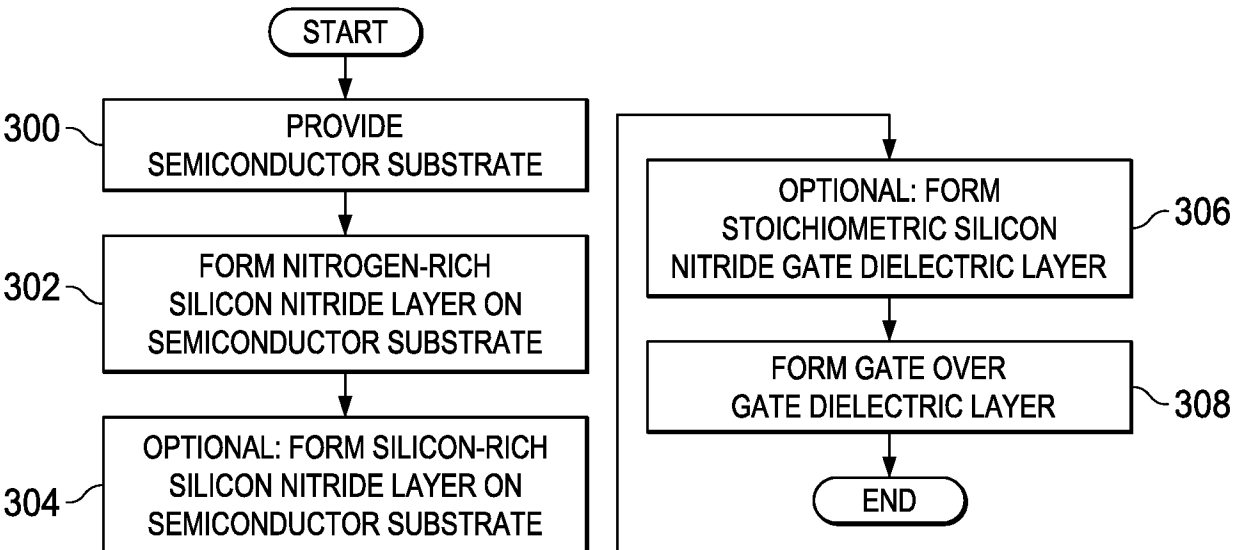

FIG. 3

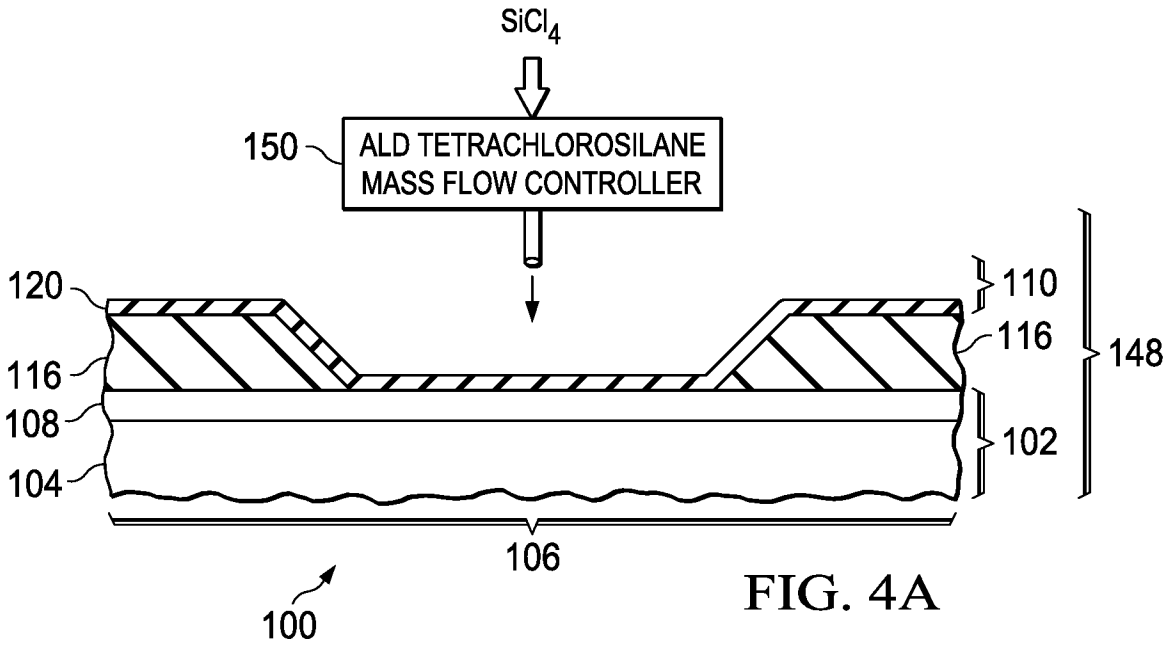
SiCl4
150
ALD TETRACHLOROSILANE
MASS FLOW CONTROLLER
120
116
108
104
110
116
148
102
106
100

FIG. 4A

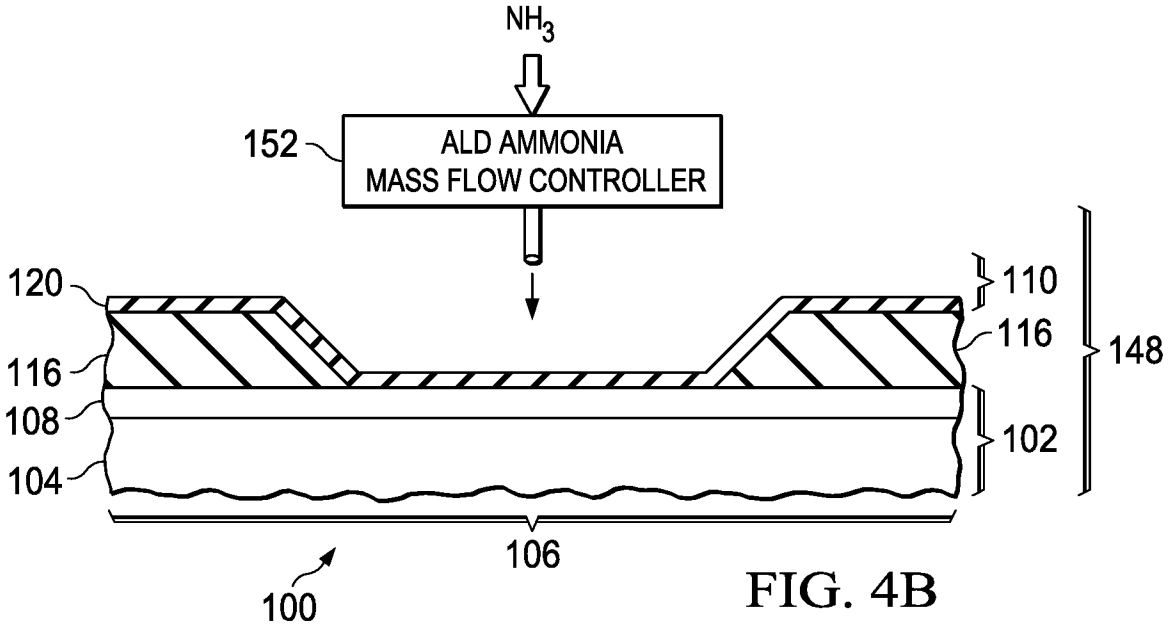
NH3
152
ALD AMMONIA
MASS FLOW CONTROLLER
120
116
108
104
110
116
148
102
106
100

FIG. 4B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/039150

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78 *(2006.01)*
H01L 21/336 *(2006.01)*
H01L 21/318 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00-23/10, 21/318, 21/336, 21/50-21/58, 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/0203541 A1 (FUJITSU LIMITED) 28.08.2008, abstract, fig. 2, par. [0038]-[0182]	1-6, 9-12, 15-16, 18-19, 23-24
A		13-14, 21-22, 26-27
X	US 2015/0145004 A1 (RENESAS ELECTRONICS CORPORATION) 28.05.2015, par. [0281]-[0282], [0152], [0111]-[0112]	1, 3-4, 6-12, 16-20, 24, 25
A	US 8354312 B2 (SUMITOMO ELECTRIC DEVICE INNOVATIONS, INC.) 15.01.2013	1-27
A	US 2011/0298060 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 08.12.2011	1-27

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2017 (14.09.2017)	28 September 2017 (28.09.2017)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer I. Baginskaya Telephone No. 8-499-240-25-91