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2001 07 27

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1998 04 08

(65)
(43)

1998 - 0081420
1998 11 25

(30)

9 - 089538
10 - 005986

1997 04 08
1998 01 14

(JP)
(JP)

(73)

가 가

1 1 1

(72)

가 가 가

1 가 가

가 가 가

1 가 가

(74)

:

(54)

MISFET

가

MISFET

MISFET

(V_{ths})

(V_{tha})

MISFET

가

가

1	MISFET			,
2	GST			,
3	GST			,
4a	4b	1		,
5a	5b	n	MIS	,
6	1			,
7	1			,
8	1			,
9a	9b	1		,
10a	10b	1	(降壓)	,
11a	11b	1		,
12	1			,
13	1			,
14	1			,
15	1			,
16	1			,
17	1			,
18a	18b			,
19a	19b	2		,
20	19a	19b		,
21a	21c	2		,
22a	22b	2		,
23	2			,

24	23		,	
25	2		,	
26a	26b		,	
27a	27b	3		가 ,
28a	28b	3		가 ,
29a	29b	3		가
, 30a	30b			,
31a	31b	4		,
32	4		,	
33	4		,	
34	4		,	
35	4		,	
36	4		,	
37	5		,	
38	5		,	
39		CMOS	,	
40				,
41a	41c	5	,	
42	5	1	,	
43	5	2	,	
44	43	2	3 - NOR	,
45	42	43	NOR	,
46	5	3	,	
47	5		,	
48	5		,	

49 5 ,
 50 5 ,
 51 5 ,
 52 6 ,
 53a 53c 6 ,
 54 7 ,
 55 7 ,
 56 55
 57 7 .

*

1 : 2 :

4 : n MISFET 5 : p MISFET

6 : 7 : 1

8 : 2 9 : MOS

11 : 12 :

13 : 14 :

15 : 19 :

20 : 21 :

22, 23, 24 : 102 :

103 : 104 :

105 : 106 :

107 : 113 :

114 :

, 1V

, MISFET 가 1
 (V_{DD}) (0V) n() MISFET(4) p() MISFET(5) M
 ISFET(4, 5) MISFET(4,5)
 (6)

1 MISFET V_{DD} (P) V_{DD}^2 가 가
 (V_{DD})

, 1 (p_d) C_L , p MISFET n MISFET
 V_{th}

$$p_d = kC_L V_{DD} / (V_{DD} - V_{th})^n \quad (k: , n=1 \sim 2)$$

(6) 0 V_{DD} 가 1V
 (V_{th}) (V_{DD}) 가 p_d 가

, CMOS

(V_{th}) , V_{th}
 Si pn

2 가 (F.As
 saderathi, D.Sinitsky, S.Parke, J.Bokor, P.K.Ko, and C.Hu, IEDM Technical Digest, 809, (1994)). 2

2 (Q1, Q2)
 , GST(Gate - Substrate Tie) , Q1 p MISFET, Q2 n
 MISFET , CMOS

2 Q2 (V_{DD}) 가 가
 0V 0V가 0V 가
 ON/OFF 가

, 0V 가 V
 V_{DD} , 가 ,
 가

, 3 2 가 가
 3 (Q1, Q2) 1 (Q3, Q4) 2
 (112) , Q1, Q3 p MISFET , Q2, Q4 n
 MISFET , CMOS 가

1 (101') , V_{DD} , 2
 (112) 0V가 , (Q3) p MISFET (V_{DD})
 (106') (102) Q3 pn , 가
 . Q2 (positive) ,
 가 . Q3 가 Q2 (106) 가 .
 , 3 (101')
 (Q4 Q1) 가 가 .
 , 0V , V_{DD} ,
 가 가 .
 , MISFET
 가 가 , (V_{DD})
 (μ_{pd}) , (V_{DD})
 (μ_{pd}) , GST .
 가 (μ_{pd}) 가 , 가
 가 .
 , ,
 가 ,
 , (V_{th}) .
 ,
 ,
 (V_{th}) (,
) GST .
 가 GST
 , 가 GST
 , /
 , .
 (1) , 2 MISFET
 , 1 , 1 2
 가 ,
 MISFET ,
 MISFET (V_{th_s}) (V_{th_a}) ,
 MISFET 가 , V_{DD} ,
 $V_{DD} (1 - V_{th_s} / V_{DD}) < V_{th_s} - V_t$ ha

가 가 MISFET n p .

(1 - 1) MISFET가 n 1 V_{DD} , 2 0V .

(1 - 2) MISFET가 p 1 0V , 2 V_{DD} .

(1 - 3) 가 MISFET .

(1 - 4) MISFET가 n p MISFET , p MISFET n MISFET ET .

(1 - 5) MISFET가 n n MISFET V_{DD} .

(1 - 6) MISFET가 p n MISFET , n MISFET p MISFET ET .

(1 - 7) MISFET가 p p MISFET 0V .

(2) , MISFET , (降壓) , n MISFET p MISFET ,

2 p MISFET , 1 MISFET MISFET / , n MISFET , 1 2 .

(2 - 1) 가 , / . p MISFET n MISFET

(2 - 2) p MISFET n MISFET 가 .

(2 - 3) 1 V_{DD} , 2 0V .

(3) ,

MISFET , (V_{DD}) 1 , V_{DD} 2 , / MISFET M ISFET , MISFET

MISFET 0V V_{DD} . 가 , MISFET

(4) 가 MISFET , ,
 1 , MISFET 2 ,
 1 2 , MISFET ,
 ,
 p MISFET n MISFET , 1 n MISFET
 , 2 p MISFET ,
 p MISFET n MISFET MISFET
 , p MISFET n MISFET , / 가
 , .

(4 - 1) 1 (V1) , (V2) (V1)
 0V , 2 (V3) ,
 (V4) (V3) 0V , 1 V1
 , V_{th1} , 1
 V2 , V_{th2}
 , 2 V3 ,
 V_{th3} , V4 ,
 V_{th4} , Vs, Va ($V_{th1} < V_s$ $V_{th3} > V_a$, $(V_{th2} > V_a)$ $V_{th1} < V_a$ $(V_{th3} > V_s)$ $V_{th4} < V_s$)
 .

(1) 가 ,
 . ,
 가
 , (2) (4)
 ,
 가 가 .

(5) p MISFET, n MISFET , p MI
 SFET , n MISFET 2
 , MISFET p MISFET
 n MISFET MISFET
 , MISFET , 가
 .

(5 - 1) 1 (V_{DD})가 , 2 가
 .

(5 - 2) MISFET pn .
 , (5) , 가 .

(6) ,

1 ,

1 1 2 ,

1 2 MISFET ,

2 1 MSIFET ,

1 2 ,

,

MISFET

,

1 MISFET ,
2 ,

1 MISFET 2 pn

,

1 MISFET 2 pn

,

1 MISFET 2 가 가

.

(7) ,

1 ,

1 1 2 ,

1 2 MISFET ,

2 1 MSIFET ,

1 2 ,

MISFET

,

1 , 2 ,
MSIFET ,1 1 2 pn ,
1 2 pn ,

1 2 , 가 가 .

, (6), (7) 가

(8) ,

1 ,

1 1 2 ,

1 2 MISFET ,

2 1 MISFET ,

,

MISFET , 1 , 2 MISFET

,

가 , 2 1

, 가 가 .

(9) ,

1 ,

1 1 2 ,

1 2 MISFET ,

2 1 MISFET ,

1 2 ,

1 2 MISFET

2 1 2 , 1 2

2 ,

1 2 , 2

1 1 , 가 가 .

, (8)(9) (overshoot) (undershoot)

ot) , 가 .

(10) , 1 2 MISFET 가 ,

1 MISFET , 1 MISFET 2 MISFET

, 2 MISFET ,

- 2 MISFET , 2 MISFET V_{th} 1 MISFET V_{th} , $V_{th} < V_{th}$ 가 ,
- 2 MISFET 가 , 가 . , 2 MISFET가
- (10 - 1) , 1 MISFET , .
- (10 - 2) 1 MISFET 2 MISFET .
- (10 - 3) 2 MISFET V_{th} $V_{th} > V_{th}$ 가 .
- (10 - 4) 2 MISFET 2 MISFET 가 가 , 가 가 .
- (10 - 5) 1 MISFET 2 MISFET 3 MISFET 3 MISFET 1 MISFET , 3 MISFET .
- (10 - 6) 2 MISFET 가 가 .
- (11) , 1 3 MISFET 가 , , 1 MISFET 2 MISFET 3 MISFET 가 , 2 MISFET , 1 MISFET 3 MISFET , 3 MISFET 가 .
- (11 - 1) , 1 MISFET , .
- (11 - 2) 4 MISFET 3 MISFET 3 MISFET , 4 MISFET 4 MISFET 4 MISFET .
- (11 - 3) 1 MISFET 2 MISFET .
- (11 - 4) 2 MISFET V_{th} $V_{th} > V_{th}$ 가 .
- (11 - 5) 2 MISFET 2 MISFET 가 가 , 가 가 .
- (11 - 6) 1 MISFET 2 MISFET 3 MISFET 3 MISFET 1 MISFET , 3 MISFET .

(10)(11) 가

(12) 1 1 1 2 2 1 2 1 5 2 6 3 2 4 5 6

(p_d) 가

가

(1)

(V_{th}) MISFET (E_{max})

V_{DD} 가 p_d

4a 4b

4a, n() MISFET(4) p() MISFET(5)

(6)(IN) , n MISFET(4) p MISFET(5)

(OUT) , n MISFET(4) 0V(2) , p MISF

ET(5) V_{DD} (1)

4a n MISFET(4) 가 (G)

(G) 2 n MISFET V_1 , V_1 -

V가

가 (E_{max})가 MISFET

5a 5b n MISFET - p SOI(silicon - on - insulator)

1, 2) , SOI

5a (1) (2) MIS 5a 5b E_C

E_V 가 , 5a , Q_B

(1) 가 (E_i) V_G

1

$$E_i = (V_G - \Psi_s - V_{FB}) / t_i$$

$$t_i = \frac{C_{ox}}{q} (V_G - V_{FB} - \Psi_s) \quad (1) \quad , \quad V_{FB} \text{ MIS} \quad , \quad \Psi_s \quad (2)$$

$$\frac{V_G - V_1}{2\phi_F} = 1 \quad (2) \quad F$$

2

$$E_i = (V_G - 2\phi_F - V_{FB}) / t_i$$

가 , (V_1) .

, $V_G < V_1$, $S < 2\phi_F$ 가 . V_G
 $V_{DD} < V_1$, CMOS , $V_G = V_{DD}$ 가 5b $V_{DD} < V_1$ E_i , E_i

pn (V_1)
 E_i , $V_{DD} < V_1$. 4a 4b 4 n MISFET
 ET , $V_{DD} = V_1$.

, $V_{DD} < V_1$ 4a , 0V가
 p MISFET(5) (C_L) 가 I_0
 (V_{DD}) V_1 n MISFET(4)
 (V_{DD}) V_1 n MISFET(4) , p MISFET(5) (C_L) 가
 , 가 .

V_{DD} 5 10%
 , 10% E_i

5a 5b (2)
 $V_1 = V_{DD}$ (1) .

V_{DD} pd , (E_{max})

, $V_1 = V_{DD}$, 4a 4b
 가 .

6 - 216346

6 - 89574

가 가 , V_{DD} 가

, 가 , 2 E_i .

가 n MISFET $(V_1 - V)$ 가 (6) $0V$ V
 τ_{pd}

3

$$\tau_{pd} = \frac{C_L V_{DD}}{V_{DD} - (V_1 - \Delta V)^e} = \frac{C_L V_{DD}}{\{(1 - \beta) V_{DD} + \Delta V\}^e}$$

V_{DD} e 2가 , 가 e 1 2 , 1.3 1.5
 V , V_{DD}

6 V 가 0, V_{DD} 가 $\tau_{pd} V_{DD}^{(1-e)}$, V 가 $\tau_{pd} V_{DD}$

4

$$V_{DD} < \Delta V / \{(e-1)(1-\beta)\}$$

V 가 (C_L) V_{DD} 가 V_{th} , V_{th} , e=
 2 4

5

$$V_{DD}(1 - V_{th}/V_{DD}) < V_{th} - V_{thc}$$

가 .

4b p MISFET (6) V_{DD} $0V$
 (τ_{pd}) . 4b 4a
 n MISFET가 p MISFET
 $s) V_1$, $(V_{th}) V_1 - V$ 가 . p MISFET (V_{th})

τ_{pd} V 가 , 가
 1, 2 (7, 8) 7a n MISFET(4) p MISFET(5)
 (7) /
 7c n MISFET(4) (7) ,
 (7) /

CMOS MOS (9) nMOS , 3 nMOS , 8a
 7a 7c n MISFET , 8b (10) p MISFET

, pd 9a 9b , (15) (14) 가
 . 9a 9b (11) , (12) ,
 (13) , (18)가 (11) (12)
 (14) . (15) , (18)가
 , V_{DD} , (13) p MISFET (12) , pnp
 (18) .
 , 9a 9b p MISFET(16), n MISFET(17) (V_{DD})
 . / 가 , (14)
 (19) , / (19) V_{DD} 0V
 .
 (14) 0V V_{DD} 0V ,
 가 (20) . (V)
 가
 9a . 10a 10b
 .
 10a 10b p MISFET(5) n MISFET(4)가 가 ,
 (f) (22) . , 10a (22) 0V V_{DL} 2
 , 10b 0V V_{DD} 2 . , 10a pMOSFET (15) (15)
 (OUT) , V_{DD} V_{DL} 가 . , (15)
 , (15)가 ,
 (I)가 (15) .
 , 10a (C_L) fC_L V_{DL} 2 . ,
 fC_L V_{DL} (V_{DD} - V_{DL}) . , 10a (I)
 , fC_L V_{DL} V_{DD} 가 . 10b V_{DL} < V_{DD}
 fC_L V_{DD} 2 .
 (V_{DD}) pd 가 가 ,
 , V_{DL} < V/{(e - 1)(1 -)} , 10a
 (V_{DD}) pd ,
 . , (I)
 .
 , 9a (19) . ,
 .
 (14) 7a 7c 9b 9b p MISFET(5)
 (19) . 9a 9b
 p MISFET(5) pn
 .

, 11a 11b (20)
 (25) . 11a , 가 (23) (24)
 / (16, 17)
 V_{DD} 0V . ,
 (19) .
 , 11b (23, 24) / ,
 / (23, 24) .
 , 9a V_{DD} , 12
 . p n
 (13) , 12
 (13) n MISFET , npn
 (12) , (18) .
 , 12 (20) p MISFET(17) MISFET(16)
 (21) . (21)
 .
 (14) 가 ,
 V .
 , (V_{DD}) V 13a V_{DD} (V_{B2})
 (21) , n MISFET(4) 가 . 13a
 (21) V_{DD} V_{B2} , V_{B1}
 (7) (21) n MISFET(4) (19) . ,
 n MISFET(4) , V_{B2} V_{B1} .
 (251) 17
 .
 13 16 (19) 가 , (V_{DD})
 (19) (51)가 . (V_{DD}) p (4) ,
 가 . ,
 .
 MISFET MISFET V_{B2} , MISFET
 V_{sub} 가 , 13a
 V_{B2} V_{DD} ,
 ,
 13a V_{DD} n MISFET(4) (19) () (5') ,
 / (one - shot)
 , 13b
 ,
 (19) 가 V_{B1} V_{DD} 가
 (V_{DD}) 가 V_{DD} .

13a , NAND NOR,

8 - 204140 , .

(21) 14a 14b . p MI
 SFET (19) V_{sub} 가 V_{DD} 0V가
 , 가 0V V_{thp} V_{DD} 가 V_{sub} 가 $(V_{DD} - V_{thp})$ 가 .
 (5)가 on off가 (V_{sub}) $(V_{DD} - V_{thp})$, V_{sub} (V_{DD})
 V_{thp} 가 , (21) (19) V_{DD}
 , .

14a 15a . 15a V_{DD} p MISFET(5'')
 , (5'') (V_{thp})
 가 . 15b (5'')가
 , (19) (5'') (5'')가
 가 V_{sub} 가 $(V_{DD} - V_{thp})$, 14
 a .

15a MOS (5'') 16 pn , p M
 ISFET가 , n MISFET MOS .

15a / (21) (7) . (21)
 ,
 V_{a1} (7)
 ,
 (251) V_{sub} V_{a1} V_{sub} V_{a2} . (21, 7)
 (21, 7)가

가, V_{a1} V_{B1} 가 (251) V_{a1} V_{sub} V_{a2} V_{B2} , n M
 ISFET V_{thn} 17 n MISFET V_{GA} ,
 $V_{GA} - V_{thn} < V_{B1}$ 가 . V_{GA}
 0V V_{DD} $V_{B1} > V_{thn}$ V_{B1} .
 V_{B1} V_{GA} 0V 가 가 .

15a (7)
 15b V_{a1} V_{B1} 0V 가 (V_{B3}), (2
 51) (21)
 V_{a2} V_{B2} 0V 가 (V_{B4}), V_{sub} (V_{B1}, V_{a2}) 가 , 15b 가
 (251) .

MISFET 가 17
 ,
 0V V_{DD} , p MISFET(5) (V_{thp}) $V_{B4} - V_{DD} < V_{thp} < V_{B2}$,
 n MISFET(4) (V_{thn}) $-V_{B3} < V_{thn} < V_{DD} - V_{B1}$.

MISFET

0V

 V_{DD}

MISFET

17 n MISFET 가 p MISFET 가
n MISFET 가 p MISFET 가

MOSFET

 V_{BSS} V_{BSa} N_A
(電氣素)

q

V

6

$$\Delta V = (2\epsilon_s q N_A)^{0.5} (t_i / \epsilon_i) \{ (2\phi_F - V_{BSS})^{0.5} - (2\phi_F - V_{BSa})^{0.5} \}$$

$1 \times 10^{18} \text{ cm}^{-3}$ MISFET $V_{BSS} = -1V$ $V_{BSa} = 0V$ V_{DD}
0.43V 가 =0.8, $V_1 = 0.8 V_{DD}$ n MOSFET e 2 V_{DD}
< $V / \{ (e - 1)(1 -) \}$ 2.15V , VDD pd , $V = 0.2[V]$, $V_1 = 0.8$
 $V_{DD, e} = 2$ $V_{DD} = 0.5V$ $V_{DD} = 0.4V$ $V_{DD} = 0.4V$ $CLVD_D / \{ (1 -)V_{DD} + V \}$ e
, MISFET MISFET

MOSFET

$$(2\epsilon_s q N_A)^{0.5} (t_i / \epsilon_i) 0.1 \text{ } 1[V^{0.5}]$$

9a

12

 (V_{DD})

가

, VDD

, pd

e 2

$$V_{DD} < V / (1 -)$$

MOSFET

$$1 \times 10^{19} \text{ cm}^{-3}$$

=6nm
6V

0V

6V

0.6 -3V

 $V t_i$

$$V_{DD} < V / (1 -)$$

가 , 가
가 e가 2 1 가 V_{DD} V_{DD} pd 가
}가 $V / \{ (e - 1)(1 -) \}$

(2)

가

CMOS

(pd)

. pd

(MOS

(武石喜幸, 原央監修), p.44).

 (V_{inv})
CMOS

18a

1

CMOS

(

)

 (V_{inv}) V_{inv}

1 n MISFET(4) p MISFET(5)

가

18a

 V_{inv} $V_{DD} / 2$ 가

18b

i, ET, 0 MISFET, 0V V_{DD} , V_{inv} , n MISFET, V_{DD} , $V_{DD}/2$ 가, $V_{DD}/2$ 가, pd, pd.

7

$$\tau_{pd} = (2V_{inv} - V_{DD})/2a_i + V_{DD}/2a_c$$

7, 0V V_{DD} , V_{inv} , 0V 가, 가, V_{DD} , 0V, V_{inv} , V_{DD} 가.

19a, 19a, n MISFET(4), p MISFET(5), (6), n MISFET(4), MISFET(4), p MISFET(5), 0V, p MISFET(5), V_{DD} , D.

19a, n MISFET(4), p MISFET(5), (10), (10)가, (C_W) , (RC_W) 가, 0V, V_{DD} , (10), (R), (10)가.

, 19a, 19b, 21a, 22a, 22b

Si

(V_{DD}) 0.6V, (C_W) MISFET, $1\mu m$, 1, 100fF, pd 가, 10, 100ps, (10), MISFET, $1\mu m$, 100.

, 20, 19a, (V_{in}) , n MISFET(4), (V_{sub}) , (V_{out}) , 0V, V_{DD} 가, (V_{th}) , n MISFET(4), C_g , n MISFET(4), p, C_{tot} , n MISFET(4), C_g/C_{tot} , V_{DD} 가, V_{DD} .

, p MISFET(5), (V_{inv}) , 0V 가, V_{DD} , (V_{in}) , V_{inv} , (10), V_{sub} 가 V_{out} , 0V가, $V_{sub} = 0V$, $V_{sub} = V_{DD}$, V_{DD} , 0V, (V_{inv}) .

, 19a (10) n MISFET(4) p MISFET(5) ,
 19b (10) , 1
 9b (i) 0V V_{DD} , p MISFET
 (5) n MISFET(4) V_{DD} ,
 n MISFET(4) (V_{inv}) V_{sub} ,
 0V , V_{DD} .
 MISFET (6 -
 085262).

가 .

21a . 21a p MISFET(5) (1
 0) , n MISFET(4) (7) .
 n MISFET(4) (10)
 , p MISFET(5) (7) , 1 (7)
 , 0V V_{DD} .

21b (10, 10'') , (10) n MISFE
 T(4) p MISFET(5) 가
 V_{DD} , V_{DD} p MISFET(5) pn

, 21c 3, 4 MISFET(26, 28) . , n MISFET(4)
 3 MISFET(26) , MISFET(26)
 , MISFET(26) V_{th} MISFET(26) (27)
 (V_1) 가 MISFET(26) (R) , MISFET(26)가
 (C_W) (RC_W) 가 0V V_{DD} MISFET(4 5)

가 4 MISFET(28) p MISFET(5) , MISFET(28)
 , MISFET(28) (29) $V_{DD} - M$
 ISFET(28) 가 .

MISFET(26) (V_{out}) ($V_1 - V_{th}$) , V_{su}
 b (V_{DD}) ($V_1 - V_{th}$) , (V_{DD})
 . 21c p MISFET(5), p MISFET(28) 가

, 22a 2 NAND , 22b 2 NOR 21a 가
 , 22a (10) , 22b (10)

, 19a 23 . 23
 Si p (31) n (32)
 (40) B P 가
 (41) .

3, 36) , As B (33, 36) CoSi TiSi (37)
 , n MISFET " 33 " W, Ti, TiN, Al Cu (31) n
 (32) (39) p MISFET " 36" (38) .

(33, 36)
 As B 가 가 (34, 35) 가
 가 (37) 가 (39) 가 (34, 35)
 , (37) 가 (34) (33)
 가 (35) (36) .

(37) 가 (35) (36)
 , 35 36 pn .

24a 24c .

10^{15} cm^{-2} 10^{15} cm^{-3} p (32) 10^{12} 10^{15} cm^{-2} p (31) 10^1
 5 cm^{-3} 10^{19} cm^{-3} 100eV 1000eV , 0.01 0.05 μm Si 10^1
 , 가 0.03 0.5 μm .

(38) (38) . 0.1 2 μm
 (38) $\pm 0.3 \mu\text{m}$, 가 (etchback) 0.1 4 μm . ,
 , n (32) , , p (31) .

1 20nm (40) .

(41) 가 ,
 (低) .

24a .

24b (42) , n
 33) n (35) 가 1 100eV 10^{13} 10^{16} cm^{-2} n (33) " 33" " 35" " 33" " 35"
 (42) ,
 p BF₂, 가 1 100eV, 10^{13} 10^{16} cm^{-2} p (36) p (34) " 35" " 36" " 33" " 34" 가
 , 0nm 0.3 μm .

, “ 33 ” “ 36 ”
 (43) 0.01 1 μ m , (34, 35) (43)
 , Co Ti 0.01 0.3 μ m , 400
 CoSi TiSi , 24c
 .
 , (44) ,
 Al W ,
 23 (37) 25a
 (44) (33, 36) ,
 (34, 35) . 25a CMOS 가
 ,
 , (42) 25b
 가 . 0.05 μ m 1 μ m , (33, 36)
 .
 (38)
 .
 (3)
 n (V_{th}) i V_{th} = 2 ϕ_F + V_{FB} - Q_Bt_i/ i (- Q_B)
 . p
 n p 가 가
 가 , 가 가 가 .
 .
 26a MISFET
 , 26a (45) p (31) n MISFE
 T , 0V . (46) n (32) p MISFET
 , p , V_{DD} , p (31) n (32) p (47)
 pn p (31) n (32)
 (32) n (35) V_{SS} (8) , p (31) p (34) V_{BB} (7)
 .
 p (46), n (32), p (47) pnp (Q1) , n (32), p
 (47), n (45) npn (Q2) . 가
 , 26b 가 .
 , I_{CO} , I_{W1} n (32) V_{SS}
 (8) , I_{S1} V_{BB} (7) p (31) , (V_{DD}) 가
 , I_H .

8

$$I_H = (I_{co}^{-\alpha_{FP}} \cdot I_{W1}^{-\alpha_{FN}} \cdot I_{S1}) / (\alpha_{FP} + \alpha_{FN} - 1)$$

(小柳光正 「 , 1987) p.182 - 183)

(Q1)

Q2

, $F_P > F_N > 0$.

8

(I_H)

가 (32)

, p (47)

8

$F_P > F_N$

$I_{s1}=0$

, $I_{w1}=$

$I_0 (> 0)$

$I_{w1}=0$

, $I_{s1}=I_0 (> 0)$

I_H

가

27a

27b

27b

pn

(Q1)

(49)

가

(49)

가 (V_{DD})

(49)

가

, n

Si

(V_{SF})

0.3 0.4V

, Si

pn

(0.6V)

n

(32)

V_{DD}

($V_{DD} - V_{SF}$)

p

MISFET

(46)

pn

n

가

pn

27a

27b

26a

, n

(32)

p

MISFET

V_{DD}

p

(46)

(48) n

(32)

, n

(32)

(48) n

((46))

n

(48)

W, TiSi, TiN, Ti, WSi, CoSi, Al

, n (32)

10^{18} cm^{-3}

TiSi CoSi

(49)

가

28b

pn

(built - in pote

ntial)

pn

Ge

pn

가

10^{18} cm^{-3}

(band gap narrowing)

pn

28a

28b

28a

26a

n (32)

p

MISFET

V_{DD}

p

(46)

n (32)

Ge가 10^{18}

10^{22} cm^{-3}

가

SiGe (51)

()

, (46)

(46)

(51)

, p (51)

n (32)

n

(51)

(V_{SF})

SiGe

Si

Si pn

(0.6V)

, N

(32)

V_{DD}

($V_{DD} - V_{SF}$)

p MISFET

(46)

, 36 2 (8) ,
 (7) , 1 (7) .
 2 (8) ,

, n (32) n (47) p (47) p (31)
 가 p (31) n (32) CMOS

1 4 (38, 40, 43) , 30keV 가

, . ,
 , . ,
 , , ,

1 4 (38) LOCOS
 (Recessed) LOCOS LOCOS ,

1 4 p Si n Si GaAs , InP

, (39) (41) , (porous silicon),
 , SiGe , GaAs, W, Ta, Ti, Hf, Co, Pt, Pd

(5)

37 5 , GST 가 . 37 , n MISFET(Q
 2) SOI(silicon - On - Insulator)

, 37 , Q2 n MISFET (Q3)
 . Q3 (106) , Q3 (107) (104)
 107) (107) 2 , (104)
 . (104) (105)

(105) (113) (103) , (103) Q3
 (103) 가 V_{active} 가 ,
 , standby 가
 . (103) /

(Q3) (Q2) 가 , Q3 Q2
 Q3 Q2

, Q2, Q1, Q2, Q1 MISFET, p MISFET가, Q1, Q2 CMOS

, 38 (105)가 0V V_{DD} ($V_{standby}$)

db) 0V, (V_{active}) V_{DD} (104), ($V_{standby2}$)

(107) $V_{active2}$ $V_{standby2}$ V_{DD} - $3V_{DD}$ 0V, 0V 0.25V

가

39 Q2, Q3, Q2, Q3 V_{th1} , V_{th2} , (W_1, W_2) W_2

39 n MISFET(Q2) n

MISFET(Q3), Q3 (106), Q

3 (107) (107) (104) (103) /

V_{DD} 가, 0V가

(S.Mutoh 1 - V Power Supply High - Speed Digital Circuit Technology with Multi - Threshold Voltage CMOS IEEE J.Solid - State Circuits. vol.30, no.8, pp.847 - 854, Aug.1995)

Q3 (107) (104), (V_{th2}) Q2 (V_{th1})

40 $V_{th1} = 0.2V_{DD}$, Q2, Q3 100mV/decade, Q2 (W_2/W_1) CMOS

Q1, Q2 10% V_{th1} 0.1 0.3 V_{DD} 0.2 V_{DD}

40 가 (V_{DD}) Q3 (V_{th2}), Q2 Q3

Q3 Q2 가 Q3 95% 40 1/1000

40, Q3

(W_2/W_1) 45, Q2 Q3가

40, Q3 (W_2/W_1)가 70

1/10000

37 Q2 GST, (V_{DD}) 가, 0V

0V가, 0V가, 0V, Q2

ON/OFF 가

39 Q3 Q3

가 , , Q3 (W₂/W₁)가 Q2 Q3

Q3 Q3

0.8V_{DD} 1/10000 Q3 0.1V_{DD} Q3 W₂/W₁=20 Q3

40 (Q3) 0V V_{DD} 95%

GST

가 6 Q3

(103) 0V V_{DD} 가 ,

가 , Q3 가 0V V_{DD} , 가 0V V_D

D , Q3 가 V_{DD}

(104) 0V V_{DD} (107) (103)

가 (106, 106')

37 (113) (107)가 가 가

t1 t2

(113)

(V_{standby2}) , V_{active2} (104)

t2) 가 (t3) 가 (

(T.Kuroda " A 0.9V 150MHz 10mW 4mm² 2D Discrete Cosine Transform Core Processor with Variable Threshold - Voltage Scheme" IEEE Journal of Solid State Circuits, vol. 31 NO.11, pp.1770 - 1779 Nov. 1996.)

t2 1 μS , t3 100 μS 37 (113)

t4 t3 Q3

(113) 41a 41c 41a

2 (t1) 41b

41a RC((108), (109))

41c (105) (103)가 V_{active} V_{standby} 가

t4 V_{standby} V_{active} 가 t1

1, 42 1 1 Q1, Q
 1 (102) GST,
 , Q1 Q2
 (S. Thompson, 1997 Symposium on VLSI Technology Digest of Technical Papers, p.
 69)

Q1
 , Q1 Q2
 Q2
 가 1 가
 , Q1 가
 가 Q2

43 2 2 1
 Q2 Q2', Q2" Q2 Q2', Q2"
 GST IN1, IN2, IN3 3 NOR
 1 Q1 GST 가 Q1 Q2 Q1
 Pn

44 2 3 NOR (n
) NOR 1
 가 p MISFET(Q1) n 가 , Q2

44 Q1, Q1', Q1" 3 가
 Q1 MISFET 3 가 , p MISFET n
 NOR 1.3 ~2 p MISFET 가 , 44
 p MISFET 가 43 2

45 43 44 (1) , (V_{DD})
 45 , 43 , 44
 (Q2) 0.3V, (Q2) 0.2V_{DD} 가
 Q2
 45 , 43 0.5V 0.7V ,
 가

46 3 p MISFET(Q1)
 p MISFET(Q4) , Q4 (106') , Q
 4 (107') (107') 2
 (104') (104')
 (105) , Q4 (114) (103)

(103) 가 V_{active} 가 , ,
 $V_{standby}$ 가 . ,
 (103) / .

(Q4) (Q1) 가 , Q4 Q1

3 Q1 Q2 Q3 Q4
 . , p MISFET(Q1)
 (Q4) Q1 .

47 1 p (133) 47 , “ 13
 0 ” n MISFET , “ 132 ” p MISFET GST
 , , 47 , “ 120 ” , 1 p (133)
 , (120) “ 121 ” p SiO_2 SiN
 , (121) (122)
 p (123) n 0.01 $2\mu m$ (124)
 (131) , (132) (131) (132) (123, 124) GST

GST p (121) n (124) , n
 (122) p (123) , GST p (122) n (124)
 121) p (123) , n (122) n (124)
 GST p (121) n (122)
 가 .

, n MISFET(130) p (121) p (123) ,
 MISFET(130) p , 2 MISFET
 가 . , n (122) p (124)
 , p MISFET n , MISF
 ET 가 .

, MISFET (128) (127),
 . (129)
 , n MISFET(130, 131) . n (125) (127)
 , p MISFET(132) . p (126) (127)
 , p (123) 가 n p (121)
 p (126 ') , n (124)
 가 n (122) n (125 ') ,

GST n (124) n (1
 24) , n (124)
 가 .

, (123) p (133) p (133) n (124)
 GST (131)가 (121) n (124) 0.
 1 1V , 가 (122) (124) pn , .
 .
 (133) , p (123) n (124)
 가 . , p (123) n (124)
 , , , .
 , p n p .
 , 48 51 .
 , 10^{15} cm^{-3} p (133)
 , 0.01 0.05 μm Si . , 가
 0.03 0.5 μm .
 , (120) . 0.1 2 μm
 0.1 4 μm , (133) $\pm 0.3\mu\text{m}$ 가
 .
 , 0.01 0.05 μm Si (134) .
 0 2000eV, 10^{13} 10^{16} cm^{-2} p (123) 가 3
 p , (120) p (120)
 .
 , 가 50 2000eV, 10^{13} 10^{16} cm^{-2} p
 n (124) p (123) .
 1가 2가 , 가 48
 가 .
 , 49 , (135)
 , 가 30 2000eV, 10^{13} 10^{16} cm^{-2} n (124')
 (120) n , p (123) n (124 124') p (133) 가 .
 700 1100 , 10 60 가 .
 , (135) (灰化) , 50 , (135)
 p (121) , p (121) n (124) 10^{16} cm^{-2} (120)
 가 . GST
 . p (121) p (123) n .

n MISFET GST (131) , n MISFET
 (130) p (123) 가
 p (121) .
 , (135) , 51 (135)
 , 가 30 500eV, 10^{13} 10^{16} cm^{-2}
 n (122) , n (122) p (123) (120)
 가 GST
 . n (122) n (124) p (123) .
 p MISFET GST (132) , p MISFET
 n (124) 가 n (122)
 . , 47 n (122) p MISFET
 가 , n (122) (133) 가
 .
 n GST p n 4 p
 , p (133) 가 , 가
 , GST , 가 가
 , .
 가 GST CMOS
 가 , ,
 700 1100 , 10 60 가 (135)
 (128) (134) , 3 100nm
 (127) , (129)
 10 300nm .
 , 가
 (129) 1 300nm ,
 . (129) ,
 .
 , n , ,
 가 1 30eV, 10^{13} 10^{16} cm^{-2} n (125) n (125 ')
 . , p BF₂,
 가 1 30eV, 10^{13} 10^{16} cm^{-2} p (126) p (126 ')
 47 .

Co Ti 0.01 0.3 μm , 600
 CoSi TiSi ,
 Al W ,
 0.1 μm , 0.2 μm , (133) $1 \times 10^{15} \text{ cm}^{-3}$, p, n (124) 0.5 μm , 가 $2 \times 10^{17} \text{ cm}^{-3}$ (12
 3) , 0.25 μm , 0.1 μm 가 , , p (12
 가 $5 \times 10^{17} \text{ cm}^{-3}$, 0.07 μm 가
 n (124 ') 0.25 μm , 가 $5 \times 10^{17} \text{ cm}^{-3}$,
 0.09 μm 가
 , p (121) , 0.13 μm , 가 $1 \times 10^{18} \text{ cm}^{-3}$,
 0.05 μm 가 , n (122) 0.13 μm ,
 가 $1 \times 10^{18} \text{ cm}^{-3}$, 0.05 μm 가
 , n (125) n (122) n (125 ')
 0.01 μm , 가 $2 \times 10^{20} \text{ cm}^{-3}$, 가 $1 \times 10^{18} \text{ cm}^{-3}$ 0.05
 μm 가 , p (126) n (121) p (126 ') ,
 BF₂ 0.01 μm , 가 $2 \times 10^{20} \text{ cm}^{-3}$, 가 $1 \times 10^{18} \text{ cm}^{-3}$
 0.05 μm 가
 n (125) 0V, p (121) 0.6V, n (124) 0.6V, p (123) 0V, n (122) 0V, p (126) 0.6V 가 n (125)
 $10^{-7} \text{ A}/\mu\text{m}^2$, p (126) $10^{-7} \text{ A}/\mu\text{m}^2$,
 (V_{DD}) 0.6V
 , npn pnp n (125) 0V
 0.6V 가 , p 0V 0.6V 가 n
 (125) 0V, p (126) 0.6V 가
 GST , 46 Q3, Q4
 0V 0.6V , GST
 GST
 (6)
 52 6 (Q3, Q4) 가 5 46 ,
 52 , Q3 (143) (140) (V_{DD})
 (142) , (142) 52 (141)
 (142) (143)가 , (103) (140) (143)가

, 52 Q4 (143') (V_{DD}) (1
40') (142') , (142') 52
0V (141') (103) (141) (114)
(140') (143')가 (142') (143')가 ,

Q3, Q4 가 , Q3 Q4
46 Q3 Q4
5 가 Q3 Q4
5 0V 가 V_{DD} 가 Q4
,
(104, 104') ,

Q3, Q4 가
MISFET 가 53a
53c .

53a , Q3 , 0.1 5V V_{DD} 6 Q3
가 , 0V , (V_{sub})
V , (V_G) 가 , 53b , 0
(V_G) 53c (I_D)

n MISFET 가
53c ,
가 가
current)가 . GIDL (Gate - Induced Drain Leakage c
53c ,
. GIDL (J.Chen, T.Y.Chan, I.C.Chen, P.K.Ko and C.Hu, " Sub
breakdown Drain Leakage Current in MOSFET ", IEEE Electron Device Letters, vol,EDL - 8.No.11, Novemb
er, pp.515 - 517, 1987)

GIDL 가 , 가 53c
53b 0V
(I_{D2}) , 가
가 GIDL
. 53c
0V 가 GIDL I_{D2}
I_{D1}
(7)

54 7 5 6 5 43 .

54 , Q2 Q1 (147) p MISFET(Q5) n MISFET(Q6)
 , Q5 , Q6 (146) (146) 2
 , (104') (104'')
 (105)

, Q6 (145) (145) 2
 (104''') (104''')
 (105) , Q5 Q6

(前段) NOR
 147 43 가 ,
 147

5 6 5

Q2 GST , Q5, Q6 GST
 54

, 54 IN1 IN3 가 “H” , V_{DD} , Q2, Q2'
 Q2” (147) V_{DD} , Q2 Q1
 (147) Q3 가 Q5
 가 GST 가 3
 Q5 V_{DD} (147)
 가

, IN1 IN3 가 “L” , 0V , Q2, Q2' Q2”
 가 (147) V_{DD} , Q6 Q6
 가 GST 가 가 (147) 가

55 54 3 OR 55
 “148” GST n MISFET
 IN_x(x=1,2,...n) "148" 56

n MISFET (Q2) n MISFET (Q2 ")
 , n MISFET (Q2 ')
 IN1 IN3 V_{DD} , IN2가 V_{DD} 147 106 가 , AND,
 OR (147) CMOS (149) 55 , (148) 149
 GST 가 가 (149)
 (147) (147) 가
 , (149) 가 NOR NAND (1
 49) (147) 가
 57 , Q3 (148) GST (Q5)가 (148)
 , Q5 , Q3 , Q5 , Q1
 , Q5 , Q1
 가 , (148) Q5가 Q1
 0V V_{DD} (V_{DD}) 0V 가
 , Q1 GST
 ON/OFF
 , 5 6 , Q3
 (Q3) Q3 ,
 , GST
 가 ,
 , 5 2 NOR
 NOR
 5 GST
 CMOS 4 , GST
 , GST
 GST CMOS 가
 ,
 , p n
 p n ,
 , 7 GST 가 가

5 7 (129, 120, 128, 134)

OS LOCOS , , LOCOS LOC

P, SiGe, (133), p-Si, n-Si, SOI, GaAs, In, MISFET, p-MISFET, As, P, Sb, In, B, BF₂.

$$\begin{aligned} & , \quad (125, 126, 125', 126') \quad (127) \\ & , \text{SiGe} \quad , \text{SiGeC} \quad , \text{GaAs, W, Ta, Ti, Hf, Co, Pt, Pd} \end{aligned}$$

가

가 , (pd) 가 ,
가 , ,
 , 가 .

(57)

1.

$$\frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) = \frac{1}{2}$$

MISFET 2

MISFET (V_{ths}) (V_{tha}) ,
$$I_{D,s} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{th})^2$$

2.

1 ,

MISFET가 n 1 V_{DD} , 2 0V .

3.

1 ,

MISFET가 p 1 0V , 2 V_{DD} .

4.

1 ,

가 MISFET .

5.

1 ,

MISFET가 n p MISFET , p MISFET n MISFET .

6.

1 ,

MISFET가 n n MISFET V_{DD} .

7.

1 ,

MISFET가 p n MISFET , n MISFET p MISFET .

8.

1 ,

MISFET가 p p MISFET 0V .

9.

1 ,

MISFET , , n MISFET p MISFET ,

T . p MISFET . 3 MISFET MISFET , n MISFE
4 /

3 4

10.

9 , 가 2 /
, p MISFET n MISFET

11.

9 , p MISFET n MISFET 가

12.

9 ,
1 V_{DD} , 2 0V .

13.

1 , MISFET , (V_{DD}) 1
1 , V_{DD} 2 , / 2 MISFET
1 MISFET , MISFET
MISFET , MISFET
MISFET OV V_{DD} 가 , MISFET .

14.

1 MISFET , 2 , 1 2
MISFET
p MISFET n MISFET , 1 n MISFET
2 p MISFET .

p MISFET n MISFET . MISFET
 , p MISFET n MISFET , / 2
 ,
 .

15.

14 ,

1 0V (V4) , 2 (V3) 0V , (V1) (V2) (V1)
 (V3) , V1
 1 V_{th1} , V
 1 V2 , V3 , V
 V_{th2} , 2 V_{th3} , V4 ,
 , V_{th4} , Vs,
 Vs) Va , (V_{th1} Vs V_{th3} Va) , (V_{th2} Va V_{th1} Va) (V_{th3} Vs V_{th1}

16.

1 2 MISFET 가 ,

1 MISFET , 1 MISFET 2 MISFET
 , 2 MISFET ,

2 MISFET , 2 MISFET V_{ths} 1 MISFET V_{th} , V_{th} V_{ths} 가
 ,

2 MISFET 가 2 , 2 MISFET가
 가 , 가 .

17.

1 3 MISFET 가 ,

1 MISFET 3 MISFET 가 , 1 MISFET 2 MISFET
 ,

1 MISFET 3 MISFET , 3 MISFET 2
 ,
 .

18.

16 ,

1 MISFET ,
 .

19.

16 ,

1 MISFET 2 MISFET .

20.

16 ,

2 MISFET V_{tha} V_{th} V_{tha} 가 .

21.

16 ,

2 MISFET 가 가 2 MISFET 가 가 ,

22.

16 ,

1 MISFET 2 MISFET 3 MISFET ,
3 MISFET 3 MISFET 1 MISFET .

23.

17 ,

1 MISFET ,
.

24.

17 ,

1 MISFET 2 MISFET .

25.

17 ,

2 MISFET V_{tha} V_{th} V_{tha} 가 .

26.

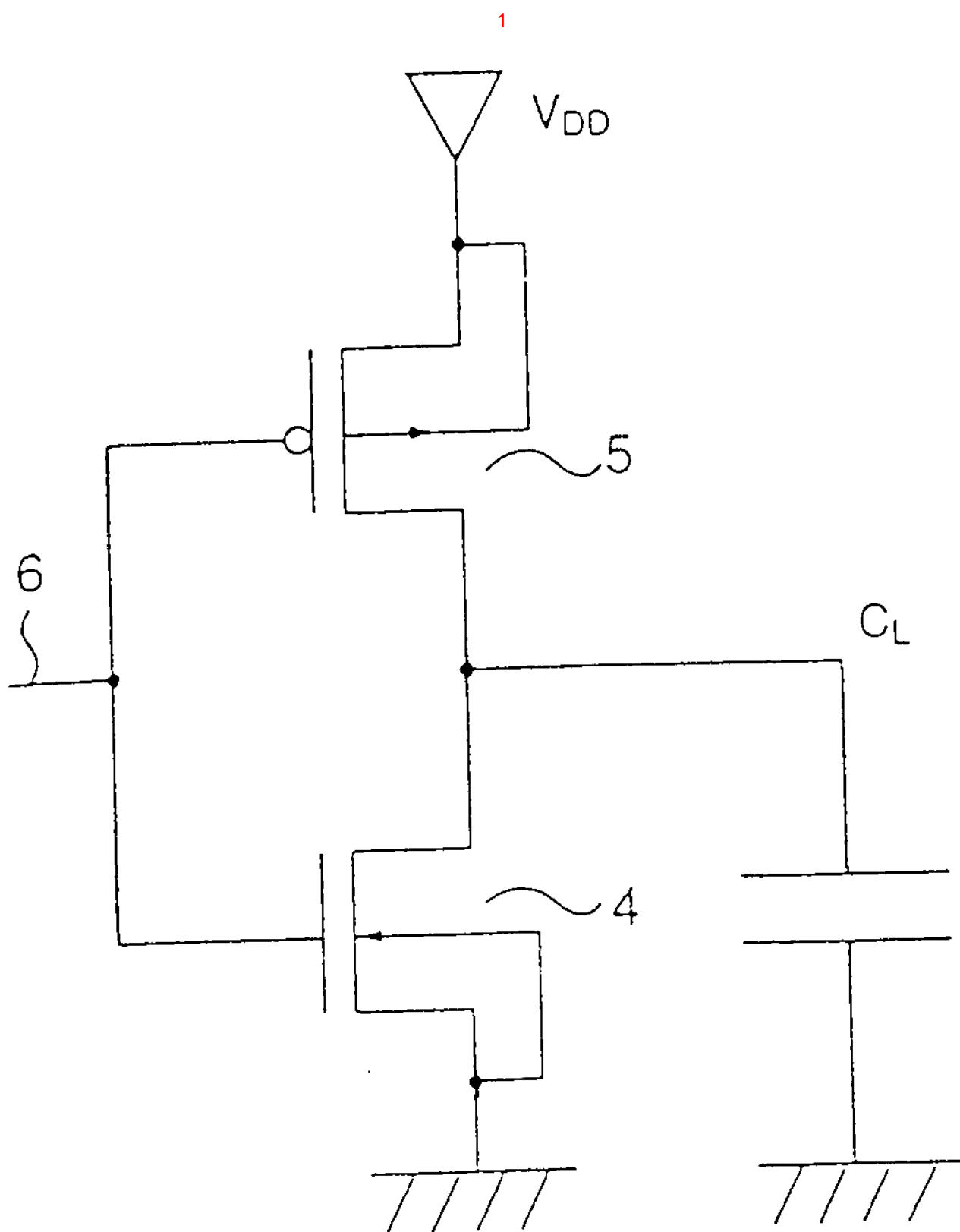
17 ,

2 MISFET 가 가 , 2 MISFET 가 가 ,

27.

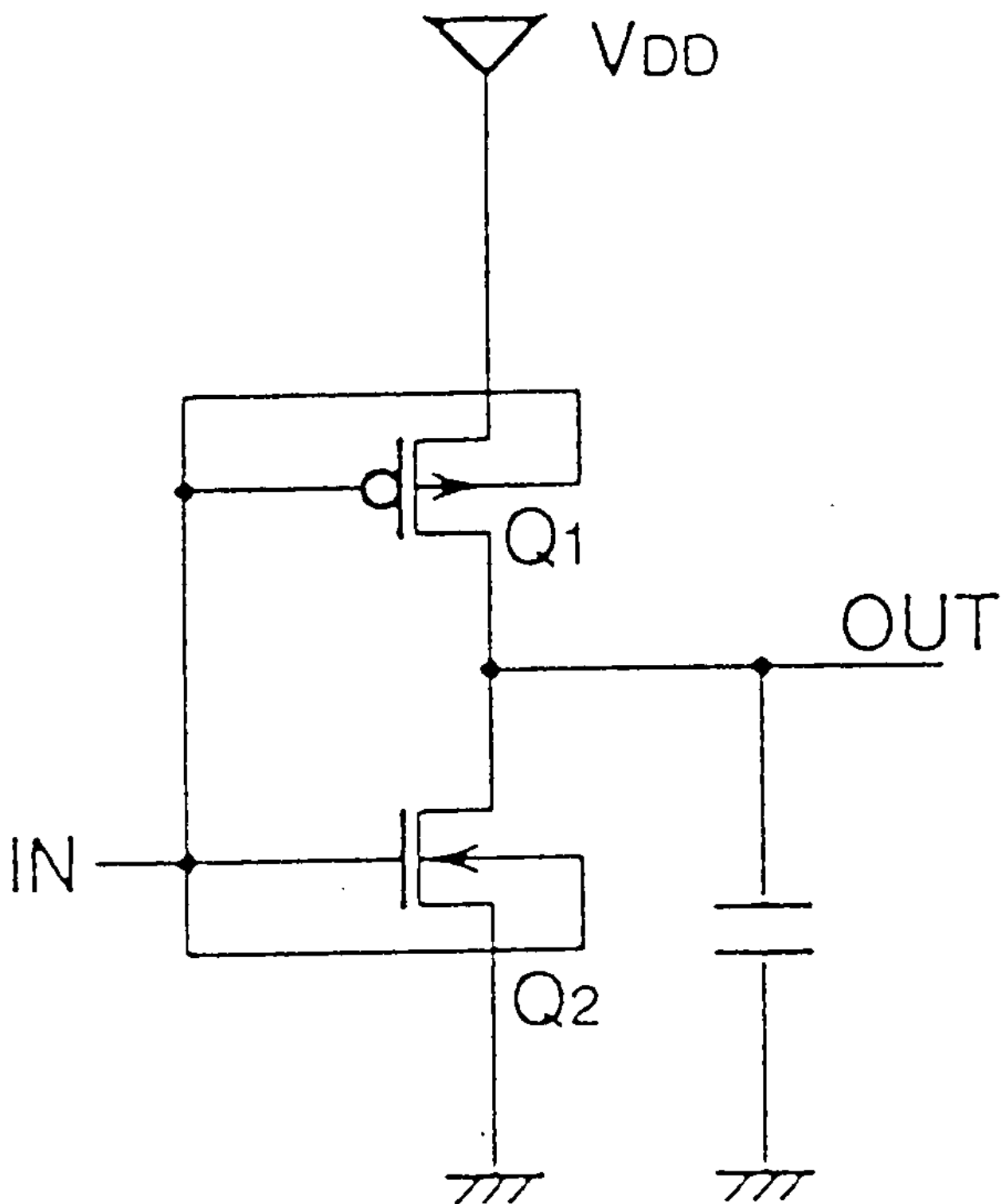
17 ,

1 MISFET 2 MISFET 3 MISFET ,
3 MISFET , 3 MISFET 1 MISFET

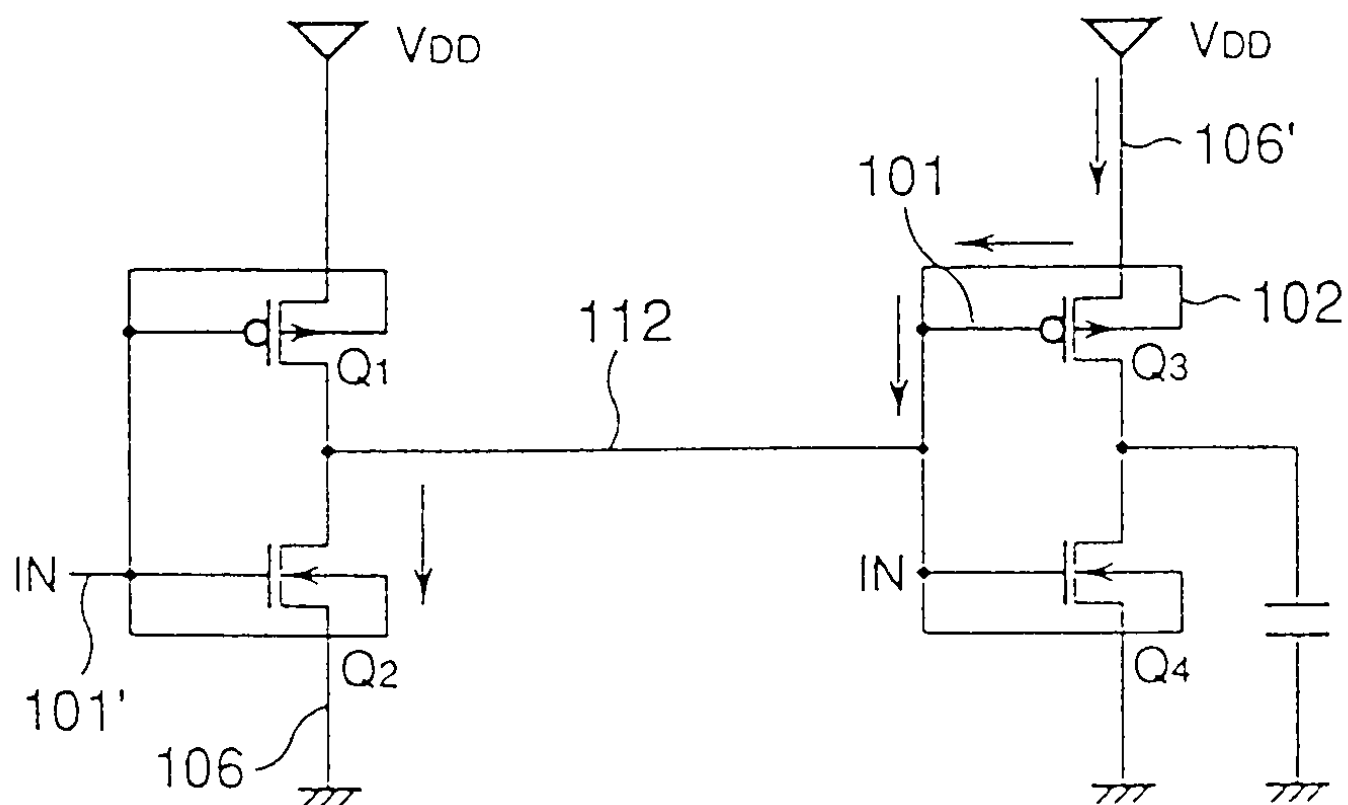


(종래기술)

2

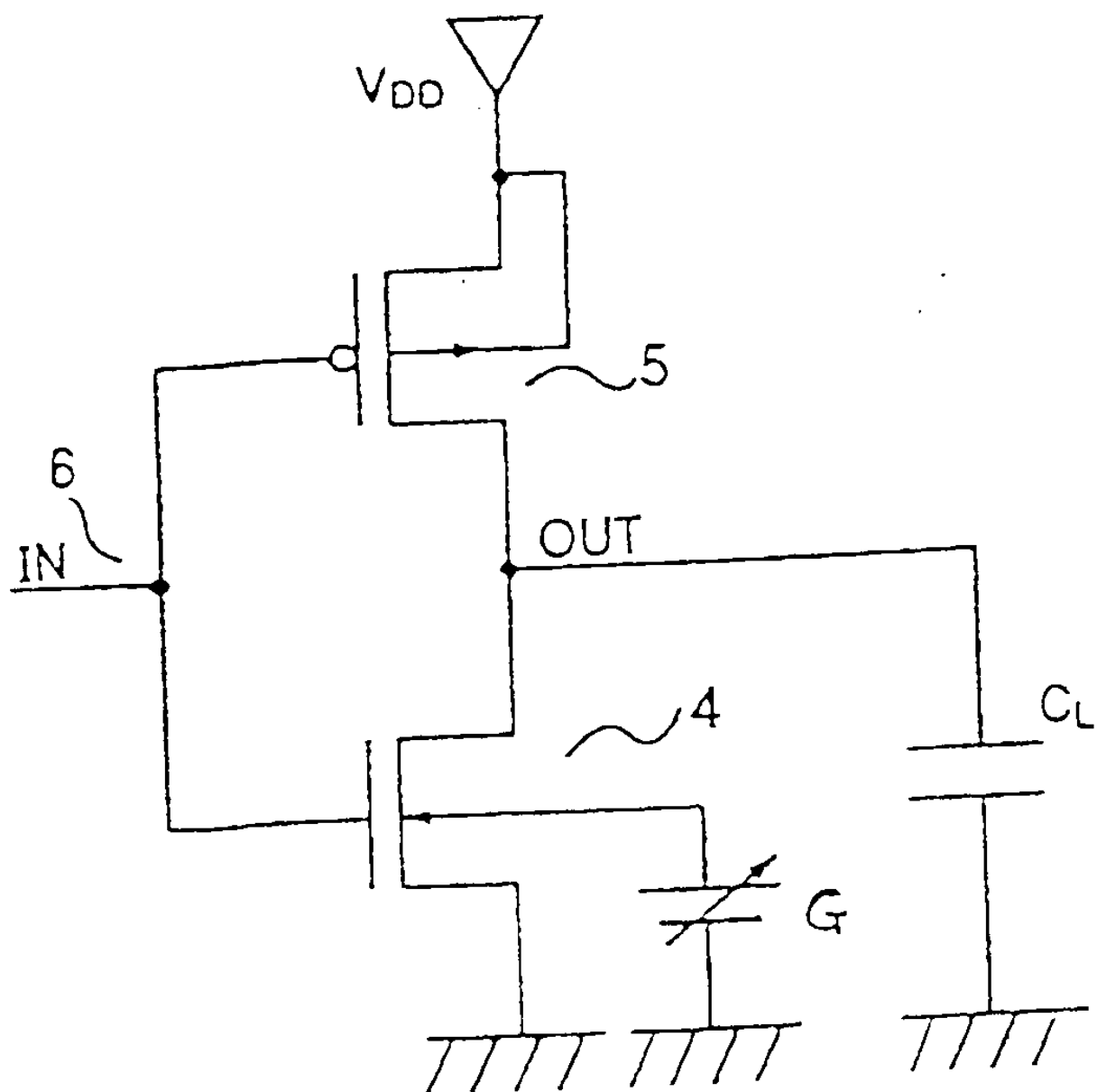


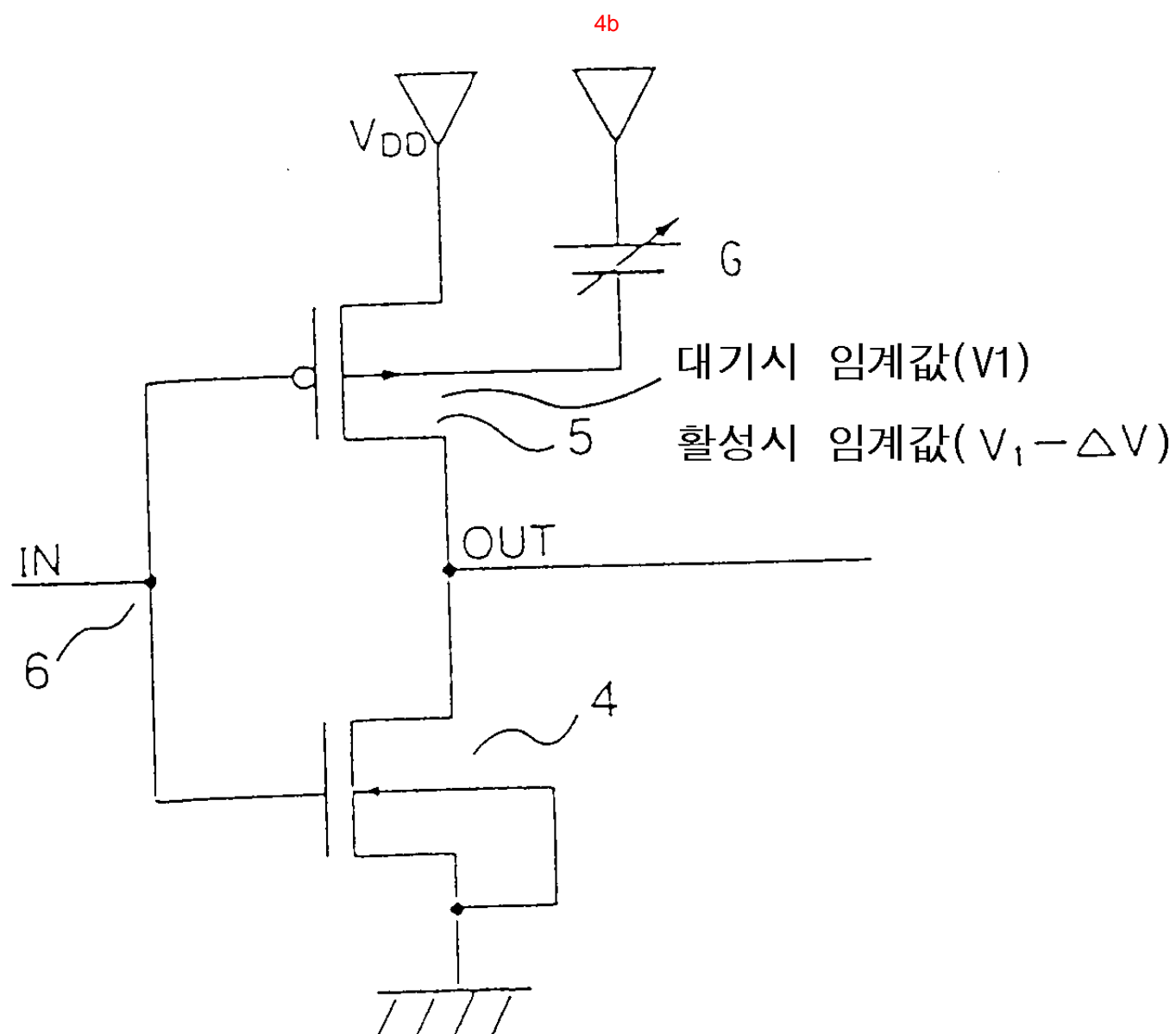
(종래기술)



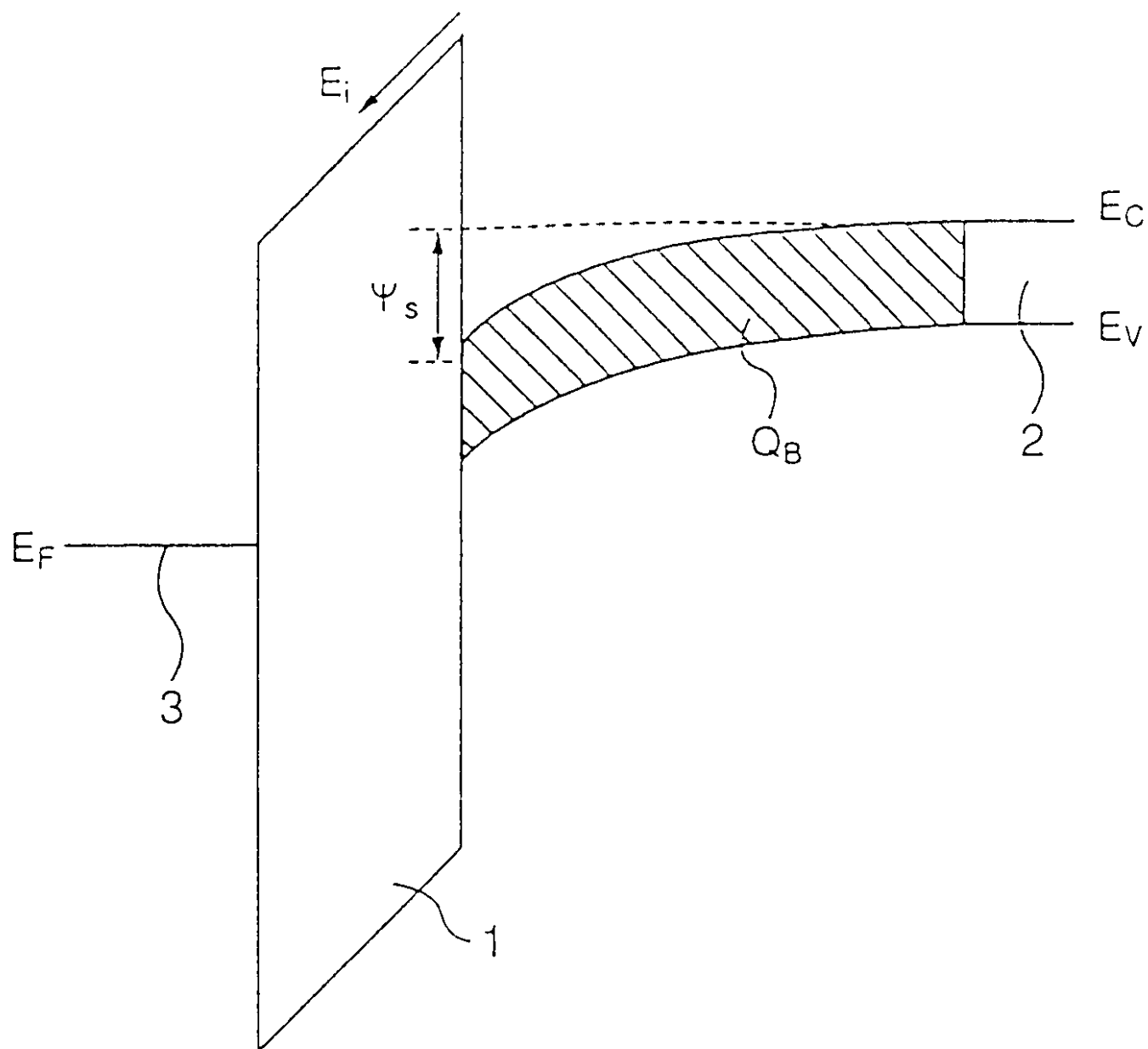
(종래기술)

4a

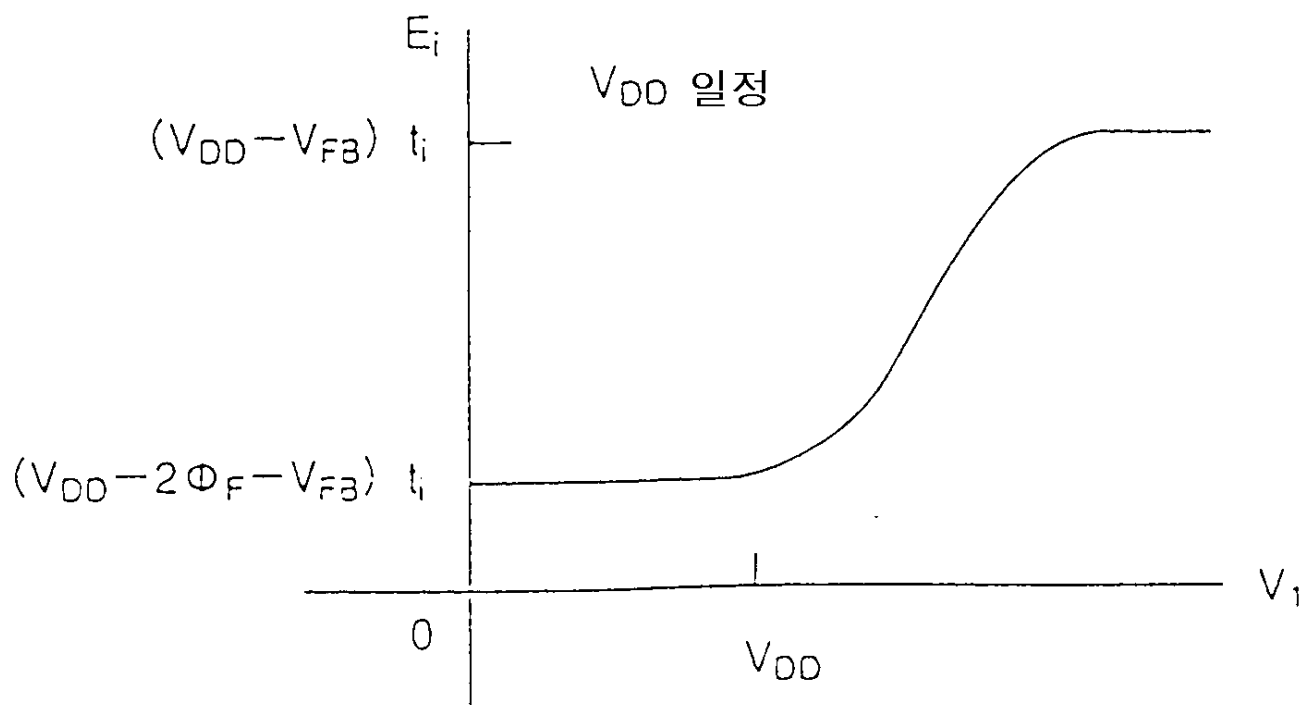


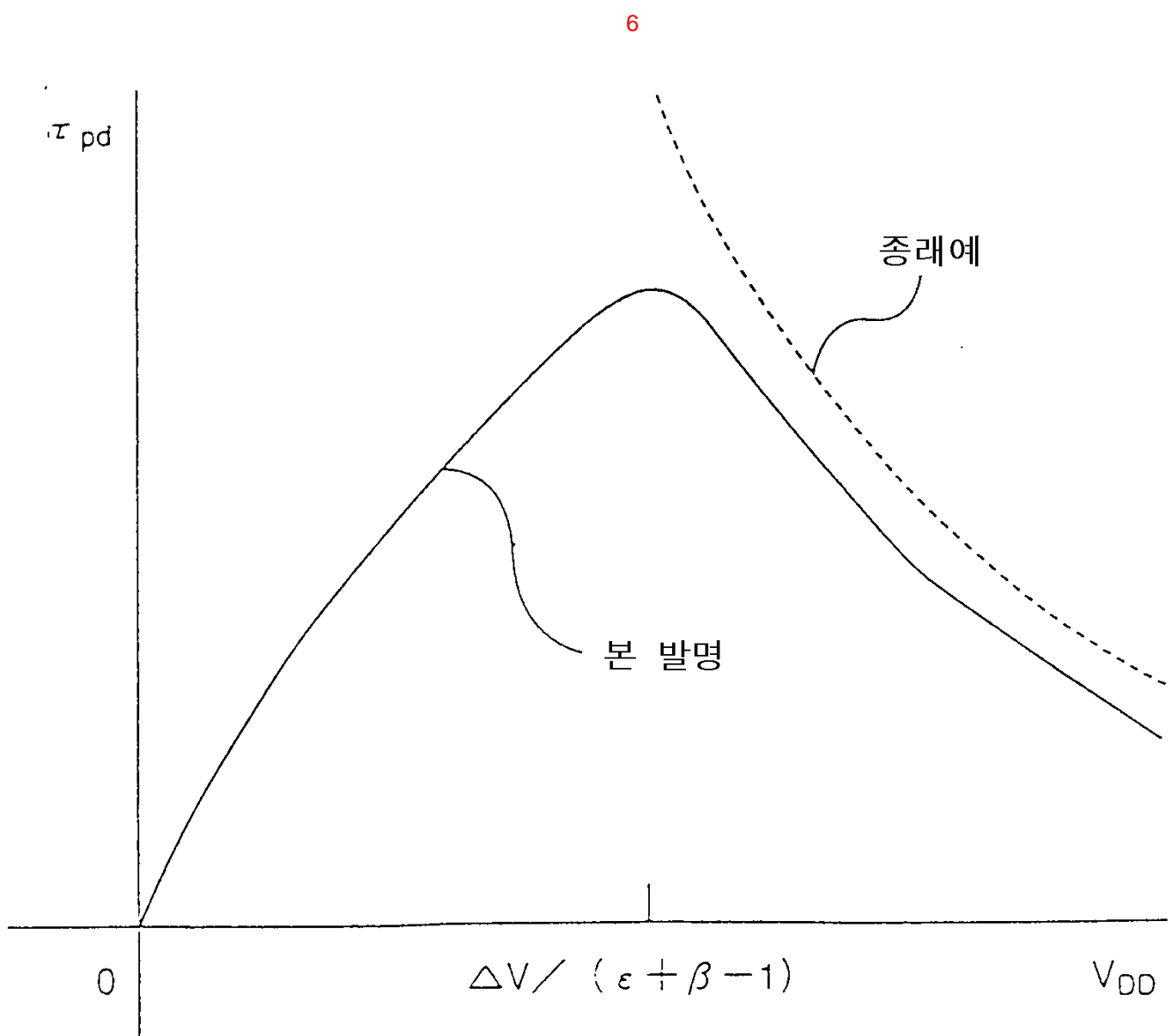


5a

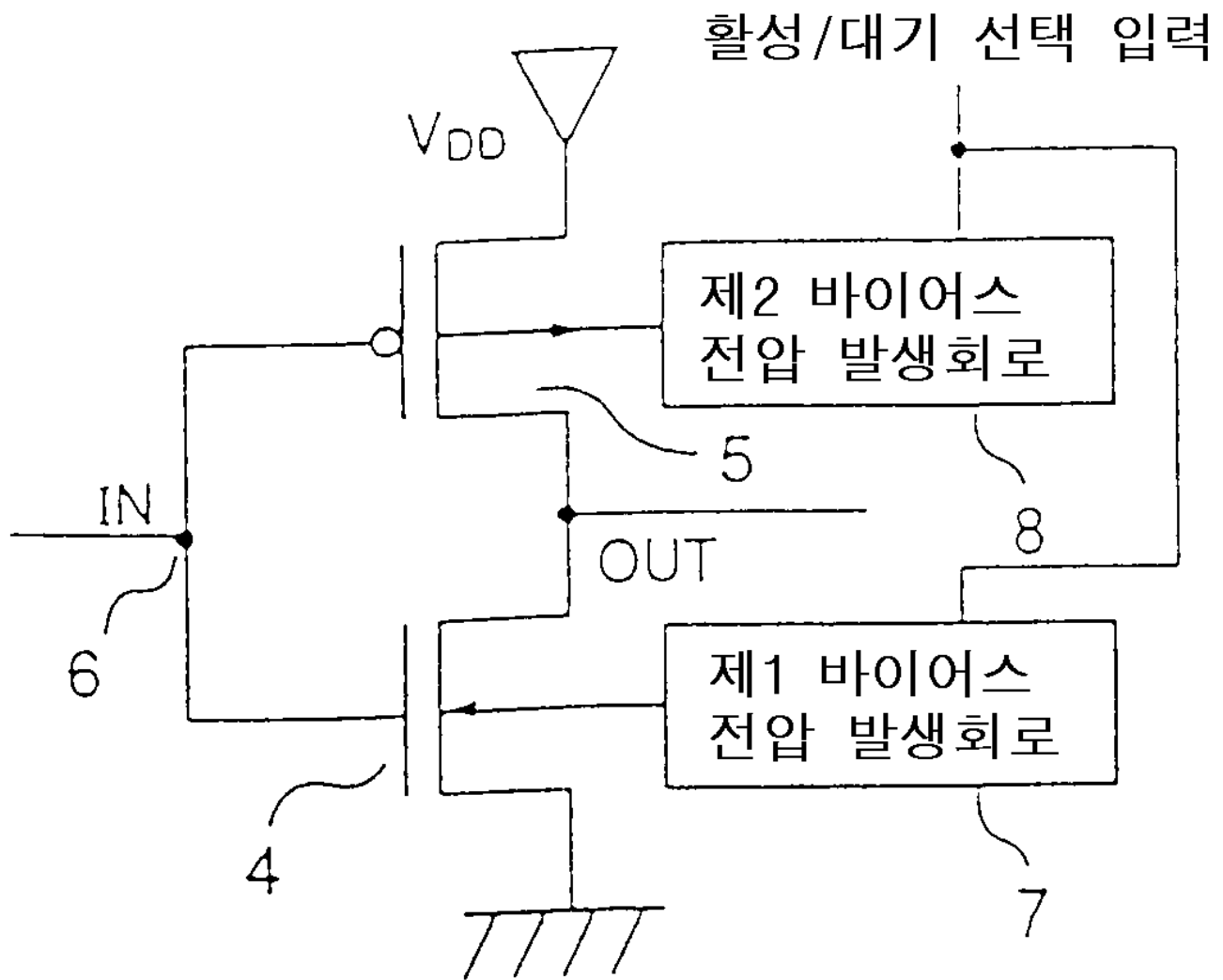


5b

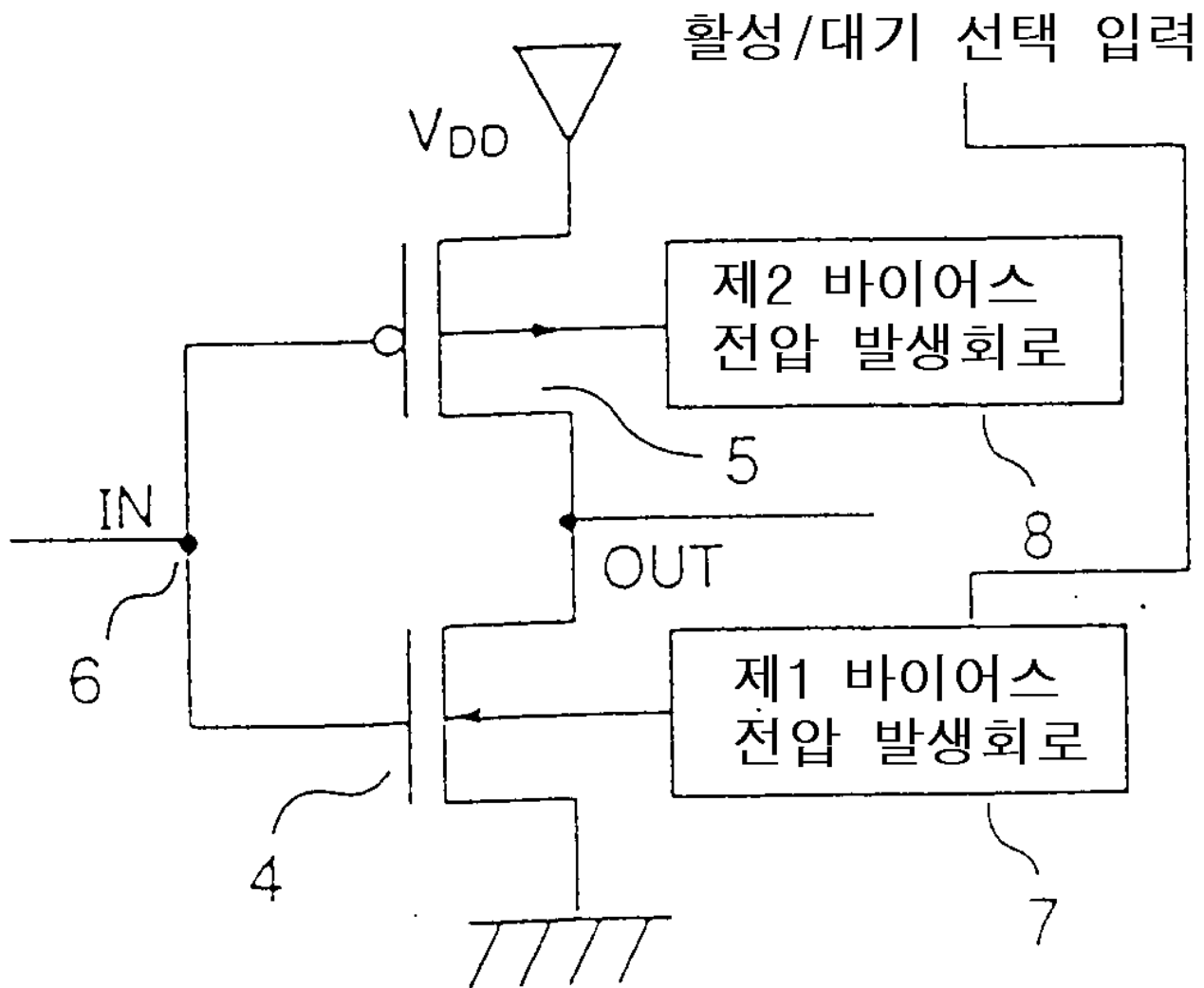




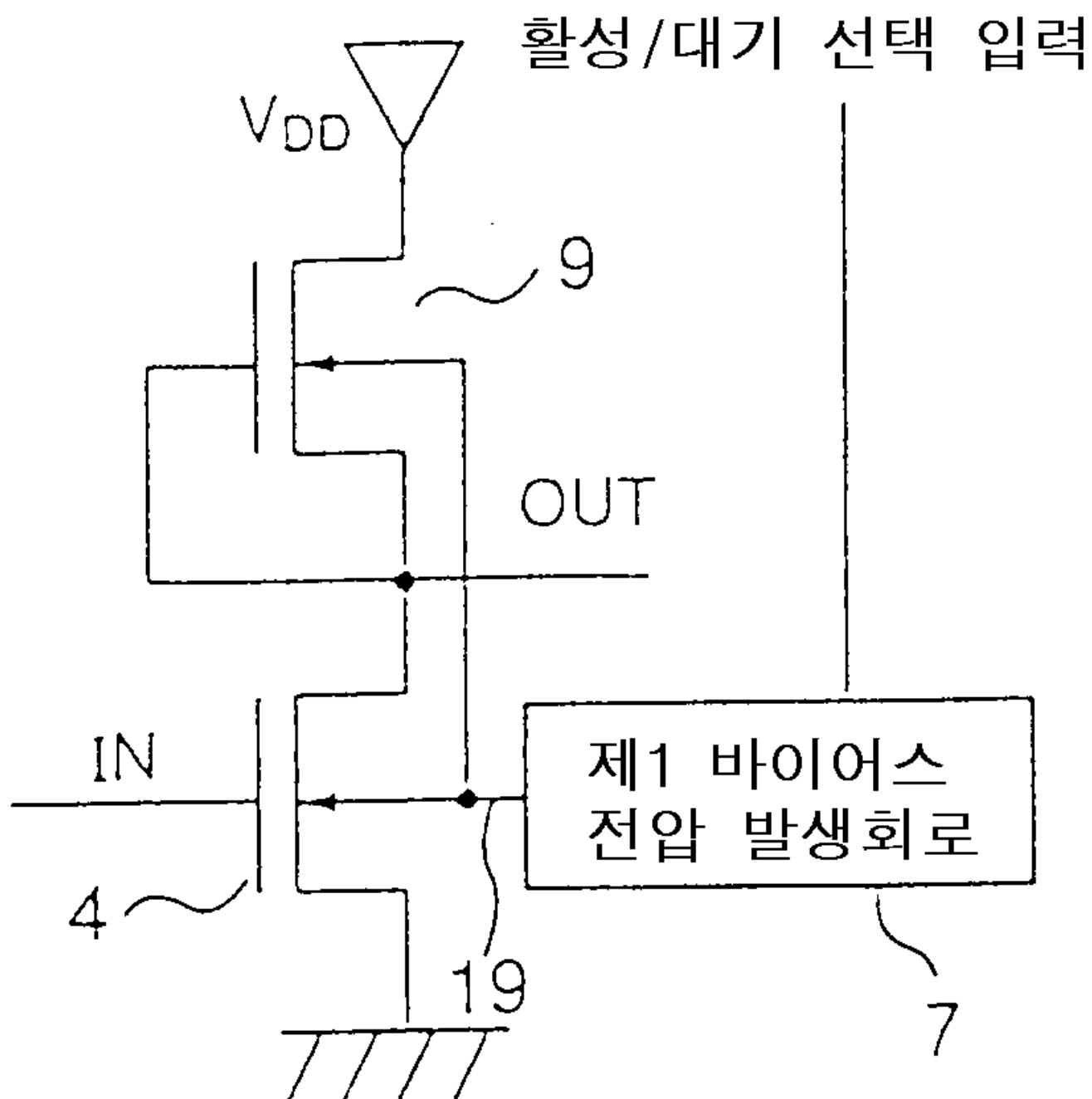
7a



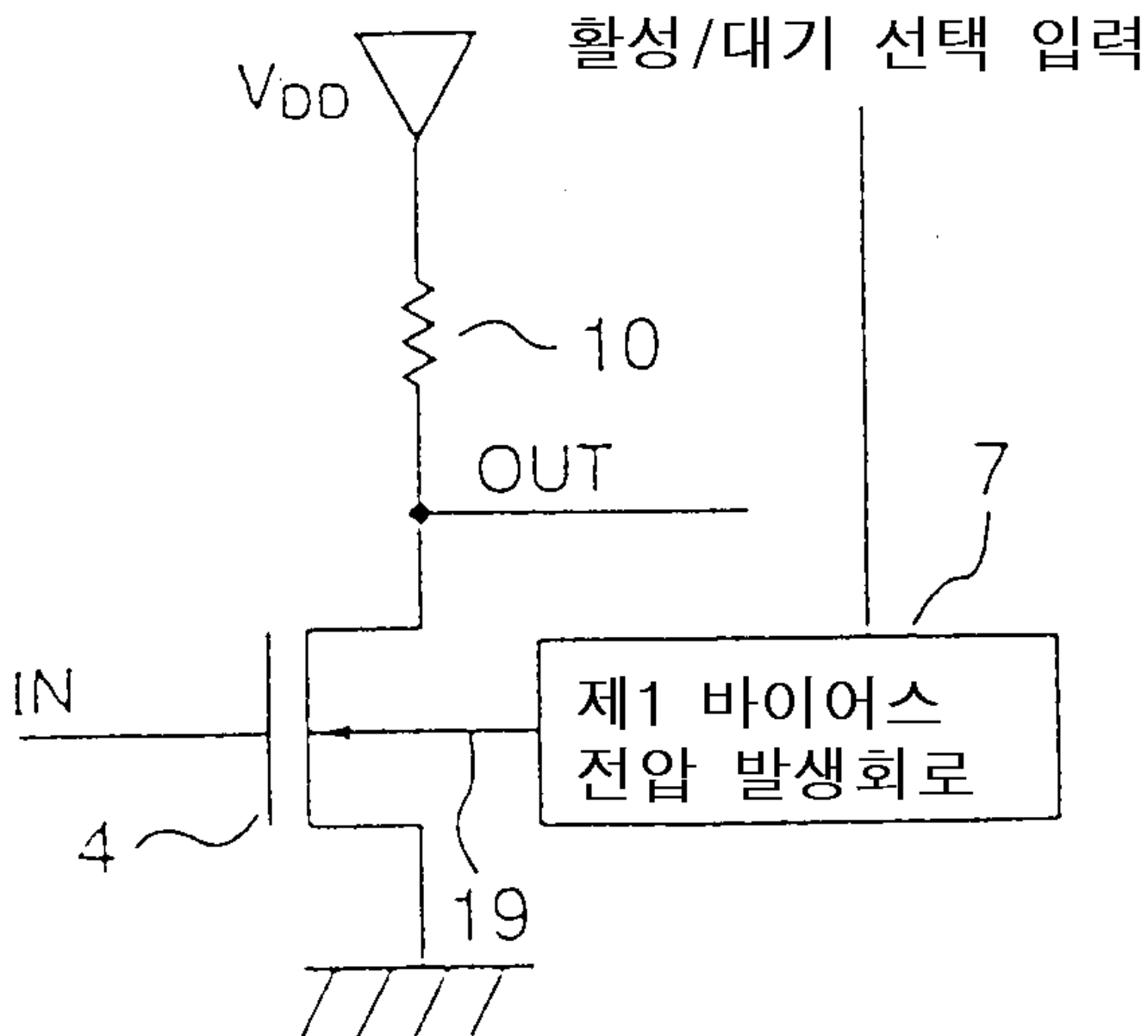
7b



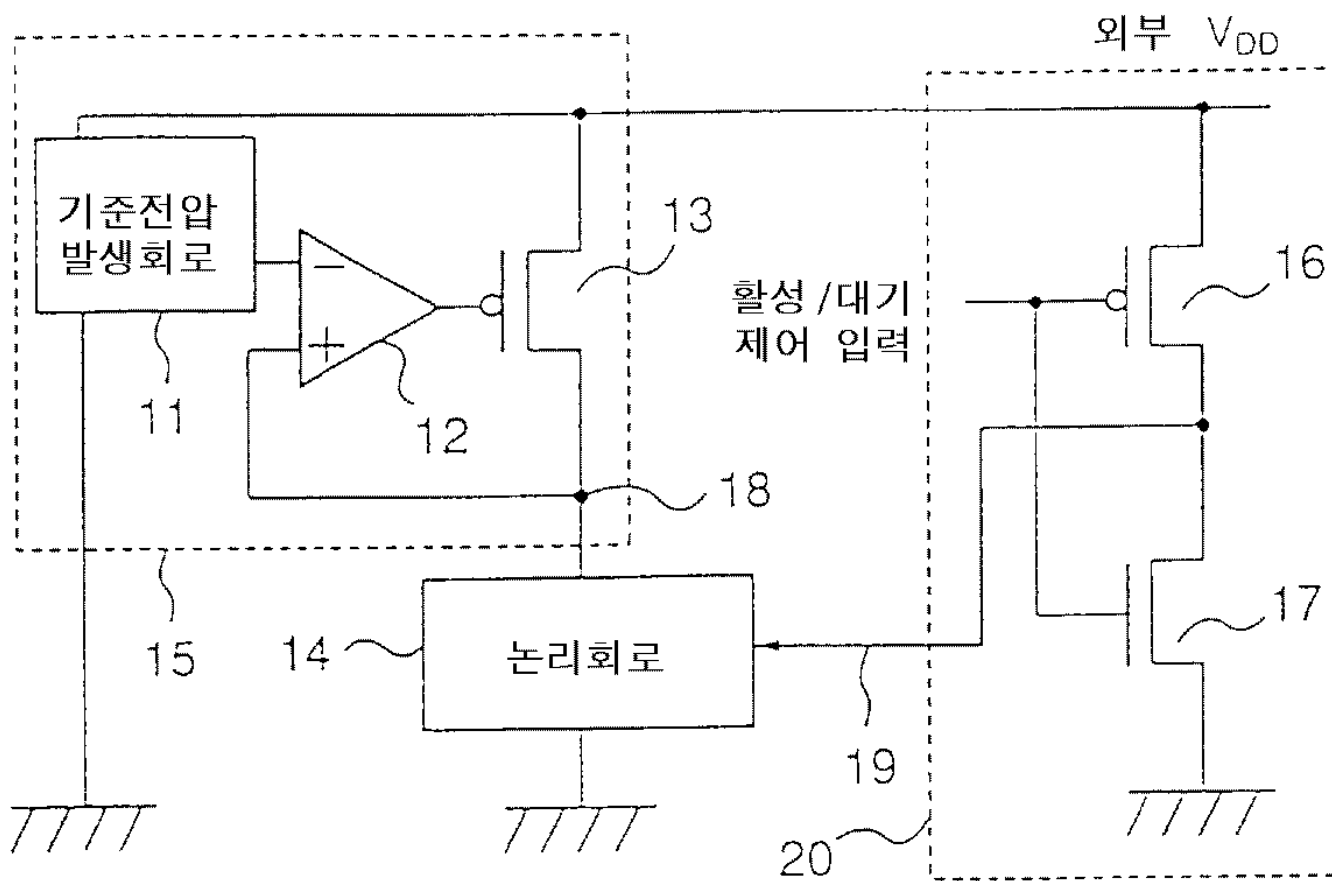
8a



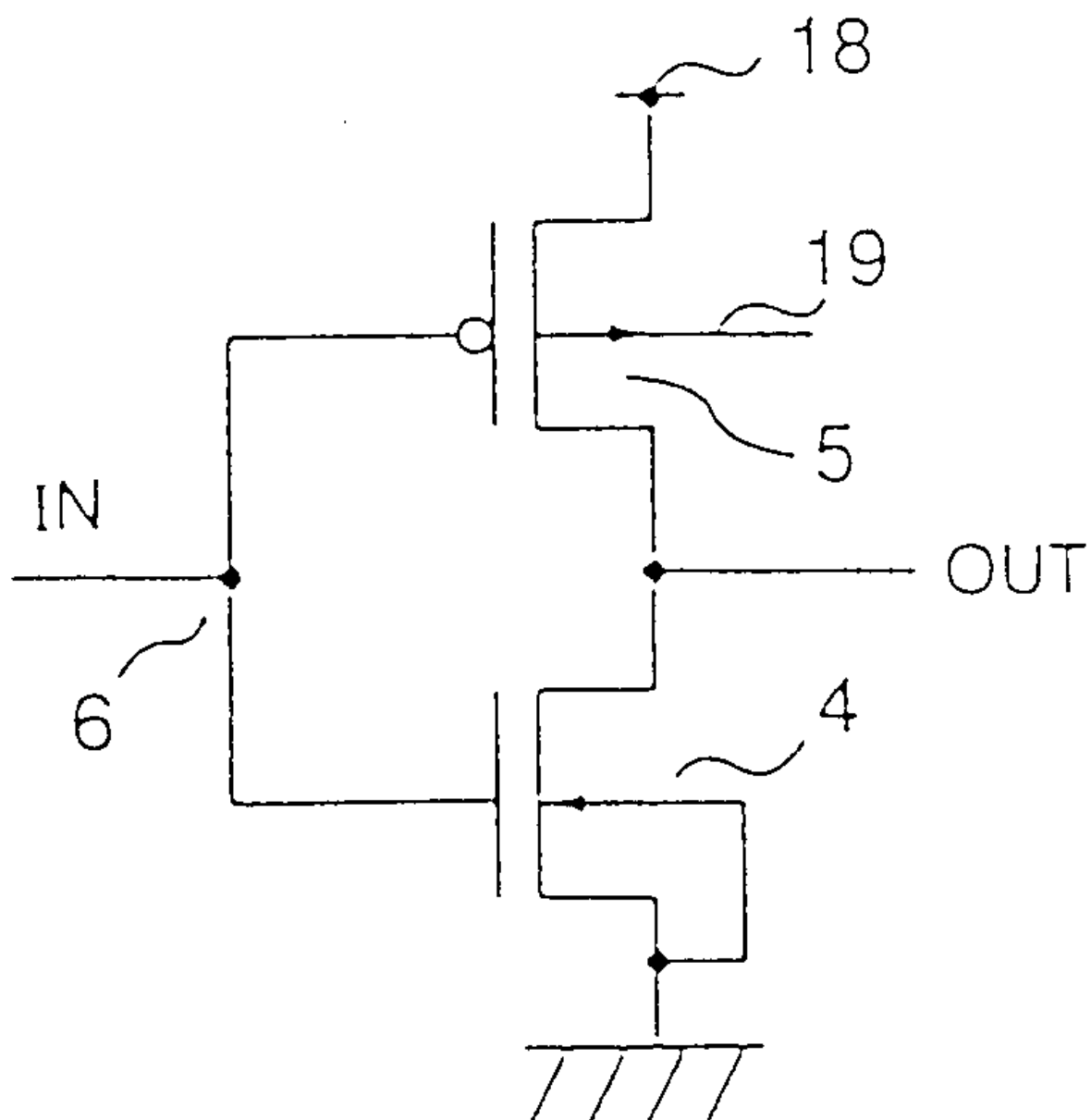
8b



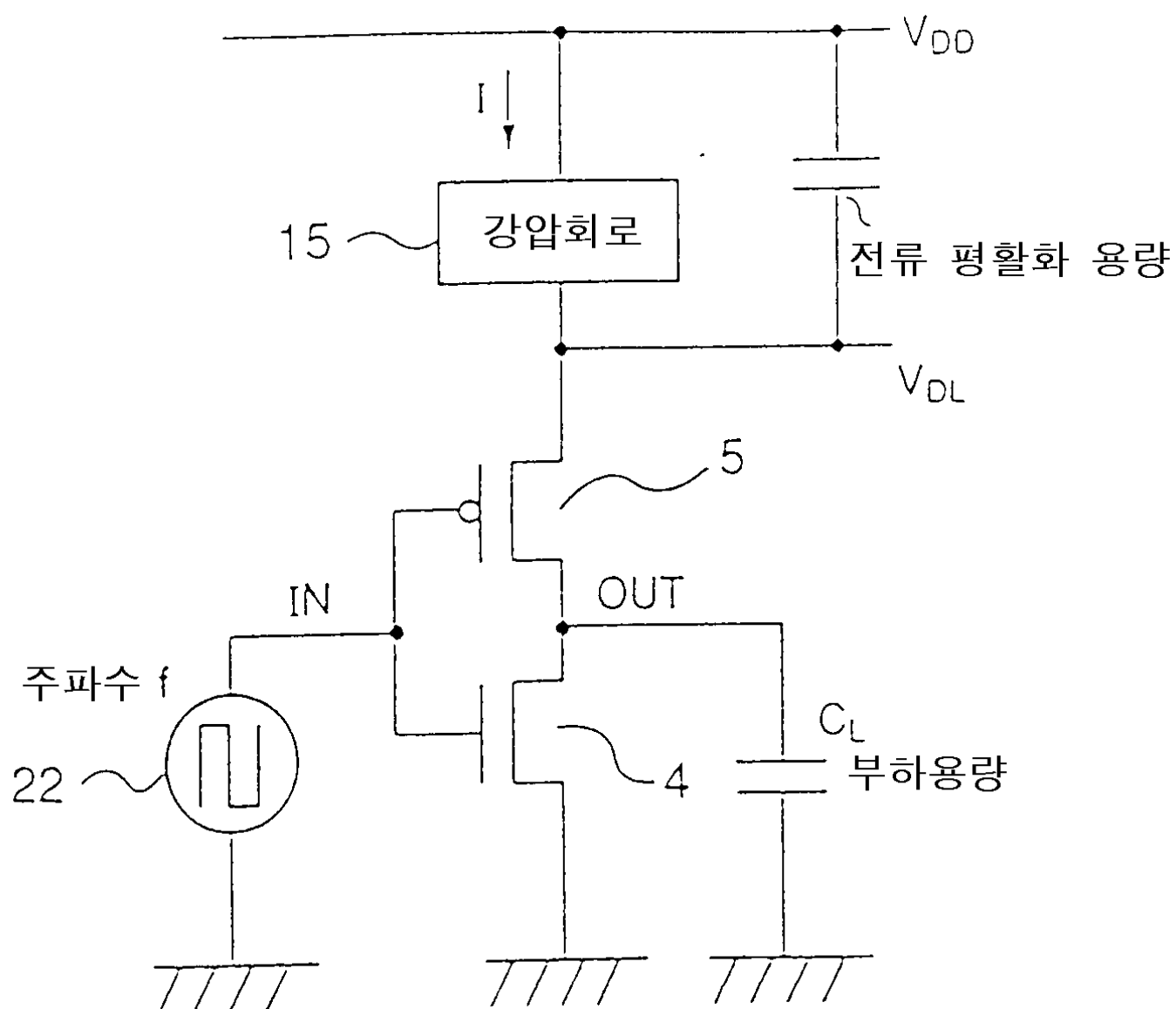
9a



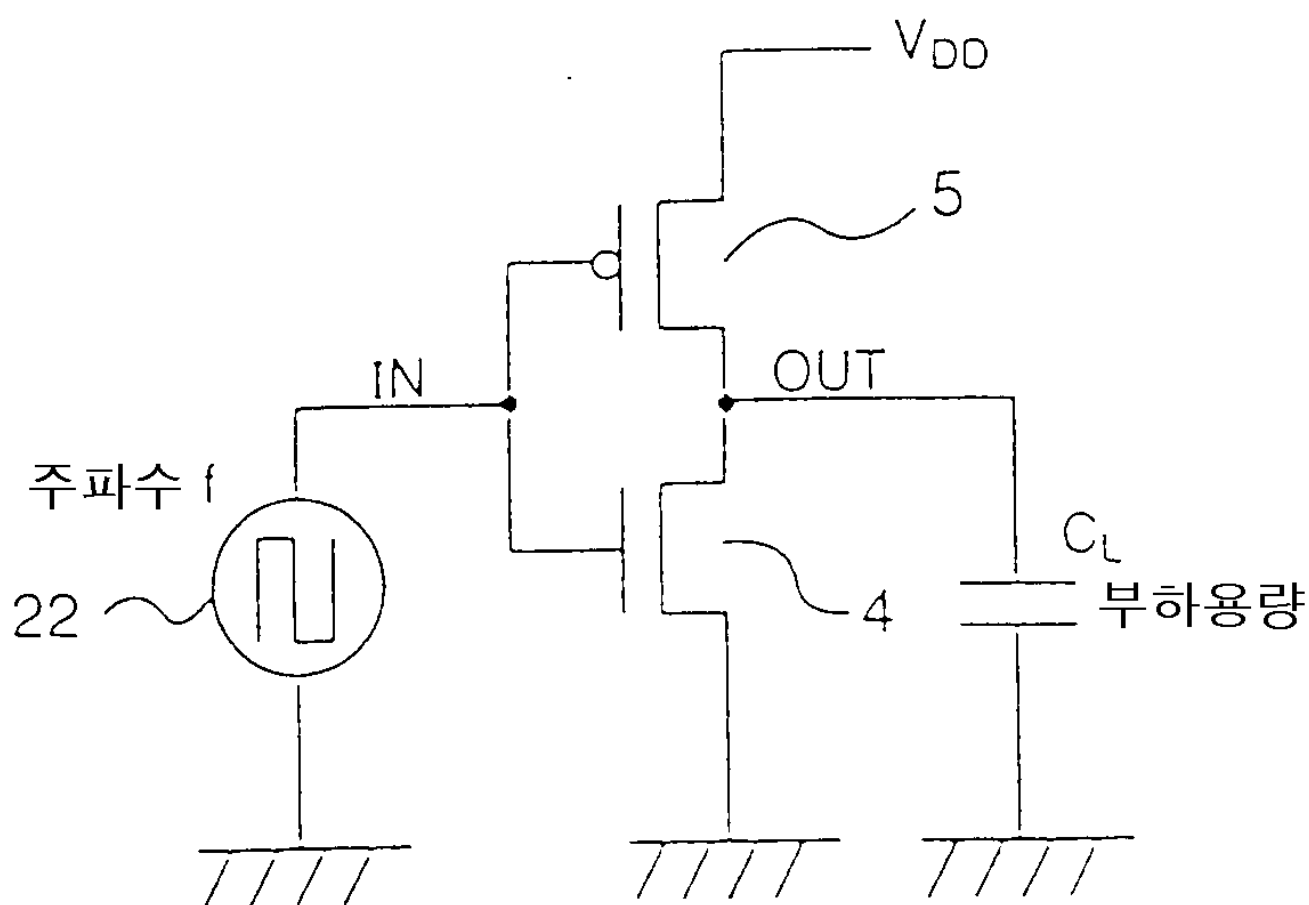
9b



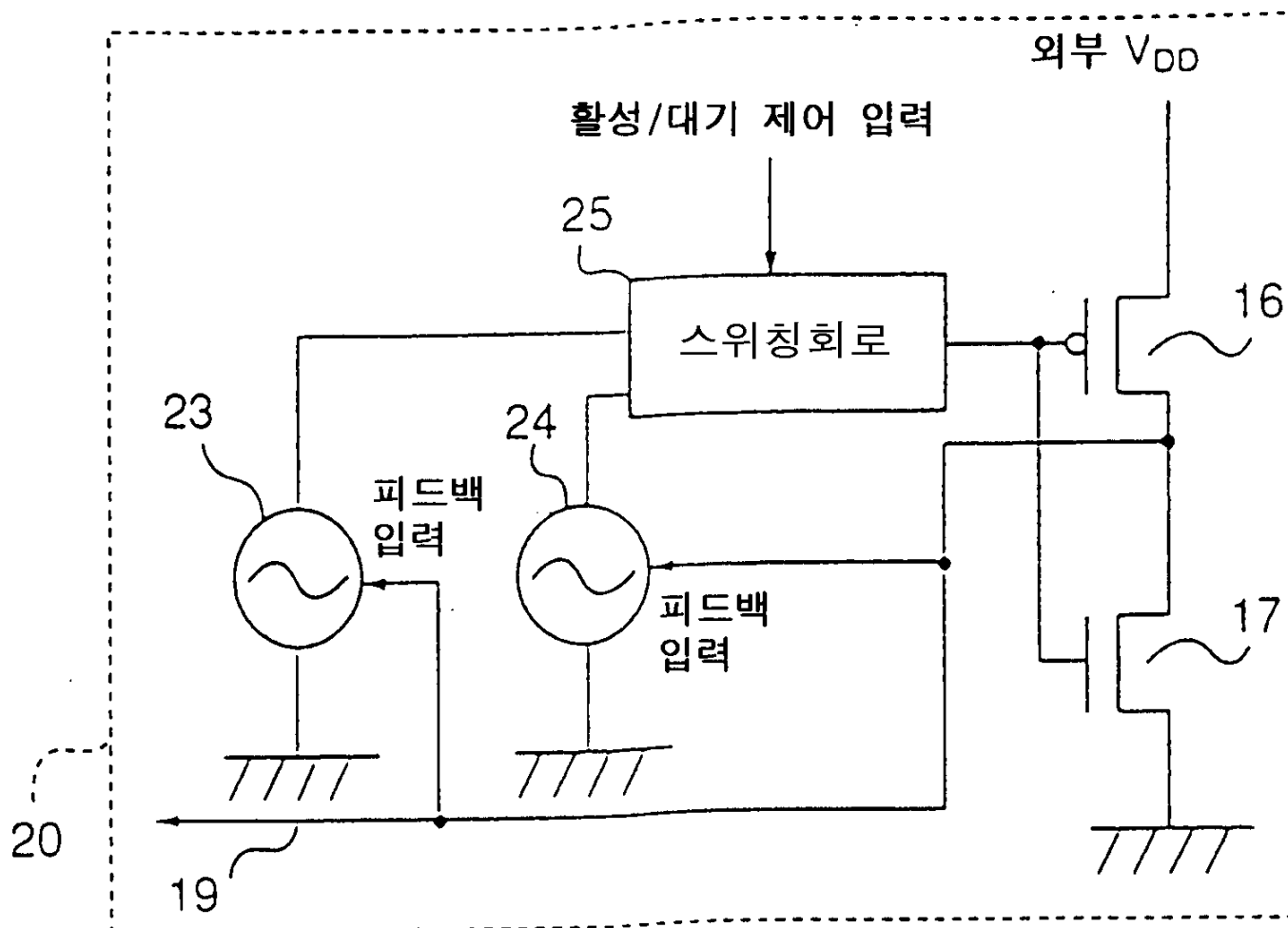
10a



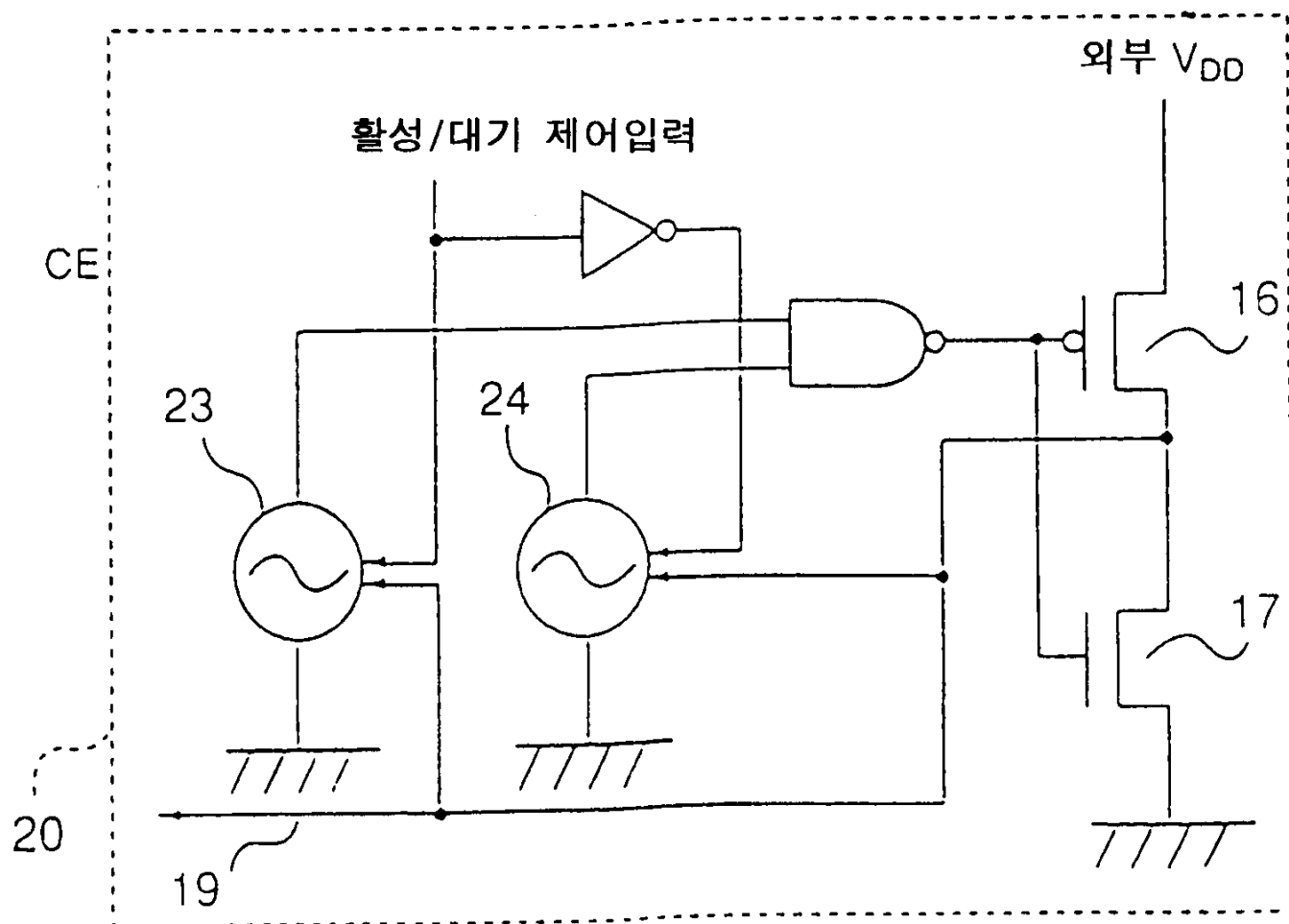
10b



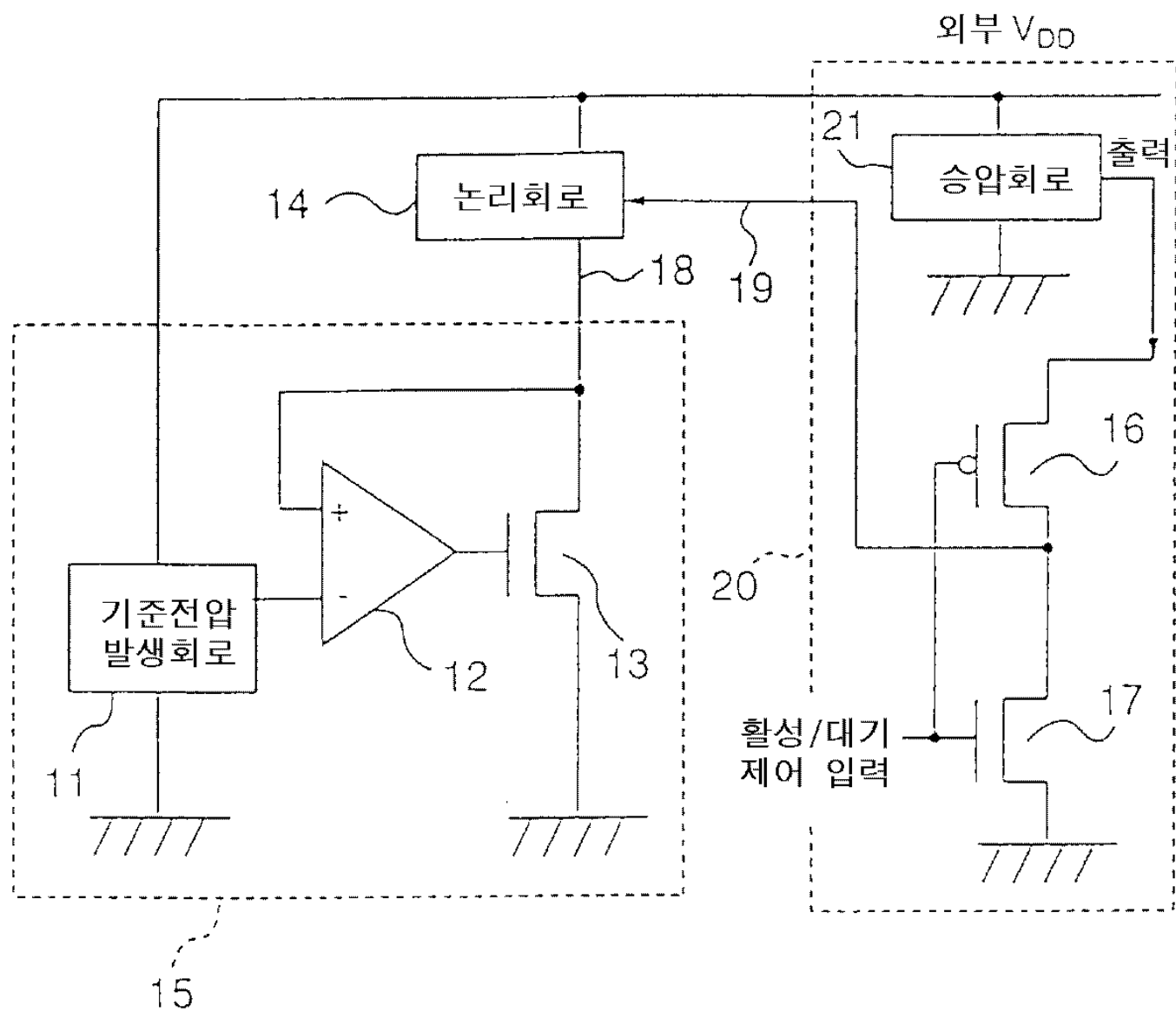
11a



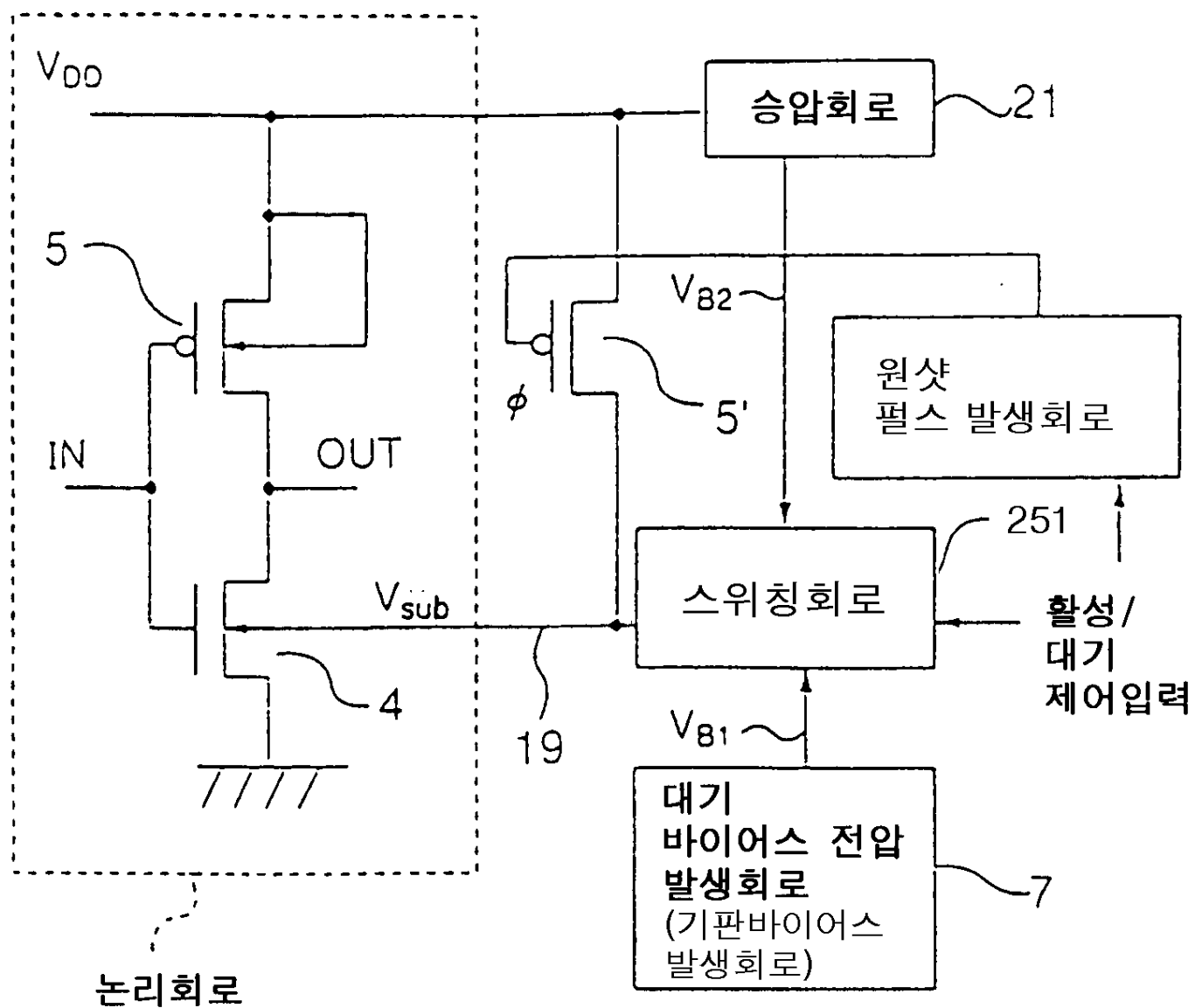
11b



12

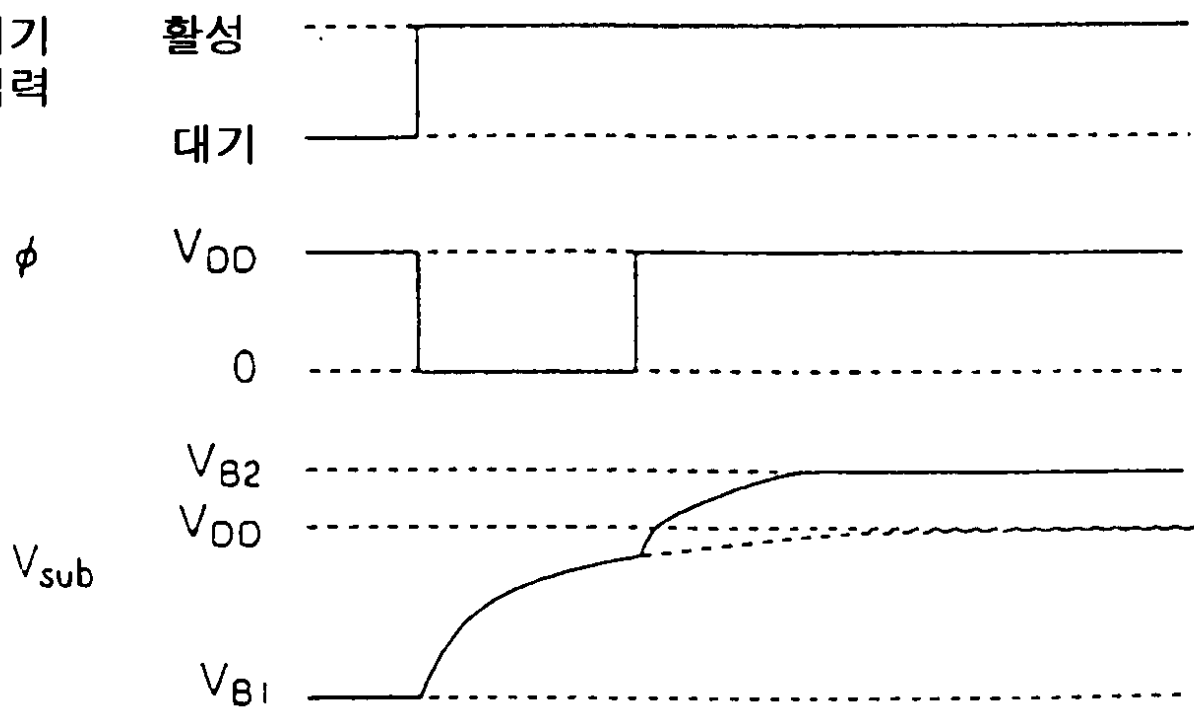


13a

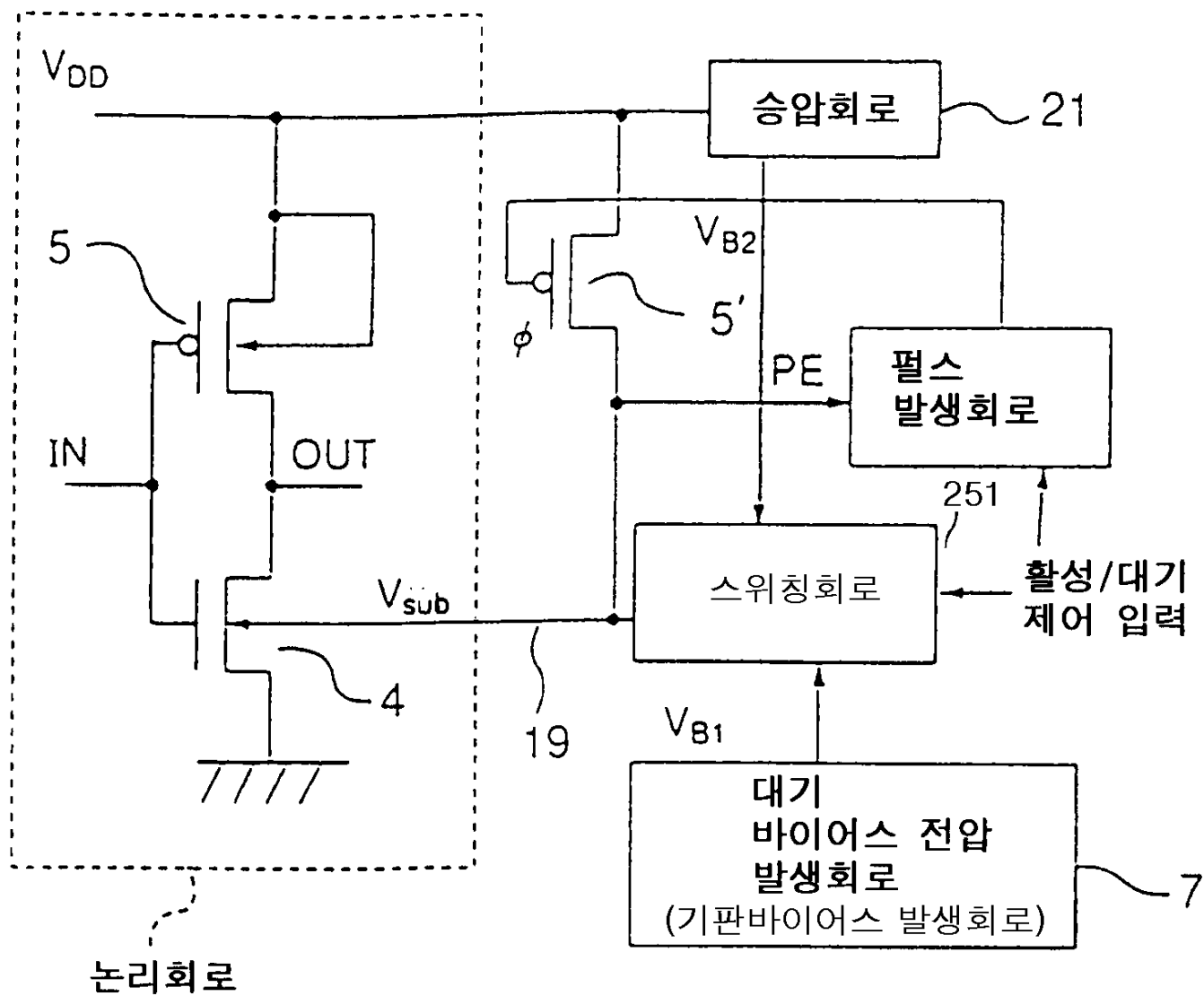


13b

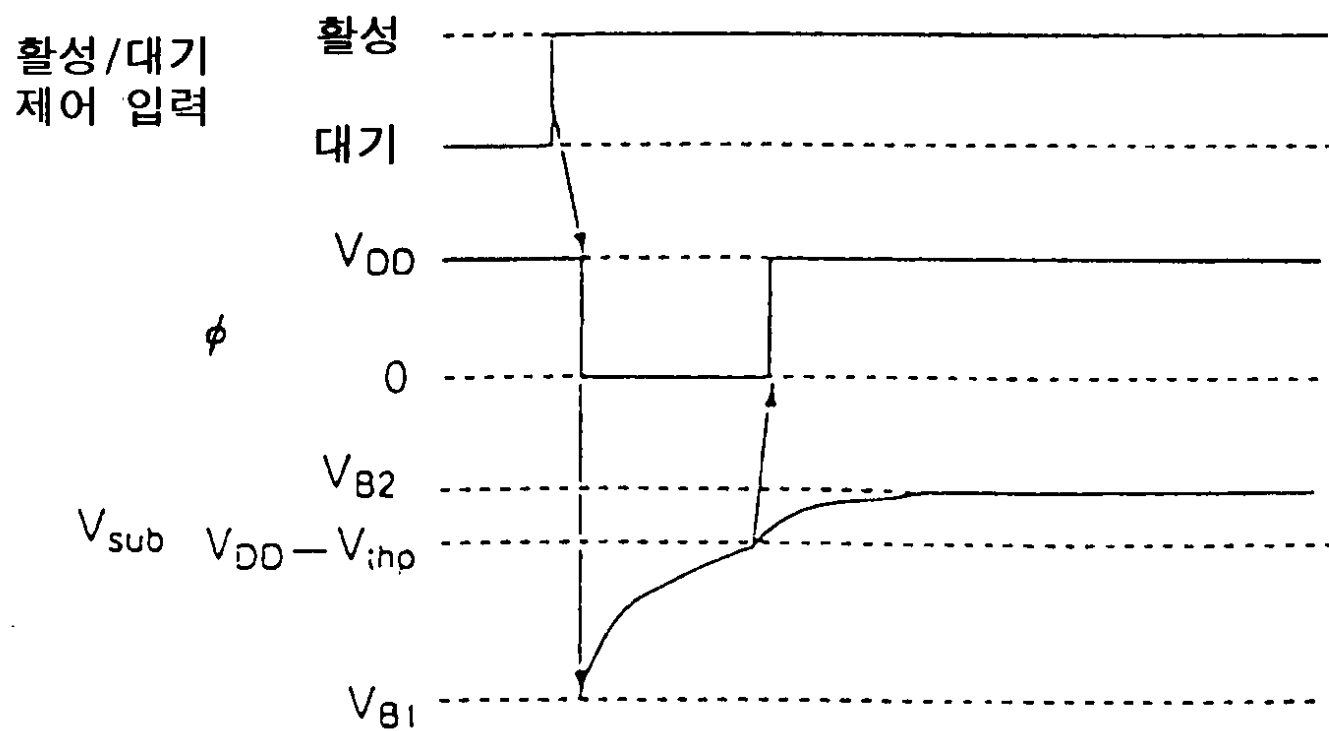
활성/대기
제어 입력



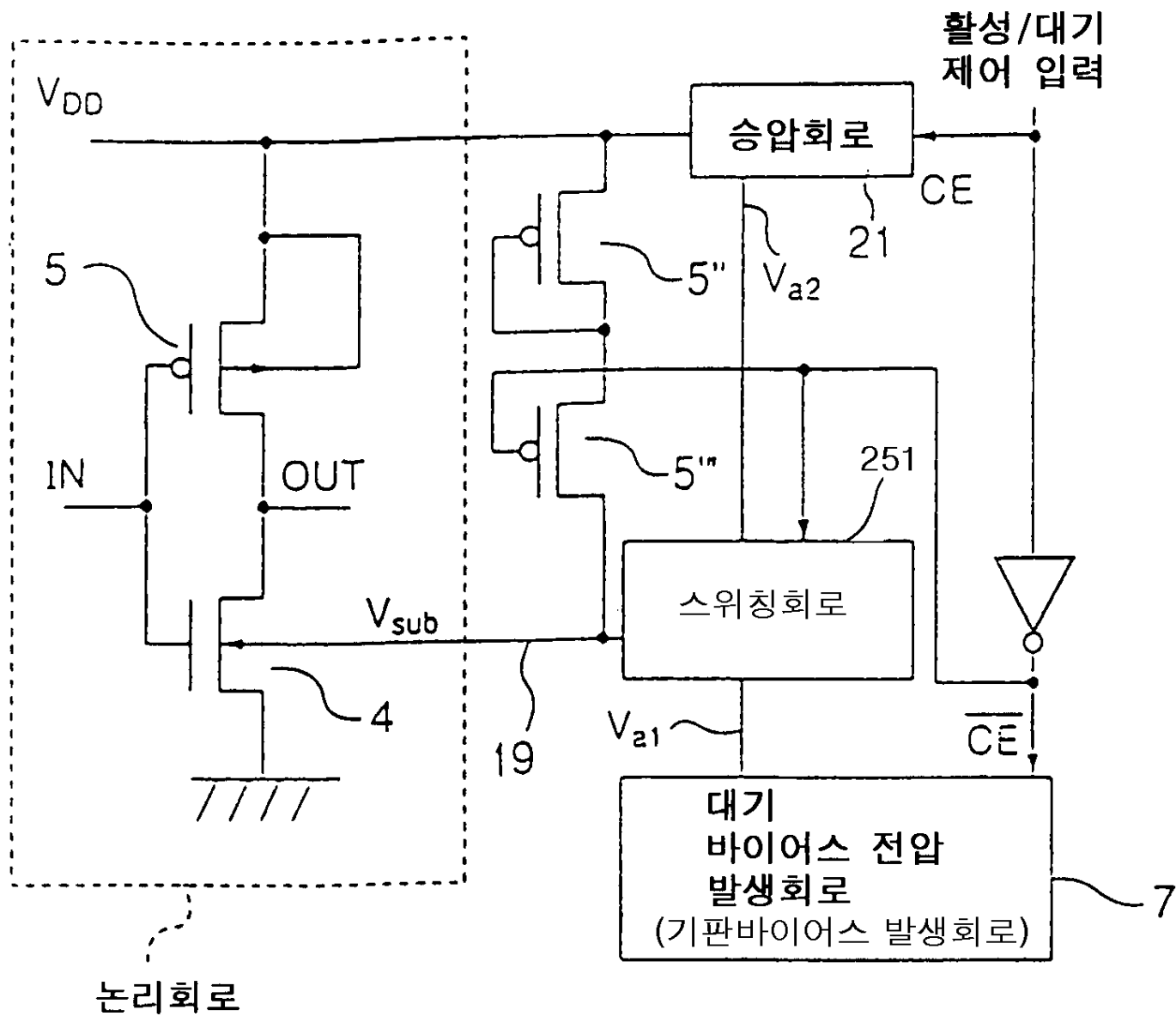
14a



14b

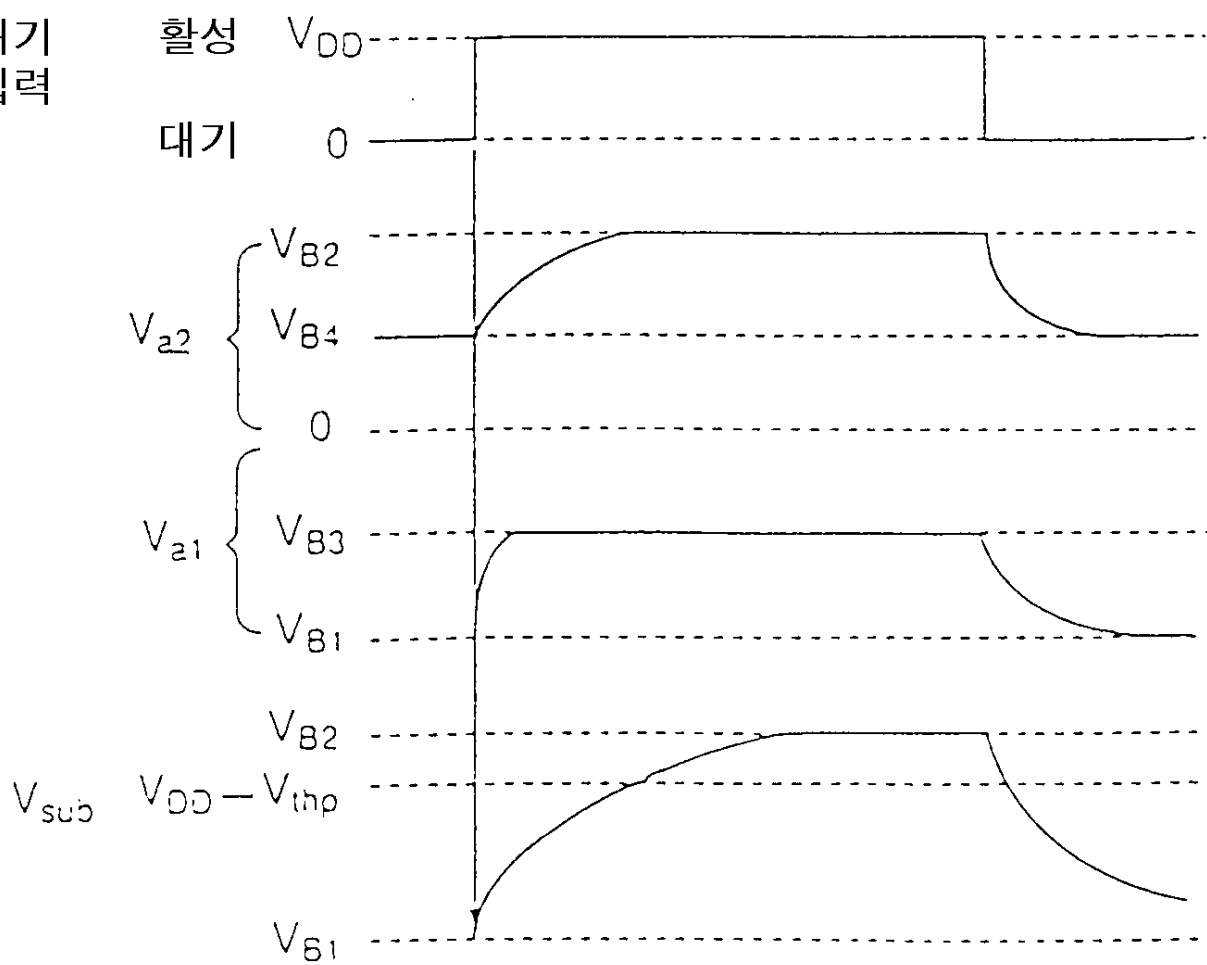


15a

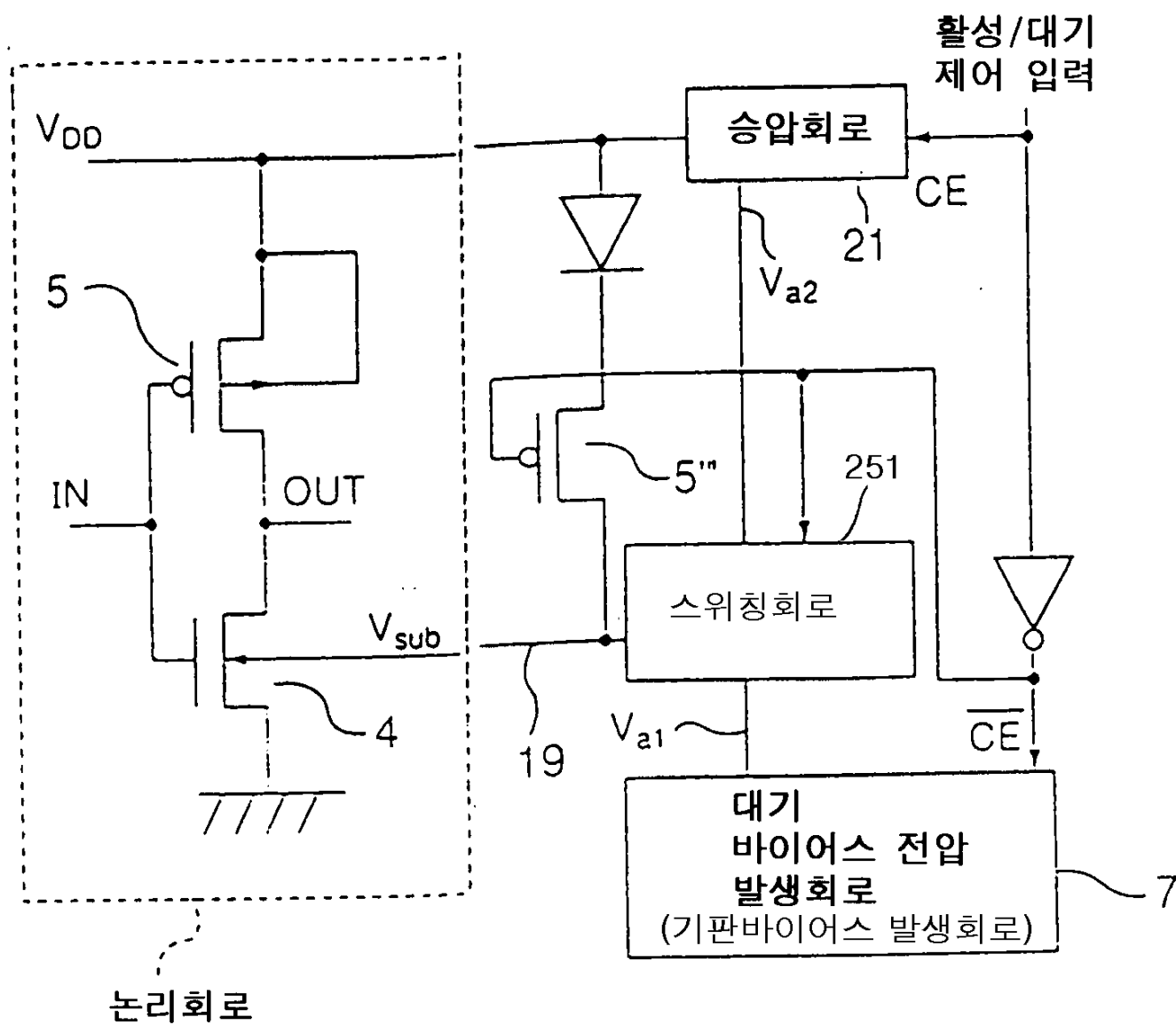


15b

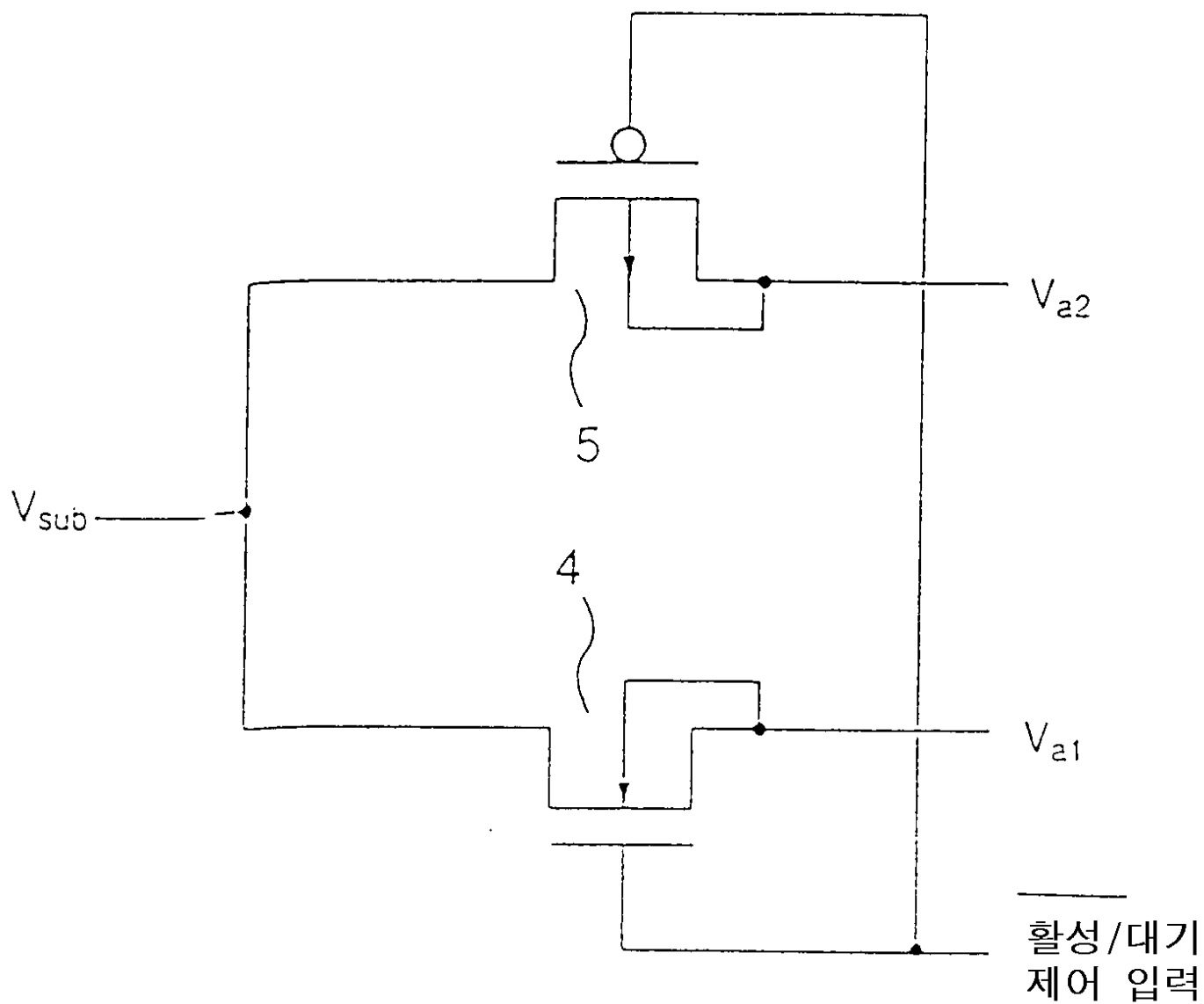
활성/대기
제어 입력



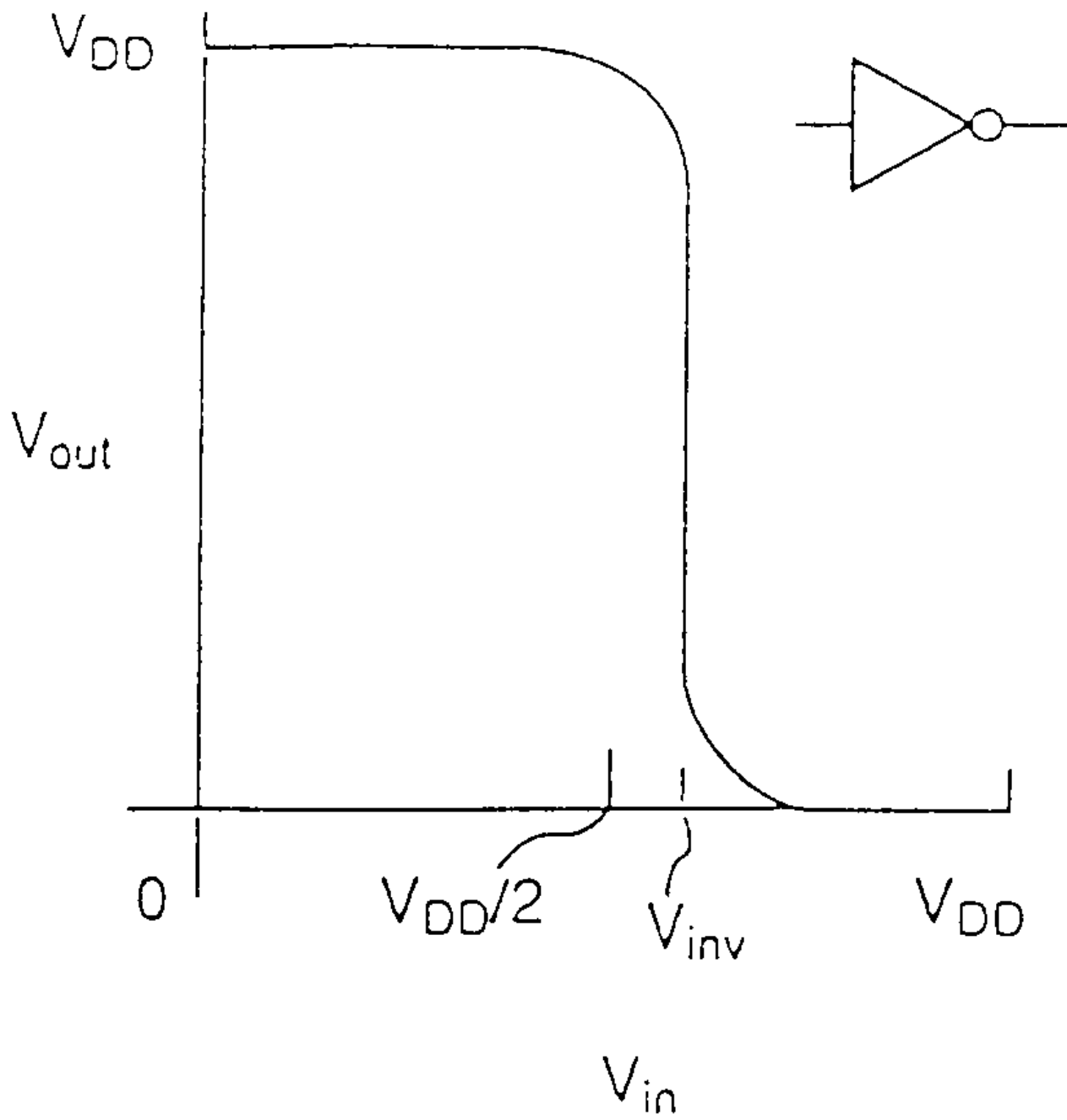
16



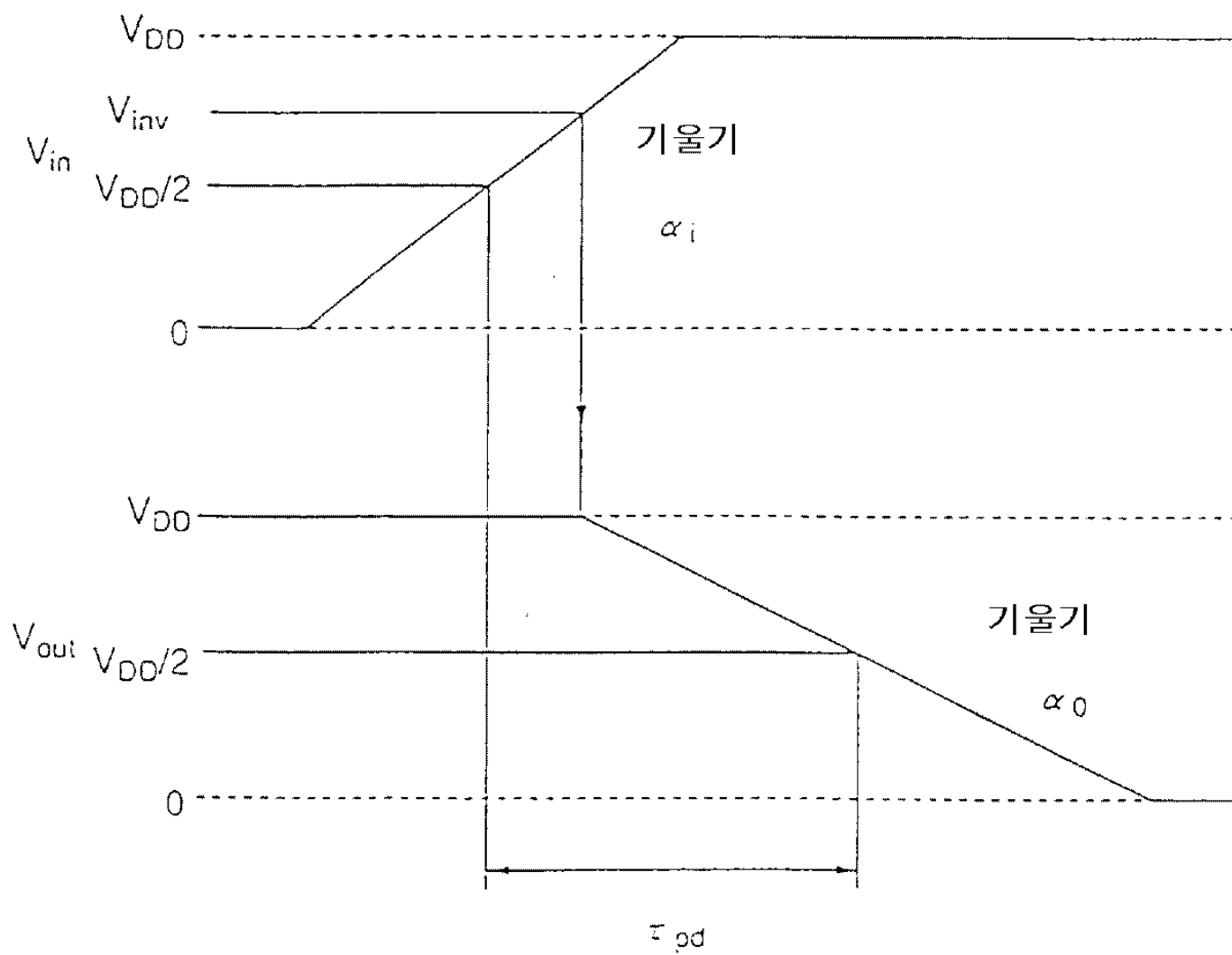
17



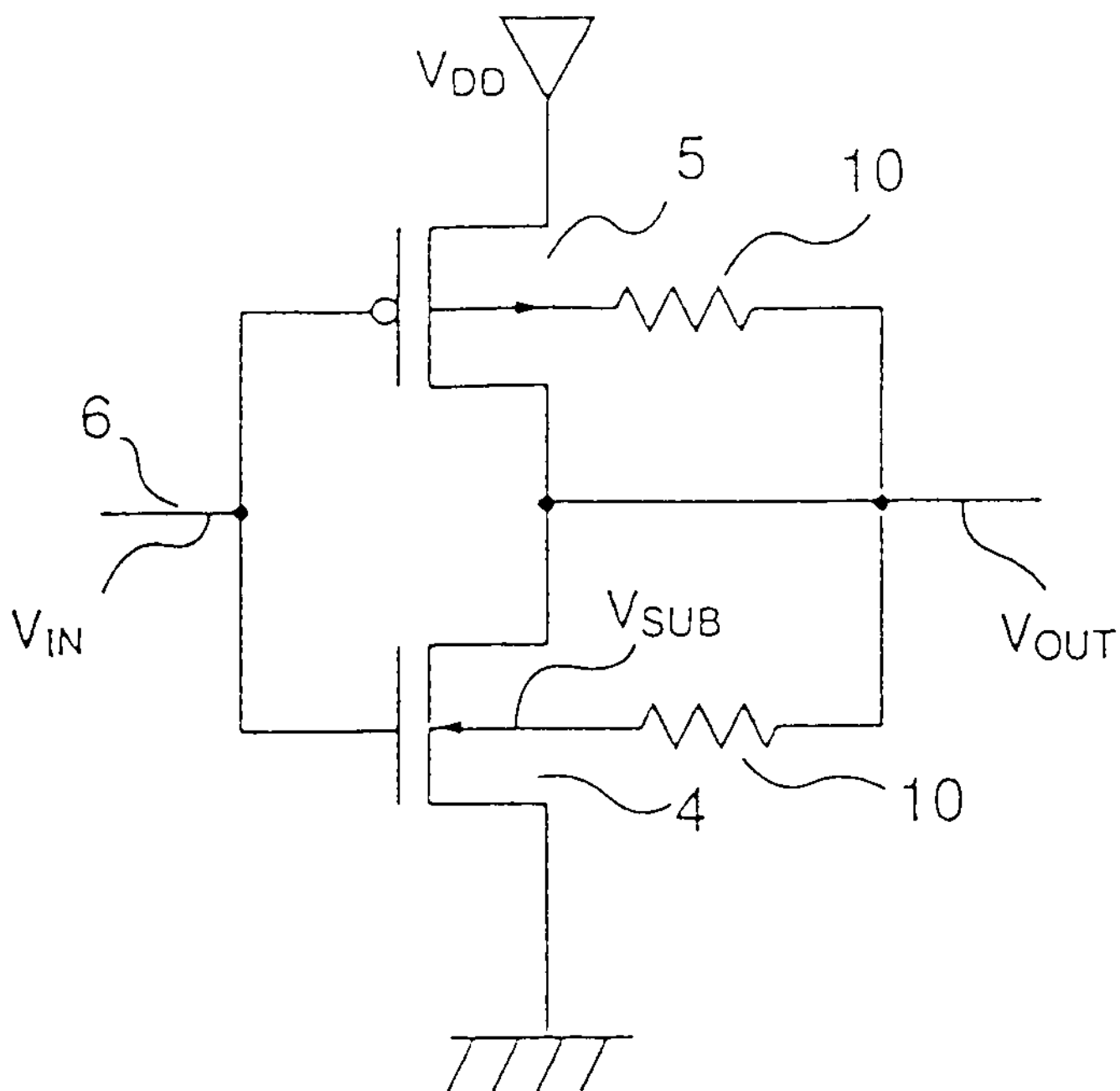
18a



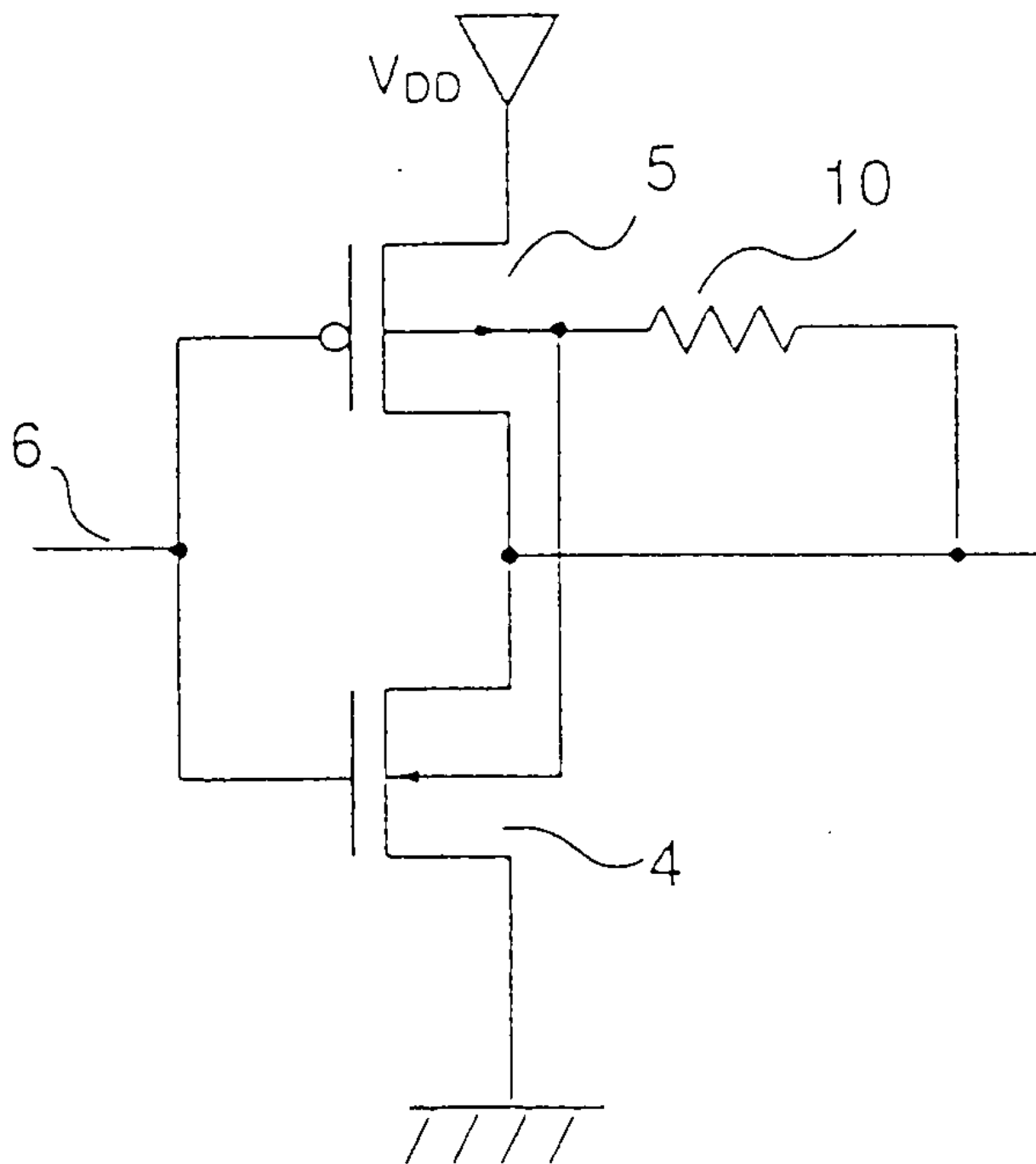
18b



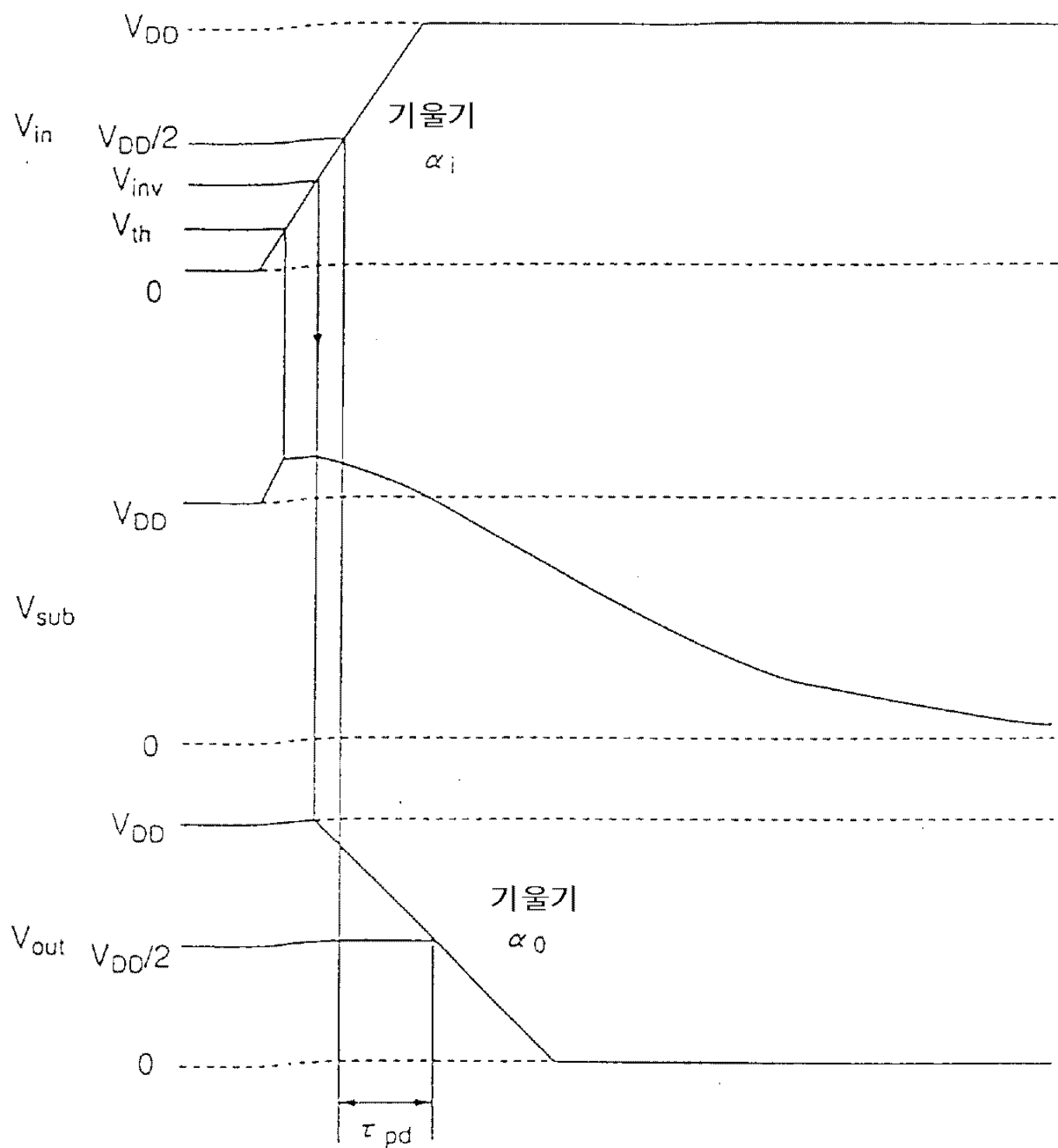
19a



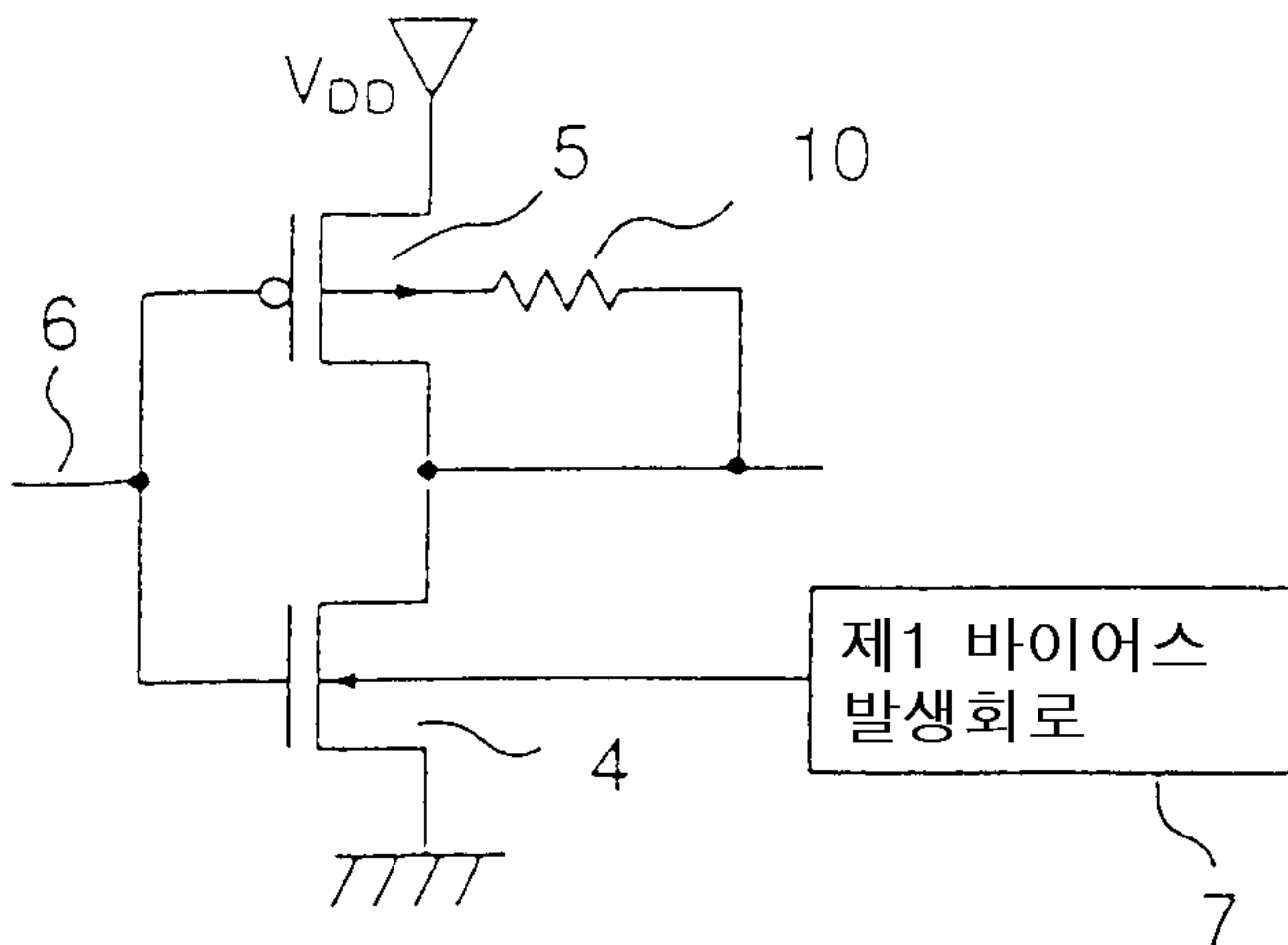
19b



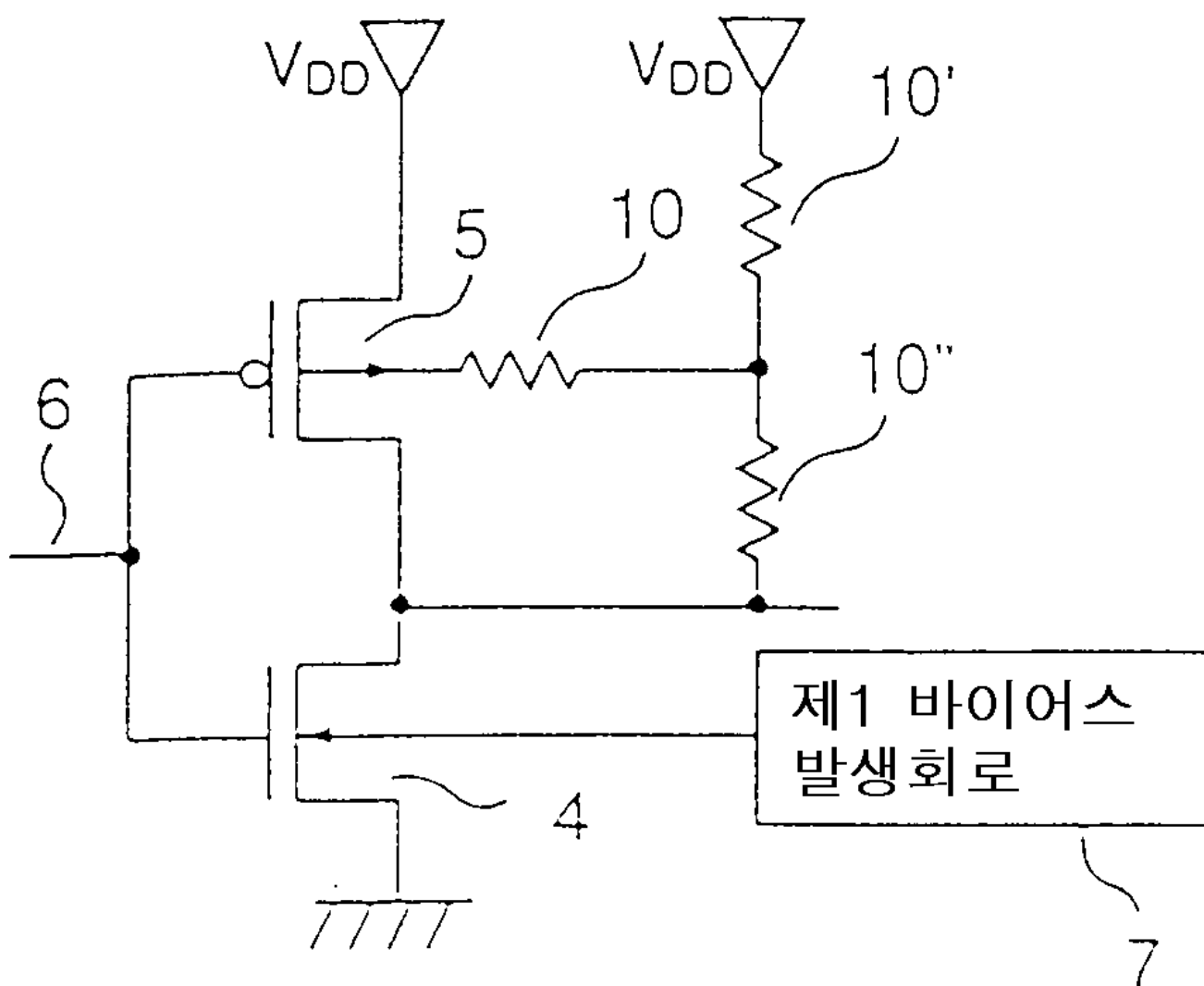
20



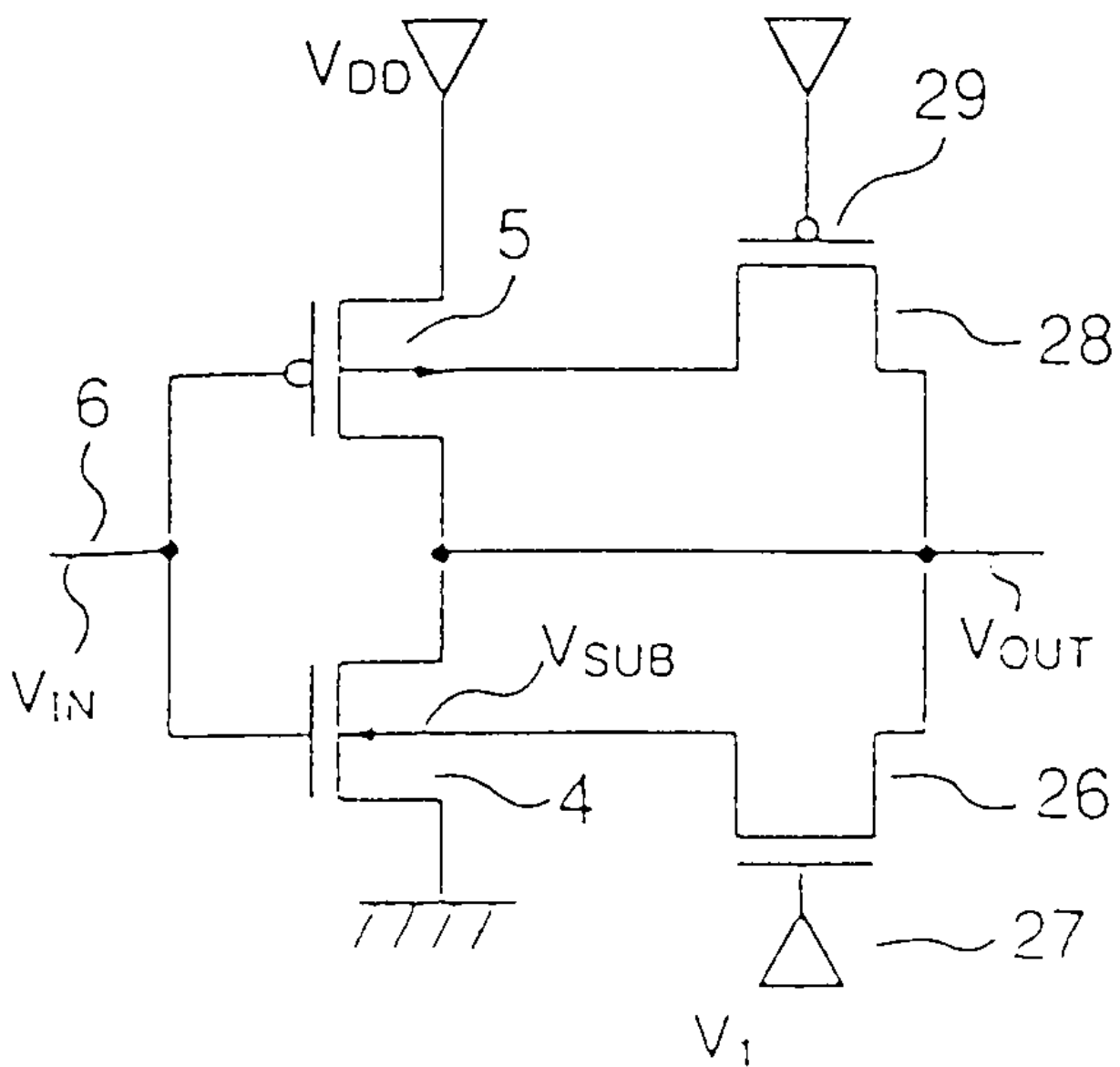
21a



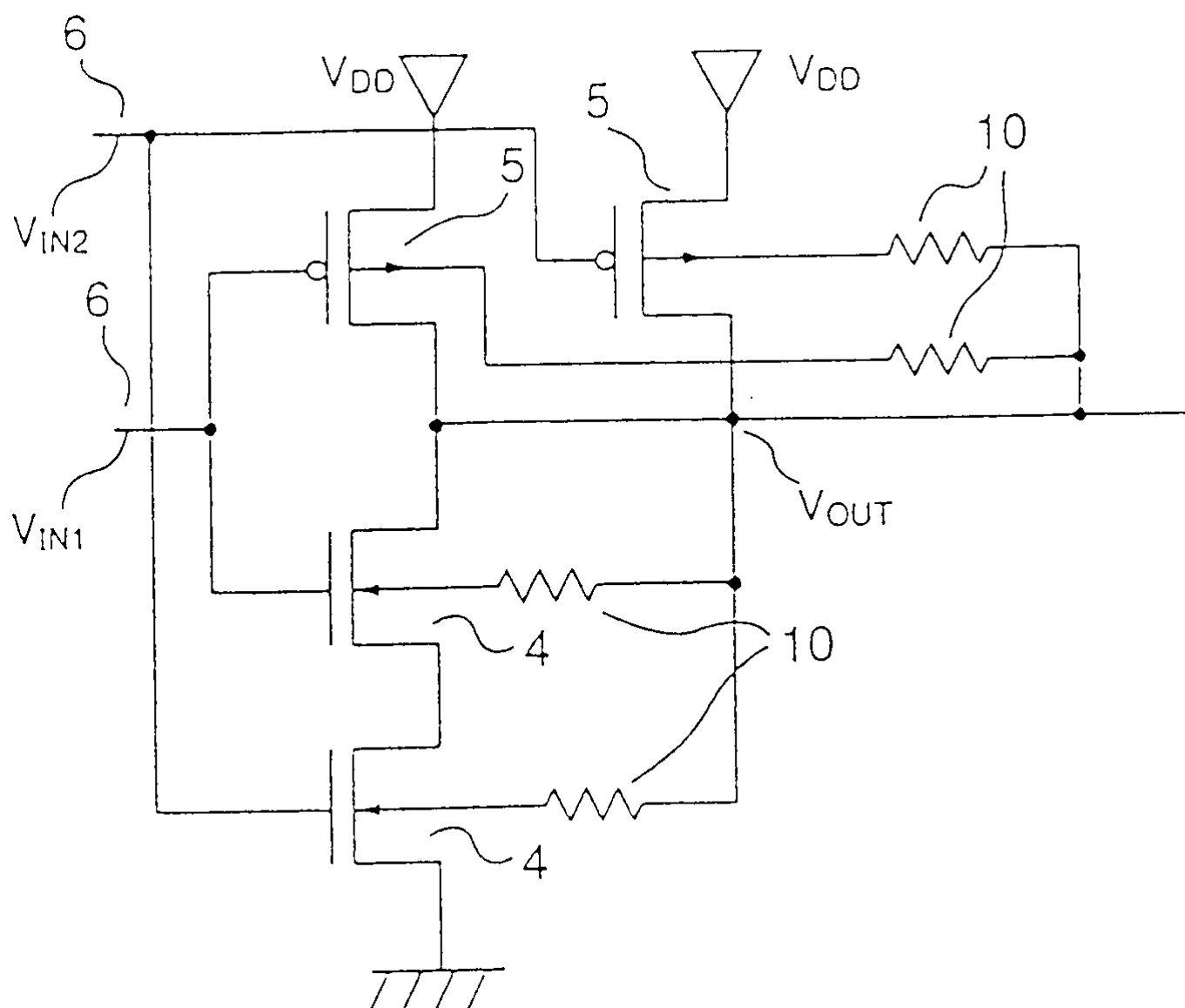
21b



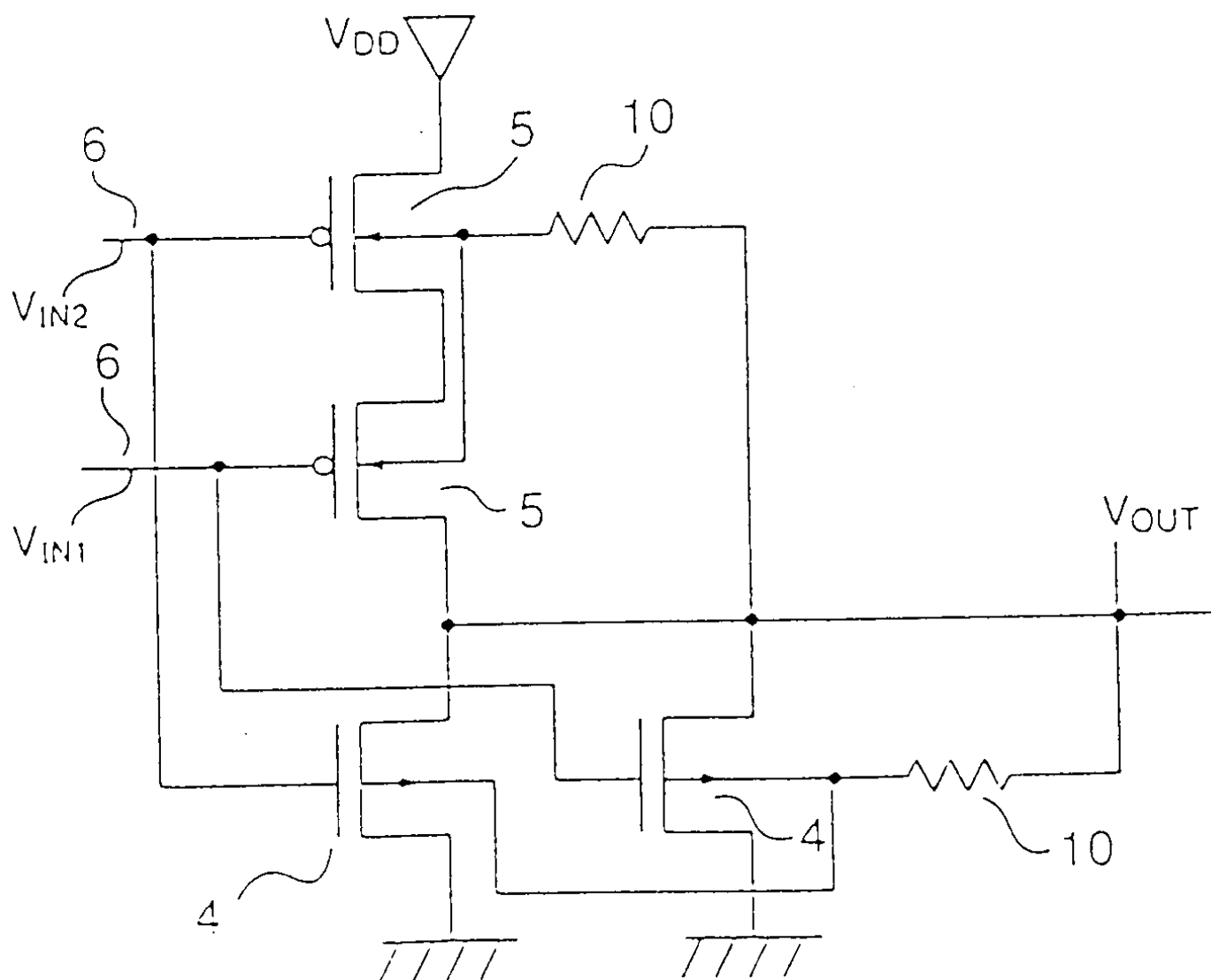
21c



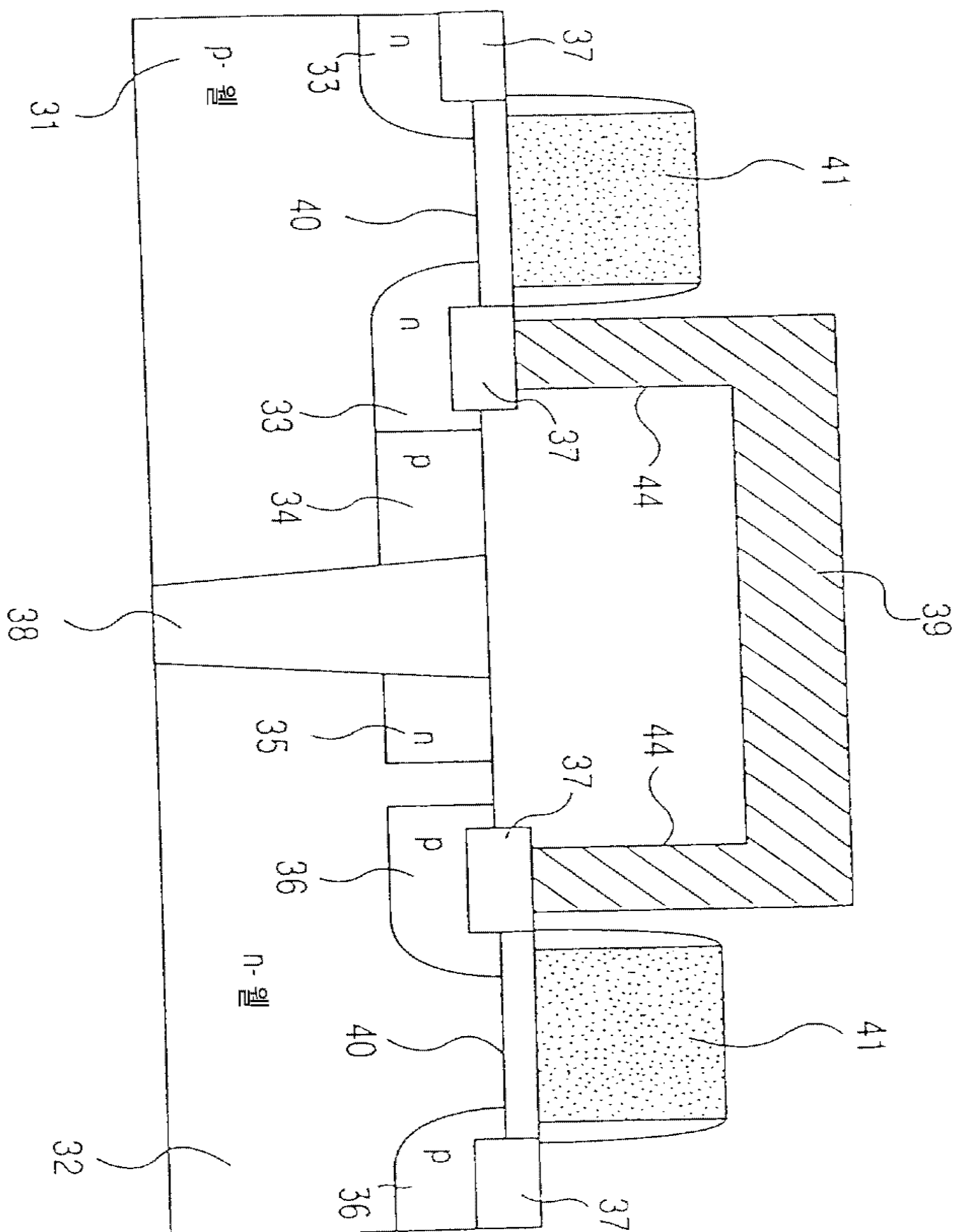
22a



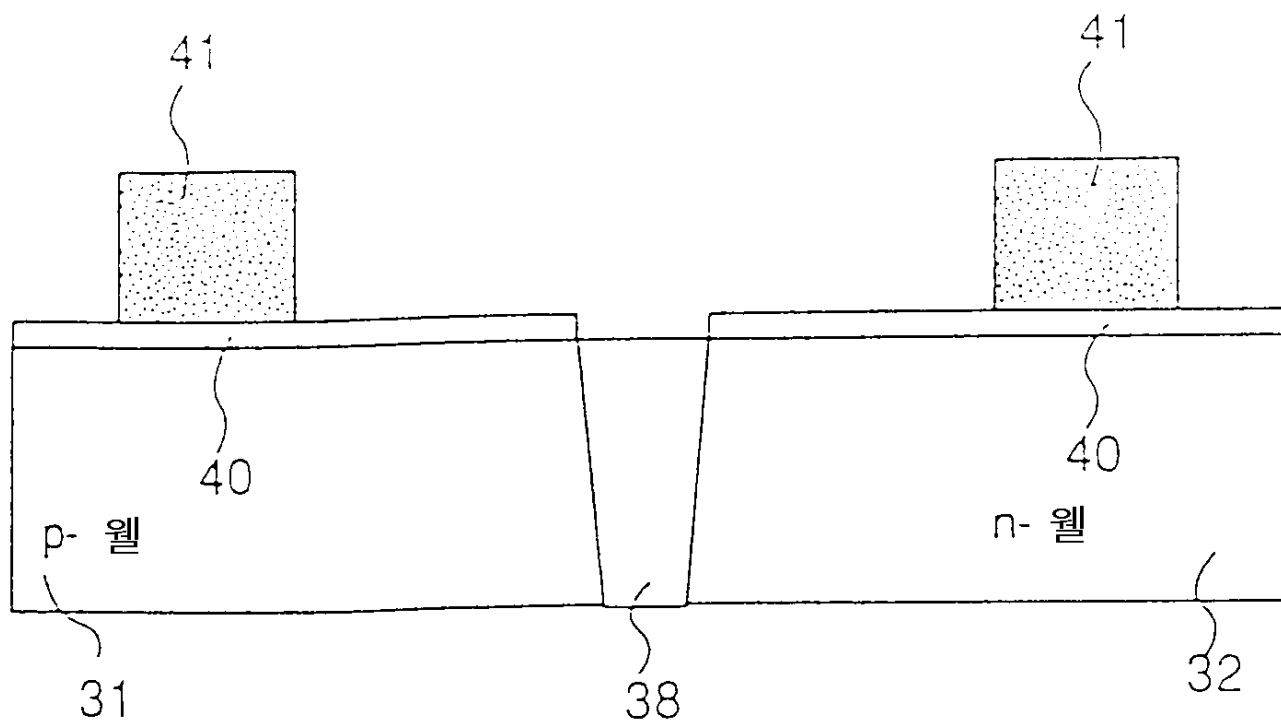
22b



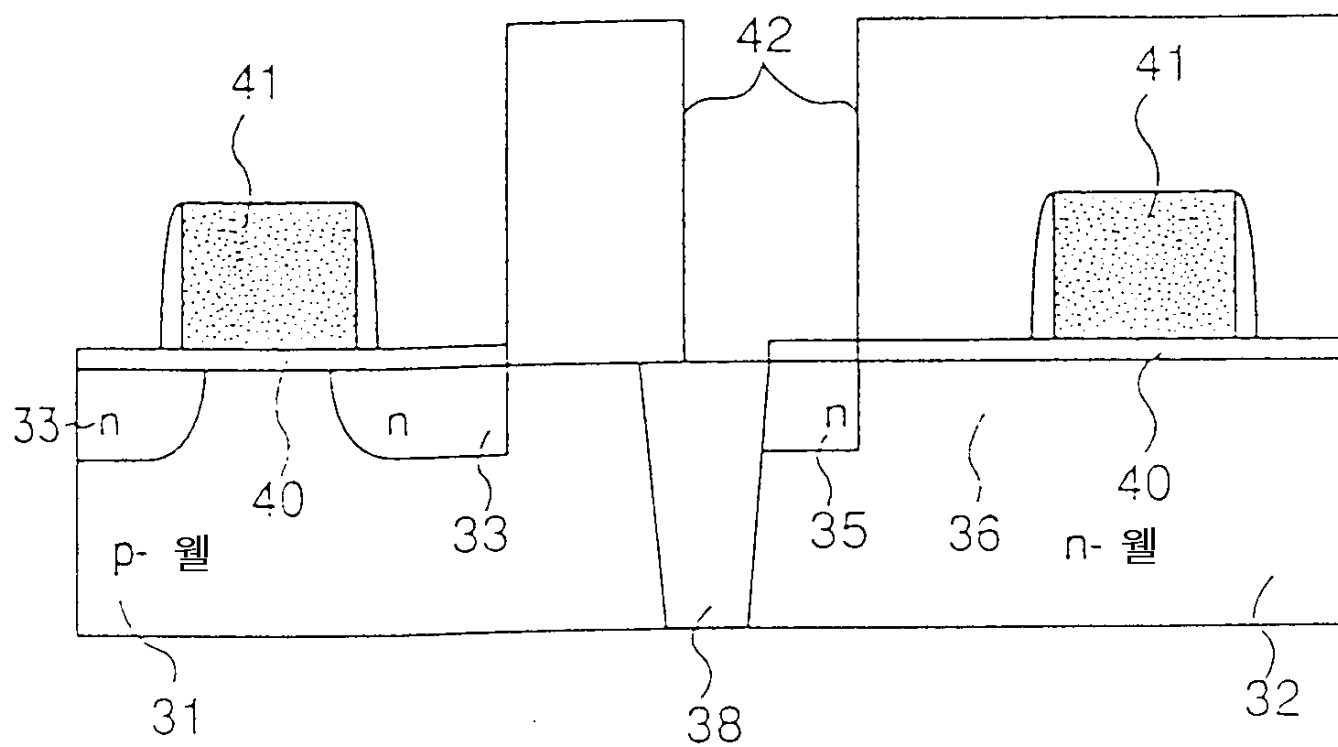
23



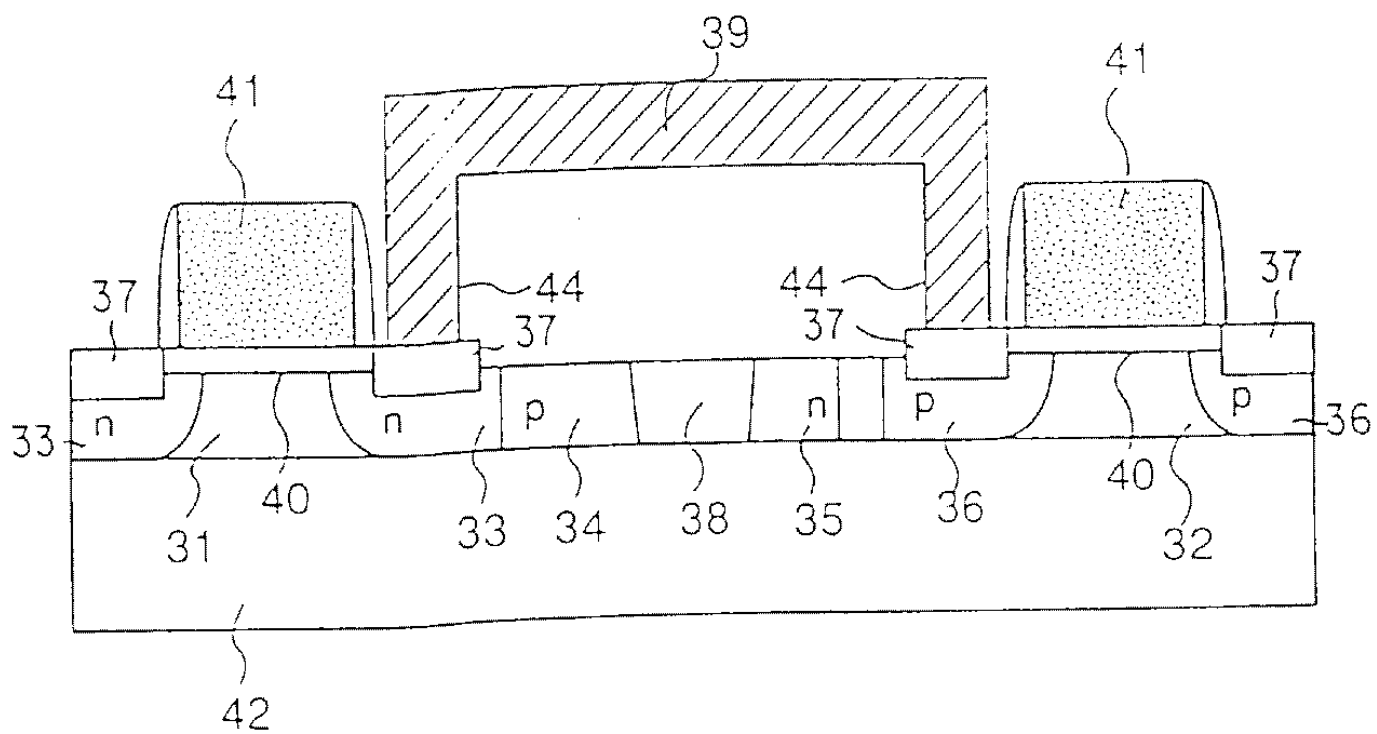
24a



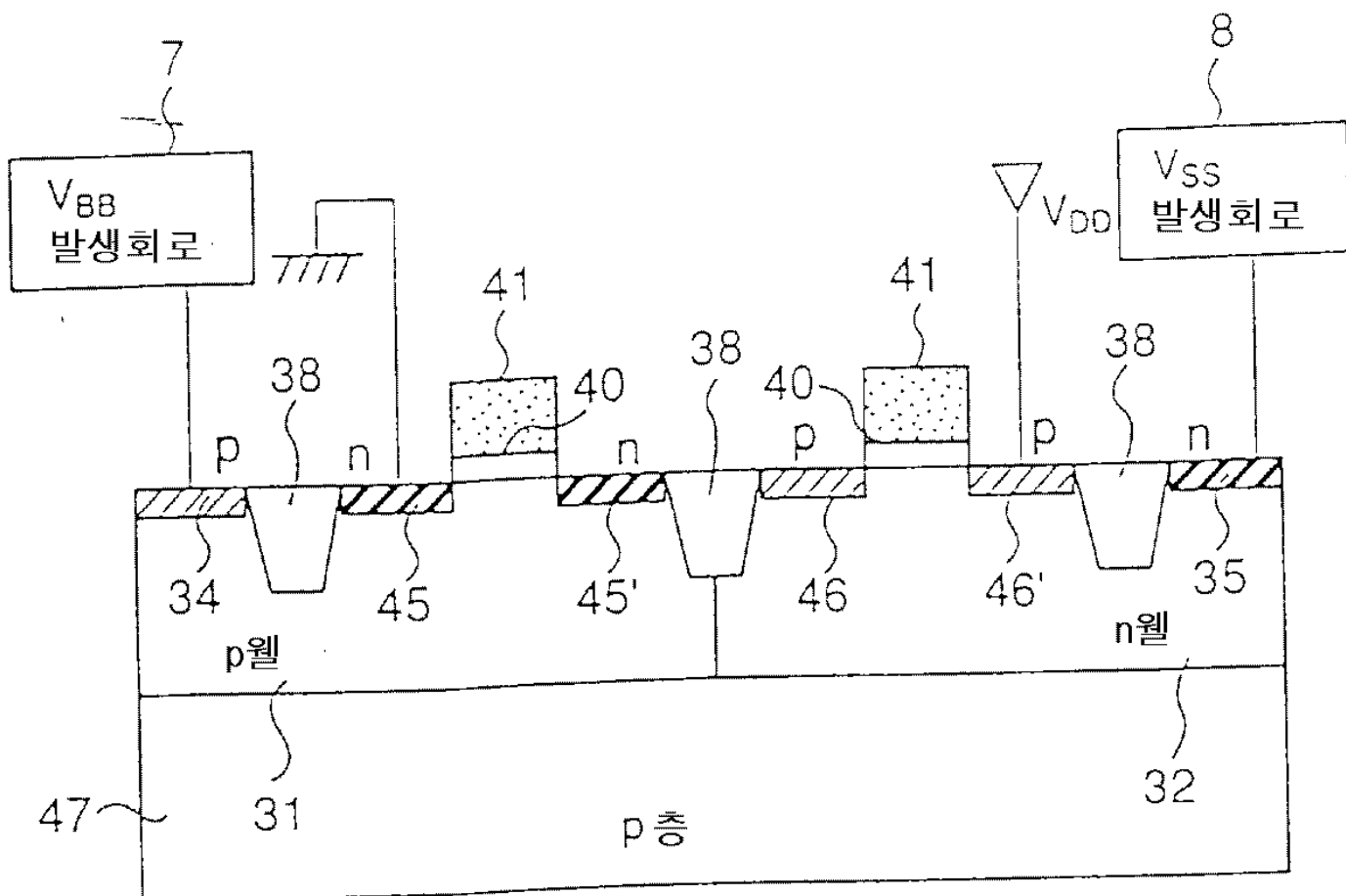
24b



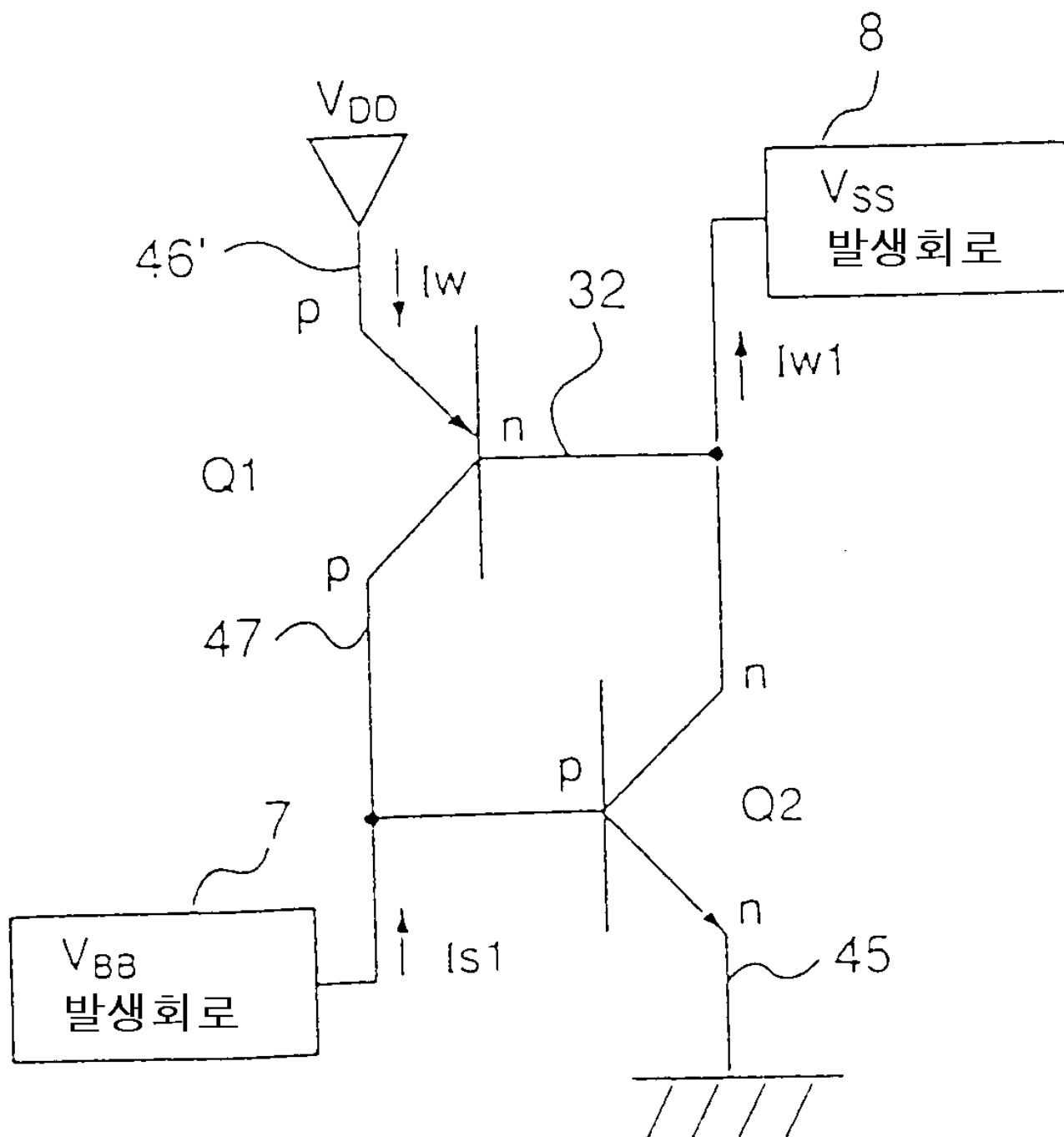
25b



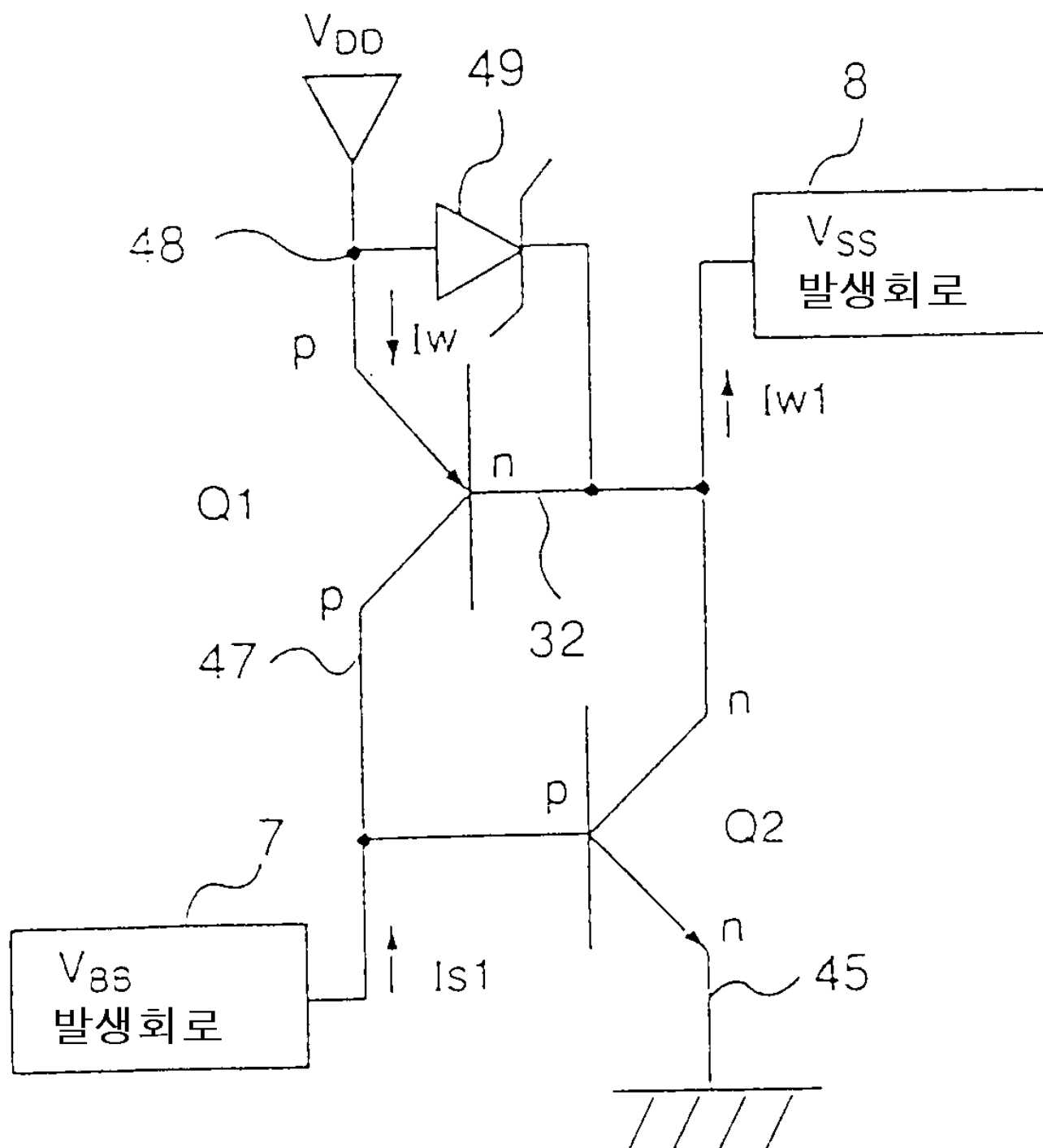
26a



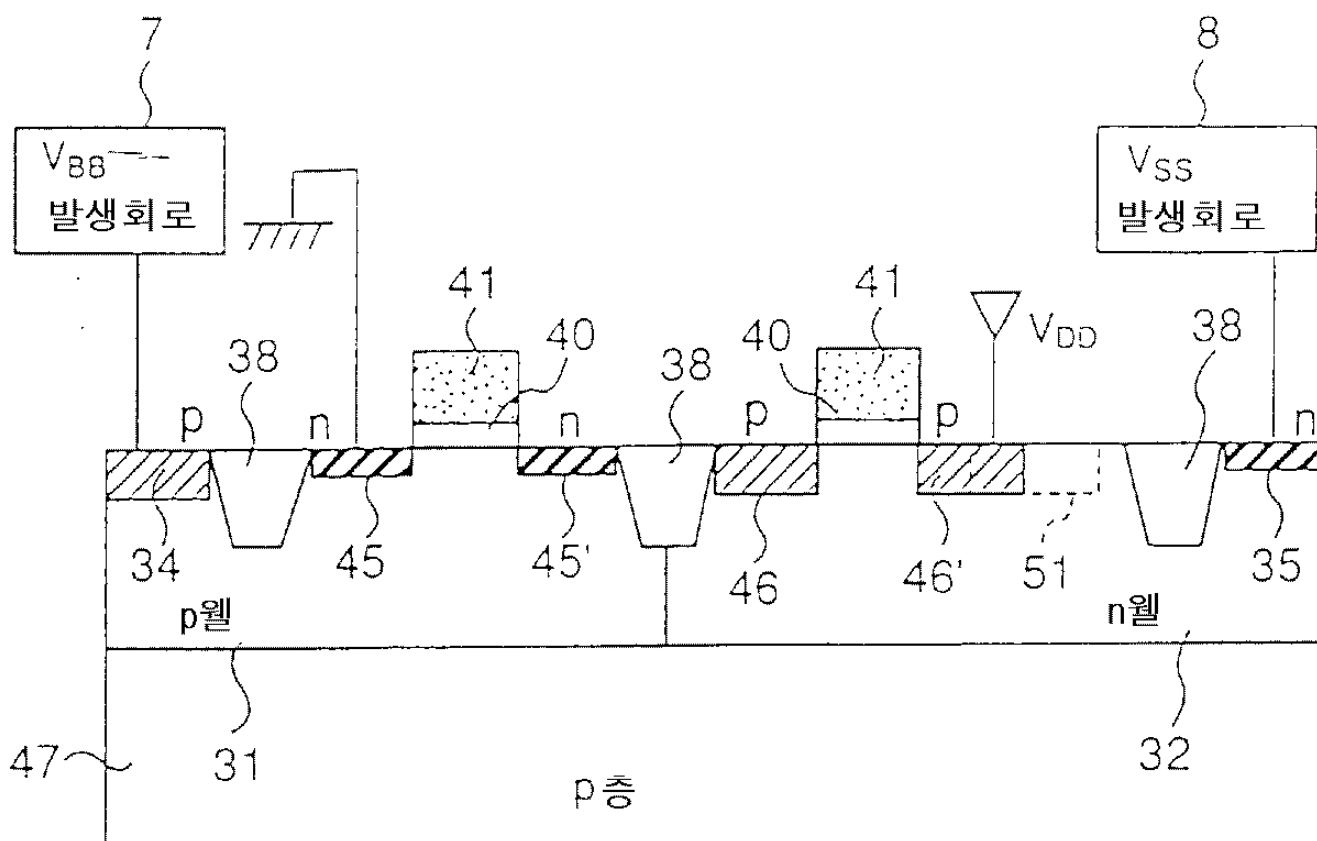
26b



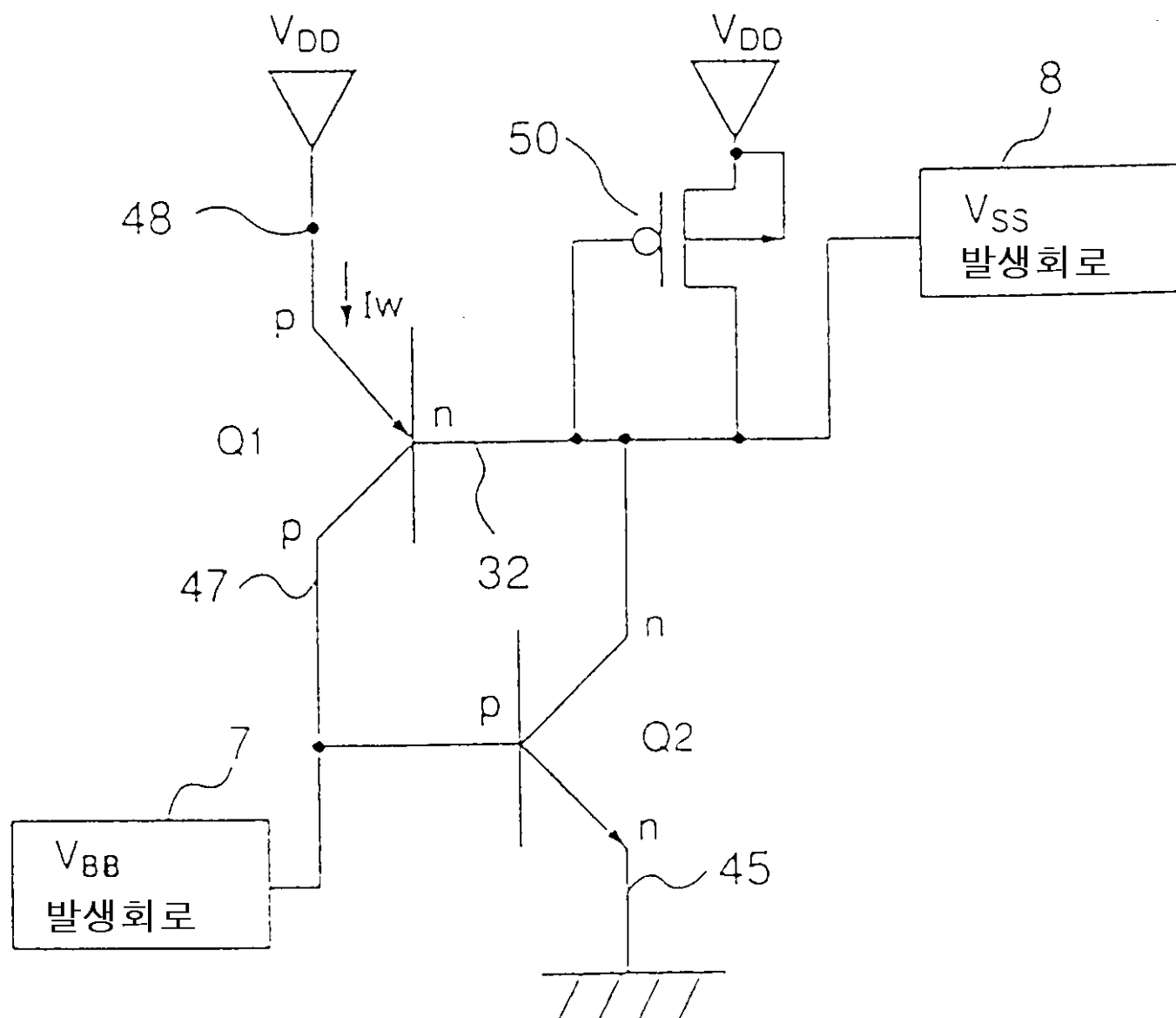
27b



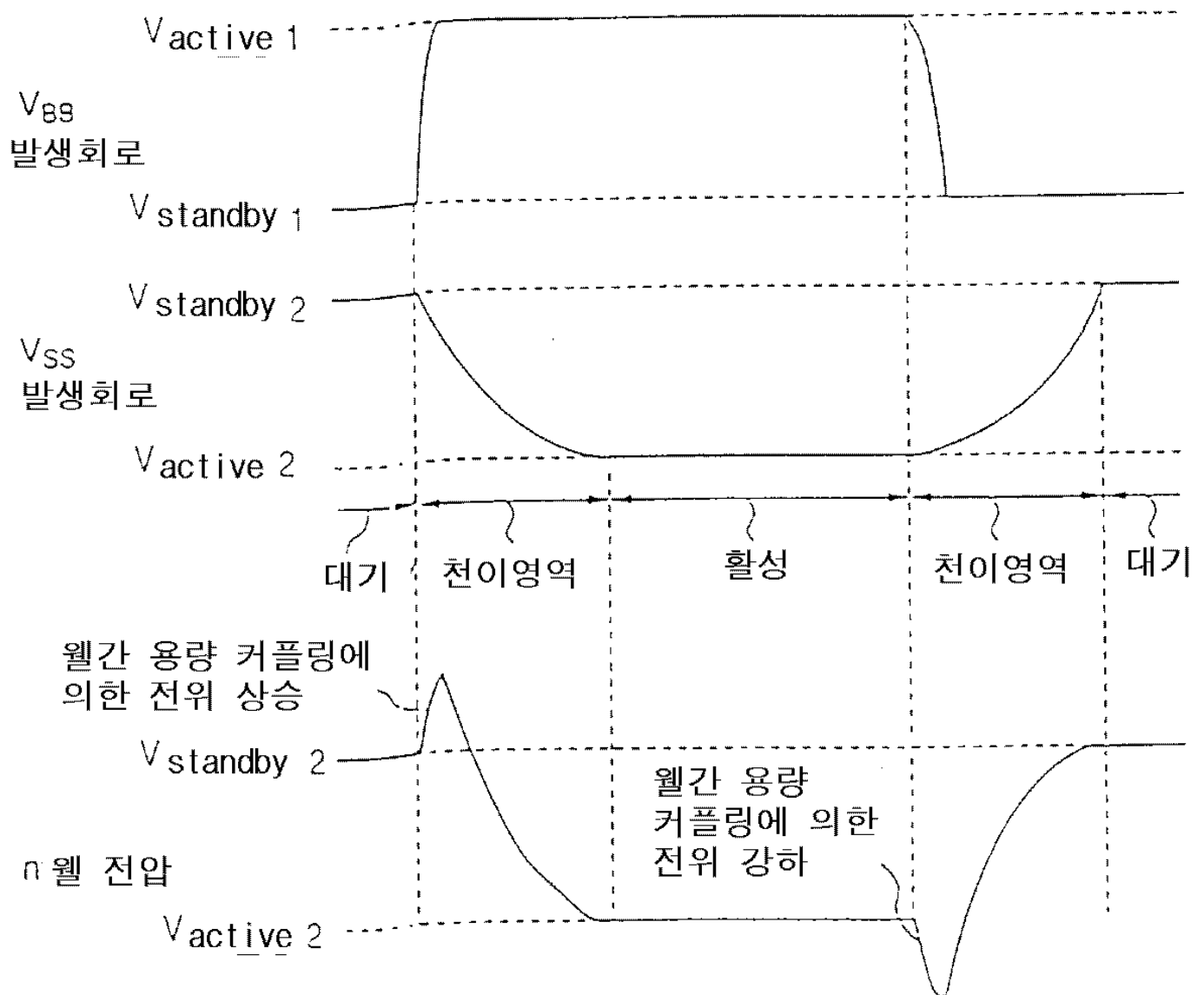
28a



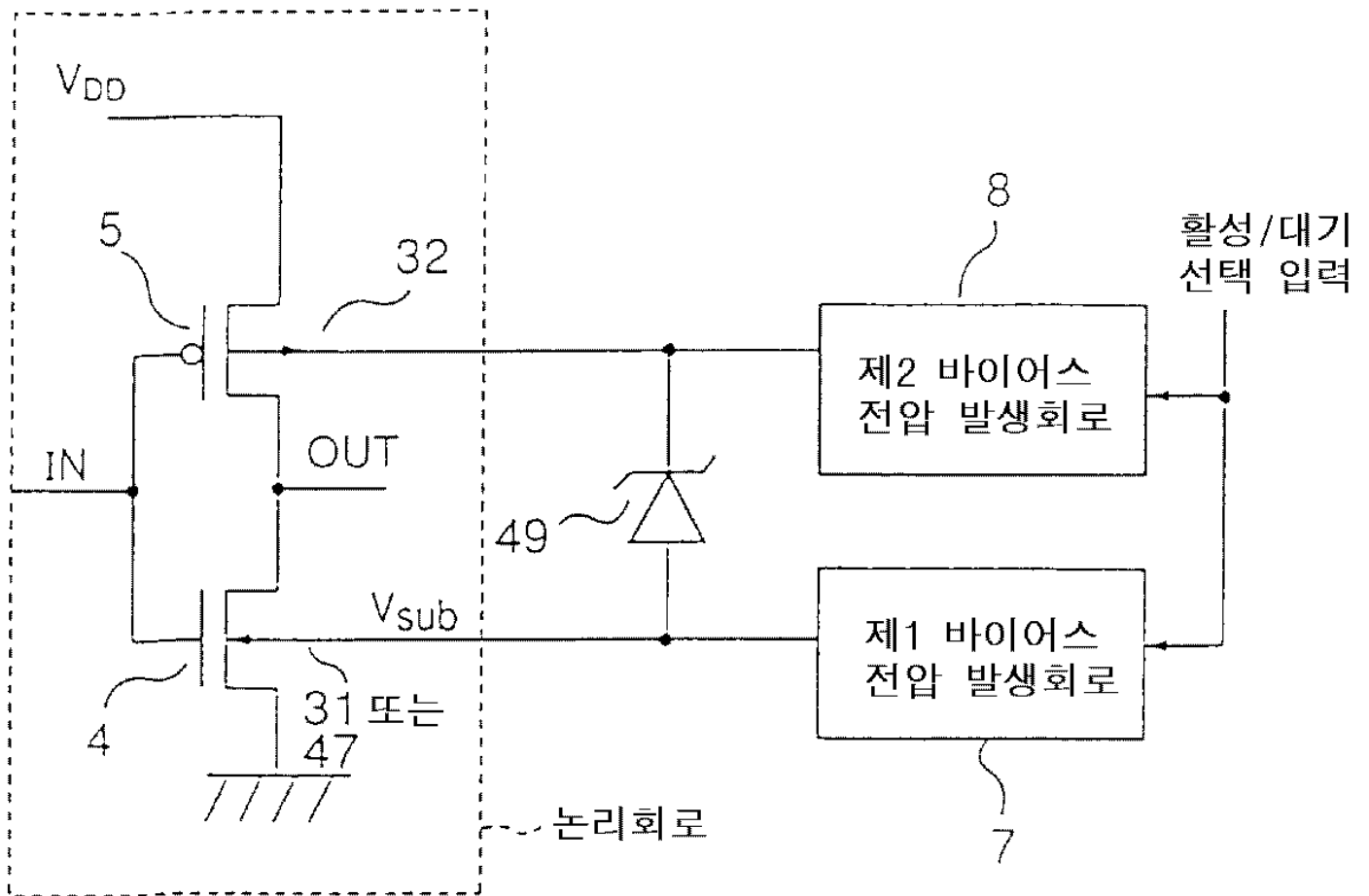
29b



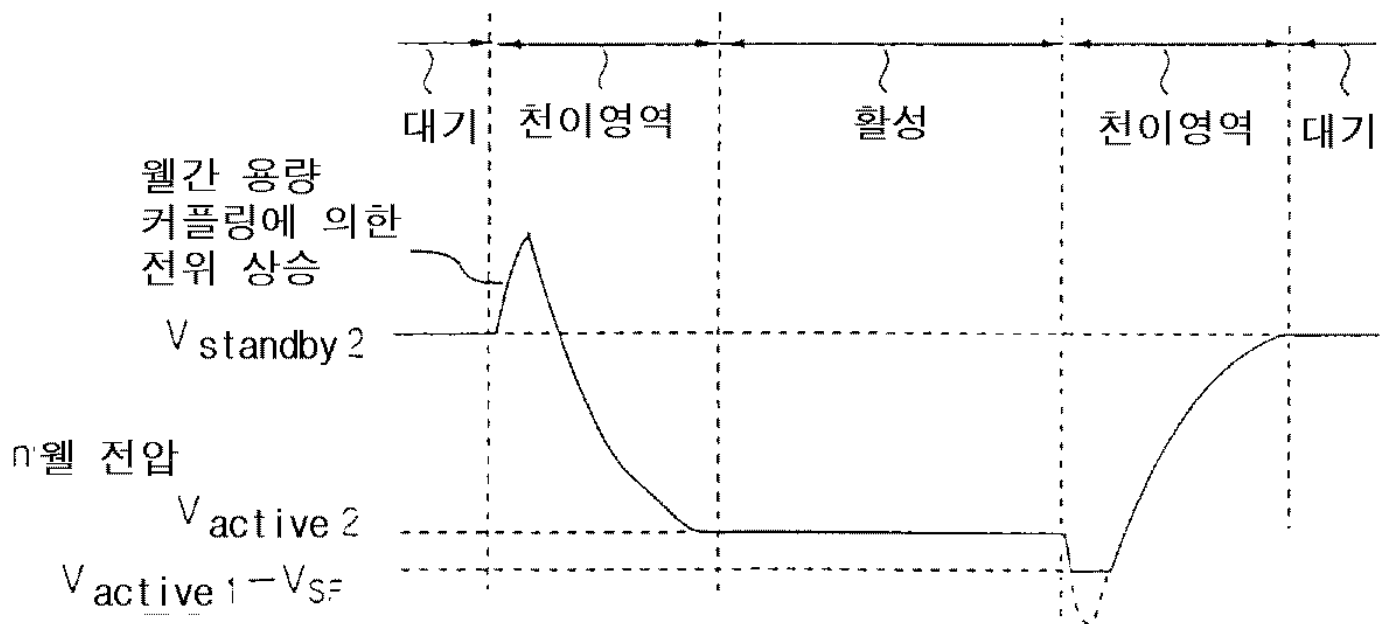
30b



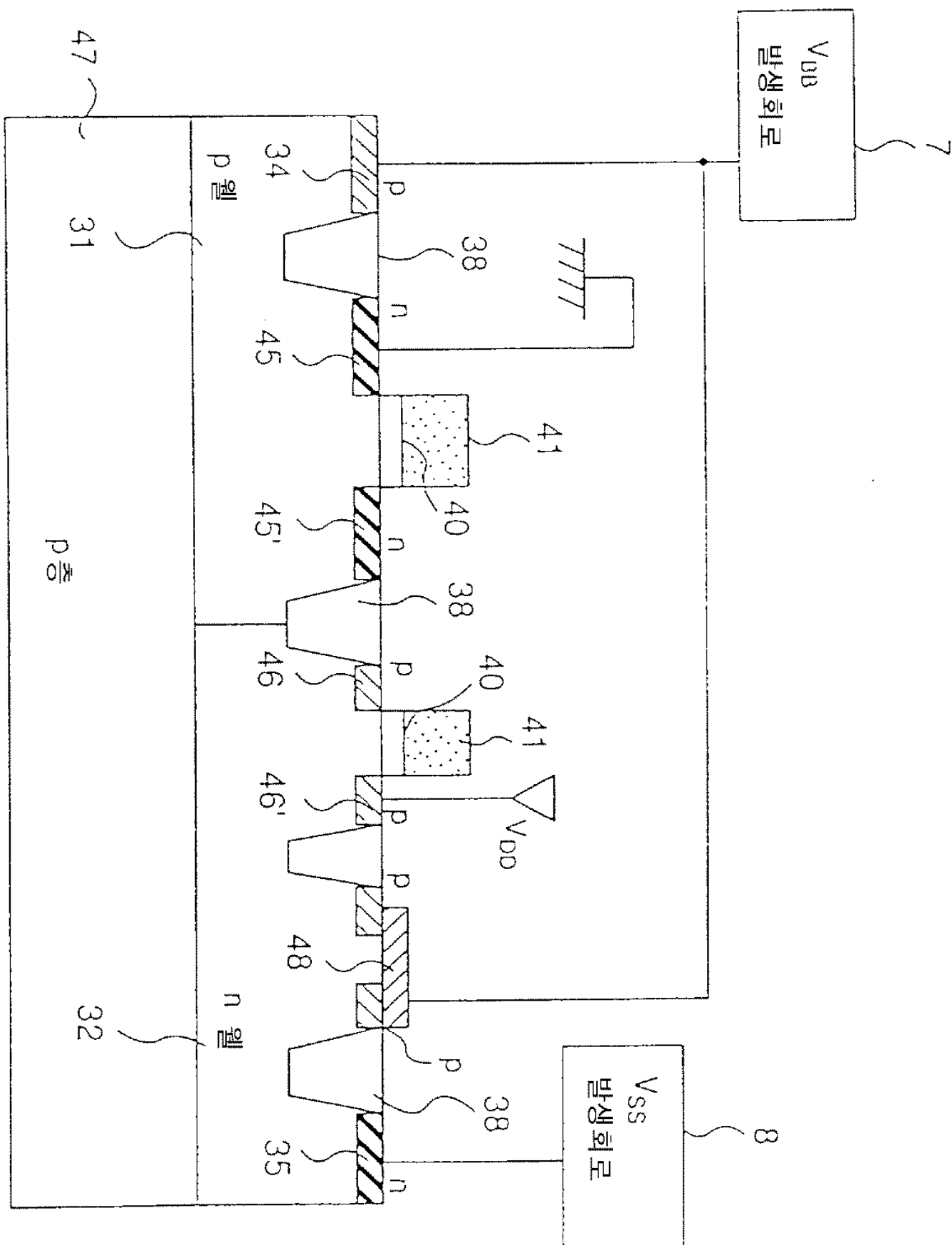
31a



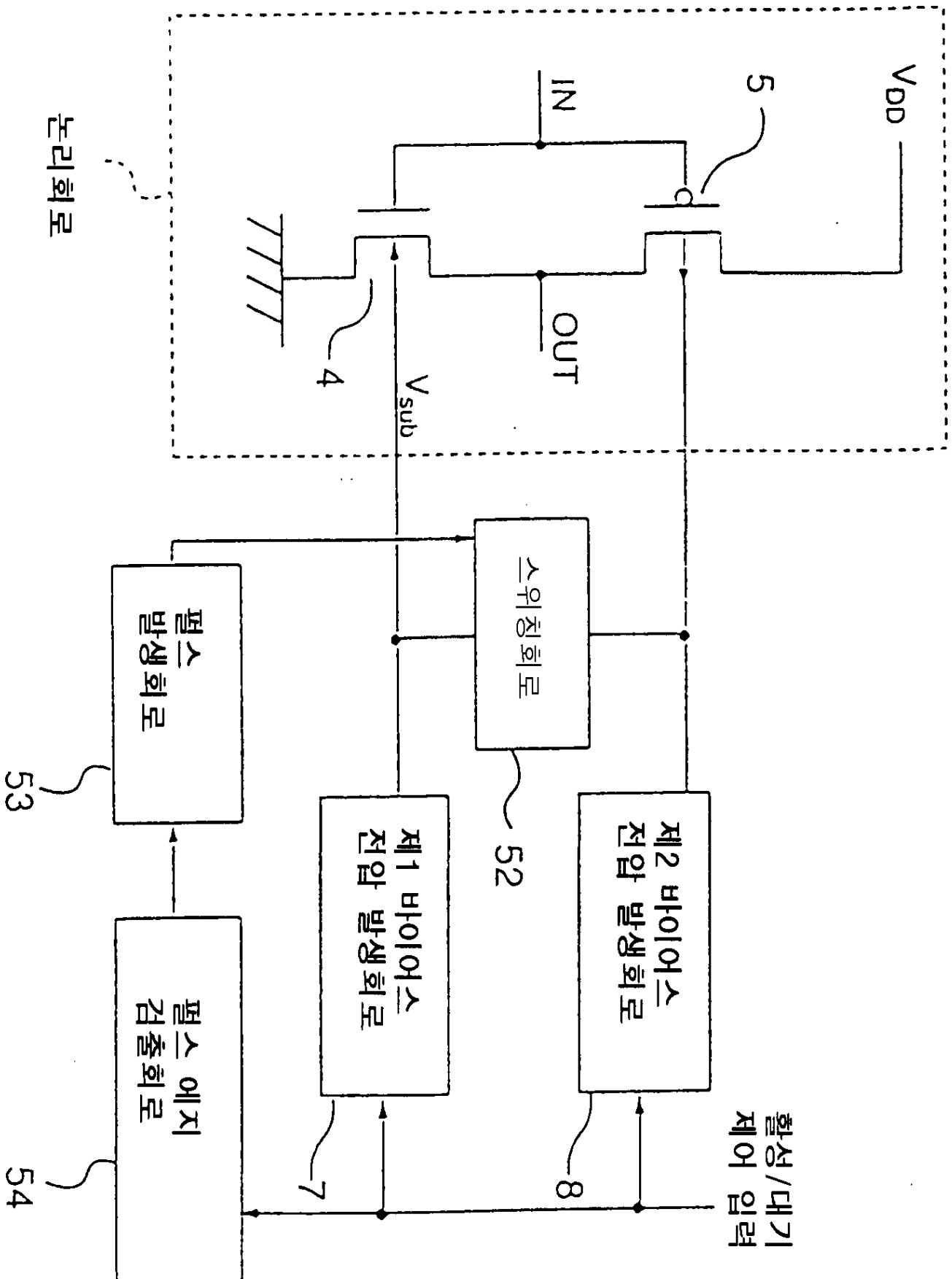
31b



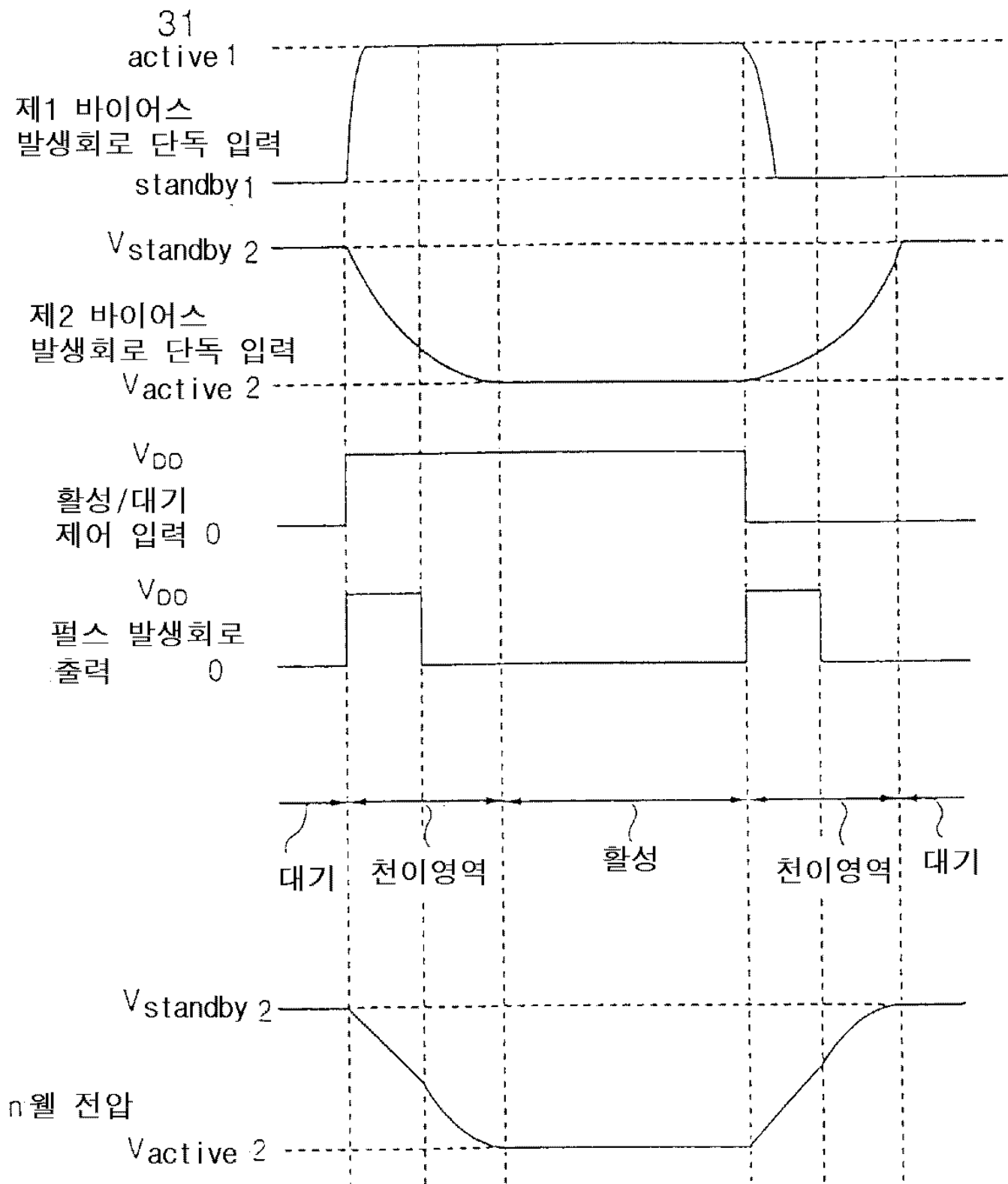
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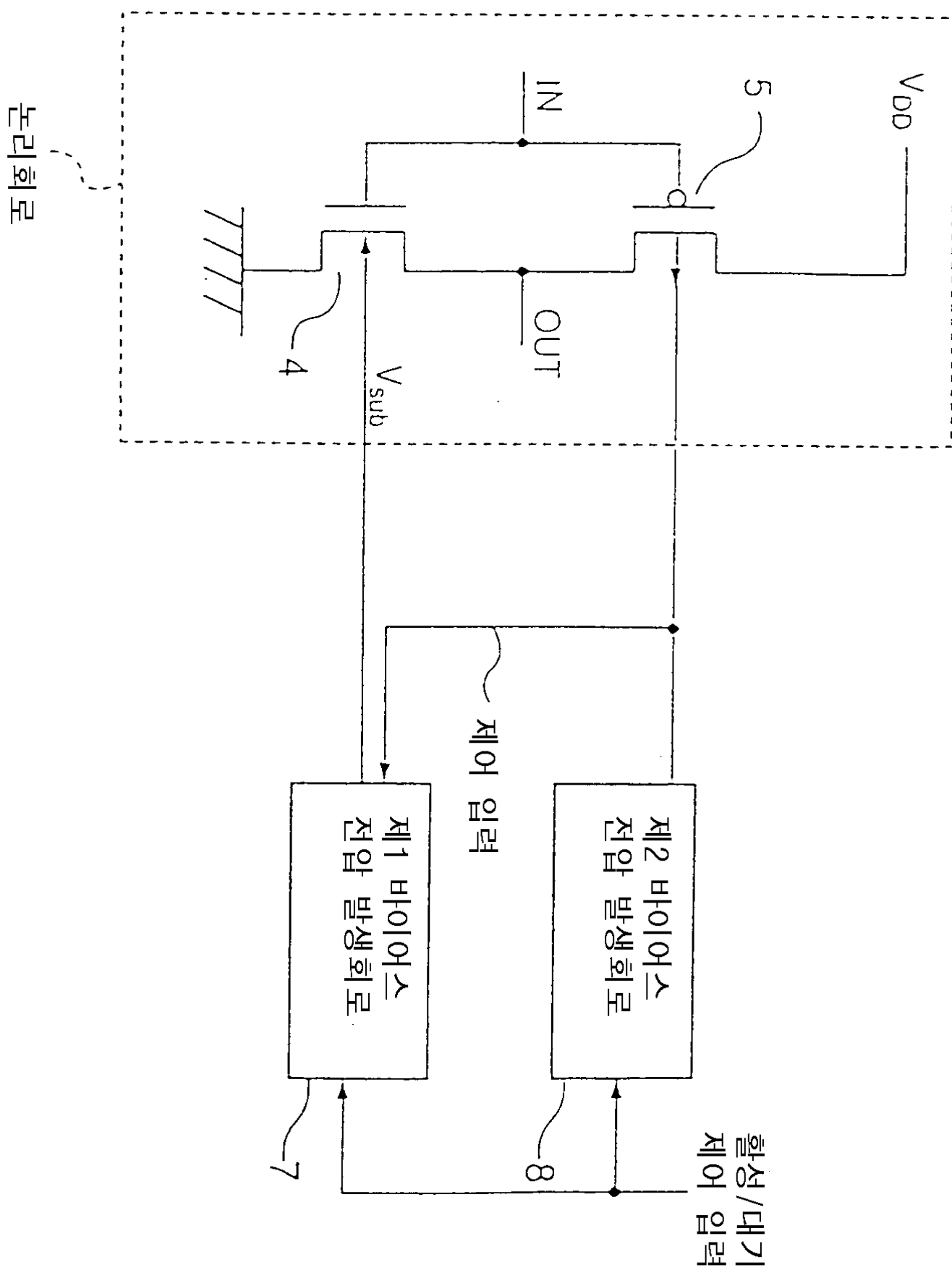


34

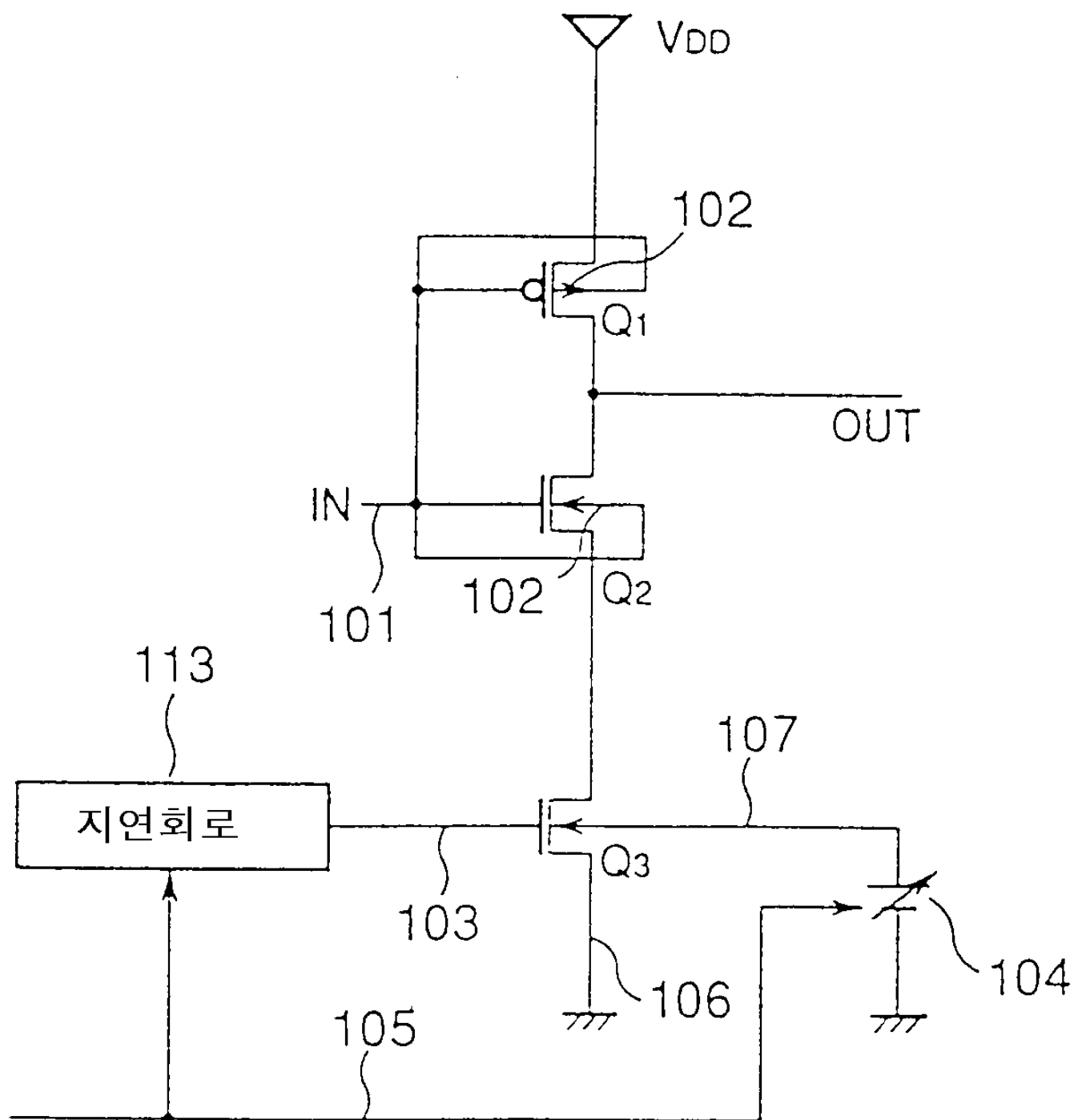


35

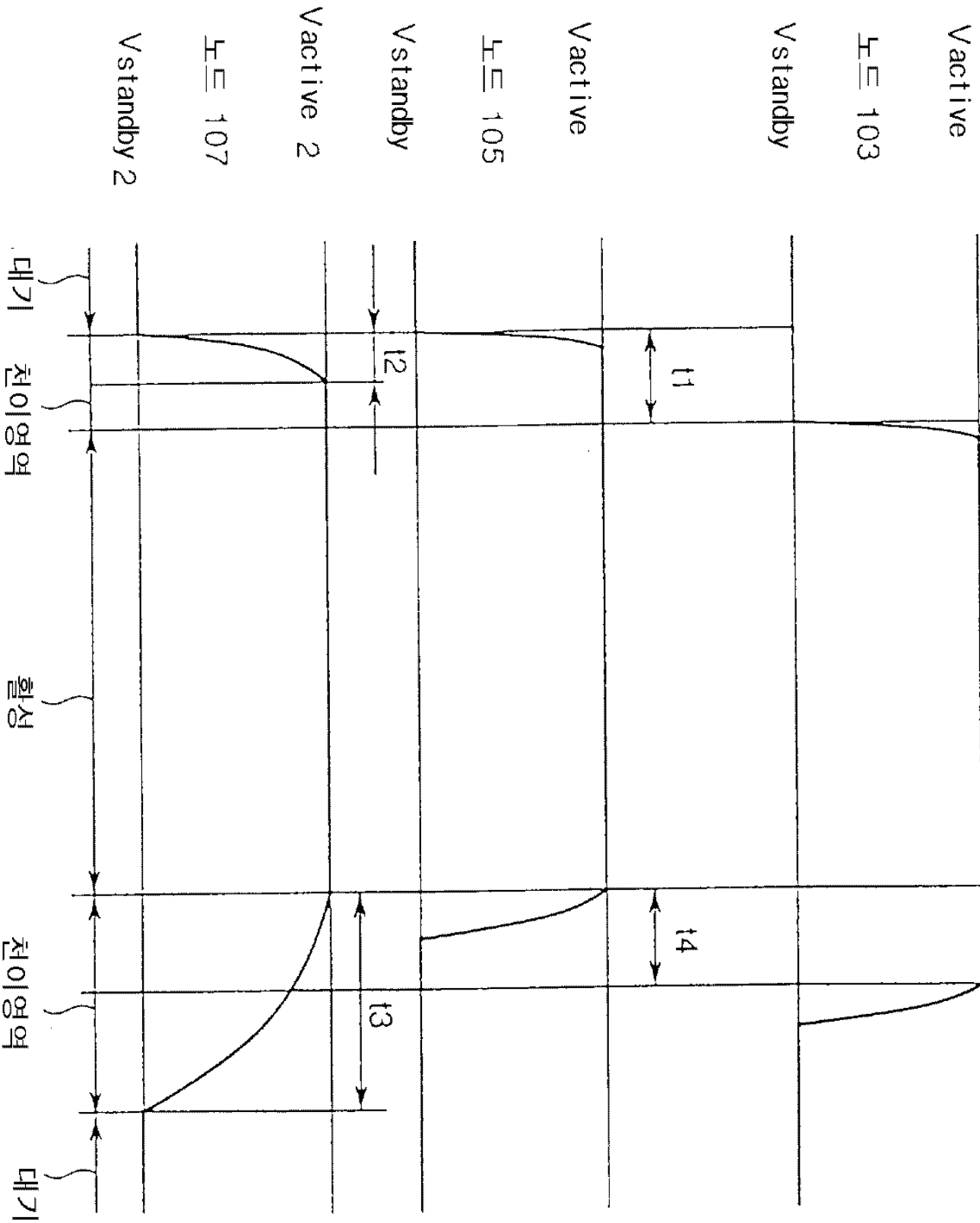


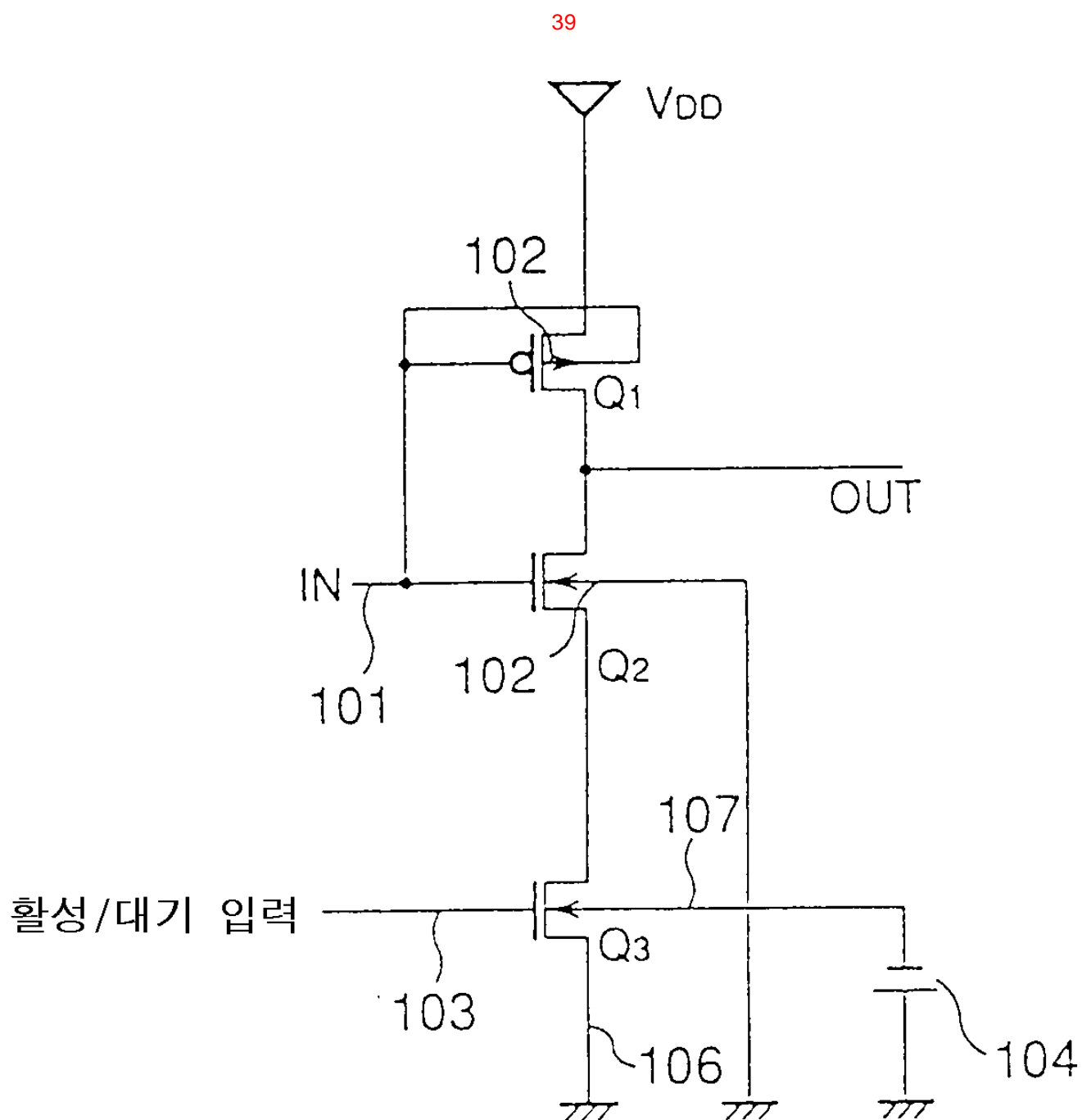


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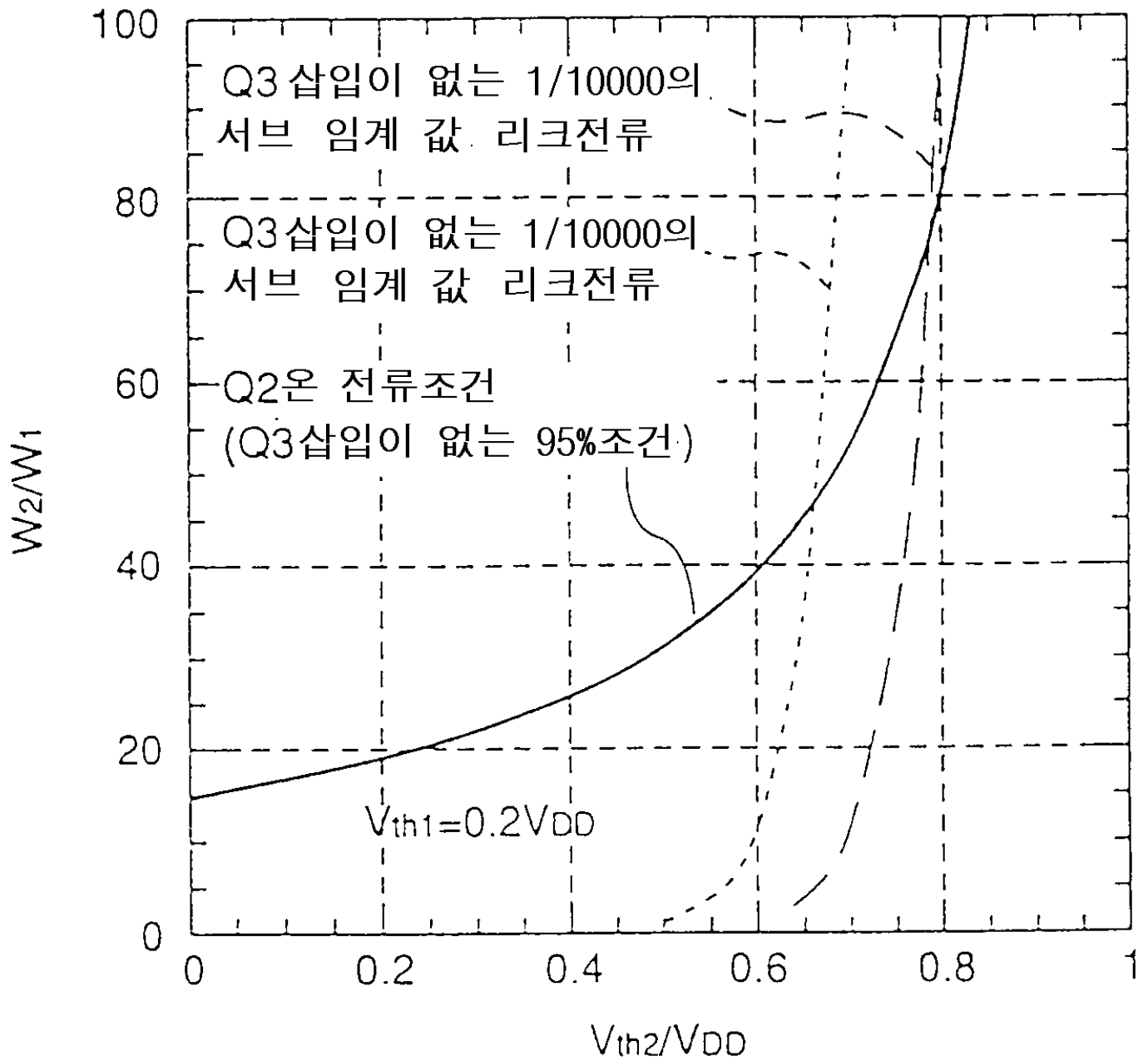


38

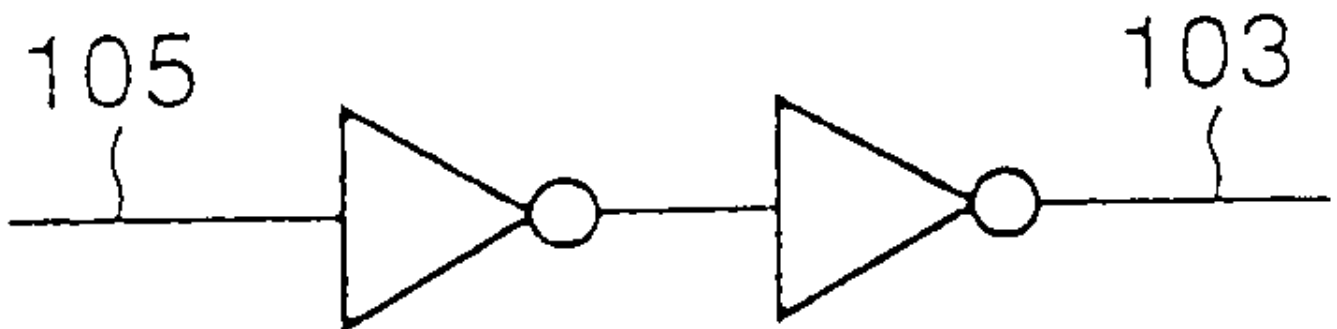




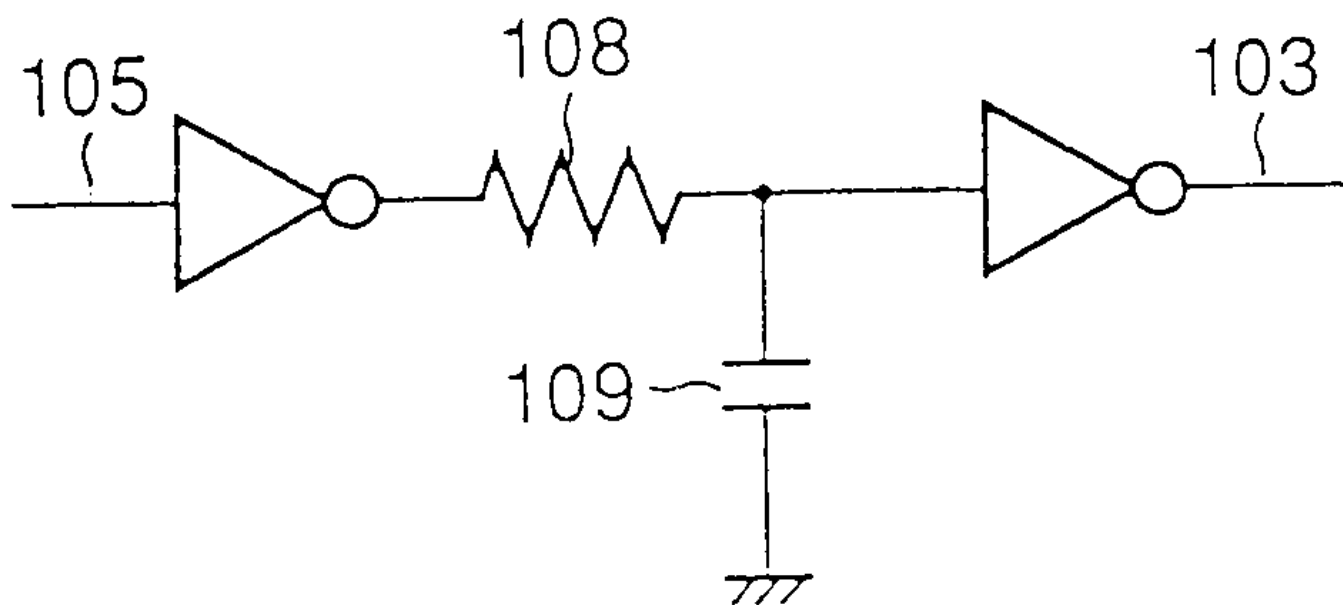
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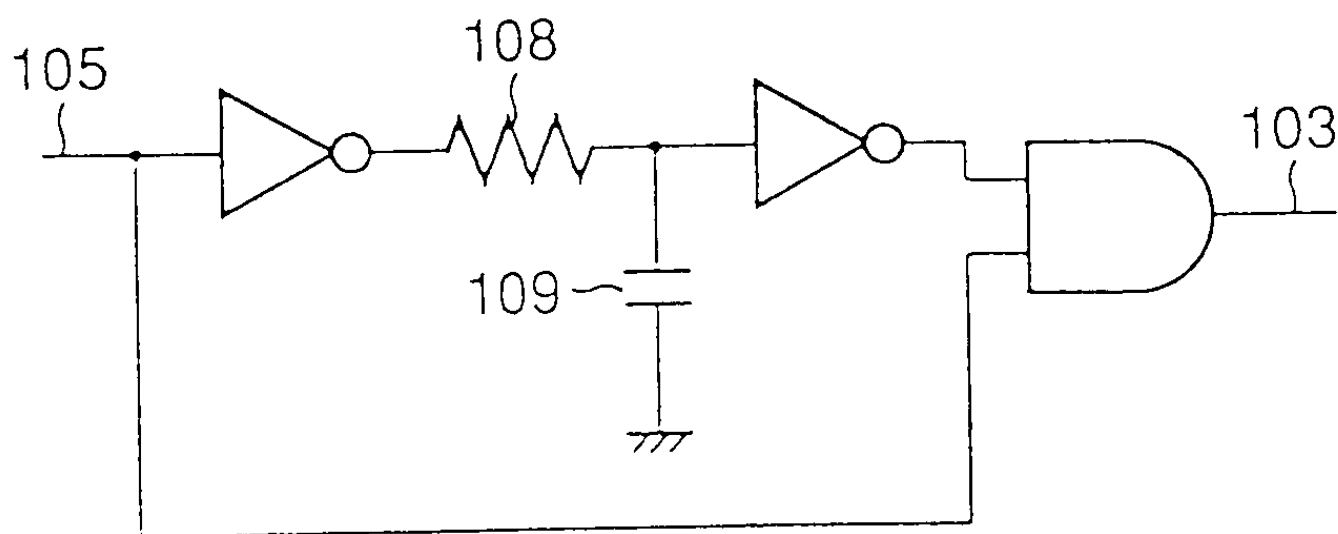
41a



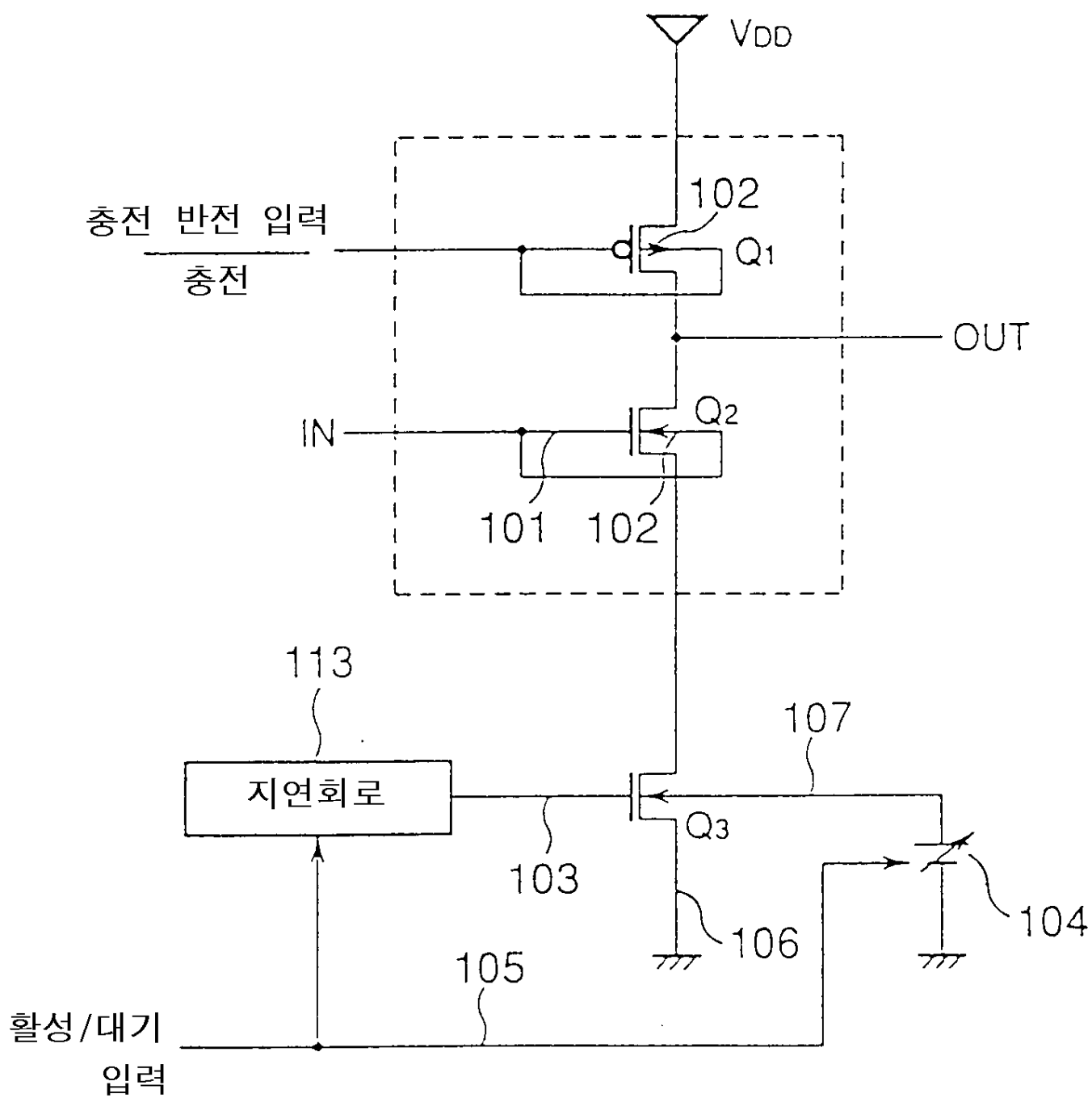
41b

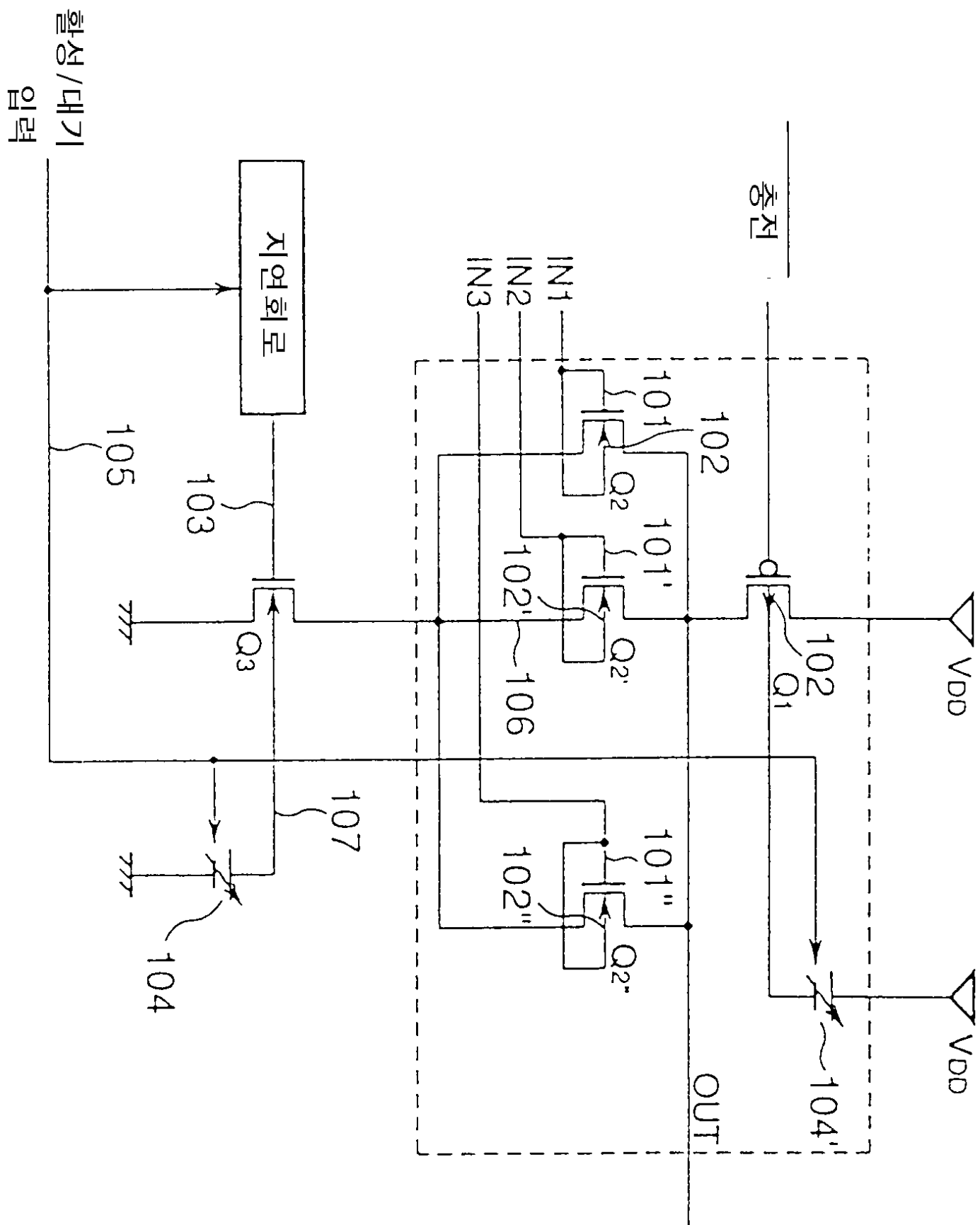


41c

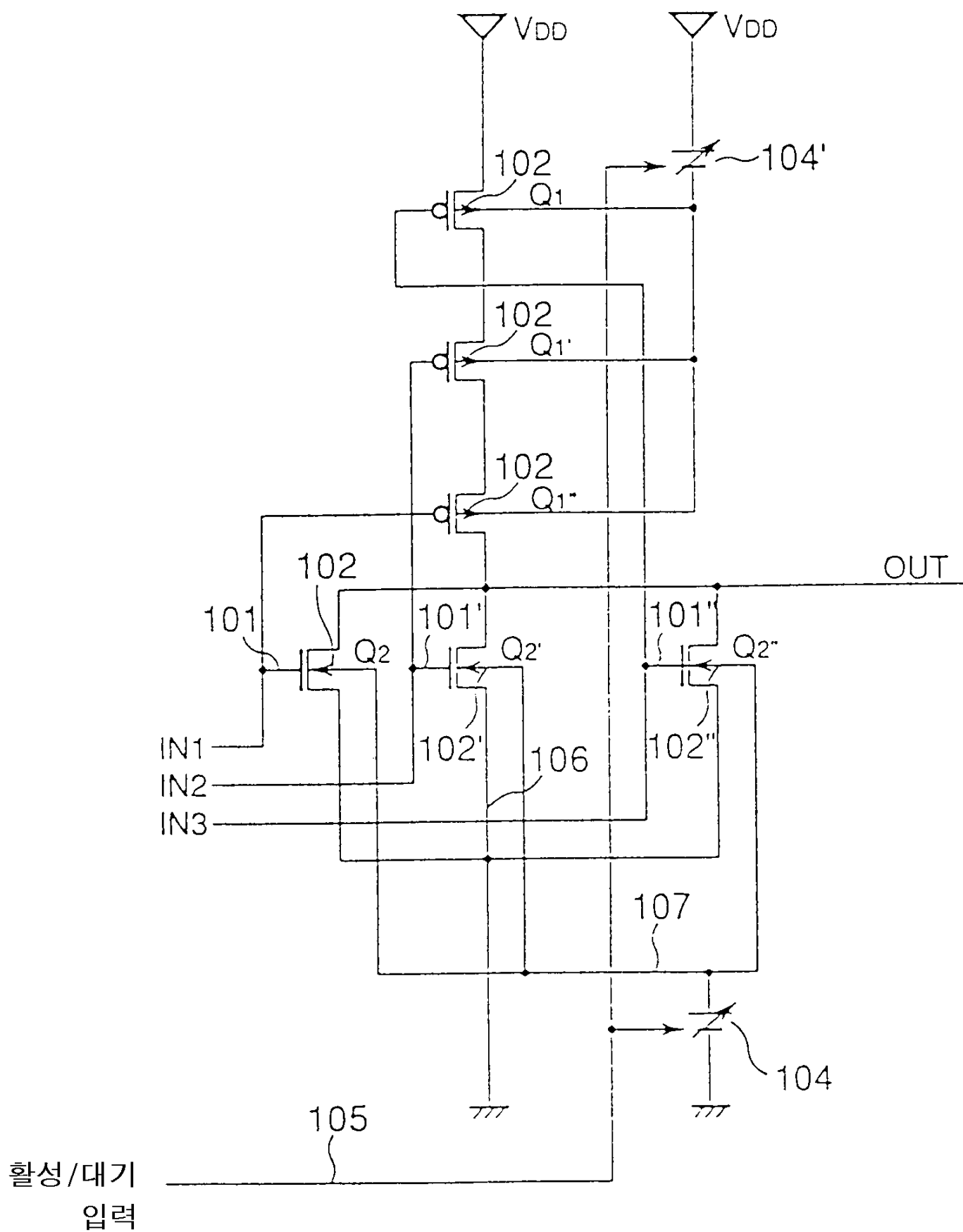


42

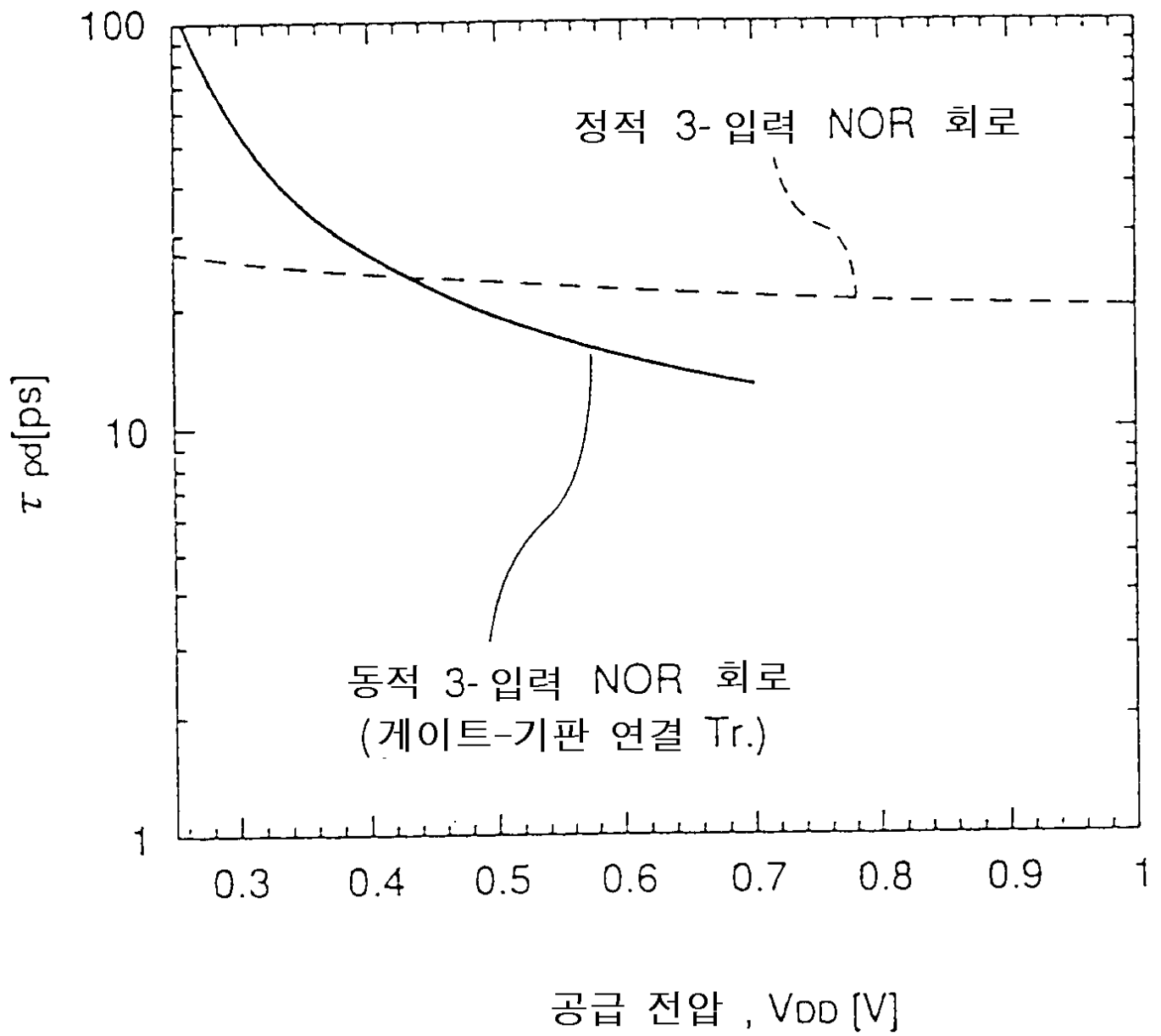




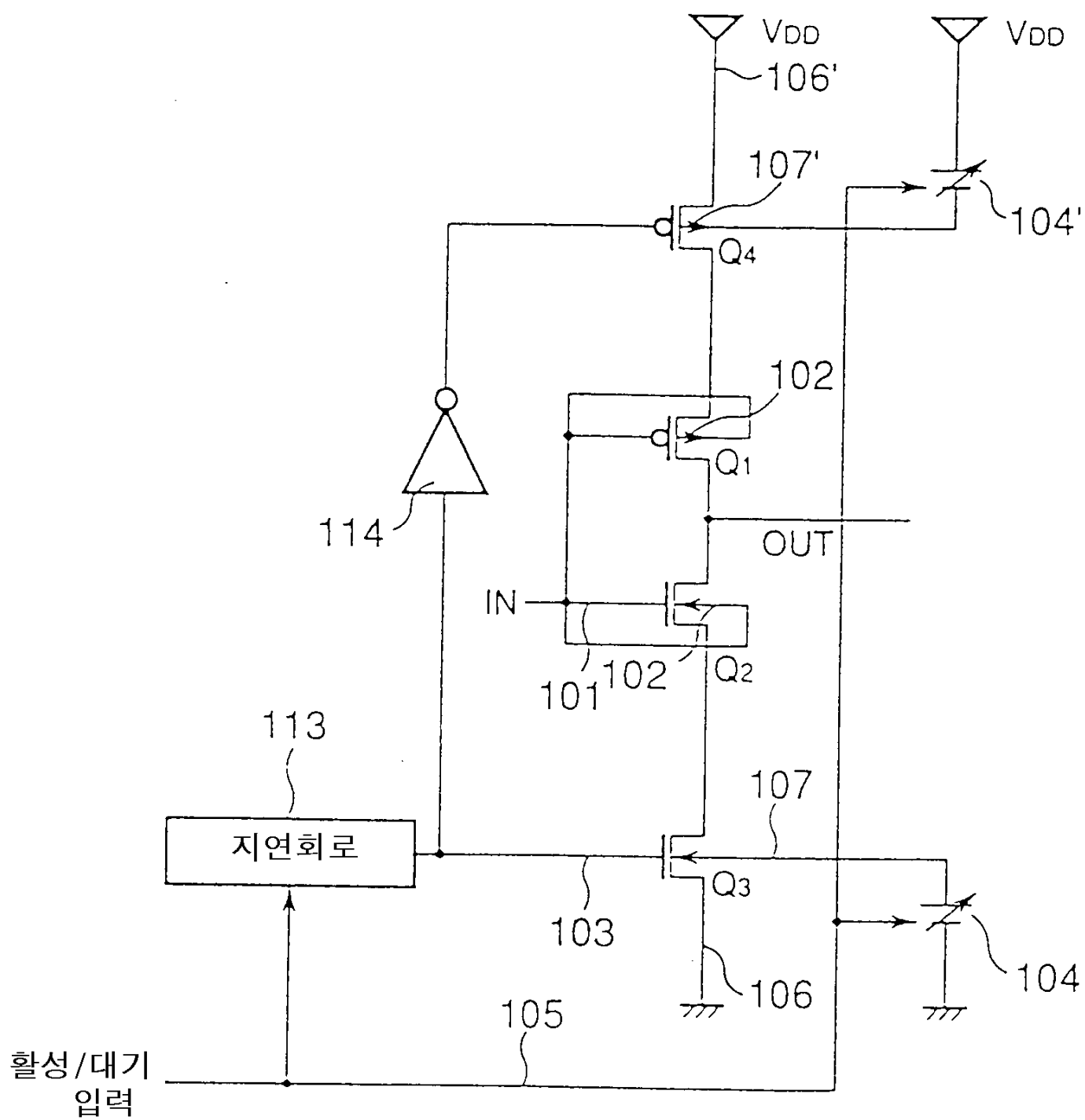
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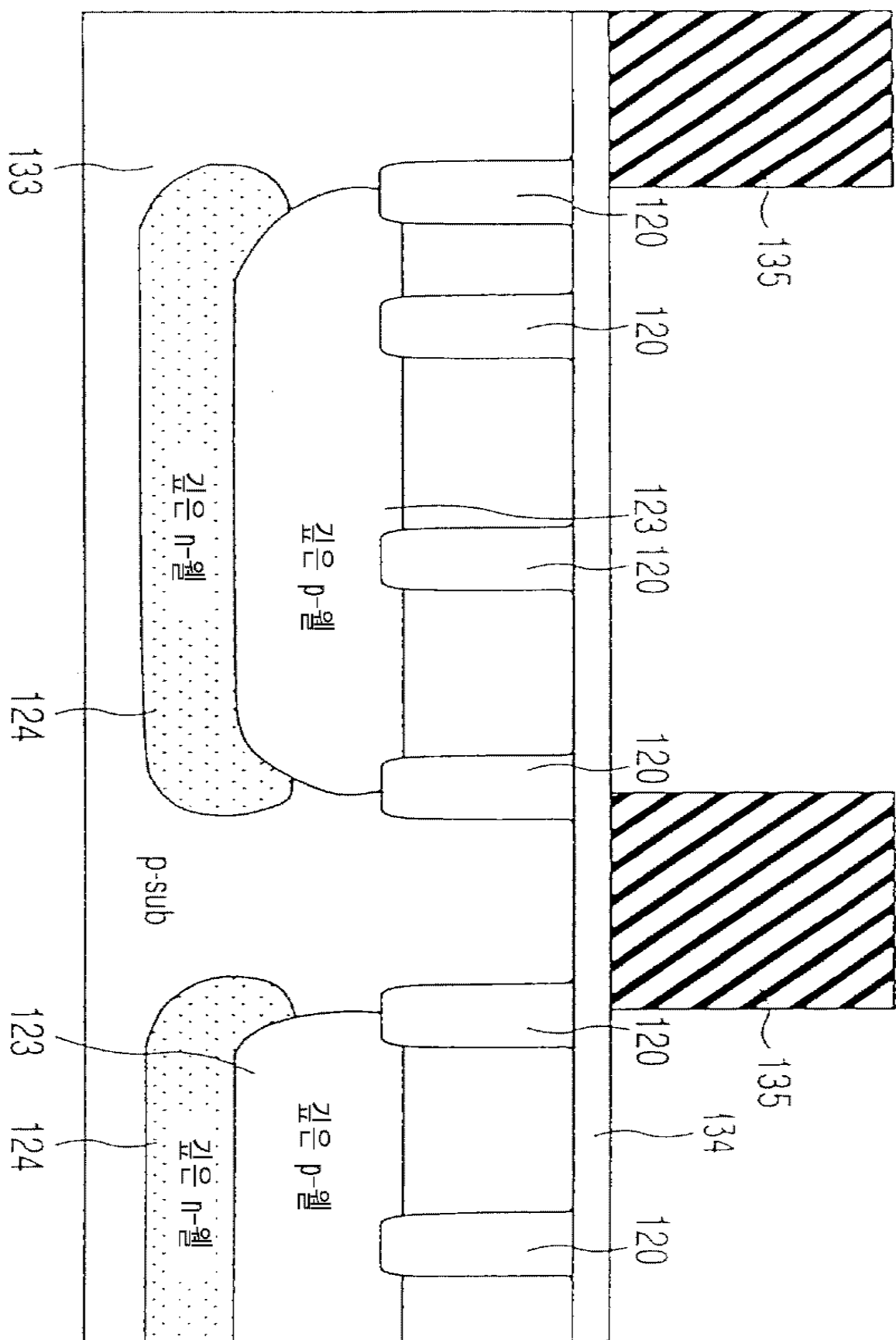


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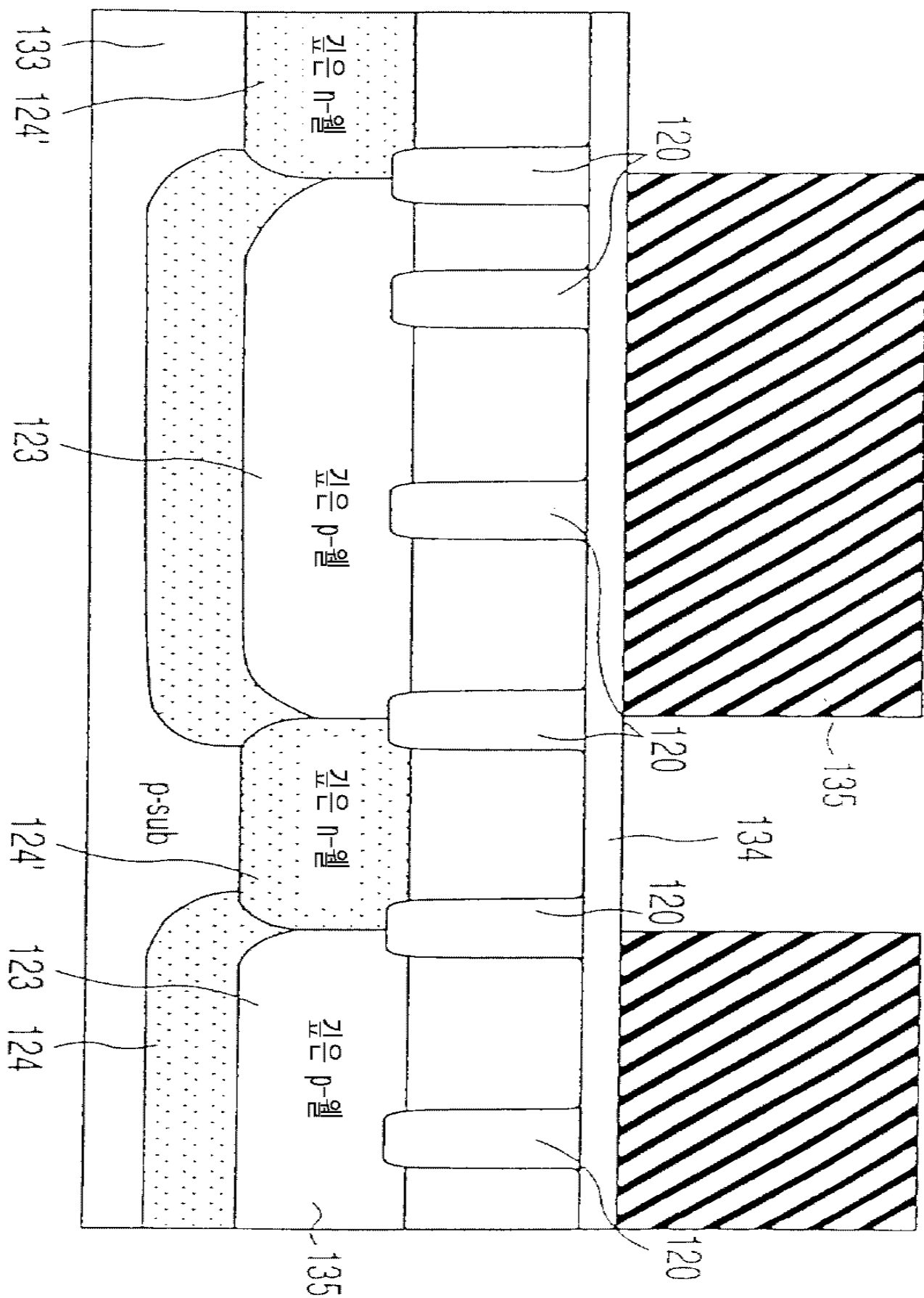


46

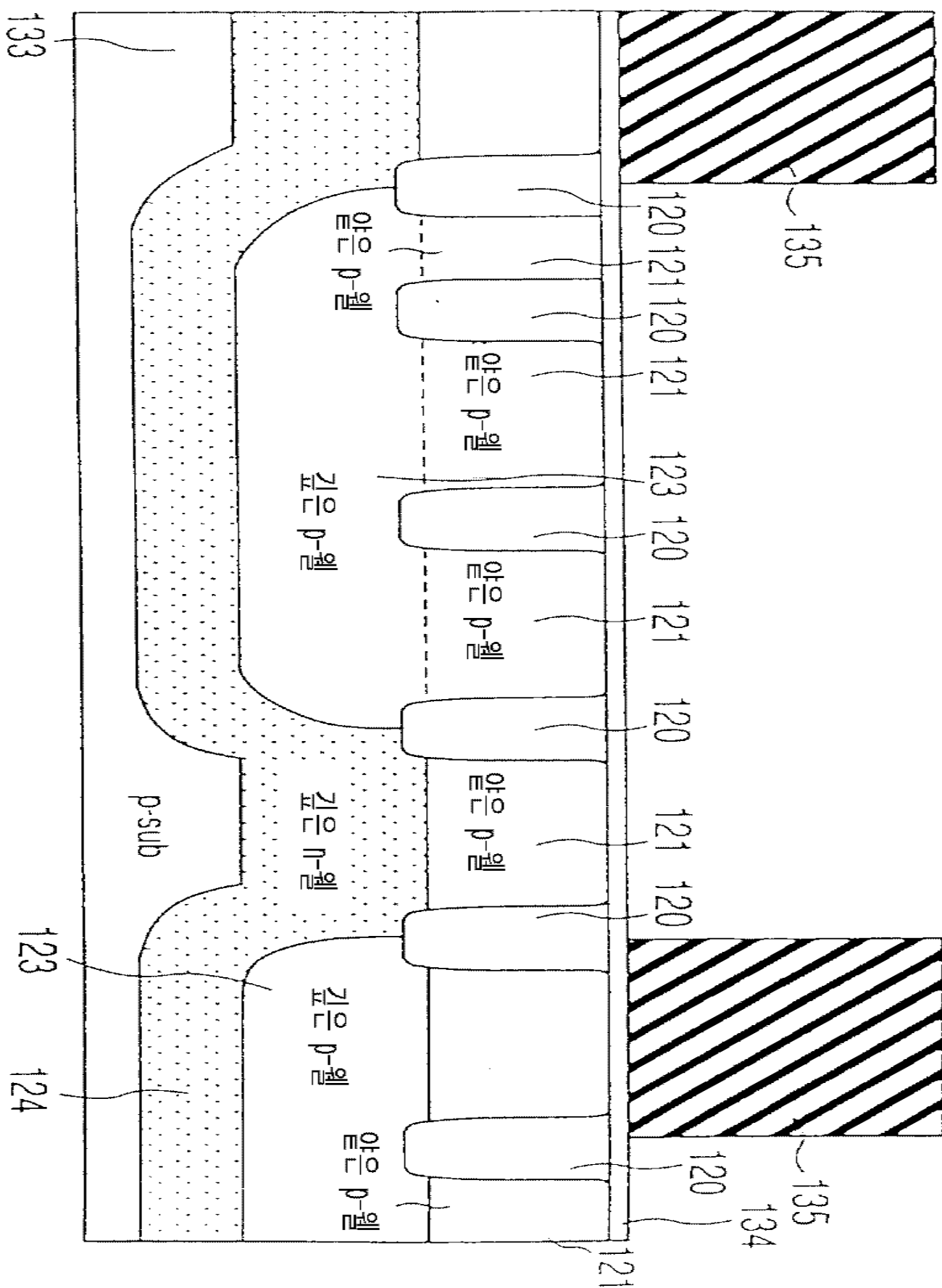




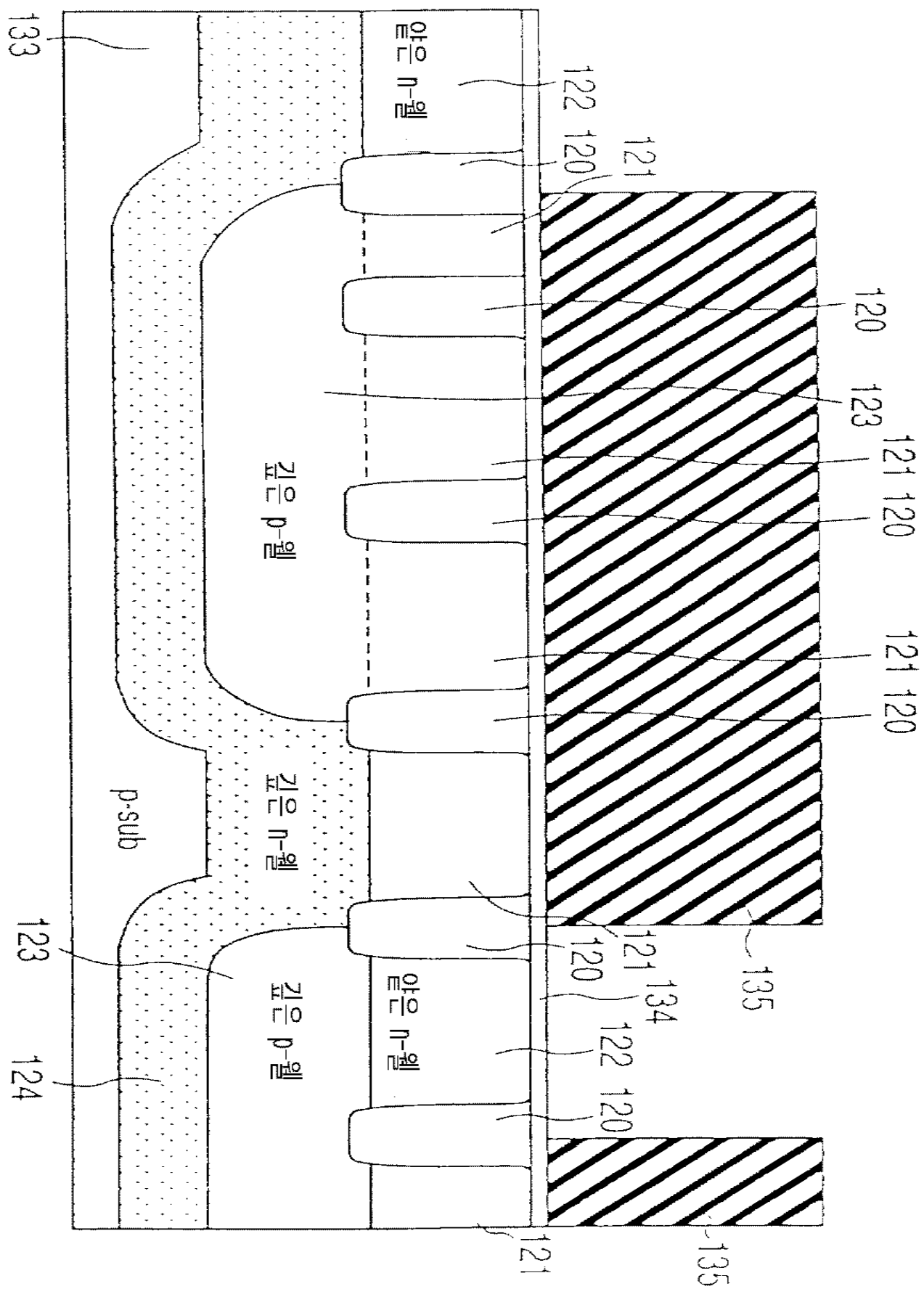
49



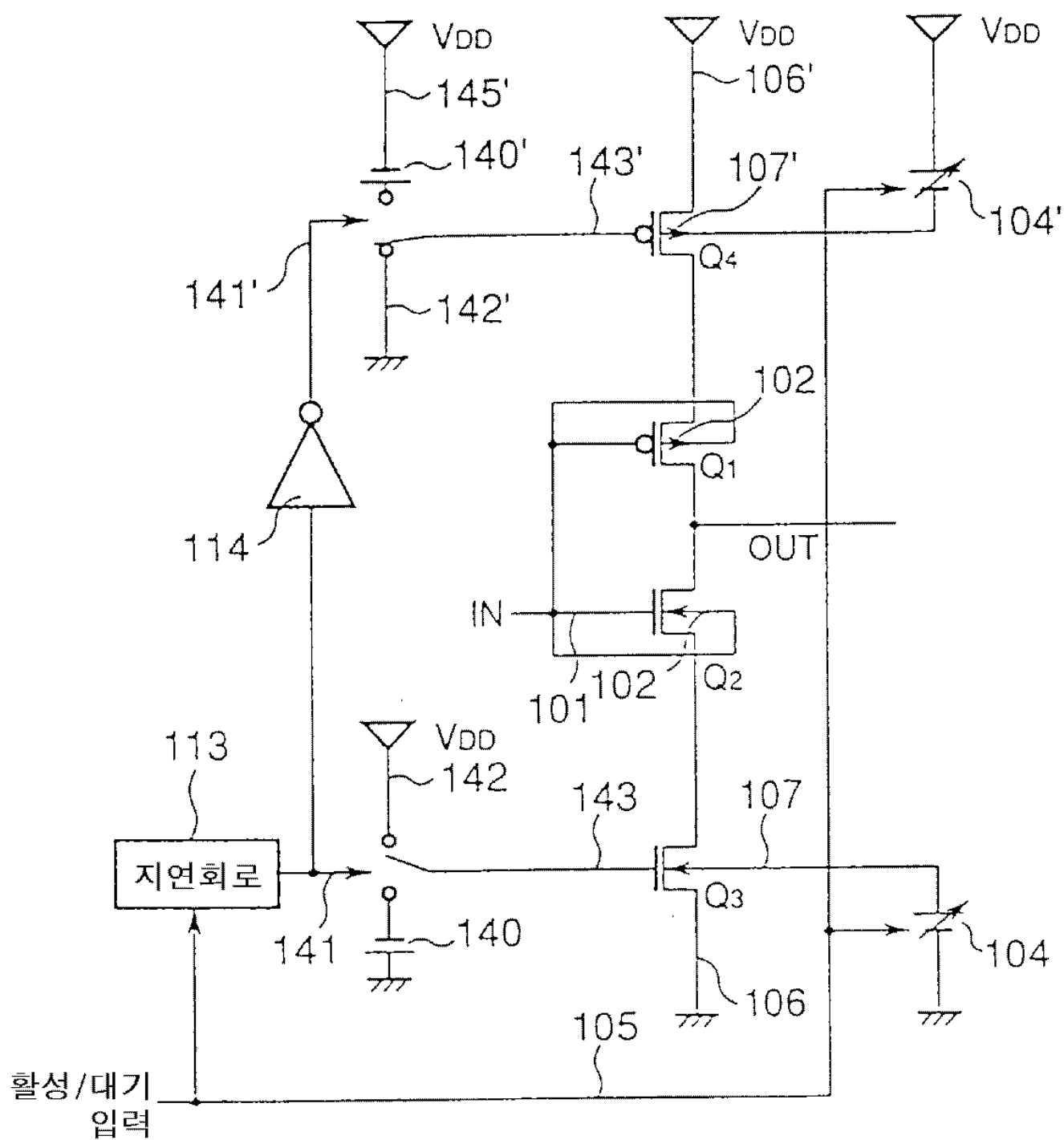
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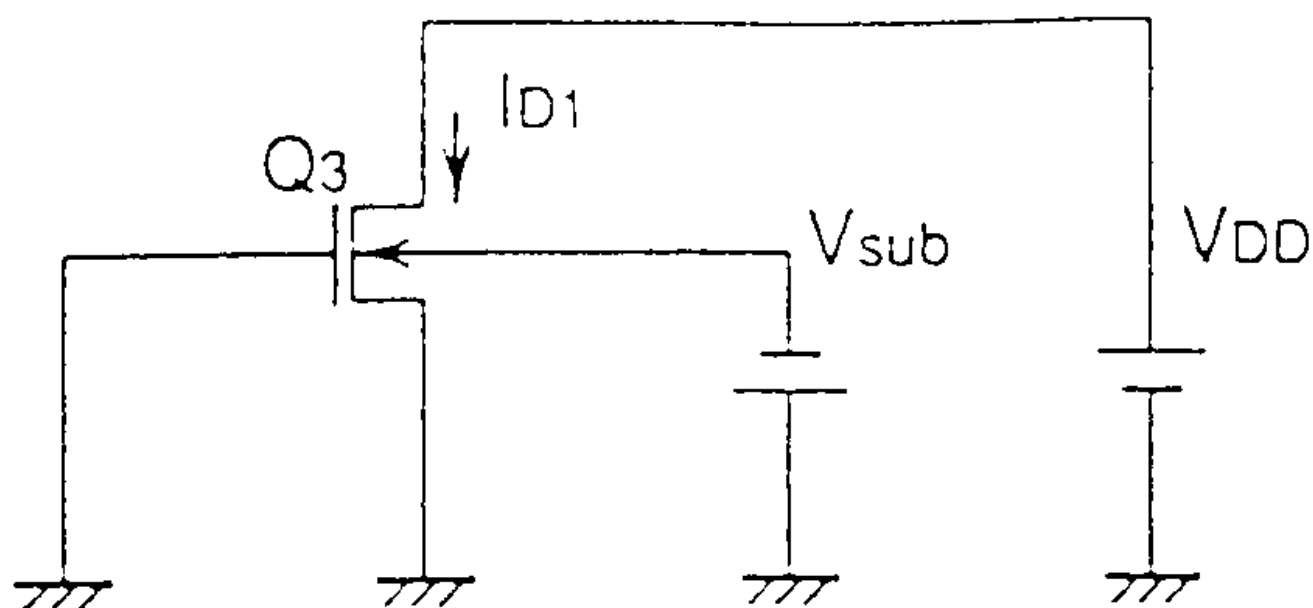
51



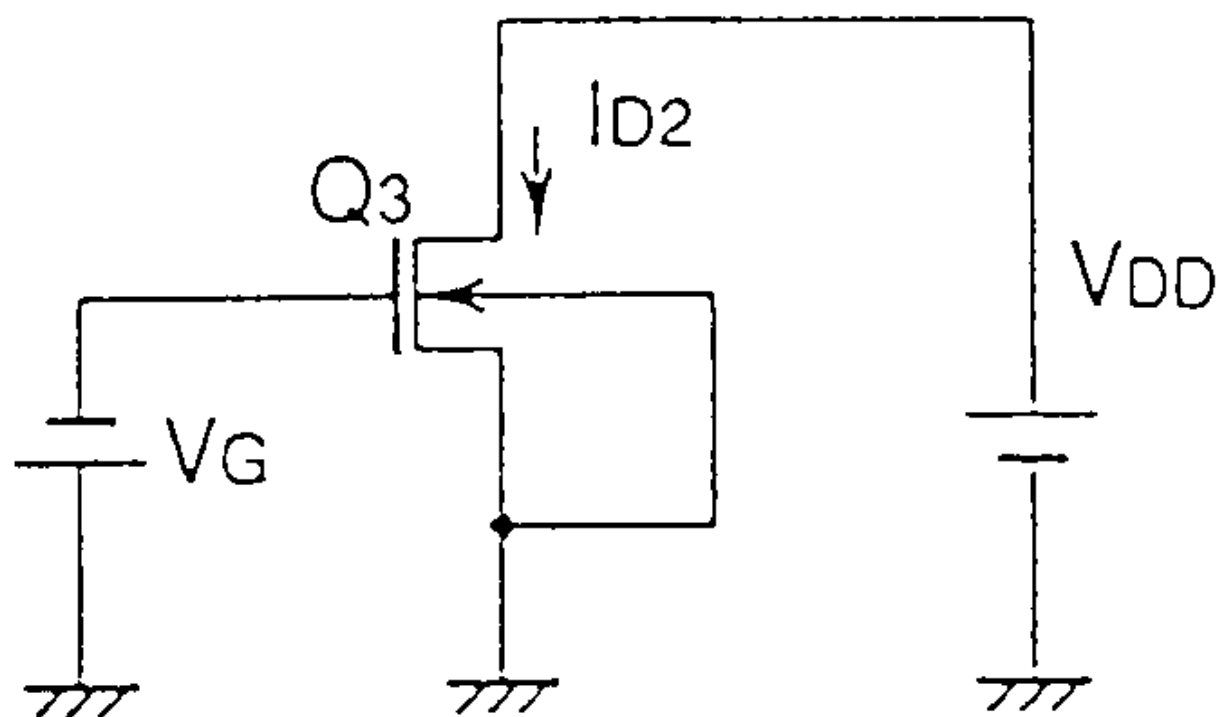
52



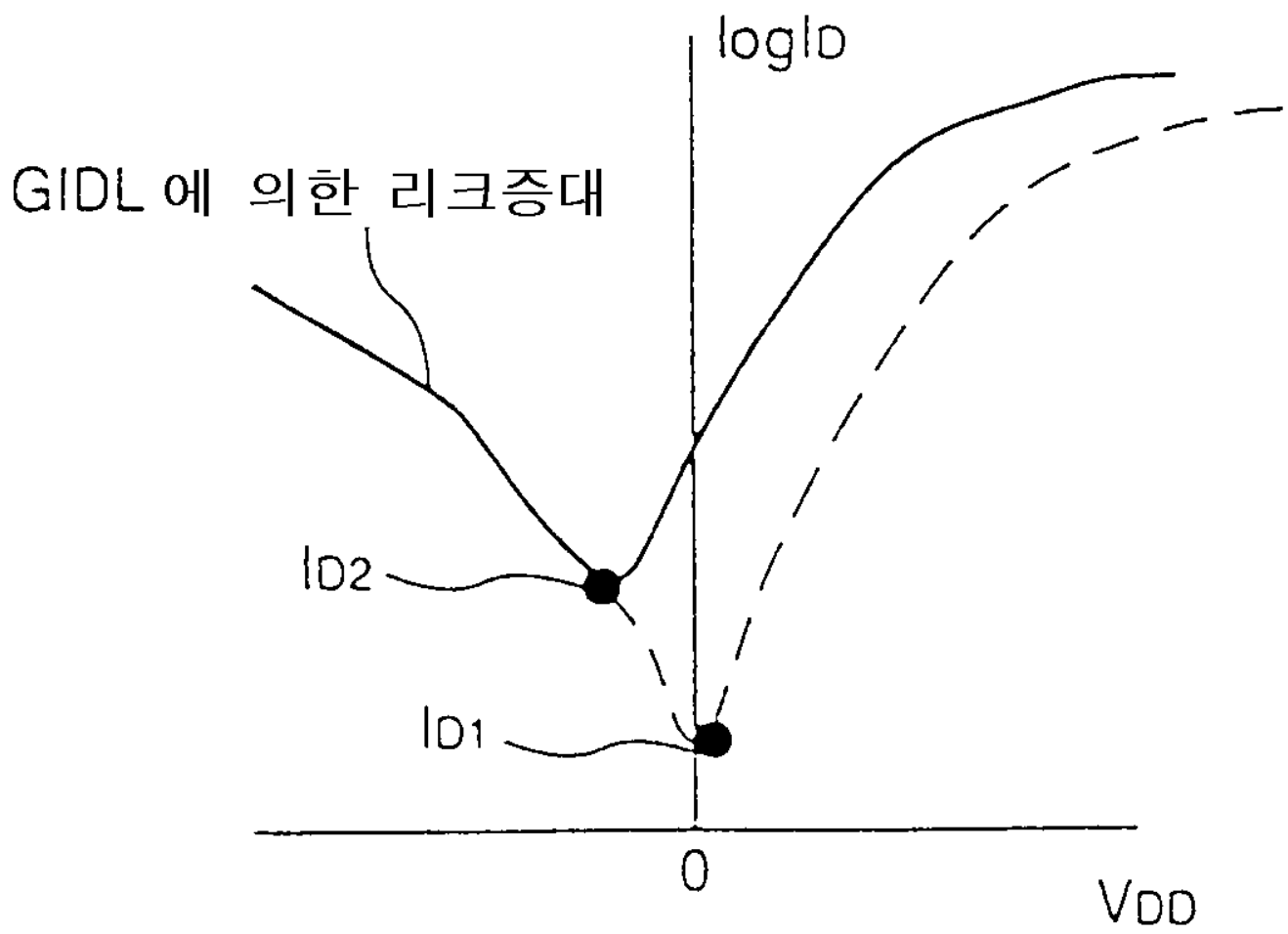
53a

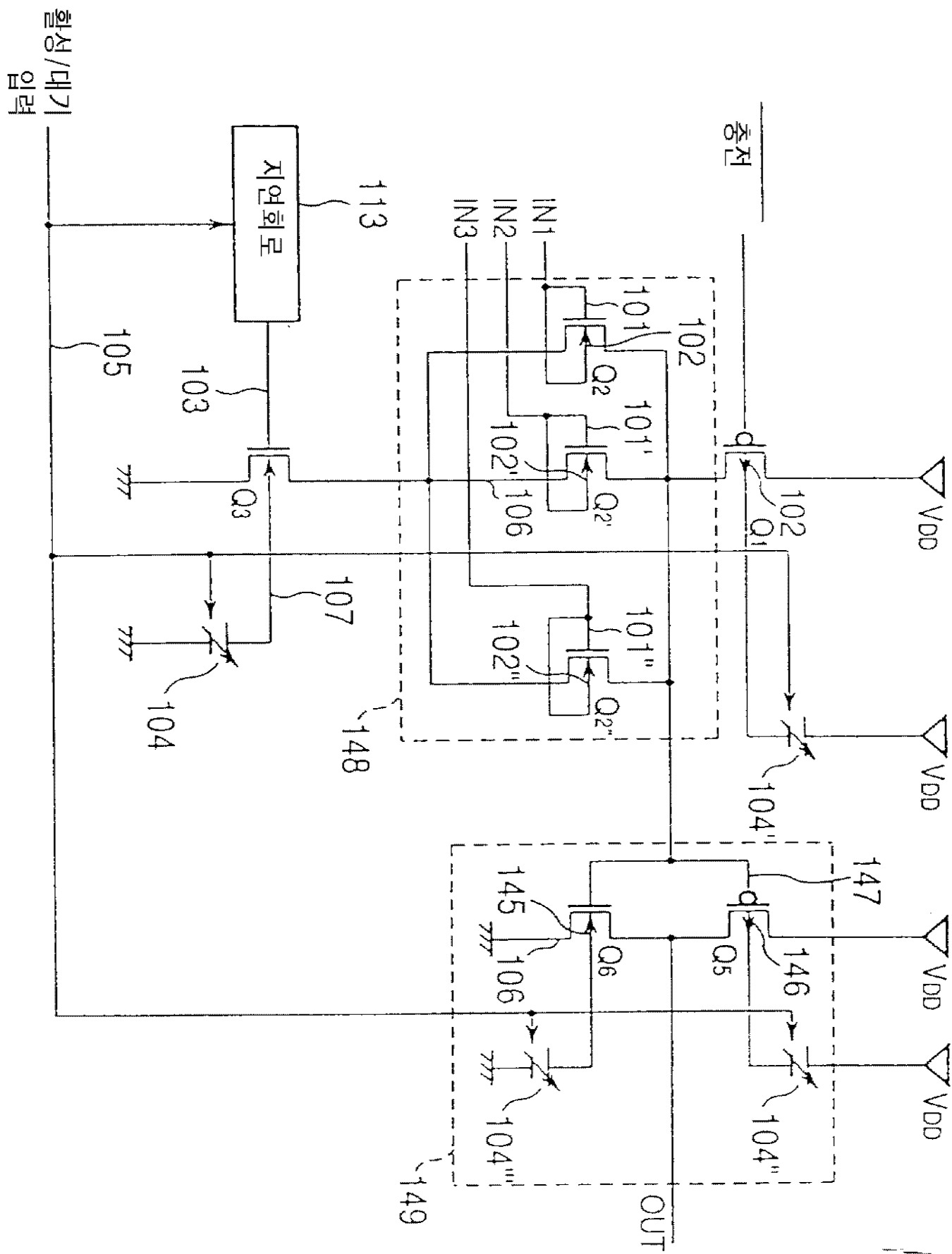


53b

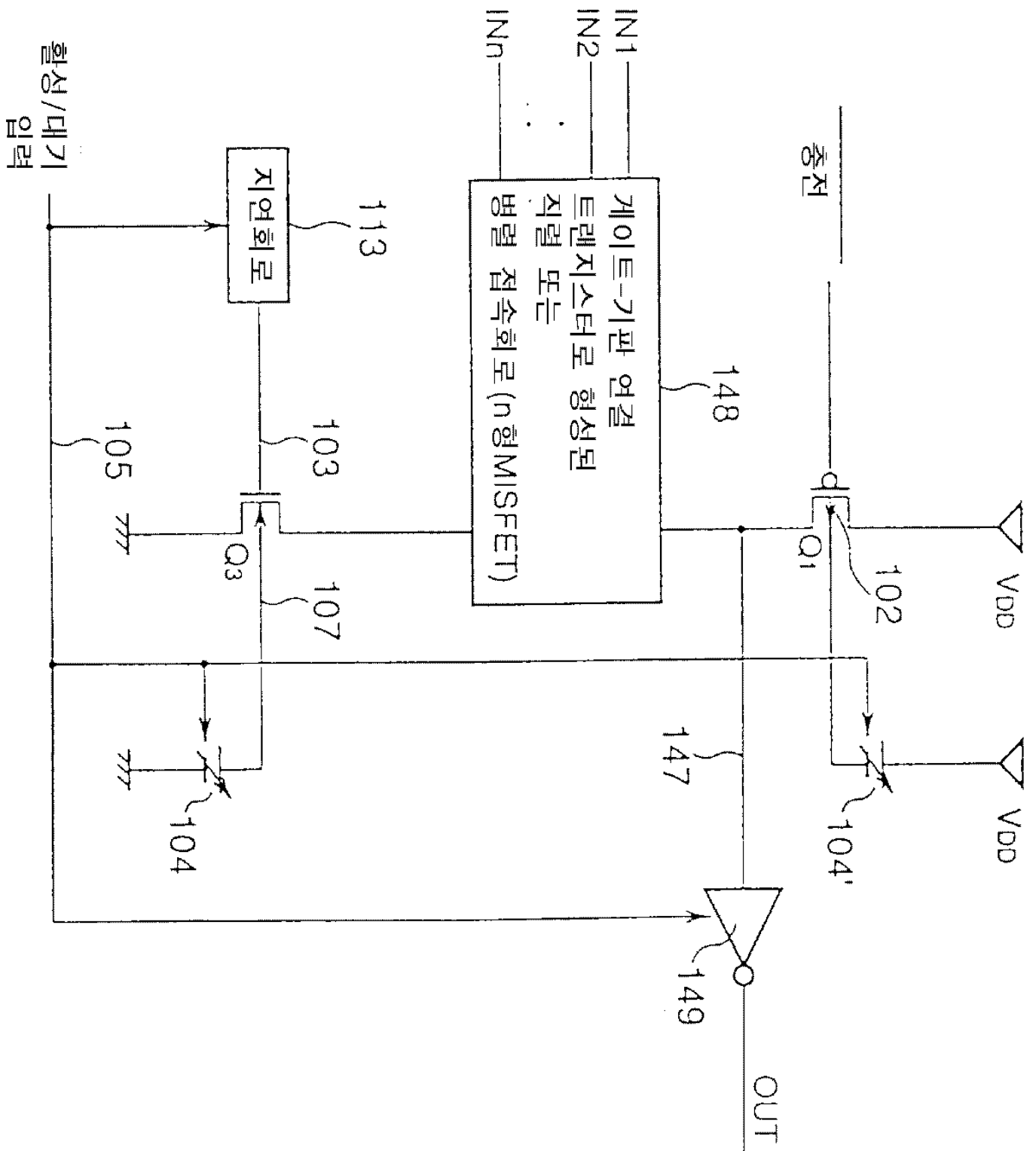


53c

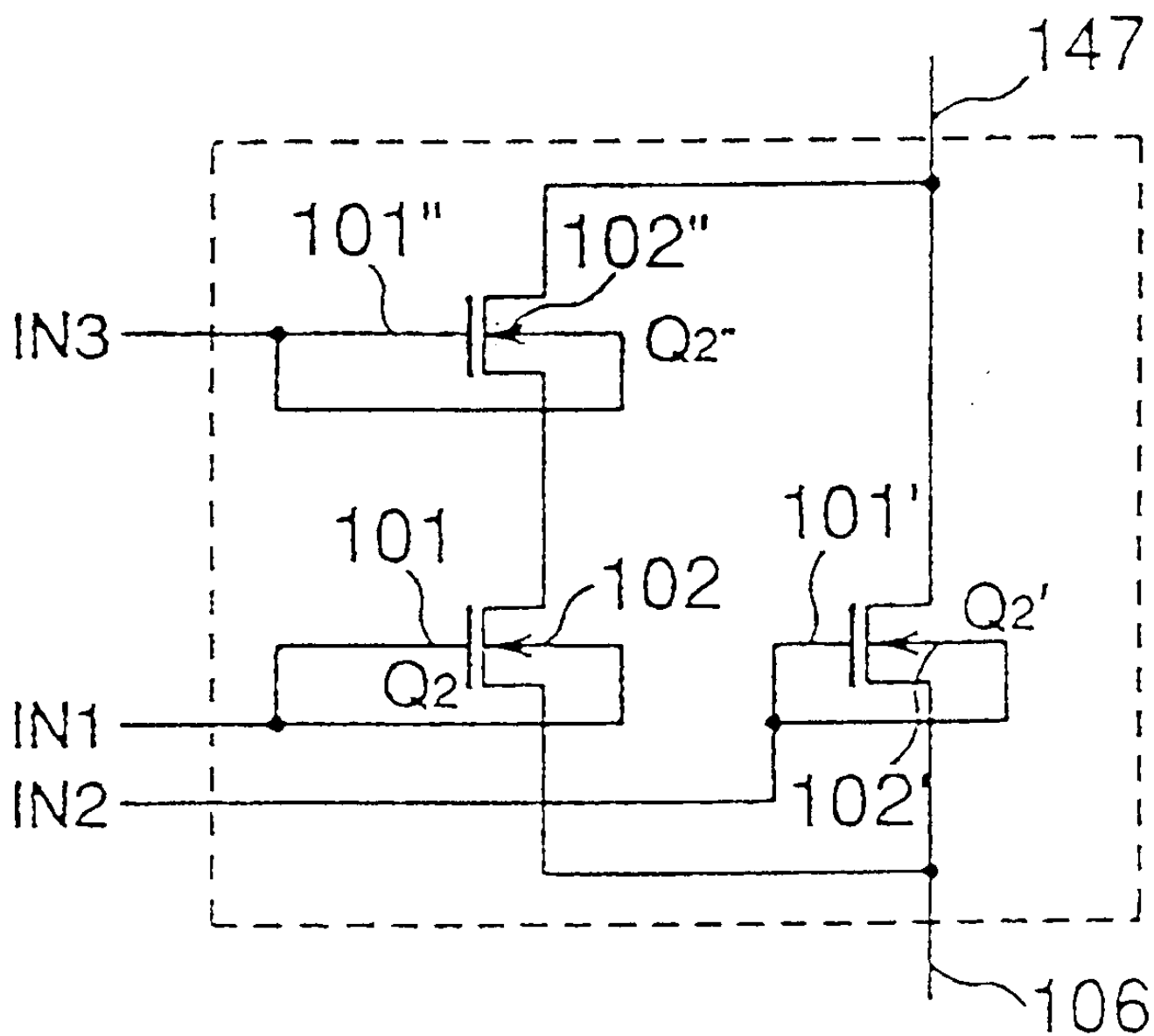




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56



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