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(54) Title: MULTI-BIT NON-VOLATILE RANDOM-ACCESS MEMORY CELLS

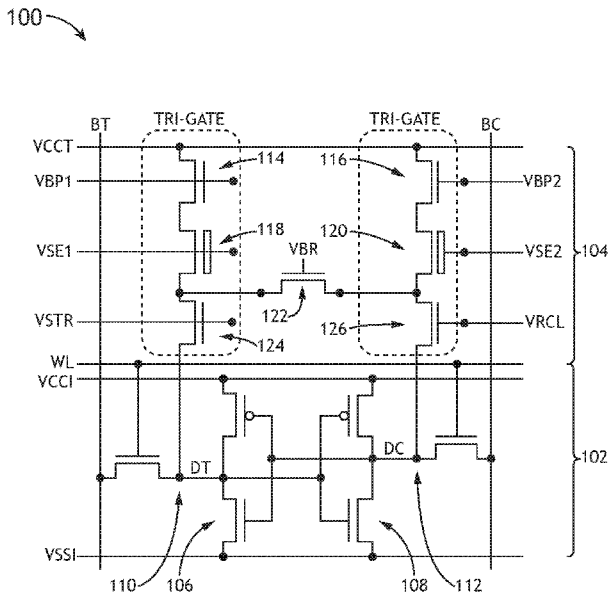

FIG.1

(57) Abstract: Multi-bit non-volatile random access memory cells are disclosed. A multi-bit non-volatile random access memory cell may include a volatile storage element and a non-volatile storage circuit. The non-volatile storage circuit may include at least one first pass transistor connected to a data true (DT) node of the volatile storage element and at least one second pass transistor connected to a data complement (DC) node of the volatile storage element. The non-volatile storage circuit may also include multiple non-volatile storage elements. Each non-volatile storage element may be configured to be selectively connectable to the DT node of the volatile storage element via the at least one first pass transistor and selectively connectable to the DC node of the volatile storage element via the at least one second pass transistor, allowing the multi-bit non-volatile random access memory cell to store/recall more than one databit per cell.

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MULTI-BIT NON-VOLATILE RANDOM-ACCESS MEMORY CELLS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is an International Application of U.S. Patent Application Serial No. 15/079,462, filed March 24, 2016, which claims the benefit and priority of U.S. Provisional Application Serial No. 62/255,000, filed November 13, 2015. Said U.S. Patent Application Serial No. 15/079,462 and U.S. Provisional Application Serial No. 62/255,000 are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of data storage devices, and particularly to non-volatile static random-access memory devices.

BACKGROUND

[0003] Non-volatile static random-access memory (nvSRAM) is a type of non-volatile random-access memory. An nvSRAM typically includes multiple nvSRAM cells. An nvSRAM cell typically includes a static random-access memory (SRAM) that is configured to facilitate read and write operations and a non-volatile storage circuit that is configured to facilitate store and recall operations. A store operation, for example, may store data from the SRAM of the nvSRAM cell to the non-volatile storage circuit of the nvSRAM cell. A recall operation, on the other hand, may retrieve data from the non-volatile storage circuit of the nvSRAM cell and load the retrieved data into the SRAM of the nvSRAM cell.

SUMMARY

[0004] An embodiment of the present disclosure is directed to an apparatus. The apparatus may include a volatile storage element having a data true (DT) node and a data complement (DC) node. The apparatus may also include a non-volatile storage circuit. The non-volatile storage circuit may include at least one first pass transistor connected to the DT node of the volatile storage element and at least one second pass transistor connected to the DC node of the volatile storage element. The non-volatile storage circuit may further include multiple non-volatile storage elements. Each non-volatile storage element may be configured to be selectively connectable to the DT node of the volatile storage element via the at least one first pass transistor and selectively connectable to the DC node of the volatile storage element via the at least one second pass transistor.

[0005] A further embodiment of the present disclosure is directed to a system. The system may include a processor and a non-volatile memory device configured to provide data storage for the processor. The non-volatile memory device may include multiple non-volatile memory cells. Each non-volatile memory cell may include a volatile storage element having a DT node and a DC node. Each non-volatile memory cell may also include a non-volatile storage circuit. The non-volatile storage circuit may include at least one first switching element connected to the DT node of the volatile storage element and at least one second switching element connected to the DC node of the volatile storage element. The non-volatile storage circuit may further include multiple non-volatile storage elements. Each non-volatile storage element may be configured to be selectively connectable to the DT node of the volatile storage element via the at least one first switching element and selectively connectable to the DC node of the volatile storage element via the at least one second switching element.

[0006] An additional embodiment of the present disclosure is directed to a method. The method may include establishing a first data storage path between a first non-volatile storage element of a plurality of non-volatile storage elements and a DT node of a volatile storage element; programming the first non-volatile storage element based on data stored in the volatile storage element utilizing the first data storage path; establishing a second data storage path between a second non-volatile storage element of the plurality of non-volatile storage elements and the DT node of the volatile storage element; and programming the second non-volatile storage element based on the data stored in the volatile storage element utilizing the second data storage path.

[0007] It is to be understood that both the foregoing general description and the following detailed description are for example and explanatory only and are not necessarily restrictive of the present disclosure. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate subject matter of the disclosure. Together, the descriptions and the drawings serve to explain the principles of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The numerous advantages of the disclosure may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 is a circuit diagram depicting an embodiment of a multi-bit non-volatile random access memory cell;

FIG. 2 is a time-based flow diagram depicting an example process performed during a store operation;

FIG. 3 is another time-based flow diagram depicting an example process performed during a store operation;

FIG. 4 is a circuit diagram depicting an example process performed during a recall operation;

FIG. 5 is a flow diagram depicting the example process performed during the recall operation;

FIG. 6 is a circuit diagram depicting an embodiment of another multi-bit non-volatile random access memory cell;

FIG. 7 is a circuit diagram depicting an embodiment of another multi-bit non-volatile random access memory cell; and

FIG. 8 is a block diagram depicting a system utilizing an embodiment of a multi-bit non-volatile random access memory.

DETAILED DESCRIPTION

[0009] Reference will now be made in detail to the subject matter disclosed, which is illustrated in the accompanying drawings.

[0010] Embodiments in accordance with the present disclosure are directed to multi-bit non-volatile random access memory cells. Multi-bit non-volatile random access memory cells are random access memory cells that are able to store/recall more than one databit per cell.

[0011] Referring generally to FIG. 1, a circuit diagram depicting an embodiment of a multi-bit non-volatile random access memory cell 100 configured in accordance with the present disclosure is shown. The multi-bit non-volatile random access memory cell 100 may include a volatile storage element 102 that is configured to facilitate read and write operations. The volatile storage element 102 may be configured utilizing any suitable volatile memory implementations. For instance, as shown in

FIG. 1, the volatile storage element 102 may implement a static random access memory (SRAM) that includes a first transistor 106 cross-coupled with a second transistor 108. The volatile storage element 102 may also include a data true (DT) node 110 and a data complement (DC) node 112 connected to the first and second transistors 106 and 108. It is noted that since SRAMs are well understood by those skilled in the art, detailed operations of SRAMs are not repeated in the present disclosure. It is also noted that multi-bit non-volatile random access memory cells 100 utilizing SRAMs as volatile storage elements 102 may be referred to as multi-bit nvSRAM cells 100 for illustrative purposes. It is to be understood, however, that using SRAMs as the volatile storage elements is only for illustrative purposes. It is contemplated that other types of volatile storage elements may be utilized instead of (or in addition to) SRAMs without departing from the spirit and scope of the present disclosure.

[0012] The multi-bit non-volatile random access memory cell 100 may also include a non-volatile storage circuit 104 that is configured to facilitate store and recall operations. The non-volatile storage circuit 104 of the multi-bit non-volatile random access memory cell 100 may be isolated from the volatile storage element 102 during read and write operations. The isolation may be achieved by turning off the switching elements (e.g., implemented as pass transistors) 124 and 126 that connect the non-volatile storage circuit 104 to the DT node 110 and the DC node 112. The isolation effectively allows the multi-bit non-volatile random access memory cell 100 to function as a volatile storage element (e.g., an SRAM) for read and write operations.

[0013] The non-volatile storage circuit 104 of the multi-bit non-volatile random access memory cell 100 may be used when data in the volatile storage element 102 needs to be stored. This may be referred to as a store

operation, which may be triggered automatically (may be referred to as autostore) if the data main voltage source is lost or drops below a threshold value. Alternatively and/or additionally, store operations may be triggered based on certain preconfigured hardware- and/or software-based actions. Regardless of the triggering event, once a store operation is initiated, a series of actions may be performed to carry out the store operation.

[0014] In the embodiment depicted in FIG. 1, the non-volatile storage circuit 104 of the multi-bit non-volatile random access memory cell 100 includes a first bulk program transistor 114 and a second bulk program transistor 116 respectively connected to a first non-volatile storage element 118 and a second non-volatile storage element 120. The first non-volatile storage element 118 and the second non-volatile storage element 120 each include a storage device capable of trapping a charge (e.g., a silicon oxide nitride oxide silicon (SONOS) transistor, a floating gate, or the like). The first non-volatile storage element 118 and the second non-volatile storage element 120 are bridged together via a bridge transistor 122. The bridge transistor 122 is configured to selectively connect one of the first or the second non-volatile storage element 118/120 to one of a DT node pass transistor 124 or a DC node pass transistor 126 shared by the first and the second non-volatile storage element 118 and 120. The ability to selectively connect one of the first or the second non-volatile storage element 118/120 to one of the DT node pass transistor 124 or the DC node pass transistor 126 allows the non-volatile storage circuit 104 to selectively store data to (and recall data from) the two non-volatile storage elements 118 and 120, which in turn provides the multi-bit non-volatile random access memory cell 100 abilities to store/recall two databits per cell.

[0015] FIG. 2 is a time-based flow diagram depicting an example process performed during a store operation 200 for establishing a data storage path

to a first non-volatile storage element 118 and storing data to the first non-volatile storage element 118 utilizing the established storage path. Referring generally to FIGS. 1 and 2, a bulk program step 202 is carried out by applying a voltage (VBP1) to the first bulk program transistor 114 and applying a positive voltage (VSE1 being positive) to the first non-volatile storage element 118 for a period of time. A subsequent step, referred to as the bulk erase step 204, may apply a negative voltage (VSE1 being negative) to the first non-volatile storage element 118 for another period of time, erasing the data stored in the non-volatile storage element 118. A program step 206 may commence after the bulk erase step 204. If DT data=1, pass gate VSTR will be "off", and the first non-volatile storage element 118 will remain at "erase" state after the program step 206. If DT data=0, pass gate VSTR will be "on", and the first non-volatile storage element 118 will go to "program" state after the program step 206.

[0016] FIG. 3 is a time-based flow diagram depicting an example process performed during a store operation 300 for establishing a data storage path to a second non-volatile storage element 120 and storing data to the second non-volatile storage element 120 utilizing the established storage path. Referring generally to FIGS. 1 and 3, a bulk program step 302 is carried out by applying a voltage (VBP2) to the second bulk program transistor 116 and applying a positive voltage (VSE2 being positive) to the second non-volatile storage element 120 for a period of time. A subsequent step, referred to as the bulk erase step 304, may apply a negative voltage (VSE2 being negative) to the second non-volatile storage element 120 for another period of time, erasing the data stored in the non-volatile storage element 120. A program step 306 may commence after the bulk erase step 304. By supplying power (VBR) to the bridge transistor 122, if DT data=1, pass gate VSTR will be "off" and the second non-volatile storage element 120 will remain at

"erase" state after the program step 306. If DT data=0, pass gate VSTR will be "on", and the second non-volatile storage element 120 will go to "program" state after the program step 306.

[0017] It is noted that the response times of the first and the second non-volatile storage elements 118 and 120 to the voltage applied on VSE1 and VSE2 shown in FIGS. 2 and 3 have been simplified for illustrative purposes. It is to be understood that the response times may not be instantaneous. It is therefore contemplated that pre-charge voltages may be utilized in some implementations to help modify/improve the response times. It is to be understood that whether (and how) such pre-charge voltages are used may vary without departing from the spirit and scope of the present disclosure.

[0018] It is noted that the non-volatile storage circuit 104 of the multi-bit non-volatile random access memory cell 100 configured in accordance with the present disclosure also supports recall operations from the two non-volatile storage elements 118 and 120. FIGS. 4 and 5 are illustrations depicting an example process performed during a recall operation 500 for recalling data stored in the first non-volatile storage element 118 into the volatile storage element 102 of the multi-bit non-volatile random access memory cell 100.

[0019] More specifically, as shown in FIGS. 4 and 5, a pre-write step 502 may be utilized to write "0"s into the volatile storage element 102 of the multi-bit non-volatile random access memory cell 100, effectively setting the DT node 110 to 0 and the DC node 112 to power. Step 504 may then set the volatile storage element 102 to a data retention mode by turning on the VCLAMP and applying a current limit to the volatile storage element 102 using the VSSIGATE. A recall path may then be established in a recall step 506. To recall data from the first non-volatile storage element 118 (as

shown in FIG. 4 for illustrative purposes), the recall step 506 may turn on VRCL, VBP1, VBR, and turn off VSTR and VBP2, effectively establishing the recall path VCCT, VBP1, VSE1, VBR, VRCL, and the DC node 110 of the volatile storage element 102. To recall data from the second non-volatile storage element 120, the recall step 506 may turn on VRCL, VBP2, and turn off VSTR, VBP1 and VBR, effectively establishing the recall path VCCT, VBP2, VSE2, VRCL, and the DC node 110 of the volatile storage element 102.

[0020] Once the appropriate recall path is established, a recharge step 508 may recharge the volatile storage element 102 of the multi-bit non-volatile random access memory cell 100 so that the volatile storage element 102 may latch to the data on the recall path. For instance, the recharge step 508 may unclamp VCCI and VSSI and apply VSSI to the volatile storage element 102, allowing the volatile storage element 102 to latch to the data on the recall path and complete the recall operation. In this manner, if the non-volatile storage element 118/120 on the recall path is in an erase state (stored data=1), the DC node 112 of the volatile storage element 102 will be pulled to ground and the DT node 110 of the volatile storage element 102 will be set to 1 at the completion of the recall operation. On the other hand, if the non-volatile storage element 118/120 on the recall path is in a program state (stored data=0), the DC node 112 of the volatile storage element 102 will have no path to be pulled down to ground and the DT node 110 of the volatile storage element 102 will therefore remain the same at the pre-write value of 0, accomplishing the recall operation as intended.

[0021] It is noted that the multi-bit non-volatile random access memory cell 100 configured in accordance with the present disclosure is not only able to selectively store data to the non-volatile storage elements 118 and/or 120, but also able to selectively recall data from the non-volatile storage elements 118 and/or 120. It is noted that this ability may help provide

several performance improvements over conventional nvSRAM cells that are limited to store/recall one databit per cell. For example, in certain implementations, the non-volatile storage elements 118 and 120 may be used alternately for data storage to help increase the endurance of the multi-bit non-volatile random access memory cell 100. In another example, one of the non-volatile storage elements 118 or 120 may be dedicated as the non-volatile storage element for data storage when power goes down (e.g., providing autostore if the data main voltage source drops below a threshold value) while the other non-volatile storage element may be used to store data when the power is on, effectively improving the robustness of data retention provided by the multi-bit non-volatile random access memory cell 100.

[0022] Additionally and/or alternatively, the non-volatile storage elements 118 and 120 may be utilized to provide redundancy that may be appreciated in certain operating conditions. For example, one of the non-volatile storage elements 118 or 120 may be used as a redundant element if the multi-bit non-volatile random access memory cell 100 fails to recall from the other non-volatile storage element. Furthermore, it is noted that the multi-bit non-volatile random access memory cell 100 configured in accordance with the present disclosure is able to provide non-inverted recalls, where after recalling from the non-volatile storage circuit 104 of the multi-bit non-volatile random access memory cell 100, the data in the volatile storage element 102 of the multi-bit non-volatile random access memory cell 100 is the same as the data in the non-volatile storage circuit 104.

[0023] It is to be understood that the configuration of the multi-bit non-volatile random access memory cell 100 described above is merely for example and is not meant to be limiting. It is contemplated that

alternative configurations may be utilized to implement the multi-bit non-volatile random access memory cell and provide the aforementioned performance improvements without departing from the spirit and scope of the present disclosure. For instance, FIG. 6 is a circuit diagram depicting an embodiment of another multi-bit non-volatile random access memory cell 600 configured in accordance with the present disclosure.

[0024] As shown in FIG. 6, the multi-bit non-volatile random access memory cell 600 includes a volatile storage element (e.g., an SRAM) 602 that is configured to facilitate read and write operations and a non-volatile storage circuit 604 that is configured to facilitate store and recall operations. It is noted that the non-volatile storage circuit 604 of the multi-bit non-volatile random access memory cell 600 may be configured differently compared to the non-volatile storage circuit 104 previously described. The non-volatile storage circuit 604 depicted in FIG. 6 may be configured to support *n*-number of non-volatile storage elements 606 (where $n \geq 2$), allowing the multi-bit non-volatile random access memory cell 600 to store/recall up to *n*-number of databits per cell.

[0025] More specifically, the non-volatile storage circuit 604 may include a first group of serially connected switching elements (e.g., pass transistors) 608 connected to the DT node 610 of the volatile storage element 602. The non-volatile storage circuit 604 also may include a second group of serially connected switching elements (e.g., pass transistors) 614 connected to the DC node 612 of the volatile storage element 602. The first group of pass transistors 608 and the second group of pass transistors 614 may be jointly connected to the *n*-number of non-volatile storage elements 606 to form a ladder network of transistors as shown in FIG. 6. This ladder network of transistors may provide the ability for the multi-bit non-volatile random access memory cell 600 to selectively connect one of the *n*-number of non-

volatile storage elements 606 to the DT node 610 or the DC node 612 of the volatile storage element 602, effectively allowing the multi-bit non-volatile random access memory cell 600 to store/recall up to *n*-number of databits per cell.

[0026] For instance, to store data to a non-volatile storage element 606A (one of the *n*-number of non-volatile storage elements 606), the multi-bit non-volatile random access memory cell 600 may turn on VSTR(n+1) and VSTRn, turn off VSTR1, VRCL1, VRCLn, and perform the aforementioned bulk program and bulk erase steps on the non-volatile storage element 606A by applying a positive voltage and a negative voltage on VSE1, respectively. The multi-bit non-volatile random access memory cell 600 may then turn off VSTR(n+1) and VSTRn, turn on VSTR1, and perform the aforementioned program step to enable data transfer from the DT node 610 to the non-volatile storage element 606A.

[0027] To recall data from the non-volatile storage element 606A, the multi-bit non-volatile random access memory cell 600 may turn on VSTR(n+1), VSTRn, and VRCL1, effectively establishing a recall path from the non-volatile storage element 606A to the DC node 612 of the volatile storage element 602. The volatile storage element 602 may then be recharged and latched to the data on the recall path (the data from the non-volatile storage element 606A in this example), accomplishing the recall operation as intended.

[0028] Similarly, to store data to the non-volatile storage element 606B, the multi-bit non-volatile random access memory cell 600 may turn on VSTR(n+1), turn off VSTR1 through VSTRn, VRCL1, VRCLn, and perform the aforementioned bulk program and bulk erase steps on the non-volatile storage element 606B. The multi-bit non-volatile random access memory

cell 600 may then turn off VSTR(n+1), turn on VSTR1 through VSTRn, and perform the aforementioned program step to enable data transfer from the DT node 610 to the non-volatile storage element 606B. To recall data from the non-volatile storage element 606B, the multi-bit non-volatile random access memory cell 600 may turn on VSTR(n+1) and VRCL1 through VRCLn, effectively establishing a recall path from the non-volatile storage element 606B to the DC node 612 of the volatile storage element 602.

[0029] It is to be understood that while only two non-volatile storage elements 606 are shown in FIG. 6, such a configuration is merely for example and is not meant to be limiting. It is contemplated that a multi-bit non-volatile random access memory cell 600 may include any number of non-volatile storage elements 606 without departing from the spirit and scope of the present disclosure, and that data may be stored to and recalled from the non-volatile storage elements 606 in manners similar to that described above.

[0030] It is also to be understood that while the *n*-number of non-volatile storage elements 606 (and the ladder network of transistors in general) are shown to be positioned on one side of the volatile storage element 602, such a configuration is merely for example and is not meant to be limiting. It is contemplated that the *n*-number of non-volatile storage elements 606 (and the ladder network of transistors in general) may be distributed on more than one side of the volatile storage element 602 without departing from the spirit and scope of the present disclosure. In certain implementations, as shown in FIG. 7, if *n* is an even number, the non-volatile storage elements 706 (and the ladder network of transistors 704 in general) may be symmetrically distributed on two opposite sides of the volatile storage element 702 to provide a balanced cell structure 700.

[0031] It is to be understood that the various circuit diagrams presented above do not necessarily need to correspond to the physical layout of the multi-bit non-volatile random access memory cells. In other words, the physical layout of the multi-bit non-volatile random access memory cells may vary without departing from the spirit and scope of the present disclosure. In certain implementations, the size of the multi-bit non-volatile random access memory cells may be approximately 1.36 micrometers wide and 5.24 micrometers long. It is contemplated, however, that the size of the multi-bit non-volatile random access memory cells may vary without departing from the spirit and scope of the present disclosure.

[0032] FIG. 8 is a block diagram depicting a system 800 utilizing a multi-bit non-volatile random access memory 802 configured in accordance with the present disclosure. The system 800 may include one or more microcontrollers (may also be referred to as processors) 804 communicatively coupled to the multi-bit non-volatile random access memory 802. The multi-bit non-volatile random access memory 802 may include one or more multi-bit non-volatile random access memory cells configured in accordance with the present disclosure. The one or more multi-bit non-volatile random access memory cells in the multi-bit non-volatile random access memory 802 may be utilized to provide data logging and data storage for the one or more processors 804.

[0033] It is to be understood that the present disclosure may be conveniently implemented in forms of a software, hardware, or firmware package. It is also to be understood that embodiments of the present disclosure are not limited to any underlying implementing technology. Embodiments of the present disclosure may be implemented utilizing any combination of software and hardware technology and by using a variety of

technologies without departing from the present disclosure or without sacrificing all of their material advantages.

[0034] It is to be understood that the specific order or hierarchy of steps in the processes disclosed is but one example. It is to be understood that the specific order or hierarchy of steps in the processes may be rearranged while remaining within the broad scope of the present disclosure. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0035] It is believed that the systems and methods disclosed herein and many of their attendant advantages will be understood by the foregoing description, and it will be apparent that various changes may be made in the form, construction, and arrangement of the components thereof without departing from the broad scope of the present disclosure or without sacrificing all of their material advantages. The form herein before described being merely an explanatory embodiment thereof, it is the intention of the following claims to encompass and include such changes.

[0036] The above description is intended to be illustrative, and not restrictive. For example, the above-described embodiments (or one or more aspects thereof) may be used in combination with each other. Other embodiments will be apparent to those of skill in the art upon reviewing the above description. In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one. In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In the event of inconsistent usages between this

document and those documents so incorporated by reference, the usage in the incorporated reference(s) should be considered supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document supersedes the usage in any incorporated references.

[0037] Although the claimed subject matter has been described with reference to specific embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of what is claimed. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense. The scope of the claims should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled. In the appended claims, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended; a system, device, article, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels and are not intended to impose numerical requirements on their objects.

[0038] The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a volatile storage element, the volatile storage element comprising a data true (DT) node and a data complement (DC) node; and

a non-volatile storage circuit, the non-volatile storage circuit comprising at least one first pass transistor connected to the DT node of the volatile storage element and at least one second pass transistor connected to the DC node of the volatile storage element, the non-volatile storage circuit further comprising a plurality of non-volatile storage elements, each non-volatile storage element of the plurality of non-volatile storage elements configured to be selectively connectable to the DT node of the volatile storage element via the at least one first pass transistor and selectively connectable to the DC node of the volatile storage element via the at least one second pass transistor.

2. The apparatus of claim 1, wherein the plurality of non-volatile storage elements comprises two non-volatile storage elements, and the non-volatile storage circuit further comprises:

a bridge transistor connected to the two non-volatile storage elements, the bridge transistor configured to selectively connect one of the two non-volatile storage elements to the DT node of the volatile storage element via the at least one first pass transistor and the DC node of the volatile storage element via at least one second pass transistor.

3. The apparatus of claim 1, wherein the at least one first pass transistor comprises a first group of pass transistors connected in series to the DT node of the volatile storage element, the at least one second pass

transistor comprises a second group of pass transistors connected in series to the DC node of the volatile storage element, and the plurality of non-volatile storage elements comprises at least two non-volatile storage elements connected to the first group of pass transistors and the second group of pass transistors to form a ladder network of transistors.

4. The apparatus of claim 3, wherein the volatile storage element comprises a static random access memory (SRAM) and wherein the ladder network of transistors is distributed on at least two sides of the SRAM.

5. The apparatus of claim 4, wherein the ladder network of transistors is distributed symmetrically on two opposite sides of the SRAM.

6. The apparatus of claim 1, wherein the plurality of non-volatile storage elements comprises a plurality of silicon oxide nitride oxide silicon (SONOS) transistors.

7. The apparatus of claim 1, wherein the non-volatile storage circuit is configured to store a databit from the volatile storage element into at least two of the plurality of non-volatile storage elements to provide data redundancy for the non-volatile storage circuit.

8. The apparatus of claim 1, wherein the non-volatile storage circuit is configured to store a databit from the volatile storage element into a first one of the plurality of non-volatile storage elements when the apparatus is powered, and the non-volatile storage circuit is further configured to store the databit from the volatile storage element into a second one of the plurality of non-volatile storage elements when the apparatus loses power.

9. The apparatus of claim 1, wherein the non-volatile storage circuit is configured to alternate data storage among the plurality of non-volatile storage elements to increase endurance of the non-volatile storage circuit.

10. A system, comprising:

a processor; and

a non-volatile memory device configured to provide data storage for the processor, the non-volatile memory device comprising a plurality of non-volatile memory cells, each non-volatile memory cell of the plurality of non-volatile memory cells comprising:

a volatile storage element, the volatile storage element comprising a data true (DT) node and a data complement (DC) node; and

a non-volatile storage circuit, the non-volatile storage circuit comprising at least one first switching element connected to the DT node of the volatile storage element and at least one second switching element connected to the DC node of the volatile storage element, the non-volatile storage circuit further comprising a plurality of non-volatile storage elements, each non-volatile storage element of the plurality of non-volatile storage elements configured to be selectively connectable to the DT node of the volatile storage element via the at least one first switching element and selectively connectable to the DC node of the volatile storage element via the at least one second switching element.

11. The system of claim 10, wherein the plurality of non-volatile storage elements comprises two non-volatile storage elements, and the non-volatile storage circuit further comprises:

a bridge element connected to the two non-volatile storage elements, the bridge element configured to selectively connect one of the two non-volatile storage elements to the DT node of the volatile storage element via the at least one first switching element and the DC node of the volatile storage element via at least one second switching element.

12. The system of claim 10, wherein the at least one first switching element comprises a first group of switching elements connected in series to the DT node of the volatile storage element, the at least one second switching element comprises a second group of switching elements connected in series to the DC node of the volatile storage element, and the plurality of non-volatile storage elements comprises at least two non-volatile storage elements connected to the first group of switching elements and the second group of switching elements to form a ladder network.

13. The system of claim 12, wherein the ladder network is distributed on at least two sides of the volatile storage element.

14. The system of claim 10, wherein the volatile storage element comprises a static random access memory (SRAM) and the plurality of non-volatile storage elements comprises a plurality of silicon oxide nitride oxide silicon (SONOS) transistors.

15. The system of claim 10, wherein the non-volatile storage circuit is configured to store a databit from the volatile storage element into at least two of the plurality of non-volatile storage elements to provide data redundancy for the particular non-volatile memory cell.

16. The system of claim 10, wherein the non-volatile storage circuit is configured to store a databit from the volatile storage element into a first one of the plurality of non-volatile storage elements when the particular non-volatile memory cell is powered, and the non-volatile storage circuit is further configured to store the databit from the volatile storage element

into a second one of the plurality of non-volatile storage elements when the particular non-volatile memory cell loses power.

17. The system of claim 10, wherein the non-volatile storage circuit is configured to alternate data storage among the plurality of non-volatile storage elements to increase endurance of the particular non-volatile memory cell.

18. A method, comprising:

establishing a first data storage path between a first non-volatile storage element of a plurality of non-volatile storage elements and a data true (DT) node of a volatile storage element;

programming the first non-volatile storage element based on data stored in the volatile storage element utilizing the first data storage path;

establishing a second data storage path between a second non-volatile storage element of the plurality of non-volatile storage elements and the DT node of the volatile storage element; and

programming the second non-volatile storage element based on the data stored in the volatile storage element utilizing the second data storage path.

19. The method of claim 18, wherein the second data storage path and the first data storage path share at least one common pass transistor connected to the DT node of the volatile storage element.

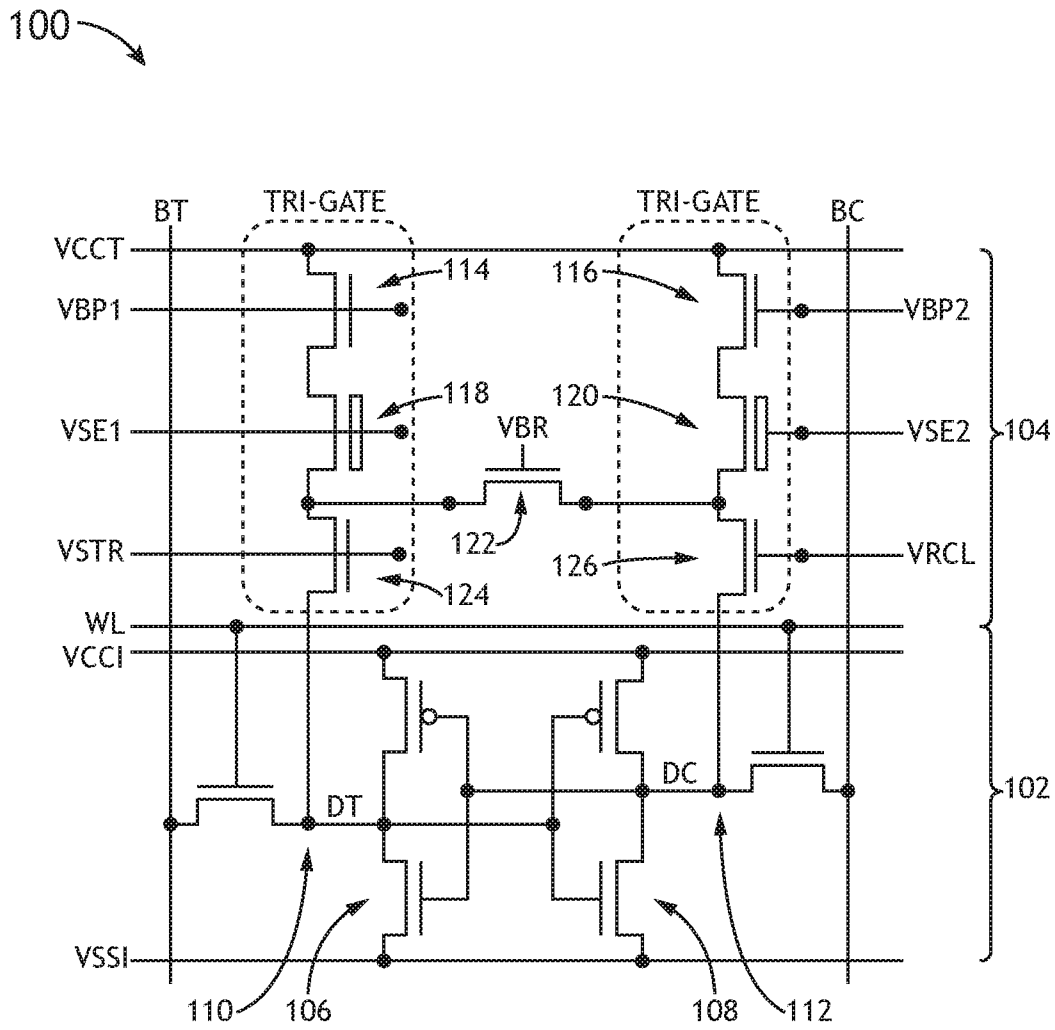
20. The method of claim 18, further comprising:

establishing a first recall path between the first non-volatile storage element of the plurality of non-volatile storage elements and a data complement (DC) node of the volatile storage element;

recalling data from the first non-volatile storage element to the volatile storage element utilizing the first recall path;

establishing a second recall path between the second non-volatile storage element of the plurality of non-volatile storage elements and the DC node of the volatile storage element; and

recalling data from the second non-volatile storage element to the volatile storage element utilizing the second data storage path.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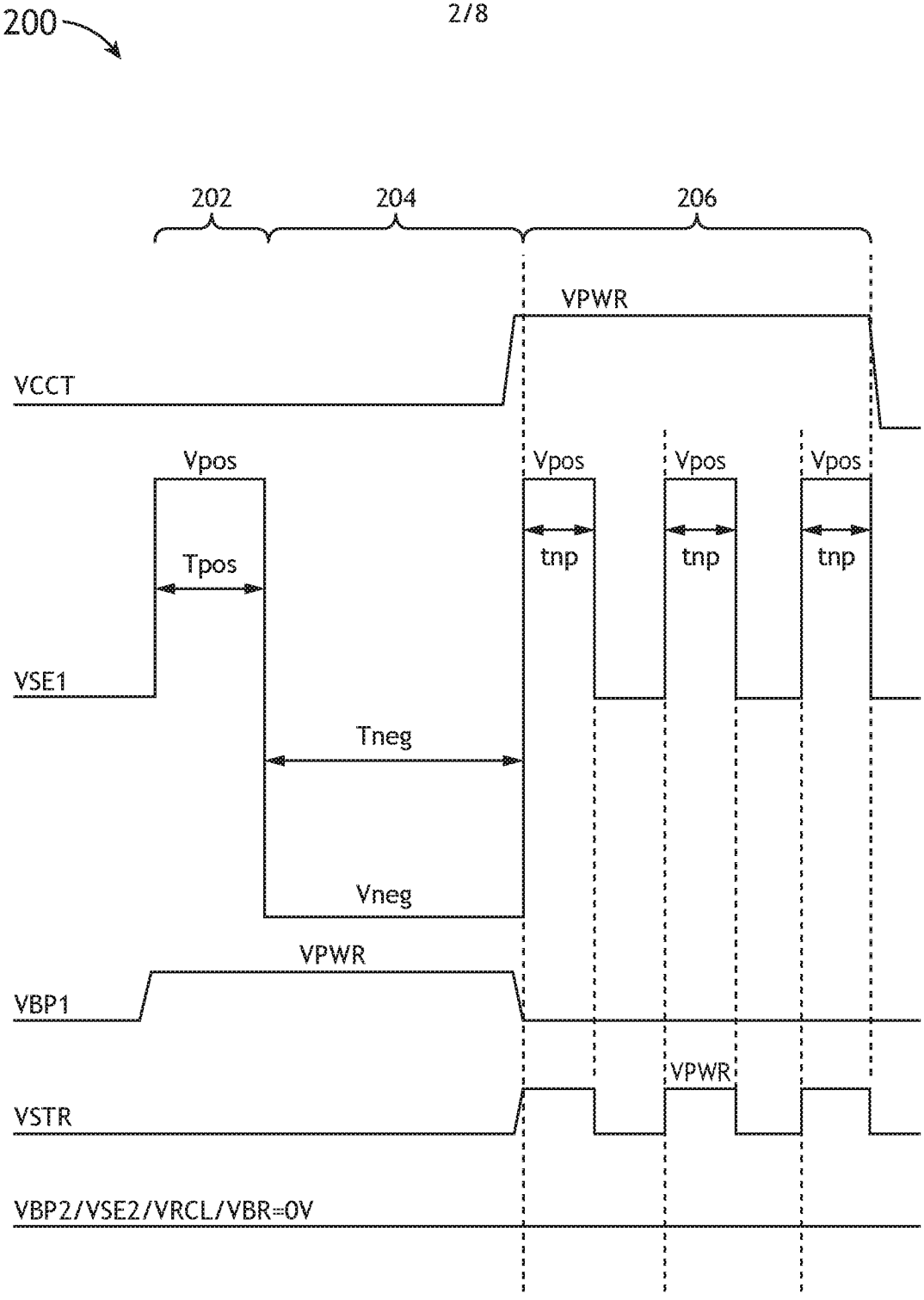
BT
TRI-GATE
TRI-GATE
BC
VCCT
VBP1
VSE1
VSTR
WL
VCCI
VSSI
VBP2
VSE2
VRCL
VBR
DT
DC
114
116
118
120
122
124
126
104
102
110
106
108
112

FIG.1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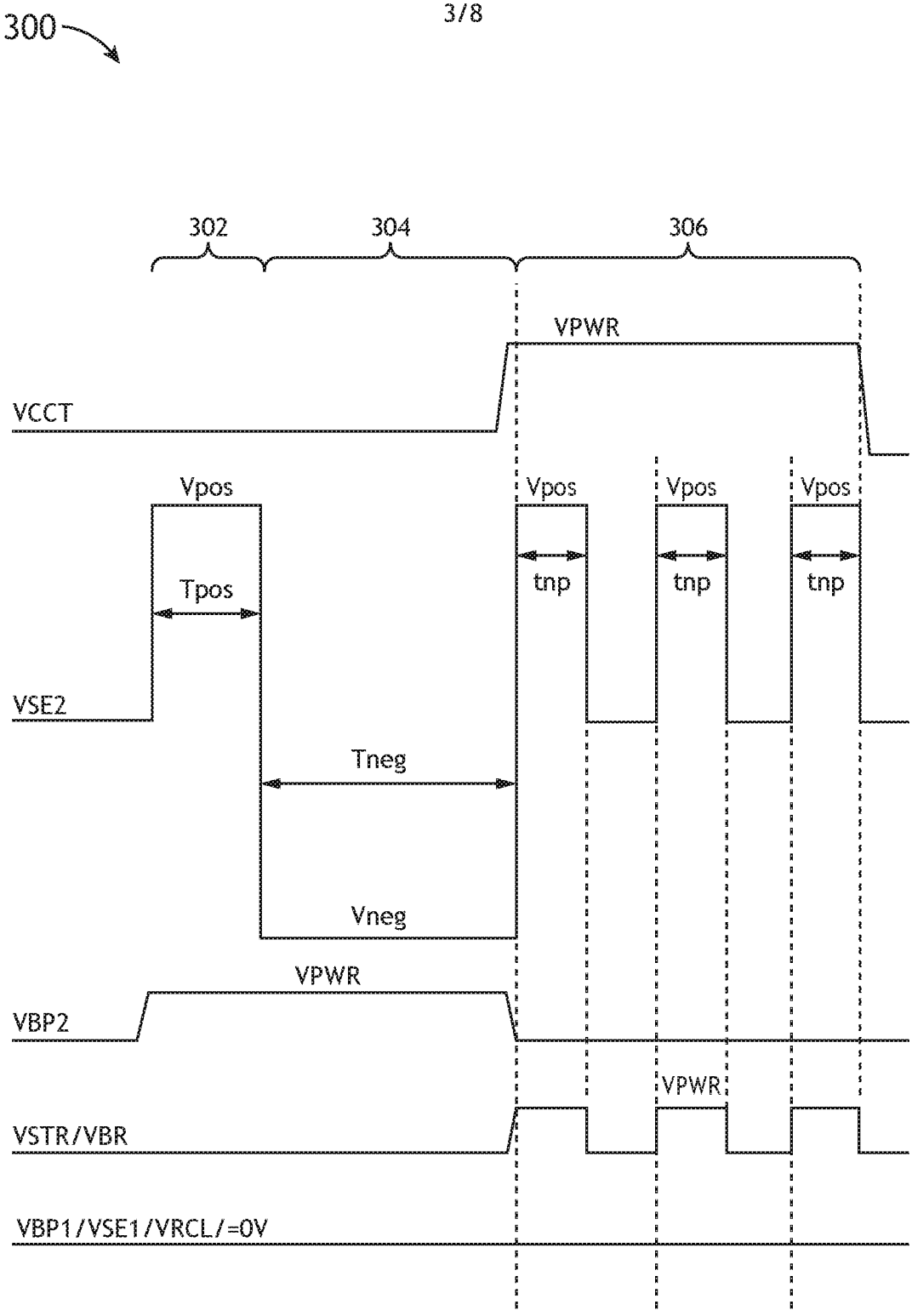
202
204
206
VPWR
VCCT
Vpos
Vpos
Vpos
Vpos
tnp
tnp
tnp
Tpos
VSE1
Tneg
Vneg
VPWR
VBP1
VPWR
VSTR
VBP2/VSE2/VRCL/VBR=0V

FIG.2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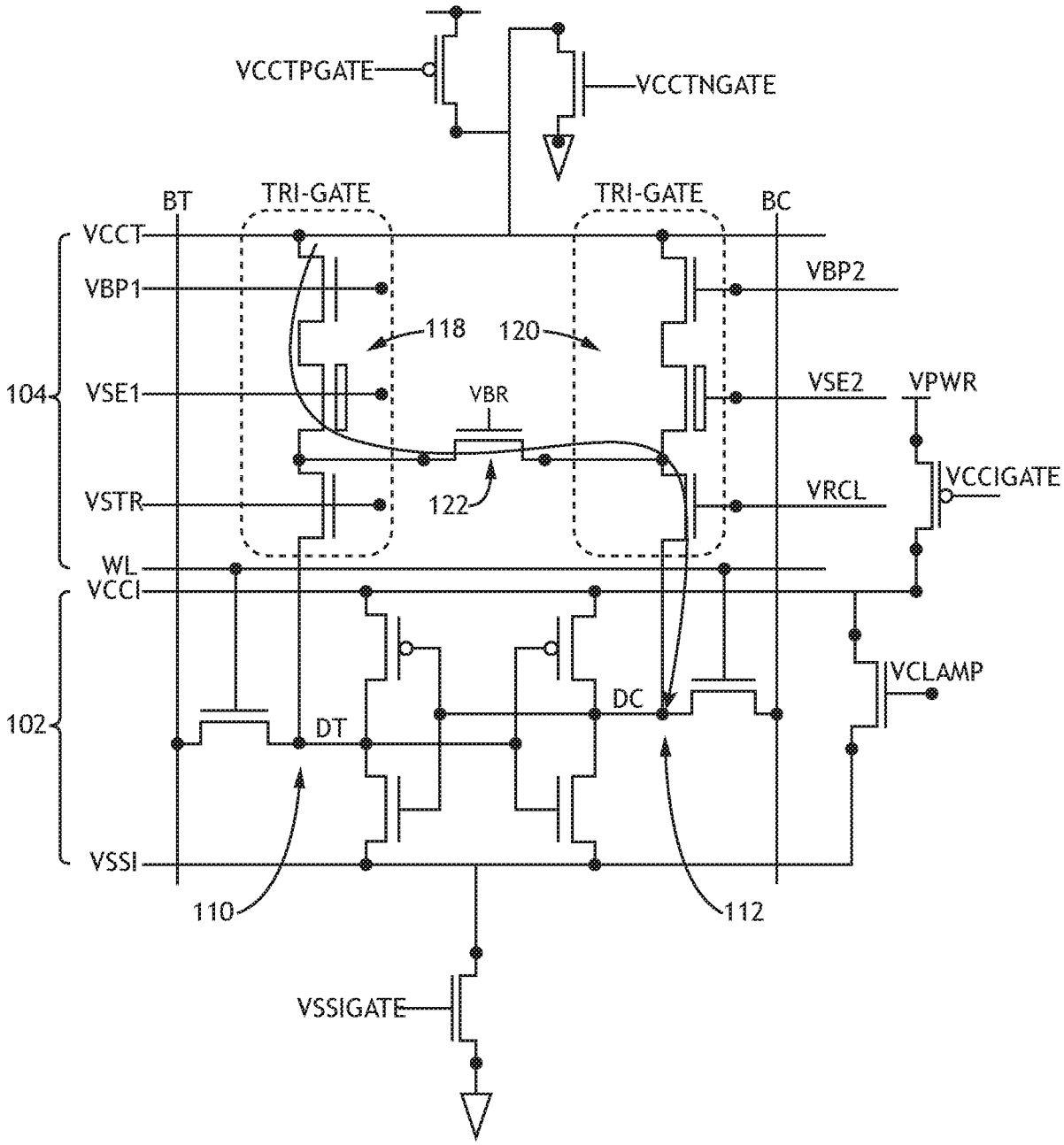
302
304
306
VPWR
VCCT
Vpos
Vpos
Vpos
Vpos
tnp
tnp
tnp
Tpos
VSE2
Tneg
Vneg
VPWR
VBP2
VPWR
VSTR/VBR
VBP1/VSE1/VRCL/=0V

FIG.3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VCCTNGATE
BT
TRI-GATE
TRI-GATE
BC
VCCT
VBP1
VBP2
118
120
104
VSE1
VBR
VSE2
VPWR
VSTR
122
VRCL
VCCIGATE
WL
VCCI
VCLAMP
DC
102
DT
VSSI
110
112
VSSIGATE

FIG.4

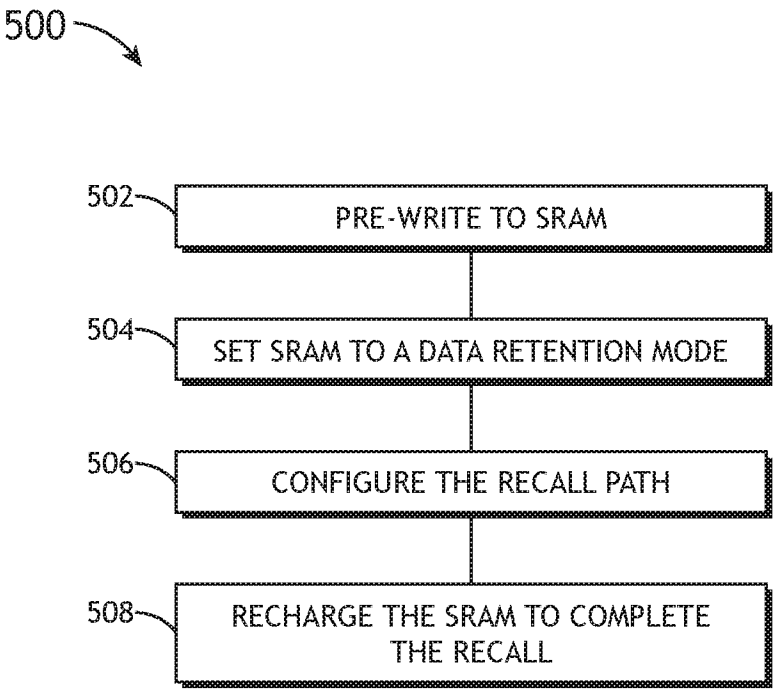
500
502
PRE-WRITE TO SRAM
504
SET SRAM TO A DATA RETENTION MODE
506
CONFIGURE THE RECALL PATH
508
RECHARGE THE SRAM TO COMPLETE THE RECALL

FIG.5

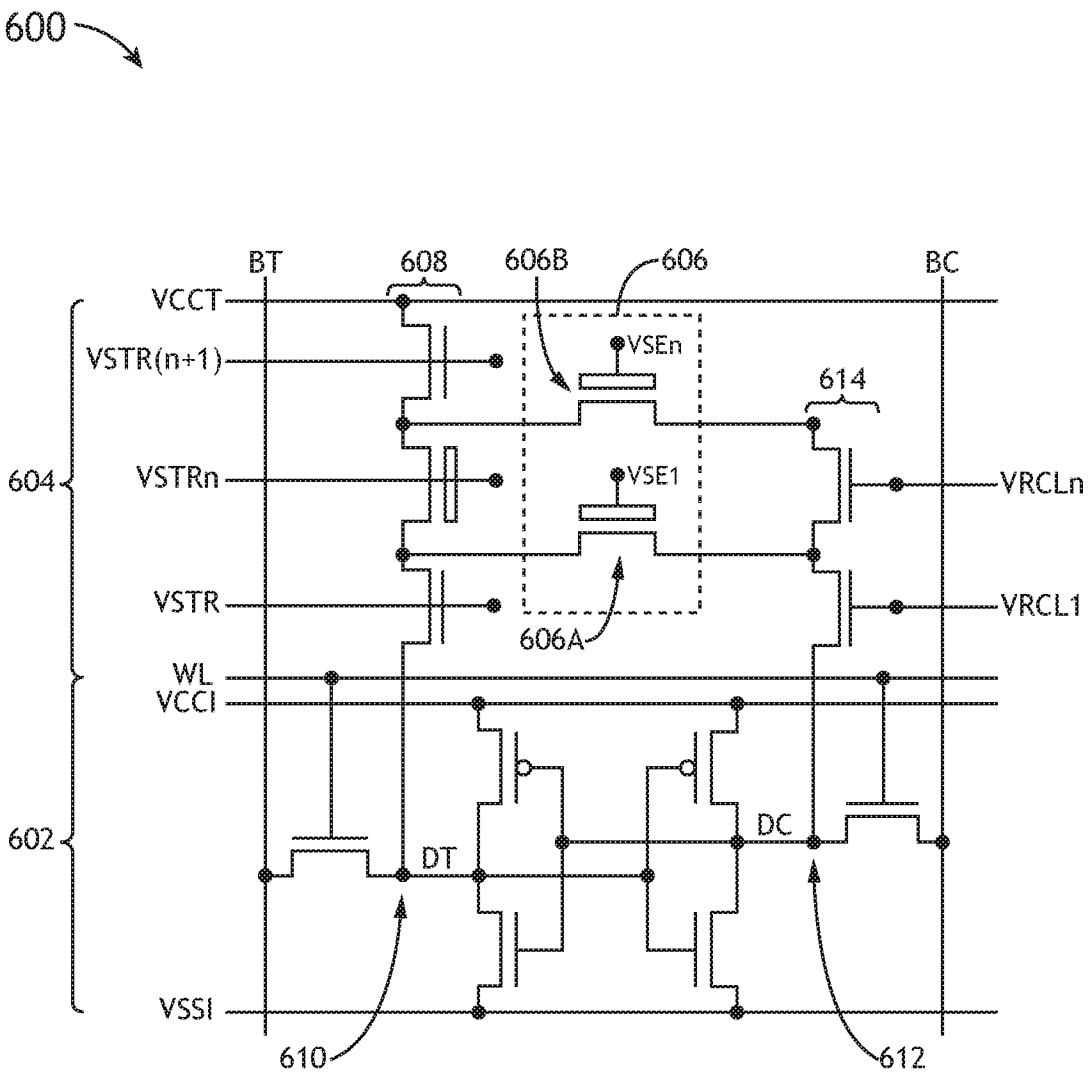
600
BT
608
606B
606
BC
VCCT
VSTR(n+1)
VSEn
614
604
VSTRn
VSE1
VRCLn
VSTR
VRCL1
606A
WL
VCCI
602
DC
DT
VSSI
610
612

FIG.6

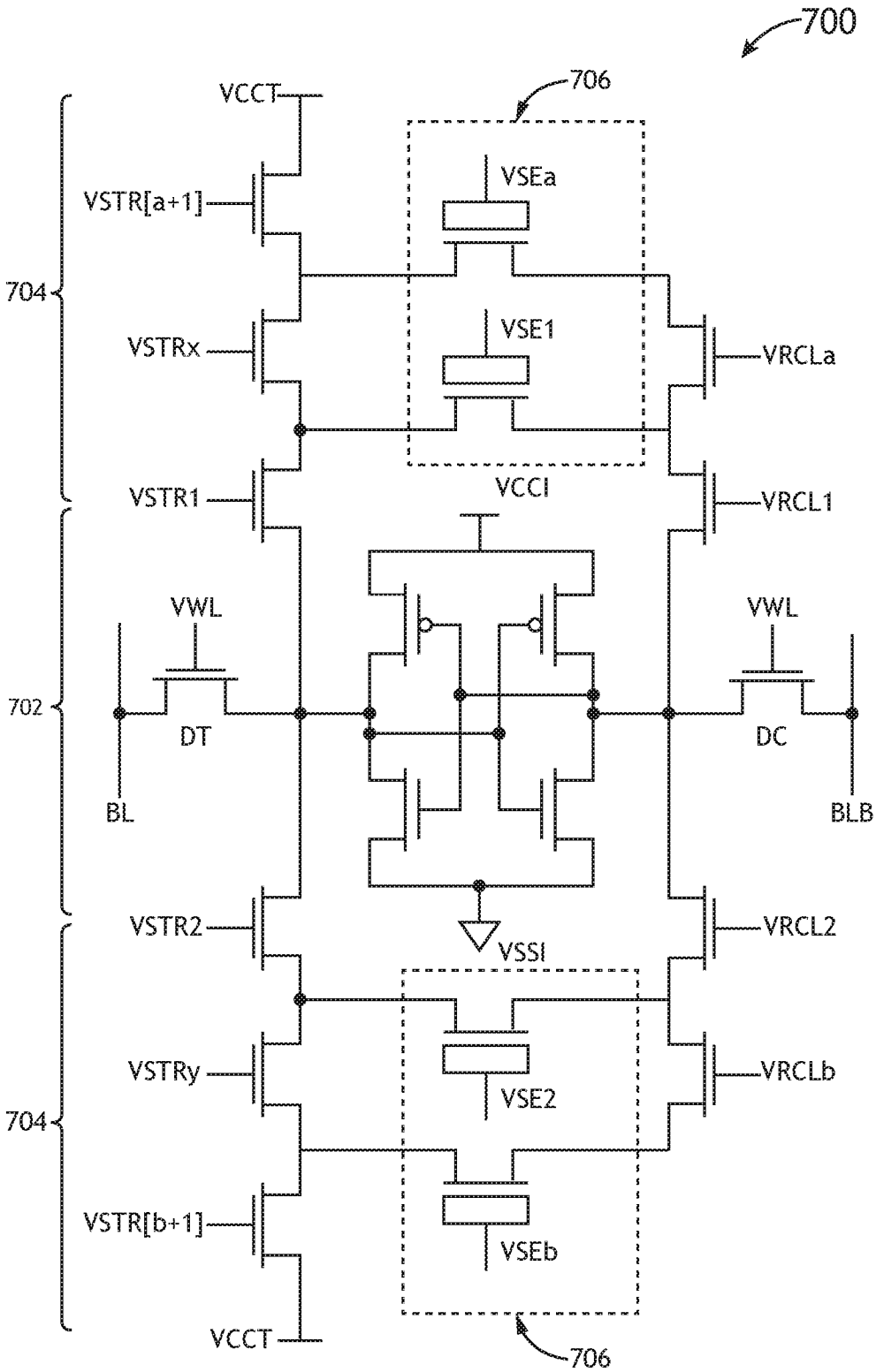
700
706
VCCT
VSEa
VSTR[a+1]
704
VSTRx
VSE1
VRCLa
VSTR1
VCCI
VRCL1
VWL
VWL
702
DT
DC
BL
BLB
VSTR2
VSSI
VRCL2
VSTRy
VRCLb
VSE2
704
VSTR[b+1]
VSEb
VCCT
706

FIG.7

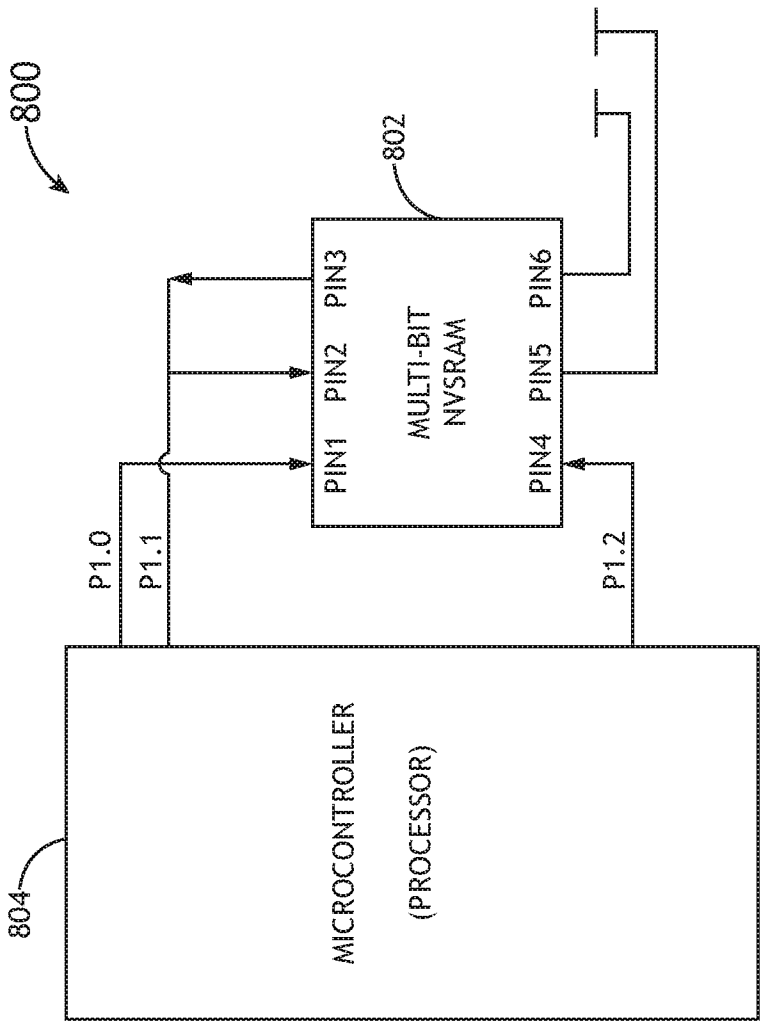
800
802
PIN1
PIN2
PIN3
PIN4
PIN5
PIN6
MULTI-BIT
NVSRAM
P1.0
P1.1
P1.2
804
MICROCONTROLLER
(PROCESSOR)

FIG.8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US16/58469

A. CLASSIFICATION OF SUBJECT MATTER
IPC: **G11C 14/00**(2006.01);**G11C 11/419**(2006.01)

USPC: G11C 14/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : G11C 14/00; G11C 14/0063

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 365/185.08

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,414,873 B1 (HERDT) 02 July 2002 (02.07.2002), entire document.	1, 3, 4, 6-10, 12 and 14-17
A	US 7,164,608 B2 (LEE) 16 January 2007 (16.01.2007), entire document.	2, 5, 11, 13 and 18-20
A	US 7,710,776 B2 (JOHAL et al.) 04 May 2010 (04.05.2010), entire document.	2, 5, 11, 13 and 18-20
A	US 8,861,271 B1 (ZAIN et al.) 14 October 2014 (14.10.2014), entire document.	2, 5, 11, 13 and 18-20
A	US 8,976,588 B2 (LEE) 10 March 2015 (10.03.2015), entire document.	2, 5, 11, 13 and 18-20
A	US 9,177,644 B2 (TSAO et al.) 03 November 2015 (03.11.2015), entire document.	2, 5, 11, 13 and 18-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 March 2017 (22.03.2017)	23 MAR 2017
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-8300	Authorized officer Seungsook Ham Telephone No. (571) 272-4300

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT	International application No. PCT/US16/58469

Continuation of B. FIELDS SEARCHED Item 3:
EAST: US-PGPUB; USPAT; DERWENT; USOCR; FPRS; EPO; JPO; IBM_TDB
Search Terms: sonos, ono, symmetr$6, non-volatile, scram, static, memory, storage, element, connect$4, nonvolatile, redundan$4, nvsram, $2ram, random, "Term Removed"