

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
29 December 2004 (29.12.2004)

PCT

(10) International Publication Number
WO 2004/114199 A1

(51) International Patent Classification⁷: **G06J 1/00**

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(21) International Application Number:
PCT/US2004/019476

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(22) International Filing Date: 17 June 2004 (17.06.2004)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/479,197 17 June 2003 (17.06.2003) US

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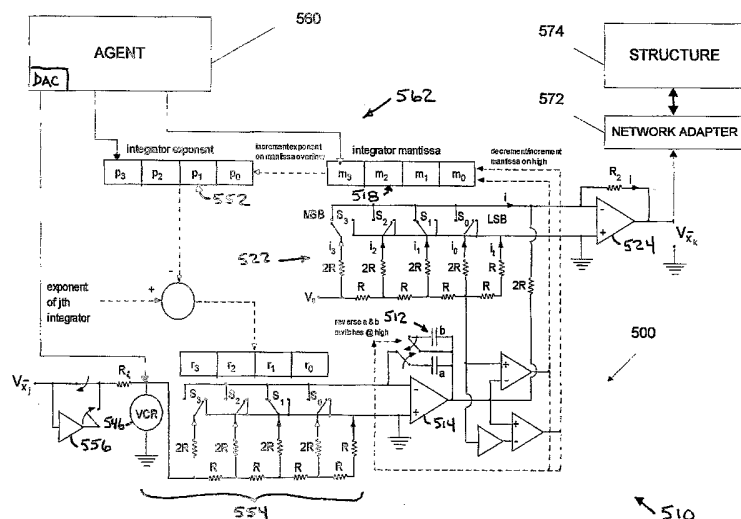
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(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: HYPBRID COMPUTATION APPARATUS, SYSTEMS, AND METHODS



(57) Abstract: An apparatus or system may include an analog accumulator coupled to one or more digital registers. The digital registers may include one or more values that are adjusted when an output of the analog accumulator is approximately equal to some selected value, and the output of the analog accumulator may be adjusted when the digital register values are adjusted. Some systems may include a digital-to-analog converter to receive the digital register values. A summing mechanism may be included, with a summed analog output approximately equal to the analog output of the converter, plus the output of the analog accumulator. Methods and articles may operate to integrate analog inputs to provide an integrated analog output, adjust a register value included in a digital register when the integrated analog output is approximately equal to a selected value, and then reset the integrated analog output.



Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

HYBRID COMPUTATION APPARATUS, SYSTEMS, AND METHODS

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Technical Field

Various embodiments relate generally to apparatus, systems, and methods for computation, including those using a combination of digital and analog approaches to the solution of various problems, such as system simulation, among others.

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Background

Accurate, realistic, and rapid simulations of dynamic systems have become increasingly important to a number of industrial sectors: virtual machinery, wherein the dynamic performance of system designs such as automobiles, aircraft, or acoustic gear can be thoroughly tested prior to making, or even without prototypes; virtual reality, for more realistic computer games, or for use in automotive and aircraft flight simulators; and computationally intensive fields such as structural dynamics with finite element modeling (FEM), computational fluid dynamics, and meteorology, to allow simulations in real time, and faster.

20

Numerical solutions and simulating such models can be severely limited by existing computer platforms. For very large scale systems, wherein system orders and/or degrees of freedom can exceed hundreds of thousands or millions, the numerical solution process may take several hours to simulate just a few seconds of real time. Stiff and strongly nonlinear systems of equations may impose further demands: time steps may need to be shortened for stability, and there may be no assurance that the generated solution is consistent (e.g., that it follows the “exact” solution if one exists), or accurate.

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Thus, there is a need for apparatus, systems, articles, and methods to more efficiently solve very large scale systems of differential equations at real-time speeds, or faster. Such activity may be useful with respect to testing and simulating machinery operations, virtual reality, realistic computer games,

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automotive and aircraft simulators, and in computationally intense fields such as fluid dynamics, structural dynamics, and meteorology.

Brief Description of the Figures

5 FIGs. 1A and 1B are block diagrams of hybrid integrator apparatus according to various embodiments of the invention;

 FIG. 2 is a block diagram of mantissa logic for a hybrid integrator apparatus according to various embodiments of the invention;

 FIG. 3 is a block diagram of a hybrid integrator apparatus with an R-2R
10 ladder converter according to various embodiments of the invention;

 FIG. 4 is a block diagram of a hybrid integrator apparatus with a voltage-controlled resistor input according to various embodiments of the invention;

 FIG. 5 is a block diagram of a hybrid integrator apparatus and system according to various embodiments of the invention;

15 FIG. 6 is a flow diagram of a neural network according to various embodiments of the invention; and

 FIG. 7 is a flow diagram of several methods according to various embodiments of the invention.

20 Detailed Description

 Various types of computer platforms may be used to address some of the challenges mentioned above. For example, some computing machines are analog, and used to simulate a dynamic system's response via a mechanical apparatus having a dynamic system topology (e.g., inertia, stiffness, and
25 damping) with differential equations and response to excitations that were similar to the actual system.

 Electronic analog computers with integrators may be used to improve this solution. Derivatives $x' = dx/dt$ constructed from the algorithm suggested by the right hand side of a system's differential equations, such as those shown in
30 Equation (1a) and (1b) below:

$$x' = f(t, x) \tag{1a}$$

$$x_k' = \sum_{j=1}^n a_{jk} x_j + g_k(t) \quad (\text{linear systems}) \quad (1b)$$

can be integrated by the analog computer's integrators into states $x(t)$.

It should be noted that Equation (1a), if vectorized, can represent a system of equations, such as the system of linear equations of Equation (1b), for $k=1,2,\dots,n$. Algebraic operations such as sums, multiplication, and division inherent in $f(t,x)$ can be implemented by active analog circuitry such as resistor coupled inputs to operational amplifiers with appropriate feedback elements, or multiplexers. The system's states $x(t)$ can be stored as charges on the integrators' feedback capacitors; the initial conditions may be set up as initial charges placed on these capacitors.

Analog computers can be set up to solve systems of time continuous differential equations. However, difficulties may arise due to a number of factors:

- (1) magnitude scaling problems when analog components exceed limits imposed by supply voltages; time scaling problems arising from time constants associated with integrator capacitors and resistors;
- (2) accuracy problems originating from components (e.g., resistors, capacitors) not being of desired values, circuit analysis approximations, and intrinsic electronic noise generated by resistors (thermal noise), direct currents (DC) (shot noise), and active devices like transistors (flicker and popcorn noise);
- (3) the inability to apply logic, in order to control the solution process, since changing to different functional forms and solution branches for nonlinear systems can be difficult;
- (4) converting a time continuous voltage into numbers for design and analysis;
- (5) synthesizing complicated nonlinear functions contained in $f(t,x)$;
- (6) recording a precise time base; and

- (7) tedious programming, possibly including manual patching of circuits.

In summary, the analog computer can be a powerful, but severely limited, tool for solving systems of equations

- 5 Differential equations may be simulated and numerically solved using digital computers with an appropriate numerical method. Time continuous differential equations may be converted into an equivalent system of time discrete difference equations, with derivatives approximated by finite differences. However, solving a dynamic system using difference equations may lead to numerical stability and accuracy problems, including stiff system issues, numerical stability, function smoothness difficulties, rounding and truncation errors, and error buildup. However, with special considerations, including extended precision, very short time steps, use of robust but slower numerical methods, and choosing numerical methods appropriate to the problem at hand, 10 stability and sufficient accuracy may still be possible. Thus, numerical solutions using digital computation systems may also suffer from various limitations.

- Neural computers, based on multiple layers of interconnected perceptrons or processing units, can self organize interconnections and "learn" nonlinear functional relationships between selected sets of input and output signals. 20 Perceptrons may include weighting elements that scale input signals, biasing elements that add constant amounts to perceptron outputs, and a sigmoidal function that operates on the overall sum of scaled inputs. The sigmoidal function can be linear over a limited domain, but may saturate outside the domain. Neural networks with an input layer, at least one hidden layer, and an output layer can approximate complicated input-output functional relations. 25 To approximate nonlinear functions, the curved sigmoidal functions of neural networks may form a basis for piecewise approximation of curved and discontinuous nonlinearities. Via proper "learning", neural networks can simultaneously store multiple input-output relations, and may be relatively insensitive to noise and other competing signals. However, neural networks may 30 have limited ability to directly program input-output relations, as these may be

learned from data. Neural networks may also have limited sequential logic capabilities.

Embodiments of the invention may include a computer platform that merges analog, digital, and neural computers into an integrated unit for solving
5 time continuous differential equations, as well as partial differential equations having time as an independent variable. The combining of computer platforms may overcome several of the problems associated with any single platform. Solutions for large and/or complex systems may be accomplished in real time or faster, with three or more digits of precision, independent of the size of the
10 system. Example applications include large scale dynamic systems (aircraft structures, motors, gearing systems, rotor dynamics) and field problems, including those found in meteorology. For example, to couple to a meteorology problem, the meteorological equations of motion might be programmed onto the hybrid computer, most likely via an agent or host computer. This approach need
15 not involve sensors as part of the hybrid computer, but sensors may serve as inputs to the agent.

Since several embodiments include analog components, time step and speed of computation issues may be reduced. Via modern circuit fabrication methods, the technology involved may be miniaturized, and placed on a chip for
20 use in a hand held device or personal computer (PC).

Some embodiments of the invention employ an analog integrator, augmented with a counter digital register. The process of integration may be compared to filling a cup of water from a high flow faucet: when a cup is filled, the cup is dumped and the volume is recorded using a count of filled cups.
25 Similarly, when the analog integrator is full, a digital register is incremented, counting the number of full integrators. This counting process constructs a mantissa for a floating point representation of a time continuous analog integration. When the counter overflows, spillover of the integer's mantissa constructs an exponent.

30 In summary, the mantissa may be decremented when the integrator voltage goes below the negative threshold, avoiding integrator saturation. Separate comparators for each analog integrator may be used to monitor positive

and negative thresholds, such that attaining or exceeding a threshold triggers a high on the appropriate comparator. High on the positive voltage monitoring comparator may trigger an increment to the associated register, high on the negative voltage monitoring comparator may trigger a decrement to the associated register. Such embodiments may extend the numerical range of an analog integrator by orders of magnitude, so that the results are comparable to digital computer floating point numbers, while still being analog.

Some embodiments of the invention do not need analog to digital converters, since the integrator with register counting approach has a dual analog and digital nature. This can avoid sampled data problems, as will be explained below.

Compared to digital computers using numerical methods to solve very large scale systems of differential and partial differential equations, the methods disclosed herein should be faster, permitting computation in real time or better. Such methods, by their nature, are time continuous, avoiding numerical truncation errors, as stability or stiff system problems may present.

The hybrid computer of some embodiments may be used to solve time continuous linear and non-linear ordinary differential equations, as well as partial differential equations with time as an independent variable. Examples could include dynamic systems such as motors, helicopters, and electrical systems, or solid or fluidic systems (for example, meteorology systems) with time as an independent variable.

In some embodiments, precision of the solution may be limited to about three to five digits, sufficient for most engineering and science applications, and virtual reality simulations. Higher precision may be achieved by applying predictor-corrector numerical methods to the generated solution. For example, treating the solution as the predictor phase, and applying an appropriate corrector to achieve any level of precision within the accuracy of the digital processor.

The precision achieved involves a trade-off between noise levels and circuit supply voltages. With certain embodiments, external and intrinsic noise levels in electronic systems can be limited to about 10-50 micro-volts root-mean-square (RMS). For the analog simulations to be most useful, the output voltages

of the analog integrators may need to be at least an order of magnitude or two greater than noise levels. Thus the switching threshold for the analog integrator, equal to the least significant bit of the digital mantissa, should be set to at least or at about 0.1 to about 1 millivolt. This becomes a lowest voltage limit for the
5 least significant bit. The upper limit is bounded by the supply voltage of the computer. For example, the electronics for many embodiments can be fabricated via complementary metal-oxide semiconductor (CMOS) fabrication methods. Certain types of CMOS technology have a maximum supply of about 3 volts; voltages higher than this may damage CMOS technology. Thus, in terms of
10 precision, the ratio of maximum to minimum output voltage is 3 volts/1 millivolt = 3,000 (or for 0.1 mV, 3 volts/0.1 millivolt = 30,000). Since 999 fills three decimal digits, 3,000 or 30,000 gives 3 to 4 digits, respectively.

In a PC, some embodiments of the invention could act as a co-processor that rivals supercomputers for solving differential equations. In simulators and
15 hand held devices such as games or personal assistants, very realistic virtual reality simulations for very complicated dynamic systems could be performed in real time or faster. Solutions provided may include numerical estimates of states at selected times.

For the purposes of this document, an "accumulator" may mean a device
20 that operates to accumulate an amount of charge over time, such as a voltage or current integrator, perhaps constructed using one or more operational amplifiers capable of being electrically coupled to one or more capacitors.

The term "analog bit" includes analog circuitry, such as the analog integrator, whose voltage output, when summed to the voltage output by a digital
25 to analog converter, produces a total output voltage that is continuous. The analog circuit is deemed an "analog bit" if its continuous output voltage is less than the voltage corresponding to the digital to analog converter's least significant bit, and if, when summed to the voltage of a digital to analog converter, produces a continuous total output voltage. The term analog bit may
30 be contrasted with a "digital bit," which, when comprising part of a digital register that controls a digital to analog converter, can only render a voltage output with discrete changes in voltage that correspond to integers.

A "hybrid integrator cell" is one complete hybrid integrating unit, comprising an analog integrator, one or more comparators, logic, registers, a digital to analog converter, and a summer. This cell is a complete integrator because its output is continuous and extends over several orders of magnitude.

5 In some embodiments, an apparatus may include a redesigned integrator, and interacting analog and digital sections. The user might use a digital computer "host" (i.e., an external agent) to enter the initial value problem, such as Equations (1a) and (1b), with initial conditions. Using hardware discussed below, a front end interface program in the digital host might be used to
10 "program" the analog elements, specifying the resistance of input and feedback resistors, capacitance of feedback capacitors, supply voltages to operational amplifiers, and initial conditions on integrators. The redesigned analog integrators, having a dual analog and digital nature, with both digital and analog outputs, can operate to integrate the differential equations. Simulations can be
15 time continuous and consistent with exact solutions, stable if the dynamic system (e.g., Equations 1a and 1b) is stable, and have all states solved substantially instantaneously and substantially in parallel. The analog solution may be accurate to three digits of precision, or better.

FIGs. 1A and 1B are block diagrams of hybrid integrator apparatus 100
20 according to various embodiments of the invention, each of which may operate in the manner described. In some embodiments, the apparatus 100 may include switched feedback capacitors 112 coupled to an analog integrator 114 and/or switched analog integrators 116.

A hybrid analog-digital integrator apparatus 100 can extend the range of
25 a purely analog integrator by storing results in a digital (mantissa) register 118 and on an analog integrator 114, 116. Results are real numbers $x = m + \lambda$, including an integer m stored in the mantissa digital register 118, and a real number λ with $|\lambda| < 1$ stored as a voltage V_λ by the analog integrator 114, 116.

30 The apparatus may have one or more feedback capacitors 112, or analog integrators 116 coupled in parallel, an array of input resistors 120, one or more digital registers (e.g., 118), a digital-to-analog converter (DAC) 122, a summer

124, perhaps including a summing amplifier, and hardwired logic (not shown in FIGs. 1A and 1B – see FIG. 2, element 230).

Input signals e_1 , e_2 , e_3 may be applied to the input 126 of the apparatus 100 via input resistors 120. Using a switching scheme, in some embodiments, only one feedback capacitor a,b (or integrator a,b) is engaged at a time. For example, in FIG. 1A, when capacitor a (or integrator a in FIG. 1B) is engaged, capacitor/integrator b is not, and vice-versa. Before an integrator 114, 116 saturates, its output voltage V_λ represents the time continuous integral of the input 126.

When switching the capacitors 112, the integrator 114 should not saturate with proper setting of the threshold voltage, (e.g., about a millivolt or more). For switching between capacitors 112, switching may be delayed by a non-instantaneous comparator. During the delay, additional residue charge beyond the switching threshold may be accumulated onto the capacitor. Compensating for switching delay might involve "dumping" the residue charge collected by the in-circuit capacitor to another capacitor to be switched into the circuit. This capacitor may be placed in a queue, awaiting its turn. The residue should be tiny compared to the least significant bit of the registers, but can accumulate over time, if not compensated. A third capacitor (i.e., the residue capacitor, not shown) can be used in this way to bring this residue back into the analog integrator as an initial charge when it is switched into the circuit. Thus, a chain of three capacitors may be switched into the circuit: one capacitor is actively engaged, and two are in a queue. The residue charge is transferred to the "residue capacitor" at the end of the queue.

FIG. 2 is a block diagram of mantissa logic 230 for a hybrid integrator apparatus 200 according to various embodiments of the invention. Whenever V_λ reaches a positive threshold $+V_0$, hardwired logic 230 (e.g., comparators 232 that compare V_λ to $+V_0$) may operate to: increase the binary number m (e.g., $m_0 \dots m_n$) in the digital register 218 (e.g., register 118 associated with the DAC 122 in FIGs. 1A and 1B) by one (or some other amount), engage the capacitor b (in FIG. 1A) or the integrator b (in FIG. 1B) to continue the analog integration, and

disengage the capacitor a (as well as discharging the capacitor a), or integrator a in preparation for the next integration cycle.

When V_λ reaches the negative threshold $-V_0$, the binary number m in the digital register 218 may be decreased by one (or some other amount); and
5 switching of integrators or capacitors (and discharge of capacitors) can then occur. The threshold voltage $+V_0$ should be approximately equal to the nodal voltage of the DAC's least significant bit (see FIGs. 1A and 1B), or to a value related to the DAC's least significant bit. Thus, many embodiments may be realized.

10 For example, referring now to FIGs. 1A, 1B, and 2, an apparatus 100, 200 may include an analog accumulator 138 and at least one digital register 118, 218. The digital register 118, 218 may include a register value m to be adjusted when an output V_λ of the analog accumulator 138 is approximately equal to some selected value (e.g., less than the saturation value of the associated
15 integrators 114, 116, 214). The output V_λ of the analog accumulator 138 may be adjusted when the register value m is adjusted.

In some embodiments, the output V_λ of the analog accumulator 138 may be adjusted by resetting the output V_λ (e.g., reset to zero). The register value m may be adjusted by incrementing the register value m if the selected value for
20 adjustment is a positive overflow or threshold value. The register value m may be adjusted by decrementing the register value m if the selected value for adjustment is a negative overflow or threshold value.

Referring to FIG. 1A, it can now be seen that in some embodiments, the analog accumulator 138 may comprise an analog integrator 114, one or more
25 capacitors 112 capable of being electrically coupled to the analog integrator 114, and at least one switch 146 capable of coupling an analog input voltage e_1 , e_2 , e_3 to the first capacitor a in a first switch state, and to the second capacitor b in a second switch state. Similarly, referring now to FIG. 1B, it can be seen that in some embodiments, the analog accumulator 138 may comprise one or more
30 analog integrators 116 and/or at least one switch 140 capable of coupling an analog input voltage e_1 , e_2 , e_3 to an input 142 of the first analog integrator in a

first switch state, and to an input 144 of the second analog integrator in a second switch state. Many other embodiments may be realized.

For example, FIG. 3 is a block diagram of a hybrid integrator apparatus 300 with an R-2R ladder converter 322 according to various embodiments of the invention. The threshold voltage $V_0 = 2^{I-N} V_s$ is the ladder's nodal voltage for the least significant bit LSB of the converter 322, where N is the number of bits for the converter 322. The voltage pertaining to m is not part of V_λ . To reconstruct the output voltage V_λ , the converter 322 may generate a voltage V_m corresponding to m , and the summer 324, which may comprise a summing operational amplifier may add this to V_λ . Using a feedback resistor $R_2 = 2R$, where R is the ladder's characteristic resistance, the hybrid integrator apparatus 300 may then provide an integrated output voltage V_x . Benefits may include:

- (1) maintaining a digital representation m and a time continuous result V_x of integral x ;
- (2) generating m without using analog to digital converters, or sample and hold devices;
- (3) extending the integrator's range beyond normal saturation limits (via the mantissa m and an exponent to be discussed below);
- (4) storing an integer m in a digital register, the most significant portion of integral x , relatively immune to electronic noise; and
- (5) relegating V_λ , that portion of x sensitive to electronic noise, below the significance of the least significant bit.

During operation, a positive input voltage V_i applied to the analog integrator 314 may pass through two operational amplifiers 314, 324, rendering a positive output V_x . For the sign of component V_m to be consistent, the supply voltage V_s to the R-2R ladder may be set to a negative value, since the ladder's output passes through one operational amplifier 324. For the converter 322 to provide negative values, a "sign bit" (not shown in FIG. 3) and an appropriate arithmetic such as 2's complement arithmetic should be included. To implement

2's complements in the converter output voltages, when the sign bit is set, an additional voltage ($-V_s$, not shown) can be added to the summing operational amplifier.

Although this scheme may extend the range of the integrator 314, the register 318 may eventually overflow or underflow, creating a different magnitude scaling problem. For example, if all bits (excluding the sign bit) of the mantissa m in FIGs. 1A, 1B are set, overflow of the analog integrators 114, 116 initiates an increment sequence, which overflows the digital register m . This situation can be avoided by introducing an exponent p and extending x to floating point numbers: $(m + \lambda)$ now becomes an extended "mantissa", and the integral is augmented to $x = (m + \lambda)2^p$. The value of the exponent p may be increased or decreased to prevent saturation of an integrator's summer (e.g., summing operational amplifier), or to compensate for overflow or underflow of the mantissa.

Several benefits may accrue. For example, the exponent factor 2^p may be used to scale the variable $(m + \lambda)$, "sliding" the operating range of the hybrid integrator apparatus 300 up or down as needed to avoid operational amplifier or converter saturation, or "wash out" of tiny signals by underlying noise. The floating point representation $(m + \lambda)2^p$ is compatible with existing digital computers. Hardwired logic may be used to increment or decrement the exponent p , changing the gains of summing operational amplifiers and to move or "slide" the voltage range of the hybrid integrator apparatus 300. Further, overflow can be compensated by rotating the mantissa register 318 right a single bit, followed by incrementing the exponent p . Rotating right halves the mantissa and the converter's voltage V_m . To compensate for this effect, the exponent p may be incremented. This operation can be initiated when a "full" analog integrator trips the hardwired logic and increments (or decrements) the "full" mantissa, wherein all bits (excluding the sign bit) are set. At this point, the integral's mantissa $(m + \lambda)$ is the binary number 0111...1 + 1 = 1000...0, within the computer's accuracy. The underlined digit is the "carry" bit. Thus, a rotate right operation, or division by 2, which renders the result 0100...0, does not typically affect digits of precision.

Such operations may scale the local state variable $x_k = \bar{x}_k 2^{p_k}$, where exponent p_k records the number of past scaling operations, and the governing differential equation. For example, upon scaling Equation (1b) would become

$$\bar{x}_k' = \sum_{\substack{j=1 \\ j \neq k}}^n a_{jk} x_j 2^{-p_k} + a_{kk} \bar{x}_k + 2^{-p_k} g_k(t) \quad (2)$$

5 Since the other integrators expect x_k and not $\bar{x}_k$, this scaling factor 2^{p_k} should be restored when feeding the output of this integrator to other integrators. That is, the scaling factor 2^{p_k} should be restored to $\bar{x}_k$ when the output is sent to another differential equation. This may eliminate the need to inform other integrators that a certain variable was scaled, since keeping track of which variables were
10 scaled, and by how much, and then sending information to other integrators, could become onerous when thousands of variables and thus, integrators, are involved.

For other integrators feeding their scaled variables $x_j = \bar{x}_j 2^{p_j}$ to the k th integrator, Equation (2) would become:

$$\bar{x}_k' = \sum_{\substack{j=1 \\ j \neq k}}^n a_{jk} \bar{x}_j 2^{p_j - p_k} + a_{kk} \bar{x}_k + 2^{-p_k} g_k(t) \quad (3)$$

This redefines the gain from other integrators from a_{jk} to $\bar{a}_{jk} = 2^{p_j - p_k} a_{jk}$. Other embodiments may be realized.

FIG. 4 is a block diagram of a hybrid integrator apparatus 400 with a voltage-controlled resistor 446 input according to various embodiments of the
20 invention. In this case, the voltage-controlled resistor (VCR) may be used to replace the input resistors (see elements 120 of FIGs. 1A and 1B) into the analog integrator 414.

The power of two factor $2^{p_j - p_k}$ can be synthesized by a switched R-2R ladder 448 into the analog integrator 414, similar to the R-2R ladder into the
25 digital to analog converter of FIG. 3. Since this scaling factor $r_{jk} = p_j - p_k$ is the difference between p_j and p_k , its magnitude may increase more slowly than the state variables. If a certain state x_k becomes large, say 2^{80} , coupling in the equations may cause other states x_j to become large, say 2^{75} . However, the

magnitude of the difference in exponents $r_{jk} = 80 - 75$ may remain considerably smaller. The 2^{-p_k} gain factor applied to the input function $g_k(t)$ can be synthesized by a ladder in the same way, or on a software level, since $g_k(t)$ can come from the host computer via a DAC, or similar element.

5 The constant factor a_{jk} may be programmed by tuning the VCR, which may include a field effect transistor (FET) operating in deep triode region with source to drain channel resistances adjusted via gate to source voltages. The scaling of $2^{p_j - p_k}$ may arise from the R-2R ladder 448 into the integrator 414. If the resistance value R is made sufficiently large, the drain to source voltage of
 10 the FET in the VCR can remain acceptably small, avoiding VCR resistance distortions. Another possibility involves using only the R-2R ladder to implement the gain coefficient a_{jk} , eliminating the resistance of the VCR and R into the ladder 448. Here initial setting of the ladder switches $s_0 \dots s_3$ can be used to adjust the value of a_{jk} , and scaling $2^{p_j - p_k}$ would arise by rotating the
 15 entire register 418 (left or right) the requisite number of bits. The ladder 448 may need many steps or rungs to achieve the desired precision and/or magnitude of gain adjustments. Many other embodiments may be realized.

For example, FIG. 5 is a block diagram of a hybrid integrator apparatus 500 and system 510 according to various embodiments of the invention. In this
 20 exemplary embodiment, the apparatus 500 includes an analog integrator 514 with switched feedback capacitors 512, a mantissa register 518 with the converter 522, exponent register 552, and a scaling circuit (e.g., an input resistor network) 554. Thus, in some embodiments, an apparatus 500 may include a scaling circuit 554 capable of coupling an analog input voltage $V_{\bar{x}_j}$ to an input of
 25 the analog accumulator 514. The scaling circuit 554 may comprise a programmable resistance ladder (e.g., an R-2R ladder).

In this figure, the conceptual examples shown in FIGs. 1-4 are collected into a computational system. The inverter 556 may be or include a FET switched into the circuitry whenever the coefficient $a_{jk} < 0$. This inverter 556 and
 30 the resistive network 554 may be implemented for every input to an integrator 514. The output of the integrator 514 may be characterized as:

$$V_{\bar{x}_k} \approx -\frac{R_2}{2R} \left(-\frac{1}{RC} \sum_j \sigma_j \frac{VCR_j}{VCR_j + R} \frac{1}{2^M} \sum_{s=0}^{M-1} r_s 2^s \int_{t_0}^t V_{\bar{x}_j} dt + \frac{V_s}{2^{N-1}} \sum_{q=0}^{N-1} m_q 2^q \right) \quad (4)$$

where σ_j is the sign from the switched inverting operational amplifier. Within the parenthesis of Equation (4), the first term arises from the analog integrator 514, and the second term from the digital register 518 with the converter 522. Here the scaling factor in the integer term $V_s/2^{N-1}$ may be on the order of millivolts, to overpower intrinsic electronic noise; $R_2/2R$ may be unity so that the hybrid integrator apparatus 500 may produce the same voltage output level as a traditional analog integrator; and $RC \approx 2^{-M/2}$, to compensate for severe attenuation of voltages imposed by exponent scaling with the ladder in the converter 522. The number of bits used for the ladders' registers $N \approx 10$ to 14 can renders three to five 5 digits of precision for V_m , and if $M \approx 10$ to 30, the scaling factors $2^{p_j - p_k}$ may be on the order of 10^3 to 10^9 . As mentioned previously, moderate scaling factors can render much larger magnitude scaling in equations.

The hybrid integrator apparatus 500 may also permit setting initial conditions: rather than placing an initial charge onto a feedback capacitor, initial conditions may be loaded as binary numbers onto the digital registers for m and p (e.g., registers 518 and 552). These registers may be referenced by a digital host processor, or external agent 560, as memory locations. Thus, in some embodiments, a digital register 562 may comprise a mantissa register 518 and an exponent register 552 that has an exponent value p to be adjusted when the mantissa register value m is approximately equal to a selected mantissa value (e.g., an overflow or underflow value). For example, the exponent value p may be adjusted by incrementing the exponent value p if the selected mantissa value m is a selected mantissa overflow value. The exponent value p may also be adjusted by decrementing the exponent value p if the selected mantissa value m is a selected mantissa underflow value.

The external agent 560, which may comprise a digital computer, such as a PC, may be used in many ways. For example, register values m, p may be

adjusted to selected initial values by the external agent 560. Initial analog values, perhaps made available using DAC residing in the agent 560, may be provided to an input of the analog accumulator 514. Other embodiments may be realized.

5 For example, an apparatus 500 may include a replication of all components shown in FIG. 5, such that an apparatus 500 may include a plurality of analog accumulators 514 and a corresponding plurality of digital registers 562. One or more of the corresponding plurality of digital registers 562 may include a register value m to be adjusted when an output of one of the plurality
10 of analog accumulators 514 to which one of the plurality of digital registers 562 corresponds is approximately equal to a selected value (e.g., an overflow or underflow value). The register value p included in the one of the plurality of digital registers 562 is capable of being adjusted responsive to a change in a condition (e.g., a change in the value m) of another one of the plurality of digital
15 registers 518.

As noted previously, the analog accumulator 514 may be adjusted by resetting the output. Register values m , p may be adjusted based on positive and negative overflow and underflow values, as described previously. In addition, as described above, the output of one or more of the plurality of analog
20 accumulators may be scaled.

In some embodiments, the values of mantissa m and exponent p may continuously evolve. To record the solution, the contents of these registers may be transferred to nonvolatile random access memory (RAM) or some form of permanent storage. If done at time increments gauged by the agent's clock, a
25 "time base" may be implicitly appended. This "sampling" process is not necessary for solution, but can be useful for recording time. The smallest "time step" δt for fetching the solution may be limited by the agent's speed of data transfer to memory, which may be one or two computer clock cycles.

Converting simulations to real time may involve the RC time constant, as
30 well as δt . Through time scaling, reducing RC time constants of integrators and presenting the input excitation functions to the system at faster rates, the solution can be generated faster than real time. Different values of feedback capacitors

can be selected by placing other (*a* and *b* pairs of feedback) capacitors in parallel with capacitors *a* and *b* of FIG. 1A, engaging via switches whatever capacitors give the desired overall capacitance.

5 With three to five digits of precision, a hybrid computer system's raw results may be sufficient for most engineering and virtual reality purposes. Numerical solution methods typically require 15+ digits to combat buildup of computational errors over time arising from rounding, truncation, and numerical approximations. A hybrid computer system may not be subject to such error buildups.

10 When greater precision is needed, a corrective numerical method could refine results to increase the number of digits. Here hybrid computer results could be treated as the predictor phase of predictor-corrector numerical methods, and then established corrector methods might be used to achieve whatever accuracy is desired. Since the hybrid computer may run faster than and be
15 independent of the agent 560, corrections may be run simultaneously. For many problems, corrections could be done in real time, or faster.

For example, a 1 GHz processor might implement roughly 2000 floating point instructions every 10 microseconds, correcting while it awaits the next solution point. For a simple trapezoidal corrector algorithm, a 1 GHz PC could
20 correct 400 states, at least two times, in that same time period. Since the numerical algorithms follow and iteratively refine solution estimates generated by the stable analog computer, the corrective numerical algorithms should be stable and relatively unaffected by the size of the "time step" δt . With a 1 GHz clock, "sample times" δt should be relatively short. Consequently, corrective
25 algorithms based on trapezoidal quadratures with truncation errors of order δt^2 , might provide more accurate results.

Resistors on the analog side may be programmed by the external agent 560, via switched R-2R ladders (e.g. within elements 522 and 554), feeding operational amplifiers, and VCRs (including FETs) 546. With voltage dividers
30 based on VCRs, the supply voltages to operational amplifiers and charges on capacitors could be controlled or set digitally. Additionally, the agent 560 could apply all input signals to the hybrid computer system, transmitting these via a

DAC, as mentioned previously. By controlling the size of capacitors and resistors of integrators (and hence their time constants, RC) and the rate of presentation of the input signals, the agent 560 may operate to time-scale and control the speed of solution.

5 Large-scale, mixed-signal, integrated circuit packages may be designed to implement the apparatus of various embodiments. For example, the analog section may include many interconnected operational amplifiers with input resistance, feedback circuits (resistance and capacitance), and supply voltage digitally programmable. The output of each summer (e.g., element 124 of FIG.
10 1A, such as a summing operational amplifier) may be coupled to the inputs of all integrators 126, such as integrating operational amplifiers. The number of interconnections (perhaps tens to hundreds to thousands) may be a design trade-off between the quantity needed to solve the vast majority of practical problems, limits on density of interconnections (e.g., as affected by geometry of circuit
15 interconnections, cross-talk, and heat removal), and fabrication expense.

Care should be taken when integrating analog and digital sub-systems. Analog and digital systems do not necessarily co-exist harmoniously, which suggests isolating these systems from each other, as is known to those of skill in the art. The fast pulses that clear and set bits in digital systems can manifest
20 themselves as high frequency "noise" with a potential for disrupting nearby analog systems. In addition, analog systems may act as low pass filters for digital pulses, rounding and reducing pulse heights, disturbing digital systems. The need for substantially simultaneous isolation and massive interconnections may require a special bus to convey signals between analog and digital sections.

25 In some embodiments, a computational system 510 may be constructed to include a computer, a digital signal processor, or a hybrid (digital/analog) computer. The system 510 may be coupled to an external agent 560, a network adapter 572 and then to a structure 574, or directly to the structure 574 that is to be characterized (in terms of vibration and/or other operational characteristics)
30 by solving systems of equations according to the apparatus, articles, methods, and systems of various embodiments of the invention. Coupling may be electric, mechanical, fluid, thermodynamic, or a combination of these. Still other

embodiments may be realized.

For example, referring to FIGs. 1A, 1B, and FIG. 5, a system 110, 510 may include one or more apparatus 100, 500, similar to or identical to each other and/or the apparatus 200, 300, and 400 previously described. The system 110, 510 may also include a converter 122, 522 having a digital input capable of receiving a register value m , with an analog output V_m responsive to the register value m . The system 110, 510, may also include a summing mechanism 124, such as a summing operational amplifier with a summed analog output V_x approximately equal to the analog output V_m plus the output V_a of the analog accumulator 114, 514 included in the apparatus 100, 500. The summed analog output V_x may be scaled.

The system 110, 510 may include a digital register 562 comprising a mantissa register 518 and an exponent register 552 having an exponent value adjusted when the register value m is approximately equal to a selected mantissa value. In some embodiments, the system 110, 510 may include a scaling circuit 554 capable of coupling an analog input voltage to an input of the analog accumulator 514, wherein the scaling circuit is capable of being communicatively coupled to the exponent register 552 and at least one other exponent register (where multiple exponent registers are coupled together).

As noted previously, in some embodiments, the analog accumulator 514 may be associated with an adjustable time constant. The register values m , p may be adjusted to desired initial values by an external agent 560, which may also provide initial analog values to an input of the analog accumulator 514. Still other embodiments may be realized.

For example, a system 510 may comprise a replication of any or all elements shown in FIG. 5, such that a system may include a plurality of analog accumulators 514 and a corresponding plurality of digital registers 562. Each one of the corresponding plurality of digital registers 562 may include a register value m to be adjusted when an output of one of the plurality of analog accumulators 514 to which the one of the plurality of digital registers 518 corresponds is approximately equal to a selected value. The register value p included in the one of the plurality of digital registers 552 may be adjusted

responsive to a change in a condition of another one of the plurality of digital registers 518.

In some embodiments, the system 110, 510 may also include a converter 122, 522 having a digital input capable of receiving the register value m included in the one of the plurality of digital registers 562, with an analog output responsive to the register value m . The system 110, 510 may include a summing mechanism 124, 524 having a summed analog output approximately equal to the responsive analog output plus the output of the one of the plurality of analog accumulators 514. The digital registers 562 may include mantissa registers 518, exponent registers 552. The system 510 may also include scaling circuits 554. External agents 560 may be used to adjust or set initial values, as described previously. Yet other embodiments may be realized.

For example, FIG. 6 is a flow diagram of a neural network 676 according to various embodiments of the invention. Neural networks 676 may be used to synthesize nonlinearities. Each node 678 may comprise an operational amplifier driven through saturation. The output f_k may be applied to one of the analog integrators described previously (e.g., element 514 of FIG. 5).

Operational amplifiers with resistor input and feedback, allowed to saturate, can behave like perceptron units, the basic artificial neuron. A few neurons, enough to form input, hidden, and output layers, may be used to approximate arbitrary nonlinear relationships between input(s) and an output(s). Using neural methods, nonlinear functions included in Equation (1a) can be synthesized for the analog elements, with substantially arbitrary accuracy. Finally, since a combination of a neural network and a hybrid analog-digital apparatus has a dual nature, data for constitutive laws of materials and dynamic system elements can be entered as digital arrays, analog signals, or the neural networks coupled to the apparatus can "learn" the functional relations inherent in data measured from tests, permitting heuristic constitutive laws to be used in computations.

The apparatus 100, 200, 300, 400, 500, systems 110, 510, capacitors 112, 512, integrators 114, 116, 214, 314, 414, 514, registers 118, 218, 318, 518, 552, 562, voltage V_λ , resistors 120, converters 122, 322, 522, summer 124, 324, 524, logic

230, input signals e_1, e_2, e_3 , input 126, capacitors a, b , integrators a, b , comparators 232, 342, numbers m, p , voltages $+V_0, V_m, V_x, V_{x_j}$, accumulator 138, switches 140, 146, inputs 142, 144, capacitors C , resistors R, R_2 , operational amplifiers 324, 342, local state variable x_i , scaled variables x_j , gains $\bar{a}_{jk}$, VCR 446, switched R-2R ladder 448, exponent register 552, scaling circuit 554, inverter 556, external agent 560, time step δt , network adapter 572, structure 574, neural network 676, nodes 678, and output f_k may all be characterized as “modules” herein. Such modules may include hardware circuitry, and/or a processor and/or memory circuits, software program modules and objects, and/or firmware, and combinations thereof, as desired by the architect of the apparatus 100, 200, 300, 400, 500 and systems 110, 510 and as appropriate for particular implementations of various embodiments. For example, such modules may be included in a system operation simulation package, such as a software electrical signal simulation package, a power usage and distribution simulation package, a capacitance-inductance simulation package, a power/heat dissipation simulation package, and/or a combination of software and hardware used to simulate the operation of various industrial systems.

It should also be understood that the apparatus and systems of various embodiments can be used in applications other than as has been specifically described in terms of a PC implementation. The principles disclosed may be used in other software and hardware products, such as file input-output subsystems, database engines, etc., or in equipment applications such as measurement gear, testers, signal processors, and/or filters. The illustrations of apparatus 100, 200, 300, 400, 500 and systems 110, 510 are intended to provide a general understanding of the structure of various embodiments, and they are not intended to serve as a complete description of all the elements and features of apparatus and systems that might make use of the structures described herein.

Applications that may include the novel apparatus and systems of various embodiments include electronic circuitry used in high-speed computers, communication and signal processing circuitry, modems, processor modules,

embedded processors, data switches, and application-specific modules, including multilayer, multi-chip modules. Such apparatus and systems may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers, workstations, radios, video
5 players, vehicles, and others. Some embodiments include a number of methods.

For example, FIG. 7 is a flow diagram of several methods 711 according to various embodiments of the invention. For example, a method 711 may (optionally) begin at block 721 with integrating an analog input to provide an integrated analog output, adjusting (e.g., incrementing or decrementing) a
10 register value included in a digital register when the integrated analog output is approximately equal to a selected value at block 725, and resetting the integrated analog output at block 731.

As noted above, the selected value may be a selected overflow value, and adjusting the register value may include incrementing the register value when the
15 integrated analog output is approximately equal to the selected overflow value. The selected value may also be a selected underflow value, and adjusting the register value may include decrementing the register value when the integrated analog output is approximately equal to the selected underflow value.

Depending on the connections between registers (e.g., how the values m and p
20 are related), the method 711 may include incrementing another register value included in another digital register when the register value is approximately equal to a selected overflow value and resetting the register value at block 725 and 731. In some embodiments, the method 711 may include decrementing another register value included in another digital register when the register value
25 is approximately equal to a selected underflow value and resetting the register value at block 725 and 731.

The method 711 may continue at block 751 with setting a register value to an initial condition value, which may in turn include setting a mantissa register value to a first initial condition value, and setting an exponent register
30 value to a second initial condition value. These first and the second initial condition values may be provided by an external agent, such as a computer. In

some embodiments, the method 711 may set an adjustable time constant associated with integrating the analog input at block 755.

The method 711 may continue with transferring one or more register values to memory at block 761, and resetting the register value to a selected
5 initial condition value at block 765. In some embodiments, the method 711 may include scaling the analog input at block 769, which in turn may include scaling the analog input responsive to an exponent value adjusted when a register value is approximately equal to a selected mantissa value. Depending on the interconnections between registers, scaling activity may comprise scaling the
10 analog input responsive to another exponent value included in another register.

The method 711 may include converting the register value to a mantissa analog output at block 773, as well as adding the mantissa analog output to the integrated analog output to provide a summed analog output, at block 773. The method may also include scaling the integrated analog output to the summed
15 analog output at block 773.

In some embodiments, the method 711 may include transferring the register value to a memory (see block 761), and resetting the register value to a selected initial condition value at block 777. The selected initial condition value may be provided by an external agent, which may comprise a computer.

20 The method 711 may include correcting a sum of the integrated analog value and an analog version of the register value using an a-posteriori iterative method, as described previously, at block 781. In some embodiments, the method 711 may include creating an implicit time base responsive to a memory transfer time associated with the register value, also as described previously, at
25 block 785.

It should be noted that the methods described herein do not have to be executed in the order described, or in any particular order. Moreover, various activities described with respect to the methods identified herein can be executed in iterative, serial, or parallel fashion. Information, including parameters,
30 commands, operands, and other data, can be sent and received in the form of one or more carrier waves.

Upon reading and comprehending the content of this disclosure, one of ordinary skill in the art will understand the manner in which a software program can be launched from a computer-readable medium in a computer-based system to execute the functions defined in the software program. One of ordinary skill
5 in the art will further understand the various programming languages that may be employed to create one or more software programs designed to implement and perform the methods disclosed herein. The programs may be structured in an object-orientated format using an object-oriented language such as Java or C++. Alternatively, the programs can be structured in a procedure-orientated format
10 using a procedural language, such as assembly or C. The software components may communicate using any of a number of mechanisms well known to those skilled in the art, such as application program interfaces or interprocess communication techniques, including remote procedure calls. The teachings of various embodiments are not limited to any particular programming language or
15 environment. Thus, other embodiments may be realized.

For example, an article according to various embodiments of the invention, such as a computer, a memory system, a magnetic or optical disk, some other storage device, and/or any type of electronic device or system may include a processor coupled to a machine-accessible medium such as a memory
20 (e.g., a memory including an electrical, optical, or electromagnetic conductor) having associated information (e.g., computer program instructions and/or data), which, when accessed, results in a machine (e.g., the system 510) performing such actions as integrating an analog input to provide an integrated analog output, adjusting a register value included in a digital register when the
25 integrated analog output is approximately equal to a selected value, and resetting the integrated analog output. The selected value may be a selected overflow or underflow value, as described above, and adjusting the register may include incrementing/decrementing the register value when the integrated analog output is approximately equal to the selected overflow/underflow value.

30 Other actions may include correcting a sum of the integrated analog value and an analog version of the register value using an a-posteriori iterative method, creating an implicit time base responsive to a memory transfer time

associated with the register value, transferring the register value to a memory, and resetting the register value to a selected initial condition value, among others.

5 With respect to purely analog computation, implementing the apparatus, systems, and methods disclosed herein may reduce magnitude scaling problems, converting the user's output from an analog voltage to a floating point digital number via methods of digitization known to those skilled in the art or described above, rendering already-computed results less susceptible to electronic noise. Compared to purely digital computers, the apparatus, systems, and methods
10 disclosed herein may reduce stability problems, give faster results, and reduce stiff system issues

Via digital-analog coordination and programming, errors associated with precision of resistors and capacitors may be reduced. Also, using neural network methods, synthesis of non-linearities may become easier to address.

15 The accompanying drawings that form a part hereof, show by way of illustration, and not of limitation, specific embodiments in which the subject matter may be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments may be utilized and derived therefrom, such that structural
20 and logical substitutions and changes may be made without departing from the scope of this disclosure. This Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of various embodiments is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled.

25 Such embodiments of the inventive subject matter may be referred to herein, individually and/or collectively, by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. Thus, although specific embodiments have been illustrated and
30 described herein, it should be appreciated that any arrangement calculated to achieve the same purpose may be substituted for the specific embodiments shown. This disclosure is intended to cover any and all adaptations or variations

of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the above description.

The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

Claims

What is claimed is:

- 5 1. An apparatus, comprising:
 an analog accumulator; and
 at least one digital register including a register value to be
adjusted when an output of the analog accumulator is approximately
equal to a selected value, wherein the output of the analog accumulator is
10 adjusted when the register value is adjusted.
2. The apparatus of claim 1, wherein the output of the analog
accumulator is adjusted by resetting the output.
- 15 3. The apparatus of claim 1, wherein the register value is
adjusted by incrementing the register value if the selected value is a
positive overflow or threshold value, and wherein the register value is
adjusted by decrementing the register value if the selected value is a
negative overflow or threshold value.
- 20 4. The apparatus of claim 1, wherein the digital register
comprises a mantissa register and an exponent register having an
exponent value to be adjusted when the register value is approximately
equal to a selected mantissa value.
- 25 5. The apparatus of claim 4, wherein the exponent value is
adjusted by incrementing the exponent value if the selected mantissa
value is a selected mantissa overflow value, and wherein the exponent
value is adjusted by decrementing the exponent value if the selected
30 mantissa value is a selected mantissa underflow value.

6. The apparatus of claim 1, wherein the analog accumulator comprises an analog integrator.

5 7. The apparatus of claim 1, wherein the analog accumulator further comprises:

a first analog integrator;
a second analog integrator; and
at least one switch capable of coupling an analog input voltage to
an input of the first analog integrator in a first switch state, and to an
10 input of the second analog integrator in a second switch state.

8. The apparatus of claim 1, wherein the analog accumulator further comprises:

an analog integrator;
15 a first capacitor capable of being electrically coupled to the analog integrator;
a second capacitor capable of being electrically coupled to the analog integrator; and
at least one switch capable of coupling an analog input voltage to
20 the first capacitor in a first switch state, and to the second capacitor in a second switch state.

9. The apparatus of claim 8, further comprising:
a scaling circuit capable of coupling an analog input voltage to an
25 input of the analog accumulator.

10. The apparatus of claim 1, further comprising:
a scaling circuit capable of coupling an analog input voltage to an
input of the analog accumulator.

30

11. The apparatus of claim 1, wherein the register value is adjusted to an initial value by an external agent.

12. The apparatus of claim 11, wherein the external agent comprises a computer.

5 13. The apparatus of claim 1, wherein an initial analog value is provided to an input of the analog accumulator by an external agent.

14. The apparatus of claim 13, wherein the external agent comprises a computer.

10 15. A system, comprising:
 an analog accumulator;
 a digital register including a register value to be adjusted when an
 output of the analog accumulator is approximately equal to a selected
15 value, wherein the output of the analog accumulator is reset or adjusted
 when the register value is adjusted;
 a converter having a digital input capable of receiving the register
 value, the converter having an analog output responsive to the register
 value; and
20 a summing mechanism having a summed analog output
 approximately equal to the analog output plus the output of the analog
 accumulator.

25 16. The system of claim 15, wherein the summed analog output is scaled.

30 17. The system of claim 15, wherein the digital register comprises a mantissa register and an exponent register having an exponent value to be adjusted when the register value is approximately equal to a selected mantissa value.

18. The system of claim 15, further comprising:

a scaling circuit capable of coupling an analog input voltage to an input of the analog accumulator, wherein the scaling circuit is capable of being communicatively coupled to the exponent register and at least one other exponent register.

5

19. The system of claim 15, wherein the analog accumulator is associated with an adjustable time constant.

10

20. The system of claim 15, wherein the register value is adjusted to an initial value by an external agent.

21. The system of claim 20, wherein the external agent comprises a computer.

15

22. The system of claim 15, wherein an initial analog value is provided to an input of the analog accumulator by an external agent.

23. The system of claim 22, wherein the external agent comprises a computer.

20

24. A method, comprising:
integrating an analog input to provide an integrated analog output;
adjusting a register value included in a digital register when the integrated analog output is approximately equal to a selected value; and
resetting the integrated analog output.

25

25. The method of claim 24, wherein the selected value is a selected overflow value, and wherein adjusting the register value further comprises:

30

incrementing the register value when the integrated analog output is approximately equal to the selected overflow value.

26. The method of claim 24, wherein the selected value is a selected underflow value, and wherein adjusting the register value further comprises:

5 decrementing the register value when the integrated analog output is approximately equal to the selected underflow value.

27. The method of claim 24, further comprising:
incrementing another register value included in another digital register when the register value is approximately equal to a selected
10 overflow value; and
resetting the register value.

28. The method of claim 24, further comprising:
decrementing another register value included in another digital
15 register when the register value is approximately equal to a selected underflow value; and
resetting the register value.

29. The method of claim 24, further comprising:
20 setting the register value to an initial condition value.

30. The method of claim 29, wherein setting the register value to the initial condition value further comprises:
setting a mantissa register value to a first initial condition value;
25 and
setting an exponent register value to a second initial condition value.

31. The method of claim 30, wherein the first and the second
30 initial condition values are provided by an external agent.

32. The method of claim 31, wherein the external agent comprises a computer.

5 33. The method of claim 24, further comprising:
 setting an adjustable time constant associated with integrating the analog input.

10 34. The method of claim 24, further comprising:
 transferring the register value to a memory; and
 resetting the register value to a selected initial condition value.

35. The method of claim 24, further comprising:
scaling the analog input.

15 36. The method of claim 35, wherein scaling the analog input further comprises:
 scaling the analog input responsive to an exponent value adjusted when the register value is approximately equal to a selected mantissa value.

20 37. The method of claim 36, further comprising:
 scaling the analog input responsive to another exponent value included in another register.

25 38. The method of claim 24, further comprising:
 converting the register value to a mantissa analog output; and
 adding the mantissa analog output to the integrated analog output to provide a summed analog output.

30 39. The method of claim 38, further comprising:
 scaling the integrated analog output to the summed analog output.

40. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

5 integrating an analog input to provide an integrated analog output;
adjusting a register value included in a digital register when the integrated analog output is approximately equal to a selected value; and
resetting the integrated analog output.

41. The article of claim 40, wherein the selected value is a selected overflow value, and wherein adjusting the register value further comprises:

incrementing the register value when the integrated analog output is approximately equal to the selected overflow value.

42. The article of claim 40, wherein the selected value is a selected underflow value, and wherein adjusting the register value further comprises:

15 decrementing the register value when the integrated analog output is approximately equal to the selected underflow value.

43. The article of claim 40, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

20 correcting a sum of the integrated analog value and an analog version of the register value using an a-posteriori iterative method.

44. The article of claim 40, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

30 creating an implicit time base responsive to a memory transfer time associated with the register value.

45. The article of claim 40, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

5 transferring the register value to a memory; and
 resetting the register value to a selected initial condition value.

46. The article of claim 45, wherein the selected initial condition value is provided by an external agent.

10 47. The article of claim 46, wherein the external agent comprises a computer.

 48. An apparatus, substantially as described and shown in Figure 1A.

15 49. An apparatus, substantially as described and shown in Figure 1B.

 50. An apparatus, substantially as described and shown in Figure 2.

20

 51. An apparatus, substantially as described and shown in Figure 3.

25 52. An apparatus, substantially as described and shown in Figure 4.

 53. An apparatus, substantially as described and shown in Figure 5.

30

 54. An apparatus, comprising:
 a plurality of analog accumulators; and

a corresponding plurality of digital registers, wherein each one of the corresponding plurality of digital registers includes a register value to be adjusted when an output of one of the plurality of analog accumulators to which one of the plurality of digital registers corresponds is
5 approximately equal to a selected value, and wherein the register value included in the one of the plurality of digital registers is capable of being adjusted responsive to a change in a condition of another one of the plurality of digital registers.

10 55. The apparatus of claim 54, wherein the analog accumulator is adjusted by resetting the output.

56. The apparatus of claim 54, wherein the register value included in the one of the plurality of digital registers is adjusted by
15 incrementing the register value included in the one of the plurality of digital registers if the selected overflow value is a positive overflow value, and wherein the register value included in the one of the plurality of digital registers is adjusted by decrementing the register value included in the one of the plurality of digital registers if the selected
20 overflow value is a negative overflow value.

57. A system, comprising:
a plurality of analog accumulators;
a corresponding plurality of digital registers, wherein each one of
25 the corresponding plurality of digital registers includes a register value to be adjusted when an output of one of the plurality of analog accumulators to which the one of the plurality of digital registers corresponds is approximately equal to a selected value, and wherein the register value included in the one of the plurality of digital registers is capable of being
30 adjusted responsive to a change in a condition of another one of the plurality of digital registers;

a converter having a digital input capable of receiving the register value included in the one of the plurality of digital registers, the converter having an analog output responsive to the register value included in the one of the plurality of digital registers; and

5 a summing mechanism having a summed analog output approximately equal to the analog output plus the output of the one of the plurality of analog accumulators.

58. The system of claim 57, wherein the one of the plurality
10 of digital registers comprises a mantissa register and an exponent register having an exponent value to be adjusted when the register value included in the one of the plurality of digital registers is approximately equal to a selected mantissa value.

59. The system of claim 57, further comprising:
15 a scaling circuit capable of coupling an analog input voltage to an input of the one of the plurality of analog accumulators, wherein the scaling circuit is capable of being communicatively coupled to the exponent register and at least one other exponent register included in the
20 plurality of digital registers.

60. The system of claim 57, wherein the one of the plurality of analog accumulators is associated with an adjustable time constant.

61. The system of claim 57, wherein the register value
25 included in the one of the plurality of digital registers is adjusted to an initial value by an external agent.

62. The system of claim 61, wherein the external agent
30 comprises a computer.

63. The system of claim 57, wherein an initial analog value is provided to an input of the one of the plurality of analog accumulators by an external agent.

5 64. The system of claim 63, wherein the external agent comprises a computer.

65. The system of claim 57, wherein the output of the one of the plurality of analog accumulators is scaled.

FIG. 1A

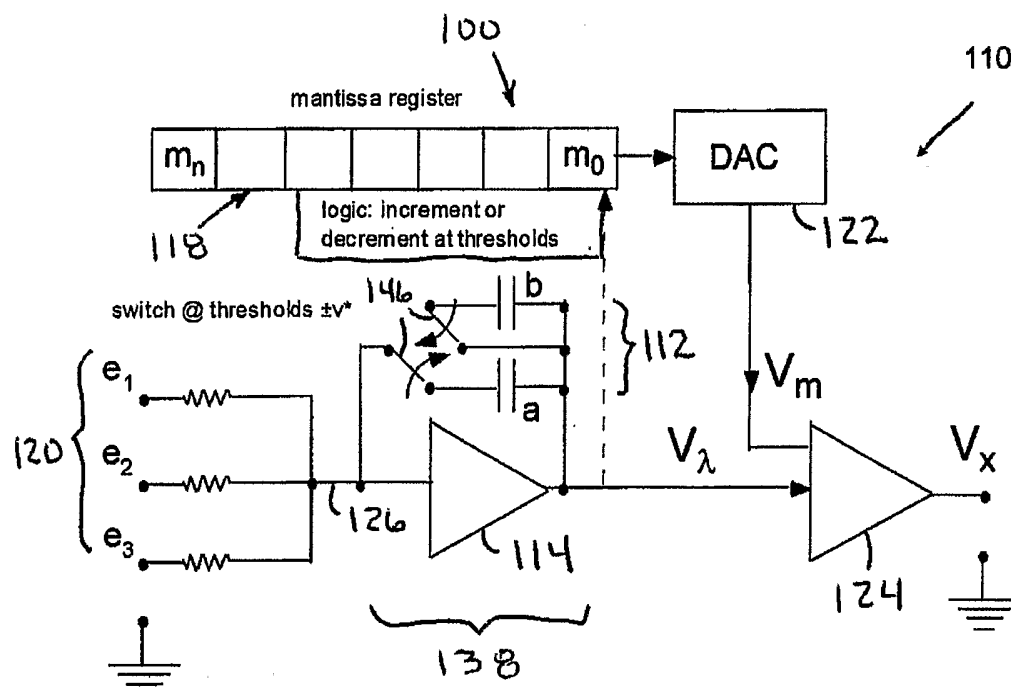


FIG. 1B

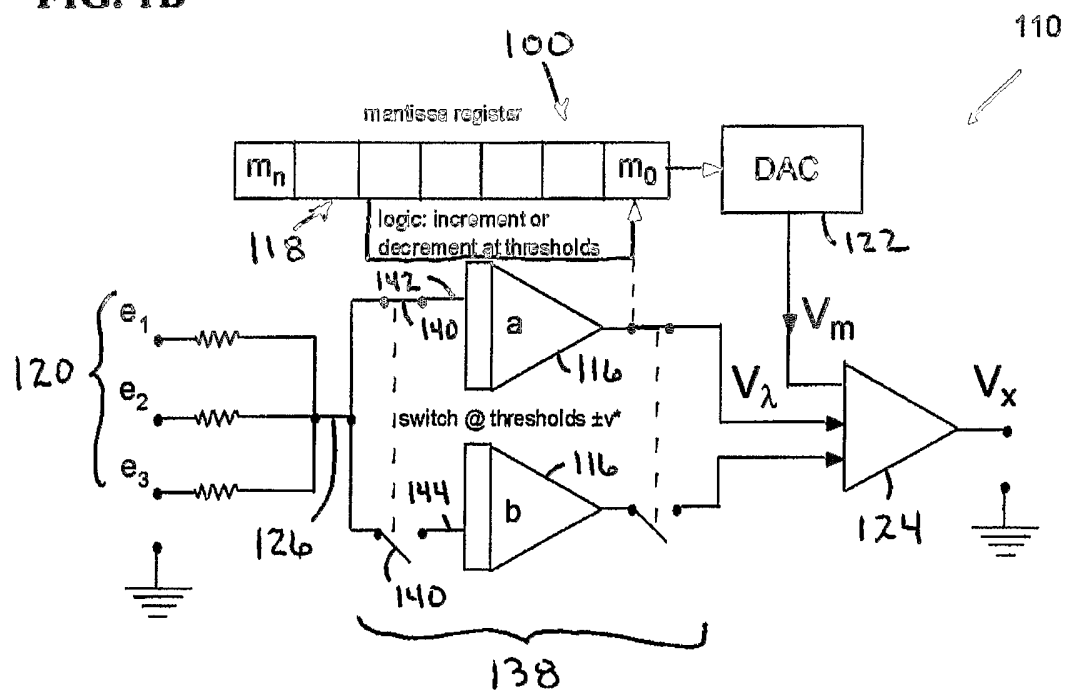


FIG. 2

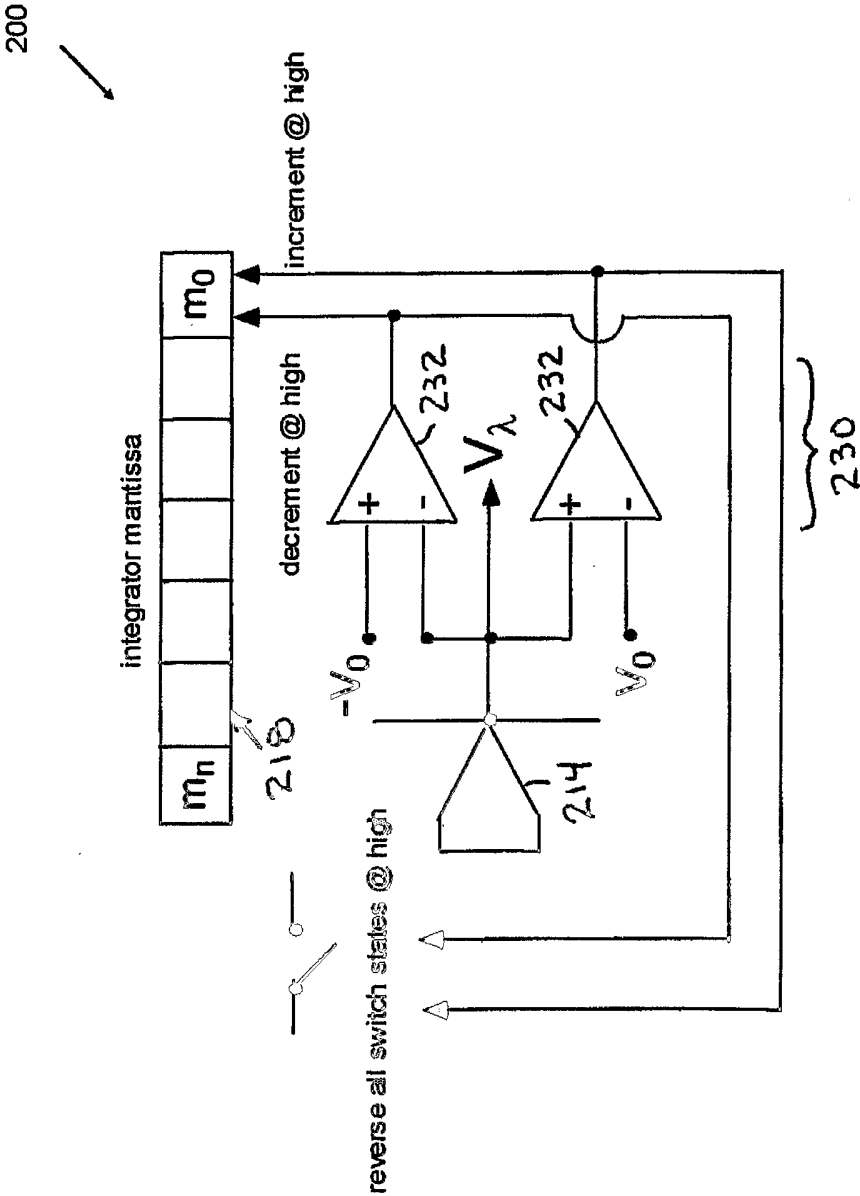


FIG. 3

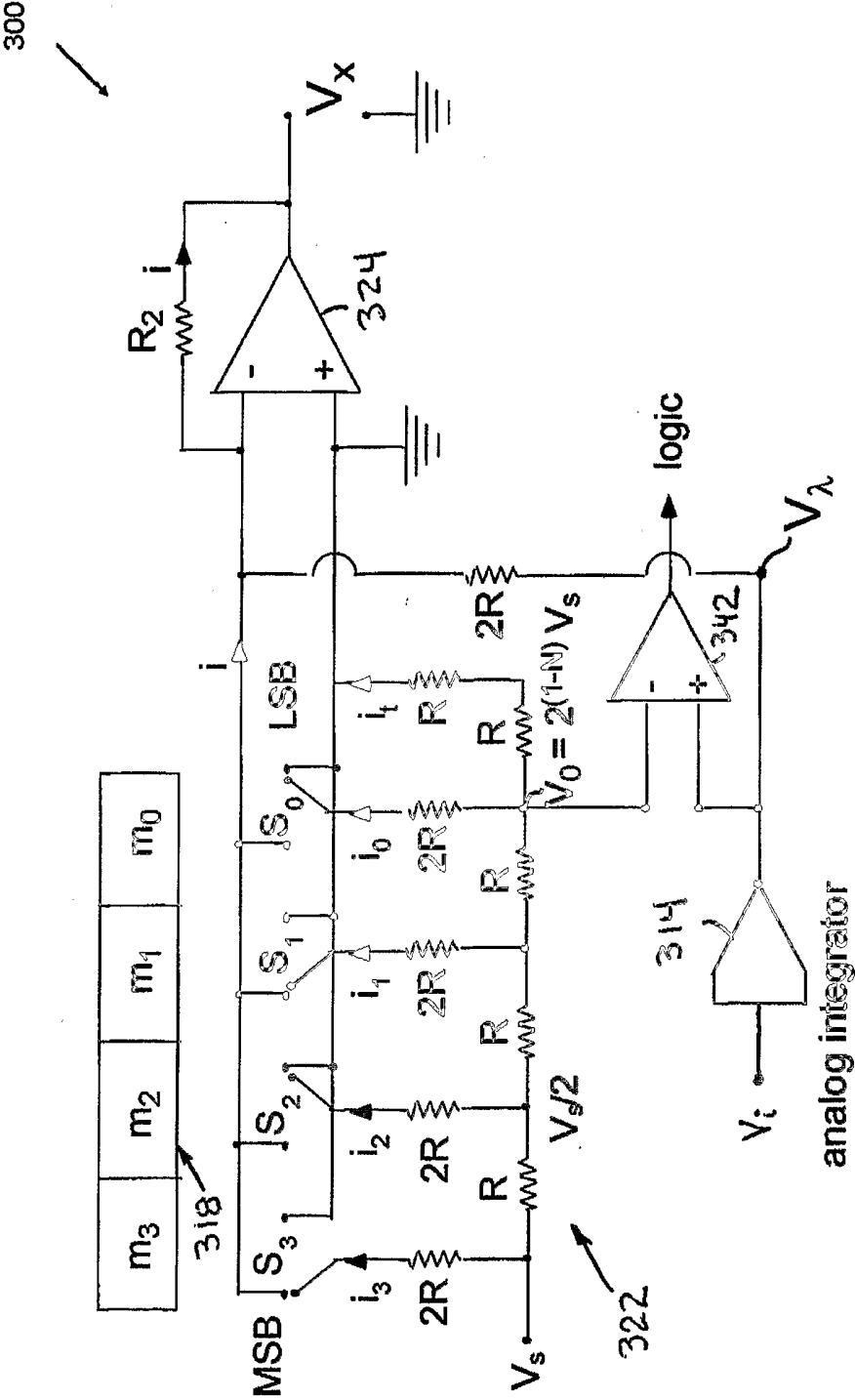


FIG. 4

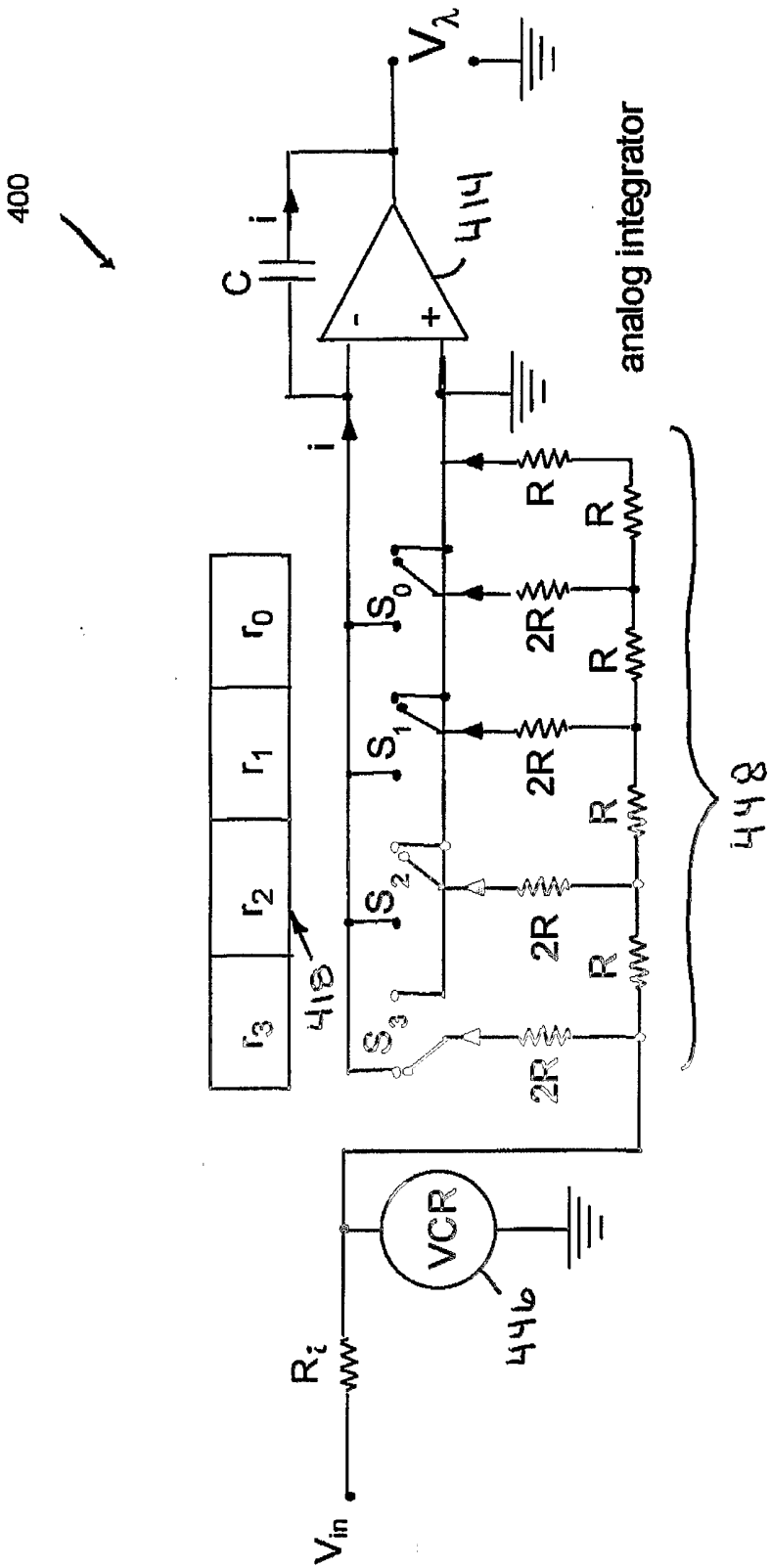


FIG. 5

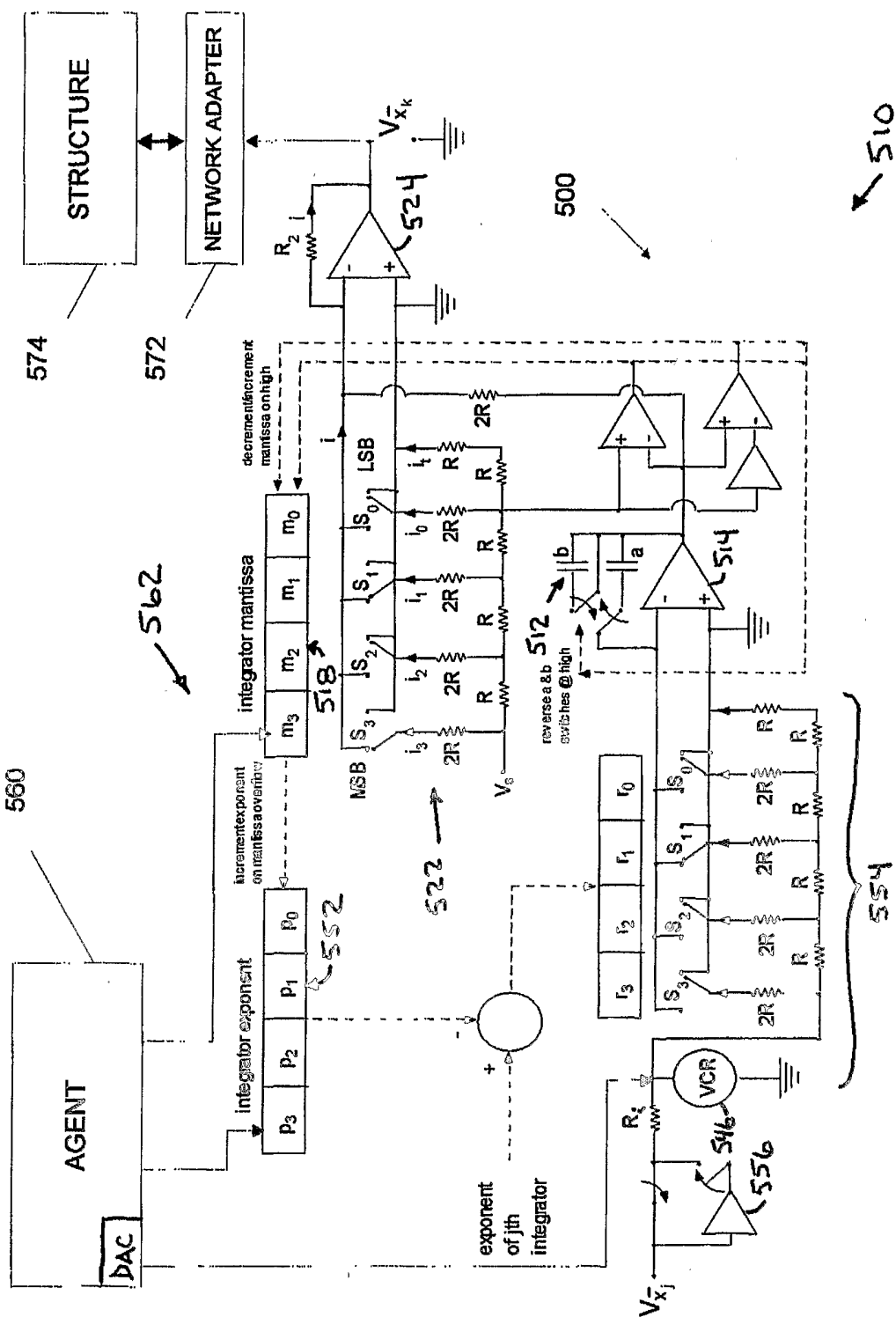


FIG. 6

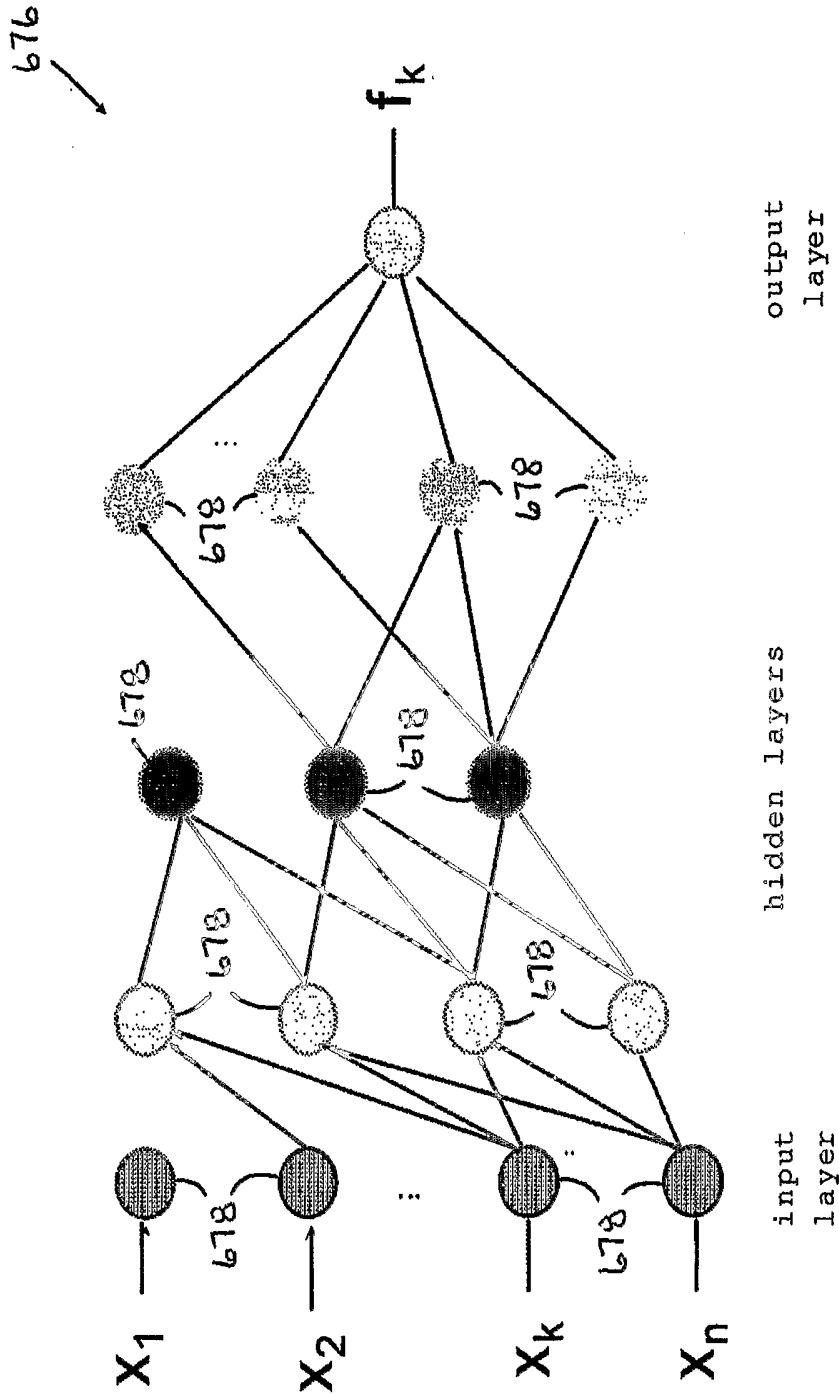
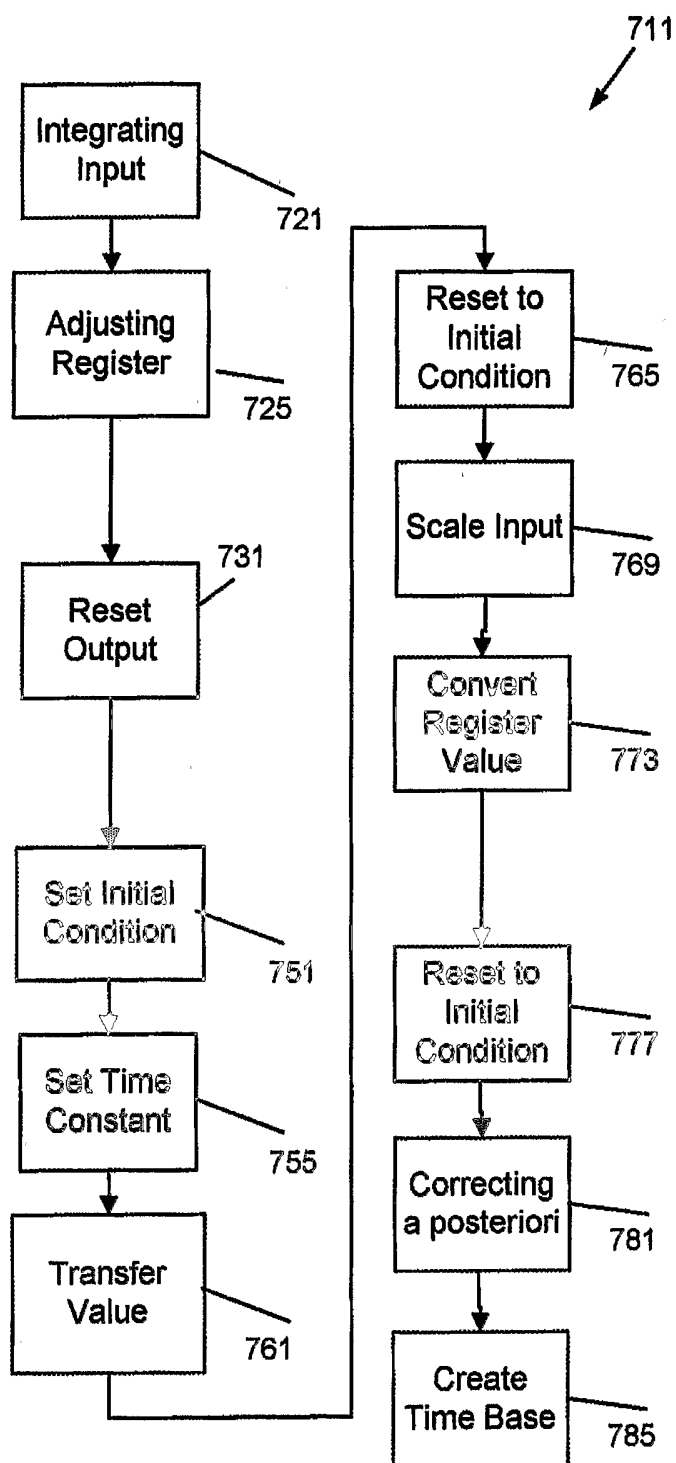


FIG. 7



INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/019476

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06J1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, IBM-TDB, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 240 070 A (RIETSCH EIKE ET AL) 16 December 1980 (1980-12-16)	1,3-6, 11-26, 29-33, 35, 40-42, 54-56
Y		2,34,45
Y	US 4 792 914 A (DARTOIS LUC ET AL) 20 December 1988 (1988-12-20) column 5, line 43 - column 5, line 48 ----- -/--	2

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- * & * document member of the same patent family

Date of the actual completion of the international search

9 November 2004

Date of mailing of the international search report

29/11/2004

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Filip, L

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/019476

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	ANONYMOUS: "Design for Adaptive Decoders Using ROM. January 1978." IBM TECHNICAL DISCLOSURE BULLETIN, vol. 20, no. 8, 1 January 1978 (1978-01-01), pages 3157-3158, XP002302335 New York, US the whole document -----	34,45

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2004/019476

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☒ Claims Nos.: 48-53
because they relate to subject matter not required to be searched by this Authority, namely:
The subject-matter of claims 48-53 relates to figures without mentioning the technical features of the invention and therefore these claims are not allowable according to Article 6 and Rules 6.2.a, 6.3.a PCT.
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US2004/019476

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