

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
30 April 2009 (30.04.2009)

PCT

(10) International Publication Number
WO 2009/055346 A1

(51) International Patent Classification:
G06F 13/24 (2006.01)

(21) International Application Number:
PCT/US2008/080537

(22) International Filing Date: 20 October 2008 (20.10.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/981,772 22 October 2007 (22.10.2007) US
11/928,110 30 October 2007 (30.10.2007) US

(71) Applicant (for all designated States except US): **SAN-DISK CORPORATION** [US/US]; 601 McCarthy Boulevard, Milpitas, California 95035-7932 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **PERRY, Nir** [IL/IL]; 25 Keren Kayemet Street, 58486 Holon (IL). **DRUCK, Asher** [IL/IL]; Balfor, 38, 22425 Nahariya (IL).

(74) Agents: **FERRAZANO, Michael J.** et al.; BEYER LAW GROUP LLP, P. O. Box 1687, Cupertino, California 95015-1687 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

— with international search report
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(54) Title: SIGNALING AN INTERRUPT REQUEST THROUGH DAISY CHAINED DEVICES

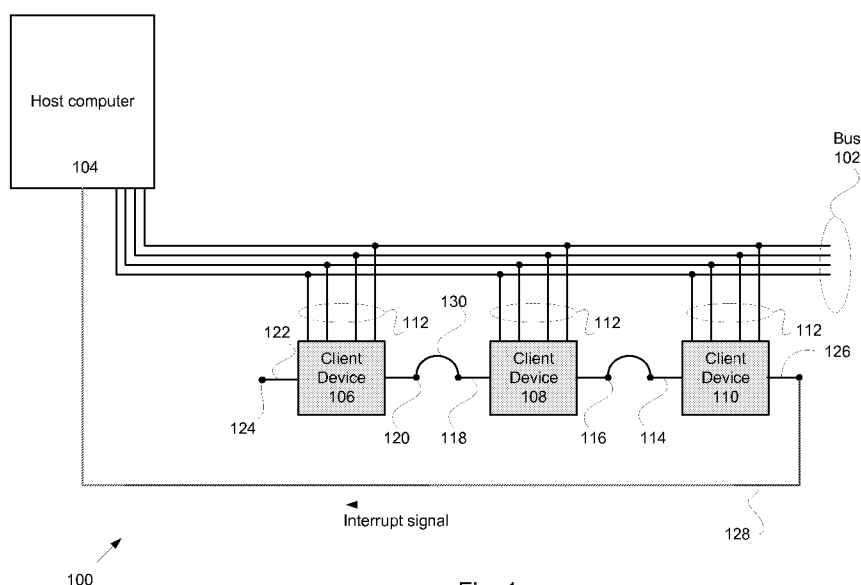


Fig. 1

(57) Abstract: A system and a method for asynchronously signaling interrupts from a plurality of devices in a computing system, while optimizing the latencies in handling the interrupts. In a particular embodiment, an interrupt is signaled via a plurality of daisy chained devices by handing over the interrupt request from one device to another while retaining information regarding any interrupts handed over (also referred to as passed). In this way, the interrupt source can be readily identified (using a binary search, for example) thereby reducing interrupt latency and memory resources required to retain interrupt history.

WO 2009/055346 A1

SIGNALING AN INTERRUPT REQUEST THROUGH DAISY CHAINED DEVICES

FIELD OF THE INVENTION

[0001] The present invention relates generally to digital devices. More
5 particularly, the present invention relates to signaling interrupts.

BACKGROUND

[0002] It has become commonplace to connect a host computer to a flexible
number of various functional devices (such as storage devices, communications
devices, sensing devices, and the like that can be either removable or fixed in nature)
10 using a plurality of conducting wires referred to as a “bus” that typically complies
with well known standards. In most situations, the number of conducting wires
included in the bus is not the same as the number of devices connected and therefore
the number of conducting wires that constitute the bus are shared amongst any and all
of the devices connected to the bus. Since all the devices share the same conducting
15 wires within the bus and in order for the host computer to communicate with each of
the devices, each device is both assigned a unique address and subsequently
programmed to respond only to messages that are addressed to that unique address.
In this way, multiple devices can share the same conducting wires that form the bus
resulting in a substantially reduced bus size than would be otherwise be required.

20 [0003] Many I/O devices have an interrupt request line to signal the host they
need attention. This is often used to notify the host new data is available or that a
previous calculation has completed. Occasionally, each device has a separate
interrupt request line to the host, so that the host can differentiate between the various
sources. In this case, the host is required to have multiple interrupt request lines,
25 which means higher cost of hardware. Occasionally, several devices share an
interrupt request line to the host such that when an interrupt is signaled the host must
query each device if it is the interrupt source. In this scenario, the host is required to
do a search on every interrupt event which is inefficient and time consuming and
increasing the latency of servicing an interrupt by the host computer resulting in more
30 resources from the host to remember interrupt history for a longer period of time.

[0004] Therefore, it is desired to support interrupt signals from many devices
without adding cost relatively to the number of devices as well as minimizing the
latency associated with servicing the interrupts.

SUMMARY OF THE DESCRIBED EMBODIMENTS

[0005] According to different embodiments of the present invention, various methods, devices and systems are described for efficiently servicing interrupt requests
5 in a system having a number of client devices sharing a bus. One embodiment describes a bus architecture that includes at least one signal line and a plurality of client devices. Each of the plurality of client devices includes a number of I/O pins selected ones of which are connected to the at least one signal line, and a first and a second interrupt pin wherein all but a first and a last of the plurality of client devices
10 are connected to one another in a daisy chain arrangement by way of the first and the second interrupt pin separate from the at least one signal line. The first client device is connected to the daisy chain arrangement only by way of the second interrupt pin and the first interrupt pin of the first device is connected to a node external to the daisy chain. The last client device is connected to the daisy chain only by way of a
15 first interrupt pin and a second interrupt pin of the last of the plurality of client devices is connected to an external circuit by way of an interrupt signal line separate from the at least one signal line. In one aspect of the invention, the external circuit is a host computer.

[0006] A method of signaling an interrupt request through a plurality of daisy-
20 chained client devices connected by way of a first and a second interrupt pin and I/O pins selected ones of which are connected to at least one signal line wherein a last one of the client devices communicates with a host computer independently of the at least one signal line. The method is carried out by requesting an interrupt by at least one of the daisy chained client devices, passing the interrupt request downstream from the
25 requesting client device through the daisy chain to the last client device bypassing the at least one signal line, communicating the interrupt request to the host computer by the last client device, identifying the requesting client device by the host computer, and servicing the requesting client device by the host computer.

[0007] A system includes a host device, at least one signal line connected to
30 the host device, and a plurality of client devices. Each of the client devices includes a number of I/O pins selected ones of which are connected to the at least one signal line, and a first and a second interrupt pin. All but a first and a last of the plurality of client devices are connected to one another in a daisy chain arrangement by way of

the first and the second interrupt pin separate from the at least one signal line. The first client device is connected to the daisy chain arrangement only by way of the second interrupt pin and the first interrupt pin of the first device is connected to a node external to the daisy chain. The last client device is connected to the daisy chain only by way of a first interrupt pin and a second interrupt pin of the last of the plurality of client devices is connected to the host computer by way of an interrupt signal line separate from the at least one signal line.

[0008] A bus architecture that includes a plurality of independent signal lines, and a plurality of client devices having a number of I/O pins and a first and a second interrupt pin. All but a first and a last of the plurality of client devices are connected to one another in a daisy chain arrangement by way of the first and the second interrupt pin separate from the plurality of signal lines. The first client device is connected to the daisy chain arrangement only by way of the second interrupt pin and the first interrupt pin of the first device is connected to a node external to the daisy chain. The last client device is connected to the daisy chain only by way of a first interrupt pin and a second interrupt pin of the last of the plurality of client devices is connected to an external circuit by way of an interrupt signal line separate from the plurality of independent signal lines.

DETAILED DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 shows a simplified wiring diagram of a system according to the present invention.

[0010] Figures 2A – 2D showing a simplified example of signaling of an interrupt throughout the system shown in Figure 1.

[0011] Figure 3 shows a simplified state machine 300 representative of client device of system shown in Figure 1.

[0012] Figure 4 shows a simplified wiring diagram of a system according to another embodiment of the present invention.

[0013] Figure 5 illustrates a system in accordance with another embodiment of the invention where not all of the client devices share the same bus.

DETAILED DESCRIPTION OF THE DESCRIBED EMBODIMENTS

[0014] Reference will now be made in detail to a particular embodiment of the invention an example of which is illustrated in the accompanying drawings. While the invention will be described in conjunction with the particular embodiment, it will

be understood that it is not intended to limit the invention to the described embodiment. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

5 **[0015]** The present invention teaches a system and a method for asynchronously signaling interrupts from a plurality of devices in a computing system, while optimizing the latencies in handling the interrupts. In a particular embodiment, an interrupt is signaled via a plurality of daisy chained devices by handing over the interrupt request from one device to another while retaining
10 information regarding any interrupts handed over (also referred to as passed). In this way, the interrupt source can be readily identified using any number of searching schemes (a binary search, for example) thereby reducing interrupt latency and memory resources required to retain interrupt history.

[0016] Embodiments of the invention are discussed below with reference to
15 Figures. 1 – 5. However, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments. It should be noted that even though in the context of this discussion, the first and second pins are referred to as first and second interrupt pins operable to pass interrupt information, the
20 first and second pins can in some embodiments operate as first and second interrupt pin used to facilitate passing of initialization information in those situations where the associated client device must undergo initialization.

[0017] Figure 1 shows a simplified wiring diagram of a system 100 according to the present invention. The system 100 includes a number of signal lines 102
25 (referred to as bus 102) used to connect a host computer 104 to a plurality of client devices 106, 108, and 110. It should be noted that even though only three client devices (106, 108 and 110) are shown, it can be appreciated that there can be any number of client devices in system 100. Each of the client devices includes a number of I/O pins 112 selected ones of which are used to electrically connect an associated
30 one of the client devices to bus 102. In addition to I/O pins 112, each client device includes at least two interrupt pins that can be used to pass interrupt information from one client device to another as well as signify an interrupt status of an associated client device. In the described embodiment, first and second interrupt pins can be

used to connect client devices 106, 108 and 110 in a daisy chain arrangement separate from bus 102. By daisy chain arrangement, it is meant that a first (input) pin of one client device is electrically connected to a second (output) pin of a neighboring client device. The connection can be either by hard soldering, by a printed circuit layout or by connection of socket pins. For example, first interrupt pin 114 of client device 110 can be connected to second interrupt pin 116 of client device 108 and first interrupt pin 118 of client device 108 can be connected to second interrupt pin 120 of client device 106. Unlike the other client devices, however, first interrupt pin 122 of client device 106 can be connected to an external node 124 and interrupt pin 126 (referred to a host monitor pin 126) of client device 110 can be connected to host computer 104 via wire 128 that can be separate from bus 102. It is by monitoring activity on interrupt pin 126 by way of wire 128, that host computer 104 can sense a change in interrupt status by at least one of the client devices 106, 108, or 110.

[0018] It should also be noted that each client device is capable of setting an associated pending interrupt flag and a passed interrupt flag. In the described embodiment, the fact that a client device is an interrupt source can be recorded by setting associated pending interrupt flag (from NOT_SET to SET, for example). On the other hand, if a client device has received notification (by way of first interrupt pin in communication with second interrupt pin of a neighboring device) that at least one “upstream” client device is an interrupt source, then this fact can be recorded by the receiving client device by setting its passed interrupt flag (from NOT_SET to SET, for example). By upstream it is meant those client devices between a particular client device and the first client device which in this case is client device 106. It should be noted that once the host computer 104 has identified and acknowledged a pending interrupt, the pending interrupt flag of the interrupt source will change from SET to NOT_SET which will, in turn, be communicated “down” the daisy chain by way of the first and second interrupt pins of the those client devices upstream (i.e., those client devices between the last client device (i.e., client device 110 in this case) and the interrupt source).

[0019] Reference is now made to Figures 2A – 2D showing a simplified example of signaling of an interrupt throughout the system 100. All client devices having been initialized and start in their respective initial states where no interrupt is pending by any of the client devices and all have their respective interrupt pins (both

first and second) set to logic level A. In this example, client device 106 signals an interrupt by changing the logic level on second interrupt pin from logic level A to logic level B and setting its pending interrupt flag to SET from NOT_SET. Since interrupt pin of client device 106 is electrically connected to the first interrupt pin 118 of client device 108, first interrupt pin 118 also changes from logic level A to logic level B. Client device 108 senses this change and in response, changes second interrupt pin 116 to logic level B from logic level A thereby passing interrupt information forward, or downstream, through the daisy chain to client device 110 since first interrupt pin 114 of client device 110 is connected to second interrupt pin 116 of client device 108. In response to the sensed change at first interrupt pin 114, client device 110 changes second interrupt pin 126 from logic level A to logic level B. In this way, information regarding the interrupt at client device 106 is passed down the daisy chain. Since second interrupt pin 126 of client device 110 is connected by way of wire 128 to host computer 104, the change in status of interrupt pin 126 is monitored by host computer 104 that, in turn, concludes that an interrupt event has occurred at least one of the client devices 106 – 110. At this point host computer 104 starts to search for and identify the interrupt source using, for example, a binary search.

[0020] In order to identify the interrupt source, host asks 104 queries client device 108 for its device status to which client device 108 responds by reporting that interrupt pin 118 is logic level B and that its pending interrupt flag is NOT_SET (indicating that it has no pending interrupts). Interrupt pin 116 will be set to logic level B if either client device 108 has a pending interrupt or an interrupt flag has been passed from a previous client device(s). In this way, host computer 104 can deduce that client device 108 is not the interrupt source (its pending interrupt flag is NOT_SET) and that the interrupt event signal was passed from at least client device 106. Since client device 106 is the known first device in the daisy chain, host computer 104 can conclude that the interrupt event signal originated at client device 106 and the search is over (as evidence by the interrupt pending flag being SET for client device 106). However, if as shown in Fig. 2B, client device 108 had reported that both the pending and passing interrupt flags are NOT_SET, indicating that no interrupt has been initiated and no interrupt has passed through it (both interrupt pins are set at logic level A and pending and passing interrupt flags are NOT_SET), then

host computer 104 could deduce that client device 110 has a pending interrupt and is therefore the interrupt source. Furthermore, had, as shown in Fig. 2C, client device 108 reported that it has a pending interrupt and no interrupt has passed through it, then host computer 104 could deduce that client device 108 has a pending interrupt and is therefore the interrupt source. It should be noted that had a device reported both it has a pending interrupt and it has its first interrupt pin set to logic level B, then host computer 104 could deduce that the client device is an interrupt source, but not the only interrupt source indicating that host computer 104 would have to continue the search in order to identify the other interrupt sources.

10 **[0021]** As shown in Figure 2D, after host computer 104 handles the interrupt called by client device 106, host computer 104 acknowledges client device 106 that its interrupt was serviced and in response, client device 106 passes this information downstream by changing the state of second interrupt pin 120 from logic level B to logic level A. This change in state is sensed by client device 108 and responds by
15 changing the status of second interrupt pin to logic level A as well (since it has no pending interrupts of its own). Further downstream, client device 110 senses the change in first interrupt pin 114 and responds by changing the status of interrupt pin 126 to logic level A. Host computer 104 senses the change at interrupt pin 126 by way of wire 128 and deduces that there are no current pending interrupts in system
20 100.

[0022] Figure 3 shows a simplified state machine 300 representative of client device 108 of system 100 of the present invention. Following initialization of client devices 106 – 110, client device 108 enters initial state 302 where both pending and passing interrupt flags are NOT_SET (i.e., there is no indication of a pending interrupt
25 by client device 108 and client device 108 has no recording of any interrupt event that has passed from any downstream client devices (in this case client device 106). In this state, both its first and second interrupt pins are at logic level A. If client device 108 signals an interrupt 350, it changes second interrupt pin from logic level A to logic level B enters state 308 where the interrupt pending flag is SET. If following state
30 308, first interrupt pin changes to logic level B at 354, client device 108 keeps second interrupt pin at logic level B and enters state 310 where both the interrupt pending and passing flags are SET. If, however, while in state 310 first interrupt pin changes back to logic level A at 356, client device 108 returns to state 308 but keeps second

interrupt pin at logic level B. If while in state 308 host computer 104 acknowledges
352 the pending interrupt, client device 108 returns to state 302 and changes second
interrupt pin to logic level A. If while in state 310 host computer 104 acknowledges
358 the interrupt then client device 108 enters state 304 and maintains the second
5 interrupt pin at logic level B.

[0023] While still in the initial state 302, if client device 108 senses that first
interrupt pin has changed from logic level A to logic level B at 322, then client device
108 responds by changing second interrupt pin to logic level B and enters state 304
where the passing event indicator is set. From this state, if client device 108 senses
10 that first interrupt pin changes back to logic level A at 324, it too changes back its
second interrupt pin to logic level A and moves back to state 302. If from state 304,
however, client device 108 needs to signal an interrupt 326, it keeps its second
interrupt pin at logic level B and enters state 306 where both pending and passing
interrupt flags are set. If while in state 306 host computer 104 acknowledges the
15 interrupt at 328, then device 108 enters state 304 and keeps second interrupt pin at
logic level B. If while in state 306 the first interrupt pin changes back to logic level A
at 330, client device 108 device enters state 308 but keeps the second interrupt pin at
logic level B.

[0024] Figure 4 shows a system 400 in accordance with another embodiment
20 of the invention whereby a mix of non-interrupting devices 402 - 404 (such as an SD
memory device) that do not generate interrupts and interrupting devices 406 - 408
(such as SDIO devices) that can generate interrupts. Since non-interrupting devices
402 - 404 do not generate interrupts and therefore should not be included in any
search for an interrupt source, daisy chaining these devices in groups or sub-groups in
25 known locations, these devices and be skipped in any search thereby improving
search time and efficiency. For example, in the case shown in Figure 4, non-
interrupting devices 402 - 404 are daisy chained upstream from interrupting devices
406 - 408. Therefore, when host computer 410 begins a search of an interrupt source,
the search can be limited to only that portion of the daisy chained client devices that
30 can generate an interrupt, namely client devices 406 - 410. It should be noted that as
long as the identity and location of the non-interrupting client devices are known to
host computer 410, then these devices can be placed anywhere and in any

combination deemed most appropriate for the application for which they are designed to be used.

[0025] Although the invention has been described using embodiments based upon a daisy chain type bus architecture, the invention is well suited for other type bus architectures. Such bus architectures include those configured to pass an interrupt from one device to another (regardless of the manner in which the interrupt is passed) and remember that an interrupt has passed through them (in order to facilitate a subsequent interrupt search, using for example, a binary search).

[0026] Figure 5 illustrates a system 500 in accordance with another embodiment of the invention where not all of the client devices share the same bus. In particular, although each client device 502 – 508 are connected together in a daisy chain arrangement as described in Figs. 1 and 4, in the system 500 each client devices 502 – 508 each communicate with host computer 510 via their own at least one signal line, or bus and do not therefore share a bus. For example, client device 502 is connected to bus 514, client device 504 is connected to bus 516, client device 506 is connected to bus 518, and client device 508 is connected to bus 520. In any case, an interrupt event is detected by host computer 510 by way of line 522 connected at host monitor node 524 separate from any of buses.

[0027] It should be noted that it is contemplated that the invention can be used for any type client device or any mix of types of client devices. For example, the client devices can include data storage devices, communications devices, sensing devices, and the like that can be either removable or fixed in nature. Such devices can include SDIO (Input/Output) cards used as an interface that extends the functionality of devices with SD card slots such as Bluetooth®, GPS, and WiFi (802.11b,g), etc. Data storage devices can include non-volatile memory such as Multi Media Card (MMC) and Secure Digital Card (SD). These devices can also be grouped according to whether or not they generate interrupts (SDIO devices, for example) or do not generate interrupts (SD memory devices, for example). In this way, searching for any interrupt sources can be made for efficient in both time and computing resources.

[0028] The invention can further pertain to an electronic system that includes a memory system as discussed above. Memory systems (i.e., memory cards) are commonly used to store digital data for use with various electronics products. The memory system is often removable from the electronic system so the stored digital

data is portable. The memory systems according to the invention can have a relatively small form factor and be used to store digital data for electronics products that acquire data, such as cameras, hand-held or notebook computers, network cards, network appliances, set-top boxes, hand-held or other small media (e.g., audio)

5 players/recorders (e.g., MP3 devices), and medical monitors.

[0029] The advantages of the invention are numerous. Different embodiments or implementations may yield one or more of the following advantages. One advantage of the invention is legacy devices (i.e., those devices that do not by their nature generate interrupts) can be added or removed without consideration of
10 modifying system hardware. Another advantage of the invention is that it can be used with any host computer without any modification (for those host computers already possessing at least one general purpose I/O line (GPIO)) or only slight modification for those without at least one GPIO or interrupt therefore reducing the cost and increasing the applicability of the invention.

15 **[0030]** The many features and advantages of the invention are apparent from the written description and, thus, it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation as illustrated and described. Hence,
20 all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

WHAT IS CLAIMED IS:

1. A bus architecture, comprising:
at least one signal line; and
a plurality of client devices wherein each of the client devices includes,
5 a number of I/O pins selected ones of which are connected to the at least one signal line, and
a first and a second interrupt pin wherein all but a first and a last of the plurality of client devices are connected to one another in a daisy chain arrangement by way of the first and the second interrupt pin separate from the
10 at least one signal line, wherein the first client device is connected to the daisy chain arrangement only by way of the second interrupt pin and wherein the first interrupt pin of the first device is connected to a node external to the daisy chain and wherein the last client device is connected to the daisy chain only by way of a first interrupt pin and wherein a second interrupt pin of the last of the
15 plurality of client devices is connected to an external circuit by way of an interrupt signal line separate from the at least one signal line.
2. A bus architecture as recited in claim 1, further comprising:
at least one legacy device configured to not generate an interrupt signal under
any circumstances having I/O pins selected ones of which are connected to the at least
20 one signal line and no interrupt pins.
3. A bus architecture as recited in claim 1, wherein the external circuit is a host computer, wherein the host computer is also connected to the at least one signal line.
4. A bus architecture as recited in claim 2 wherein when at least one of the client devices requests an interrupt, then the requesting client device sends an interrupt
25 request up the daisy chain of client devices.
5. A bus architecture as recited in claim 4, wherein the interrupt request is received by the host computer by way of the interrupt signal line.
6. A bus architecture as recited in claim 5, wherein when the host computer receives the interrupt request, then the host computer identifies the requesting client
30 device.
7. A bus architecture as recited in claim 6, wherein the host computer identifies the requesting client device by,

performing a search of all client devices connected to the at least one signal line.

8. A bus architecture as recited in claim 7, wherein the search is a binary search.

9. A bus architecture as recited in claim 8, wherein the binary search comprises:

5 querying a client device located midway between the first and the last client device about a pending interrupt status and a passing interrupt status; and

determining the identity of the requesting client device based upon the pending and the passing interrupt status by,

10 (a) locating the requesting client device in an upstream portion of the daisy chain or a downstream portion of the daisy chain in relation to the queried client device;

(b) querying a second client device located midway in the upstream portion or the downstream portion located in (a); and

(c) repeating (a) and (b) until all requesting client devices are identified.

15 10. A bus architecture as recited in claim 9, wherein if the pending interrupt status of the queried client device is SET and a first initialization pin is the second logic level, then the queried client device is the only requesting client device.

11. A bus architecture as recited in claim 9, wherein if the pending interrupt status of the queried client device is SET and a first initialization pin is a first logic level,
20 then the queried client device is the one of at least another requesting client device.

12. A bus architecture as recited in claim 9, wherein if the pending interrupt status of the queried client device is NOT_SET and the passing interrupt status is NOT_SET then the requesting client device is downstream of the queried client device.

13. A bus architecture as recited in claim 9, wherein if the requesting client device
25 is downstream, then a next queried client device is midway between the current queried client device and the last client device.

14. A bus architecture as recited in claim 9, wherein if the pending interrupt status of the queried client device is NOT_SET and the passing interrupt status is SET then the requesting client device is upstream of the queried client device.

30 15. A bus architecture as recited in claim 9, wherein if the requesting client device is upstream, then a next queried client device is midway between the current queried client device and the first client device.

16. A method of signaling an interrupt request through a plurality of daisy-chained client devices connected by way of a first and a second interrupt pin and I/O pins selected ones of which are connected to at least one signal line wherein a last one of the client devices communicates with a host computer independently of the at least one signal line, comprising:
- 5 requesting an interrupt by at least one of the daisy chained client devices;
passing the interrupt request downstream towards a last client device from the requesting client device through the daisy chain to the last client device bypassing the at least one signal line;
- 10 communicating the interrupt request to the host computer by the last client device;
identifying the requesting client device by the host computer; and
servicing the requesting client device by the host computer.
17. A method as recited in claim 16, wherein the passing the interrupt request
- 15 downstream, comprises:
setting a pending interrupt flag to SET in the requesting client device;
(a) setting a second interrupt pin of the requesting client device to a first logic level; and
(b) updating a first interrupt pin of a next client device to the first logic level in
- 20 response to the setting (a).
18. A method as recited in claim 17, wherein the host computer identifies the requesting client device by,
performing a binary search of all client devices connected to the at least one signal line.
- 25 19. A method as recited in claim 18, wherein the binary search comprises:
querying a client device located midway between the first and the last client device about the pending interrupt status and the passing interrupt status; and
determining the identity of the requesting client device based upon the pending and the passing interrupt status and the logic levels of the first and the second
- 30 interrupt pins.
20. A method as recited in claim 19, wherein if the pending interrupt status of the queried client device is SET and a first initialization pin is the second logic level, then the queried client device is the only requesting client device.

21. A method as recited in claim 19, wherein if the pending interrupt status of the queried client device is SET and a first initialization pin is a first logic level, then the queried client device is the one of at least another requesting client device.
22. A method as recited in claim 19, wherein if the pending interrupt status of the queried client device is NOT_SET and the passing interrupt status is NOT_SET then the requesting client device is downstream of the queried client device.
23. A method as recited in claim 22, wherein if the requesting client device is downstream, then a next queried client device is midway between the current queried client device and the last client device.
24. A method as recited in claim 19, wherein if the pending interrupt status of the queried client device is NOT_SET and the passing interrupt status is SET then the requesting client device is upstream of the queried client device.
25. A method as recited in claim 22, wherein if the requesting client device is upstream, then a next queried client device is midway between the current queried client device and the first client device.
26. A system, comprising:
a host computer;
at least one signal line connected to the host device; and
a plurality of client devices wherein each of the client devices includes,
a number of I/O pins selected ones of which are connected to the at
least one signal line, and
a first and a second interrupt pin wherein all but a first and a last of the
plurality of client devices are connected to one another in a daisy chain
arrangement by way of the first and the second interrupt pin separate from the
at least one signal line, wherein the first client device is connected to the daisy
chain arrangement only by way of the second interrupt pin and wherein the
first interrupt pin of the first device is connected to a node external to the daisy
chain and wherein the last client device is connected to the daisy chain only by
way of a first interrupt pin and wherein a second interrupt pin of the last of the
plurality of client devices is connected to the host device by way of an
interrupt signal line separate from the at least one signal line.

27. A system as recited in claim 26, further comprising:
at least one legacy device configured to not generate an interrupt signal under any circumstances having I/O pins selected ones of which are connected to the at least one signal line and no interrupt pins.
- 5 28. A system as recited in claim 26, wherein the host computer is also connected to the at least one signal line.
29. A system as recited in claim 27 wherein when at least one of the client devices requests an interrupt, then the requesting client device sends an interrupt request up the daisy chain of client devices.
- 10 30. A system as recited in claim 29, wherein the interrupt request is received by the host computer by way of the interrupt signal line.
31. A system as recited in claim 30, wherein when the host computer receives the interrupt request, then the host computer identifies the requesting client device.
32. A system as recited in claim 26, wherein the host computer identifies the
15 requesting client device by,
performing a search of all client devices connected to the at least one signal line.
33. A system as recited in claim 32, wherein the search is a binary search.
34. A system as recited in claim 33, wherein the binary search comprises:
20 querying a client device located midway between the first and the last client device about a pending interrupt status and a passing interrupt status; and
determining the identity of the requesting client device based upon the pending and the passing interrupt status.
35. A bus architecture, comprising:
25 a plurality of independent signal lines; and
a plurality of client devices having a number of I/O pins, and a first and a second interrupt pin wherein all but a first and a last of the plurality of client devices are connected to one another in a daisy chain arrangement by way of the first and the second interrupt pin separate from the plurality of signal lines, wherein the first client
30 device is connected to the daisy chain arrangement only by way of the second interrupt pin and wherein the first interrupt pin of the first device is connected to a node external to the daisy chain and wherein the last client device is connected to the daisy chain only by way of a first interrupt pin and wherein a second interrupt pin of

the last of the plurality of client devices is connected to an external circuit by way of an interrupt signal line separate from the plurality of independent signal lines.

36. A bus architecture as recited in claim 35, wherein none of the plurality of client devices share any of the plurality of independent signal lines with any other of the plurality of client devices.

37. A bus architecture as recited in claim 35, wherein at least two of the plurality of client devices share at least one of the plurality of independent signal lines.

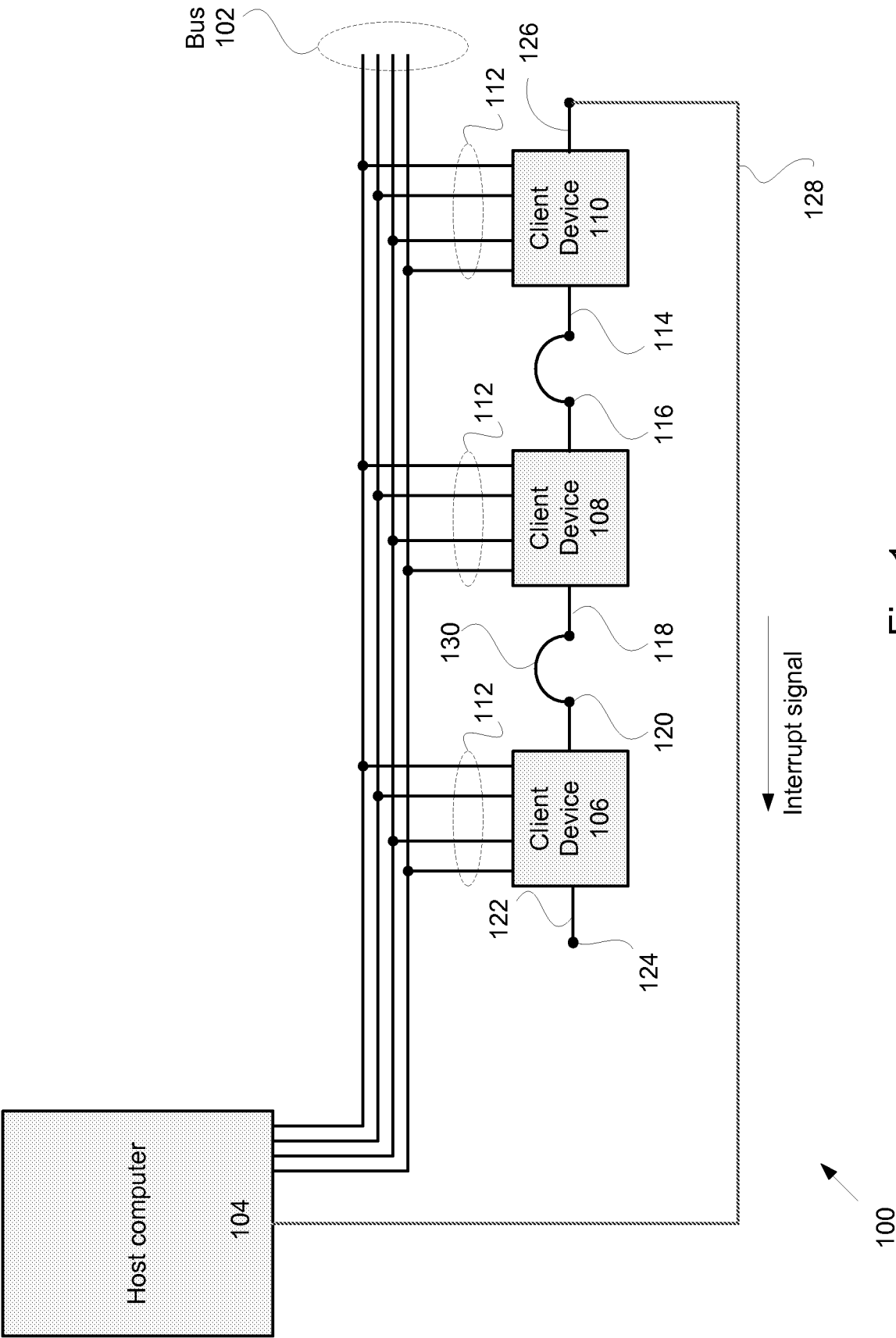


Fig. 1

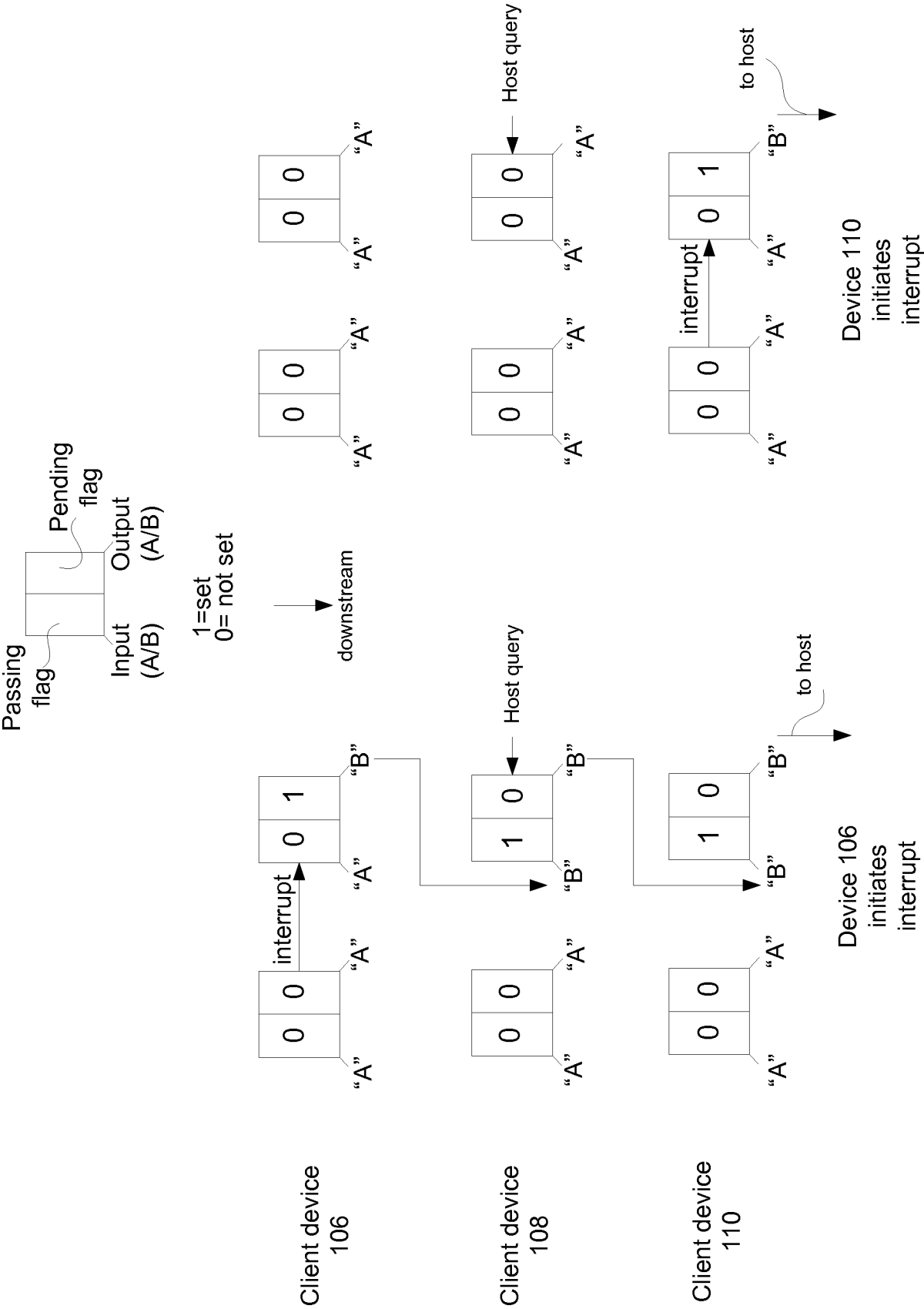


Fig. 2B

Fig. 2A

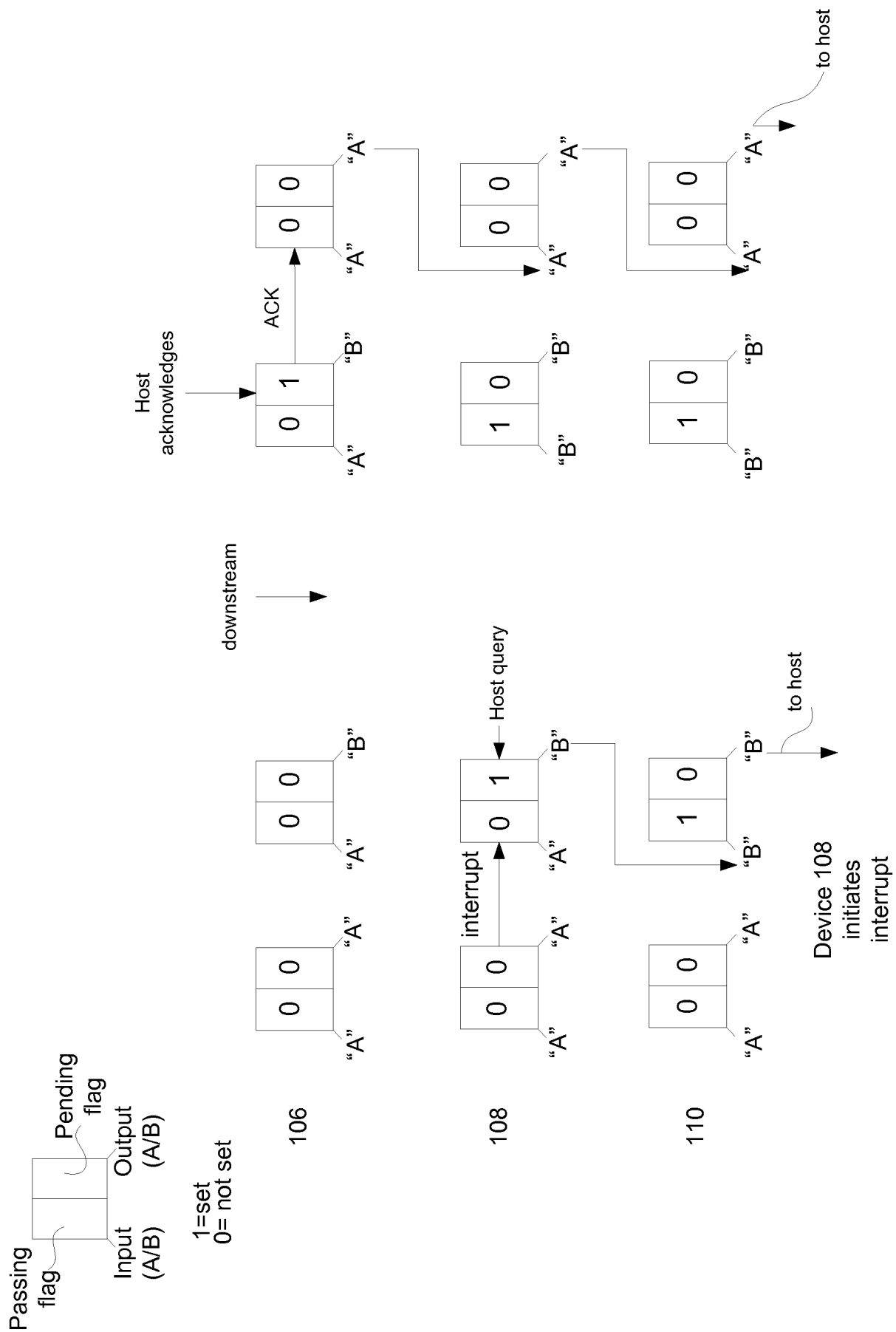


Fig. 2D

Fig. 2C

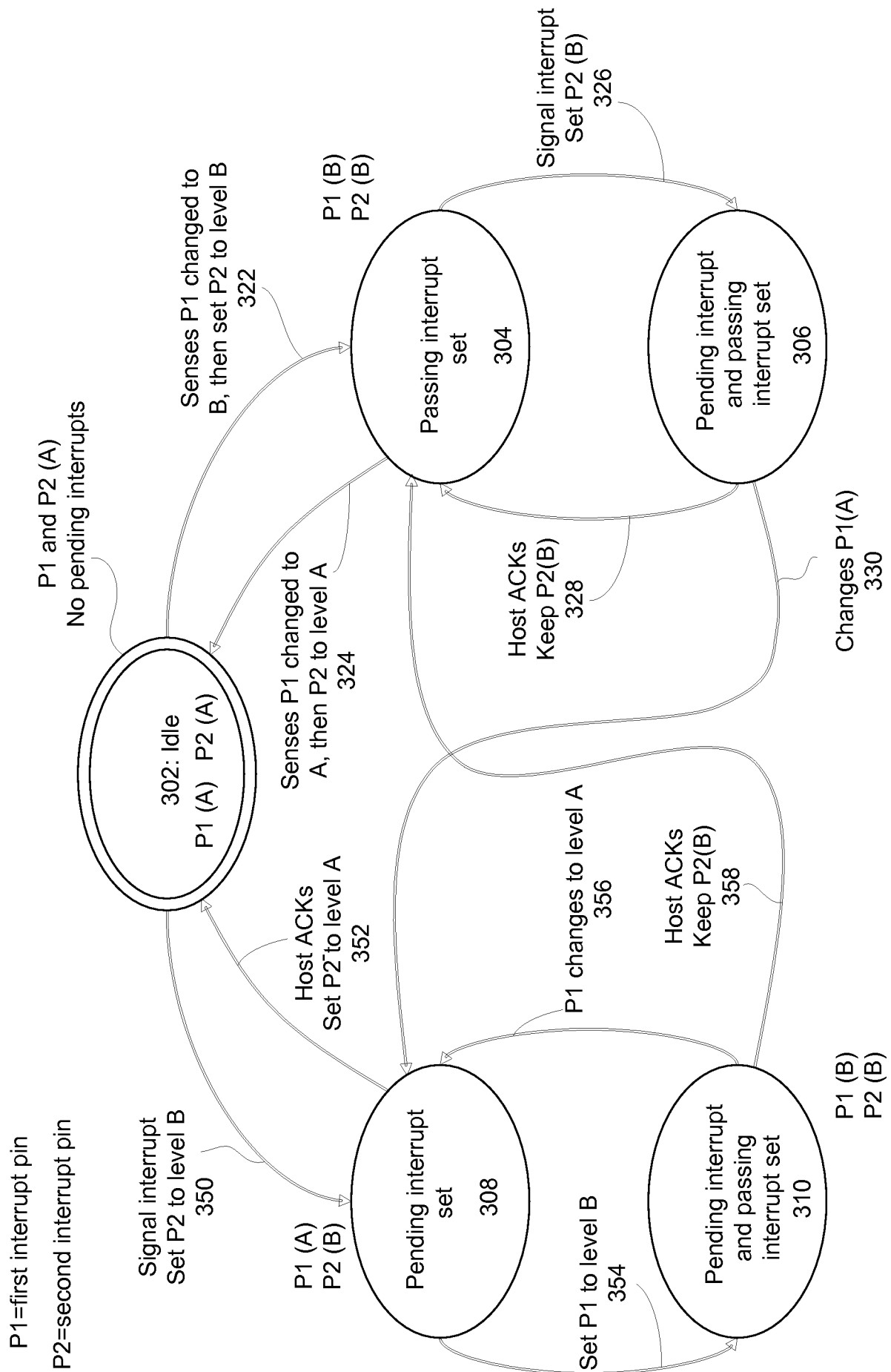
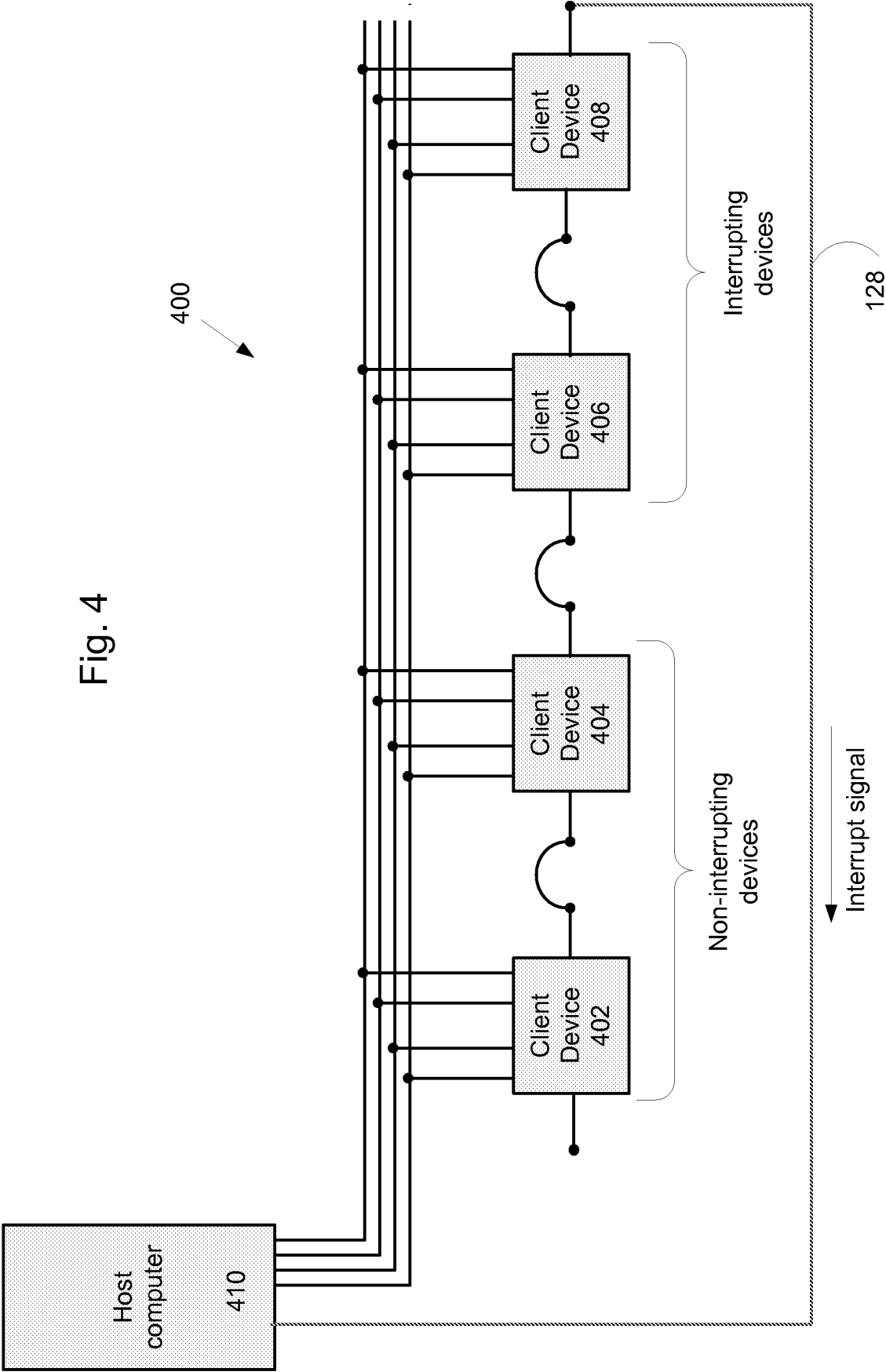
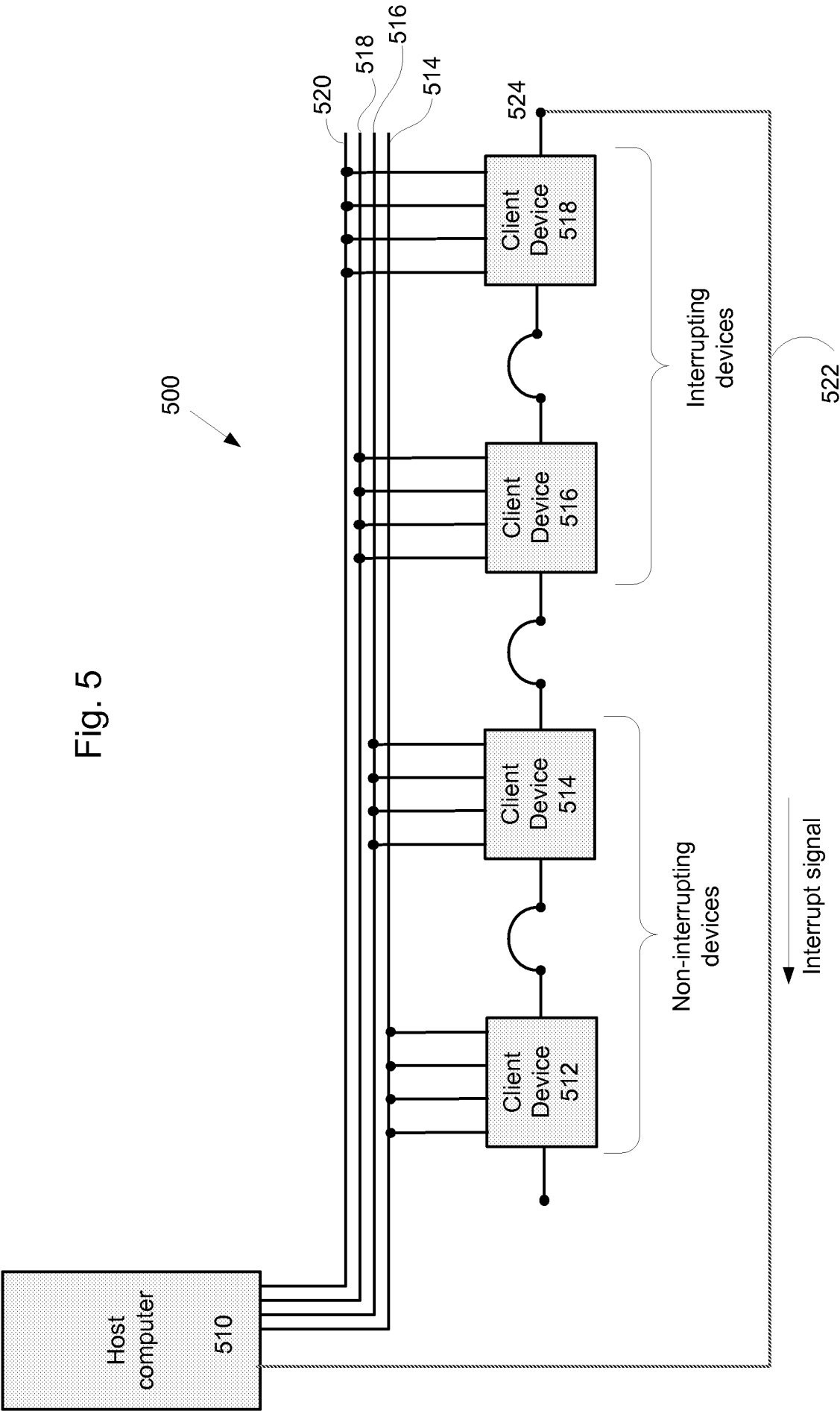


Figure 3





INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/080537

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F13/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 355 856 A (TOKYO SHIBAURA ELECTRIC CO [JP]) 28 February 1990 (1990-02-28) column 3, line 29 - column 4, line 49 figure 2	1-7, 16, 17, 26-32, 35-37
A	----- DATABASE INSPEC [Online] THE INSTITUTION OF ELECTRICAL ENGINEERS, STEVENAGE, GB; November 1982 (1982-11), KURTZ H L ET AL: "Multilevel, single-line, serial priority poll featuring poll-in, poll-out and poll-capture" XP002516452 Database accession no. 2014330 the whole document -/--	1-37

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

23 February 2009

Date of mailing of the international search report

10/03/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

van der Meulen, E

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/080537

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	& IBM Technical Disclosure Bulletin USA, vol. 25, no. 6, November 1982 (1982-11), pages 3037-3041, ISSN: 0018-8689 ----- WO 98/12634 A (PHILIPS ELECTRONICS NV [NL]; PHILIPS NORDEN AB [SE]) 26 March 1998 (1998-03-26) page 1 figures 1,4,7 -----	1-37

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/080537

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
EP 0355856	A	28-02-1990	JP	2059949 A	28-02-1990
WO 9812634	A	26-03-1998	DE	69726400 D1	08-01-2004
			DE	69726400 T2	26-08-2004
			JP	2000501538 T	08-02-2000
			JP	3894579 B2	22-03-2007
			US	6098144 A	01-08-2000