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(54) **METHOD OF FORMING INTEGRATED BONDING PADS INCLUDING CLOSED VIAS AND CLOSED CONDUCTIVE PATTERNS**

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(52) **U.S. Cl.** **438/612**; 438/614

(57) **ABSTRACT**

Multilayer bonding pads for integrated circuits include first and second spaced apart conductive patterns and a dielectric layer therebetween. A closed conductive pattern is included in the dielectric layer that electrically connects the first and second spaced apart patterns. The closed conductive pattern encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer. The closed conductive pattern may be a circular, elliptical, polygonal or other conductive pattern. A second closed conductive pattern may also be included in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns. An open conductive pattern having end points, may also be included in the dielectric layer. The open conductive pattern may be included in the inner portion of the dielectric layer, in the outer portion of the dielectric layer or both. Bonding pads may be formed by forming a dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via therein that encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer. A conductive pattern is formed in the closed via and on the dielectric layer opposite the substrate. The conductive pattern preferably fills the closed via. The steps of forming a dielectric layer and forming a conductive pattern may be repeatedly performed, to form a multilayer bonding pad on the integrated circuit substrate.

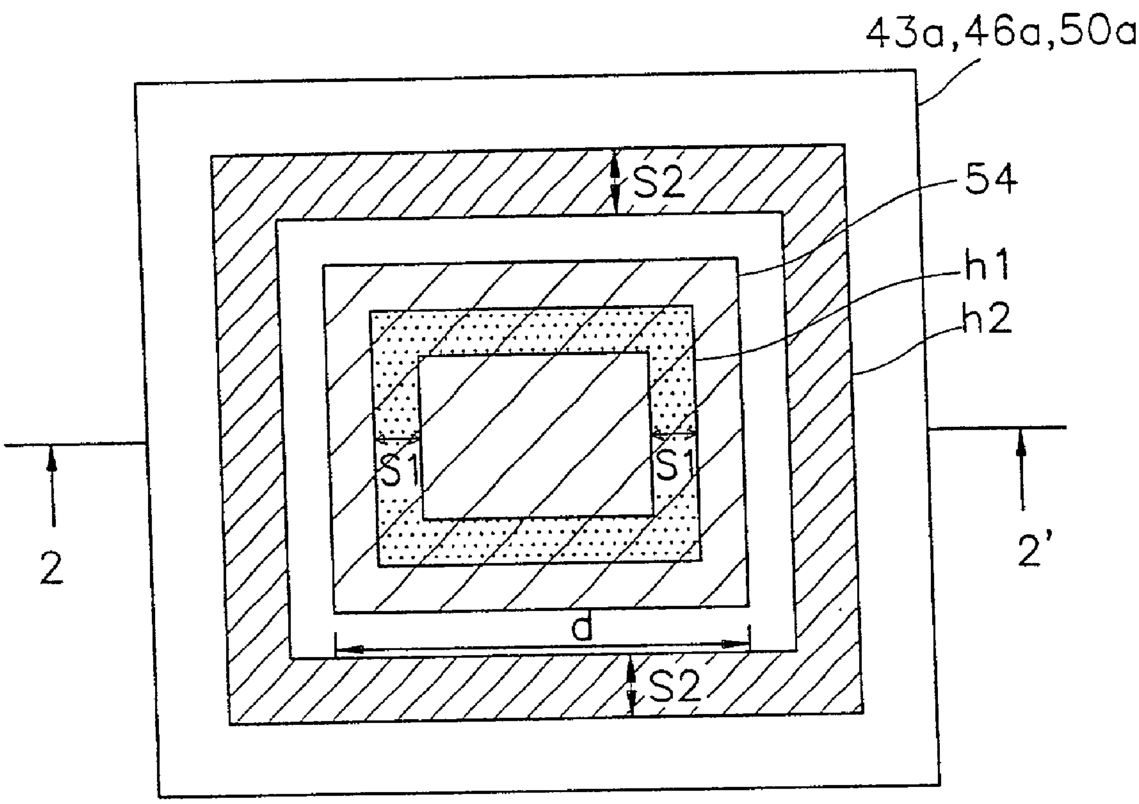


FIG. 1

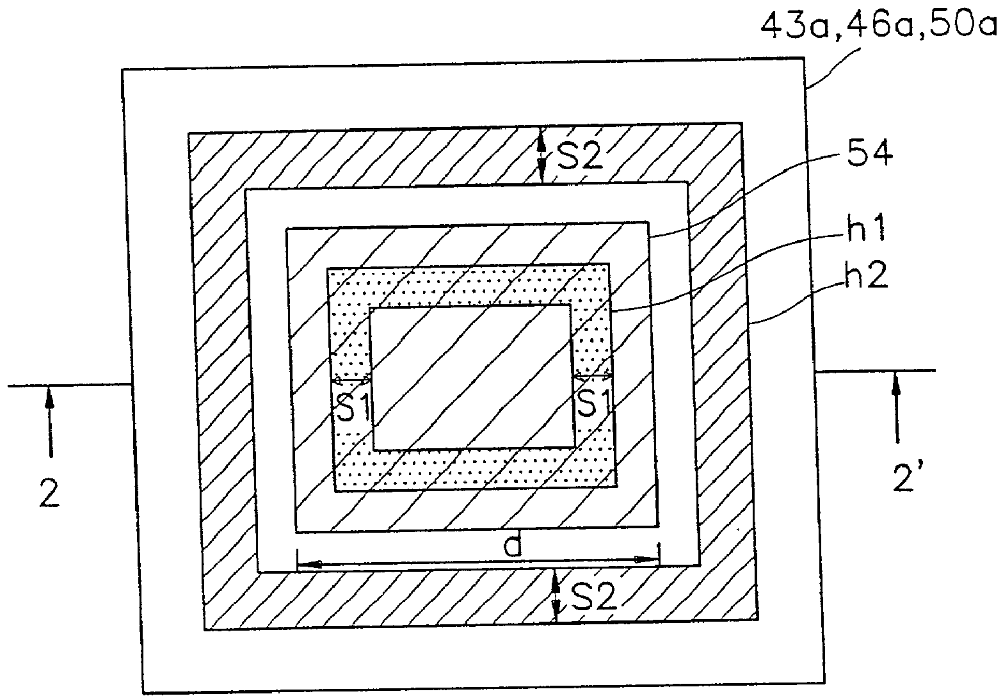

43a,46a,50a
S2
54
h1
h2
S1
S1
2
2'
d
S2

FIG. 2

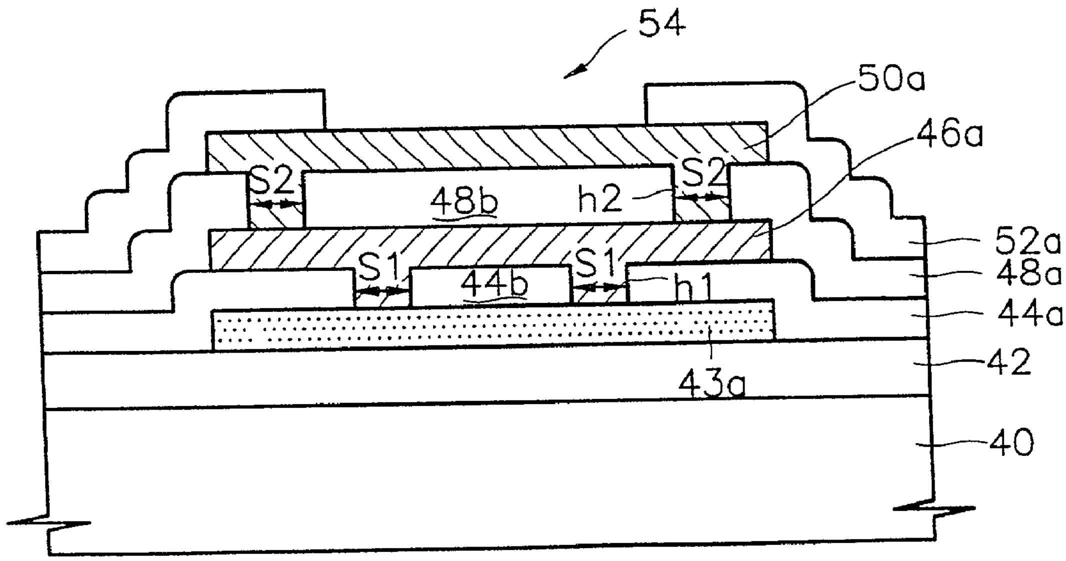

54
50a
46a
S2
S2
48b
h2
52a
48a
S1
44b
S1
h1
44a
42
43a
40

FIG. 3

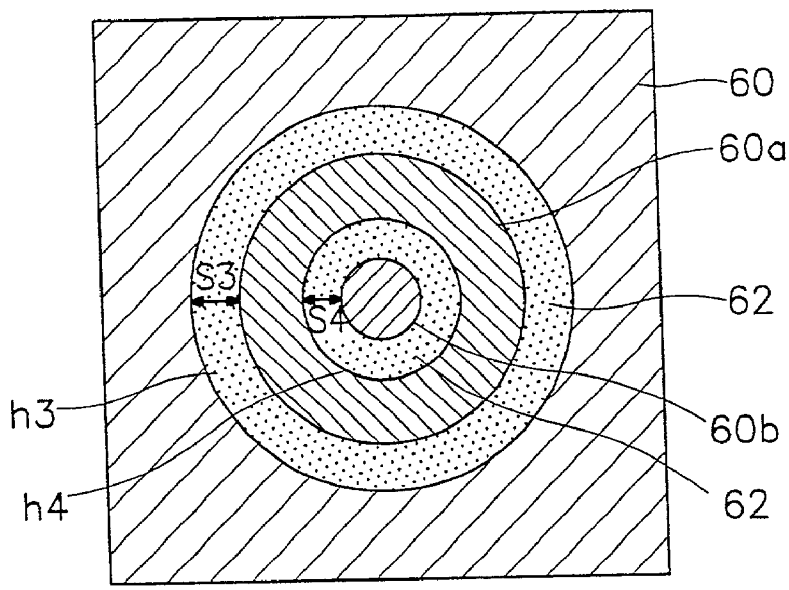


FIG. 4

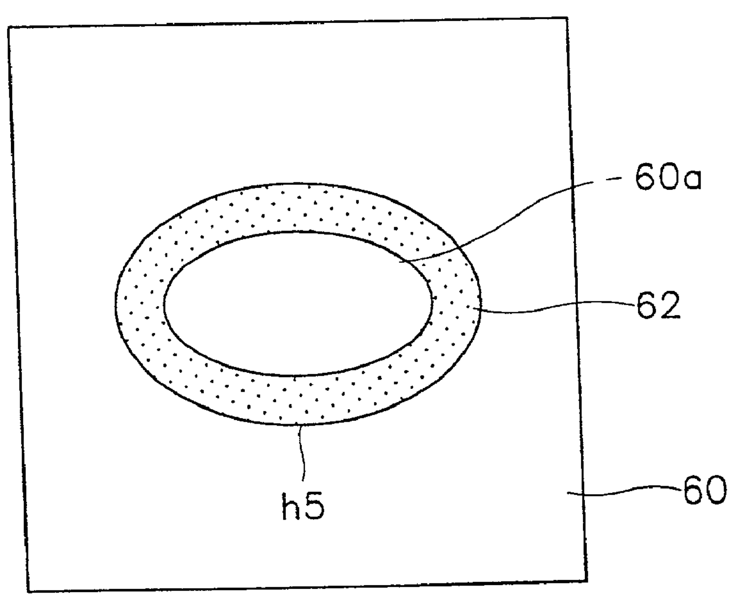


FIG. 5

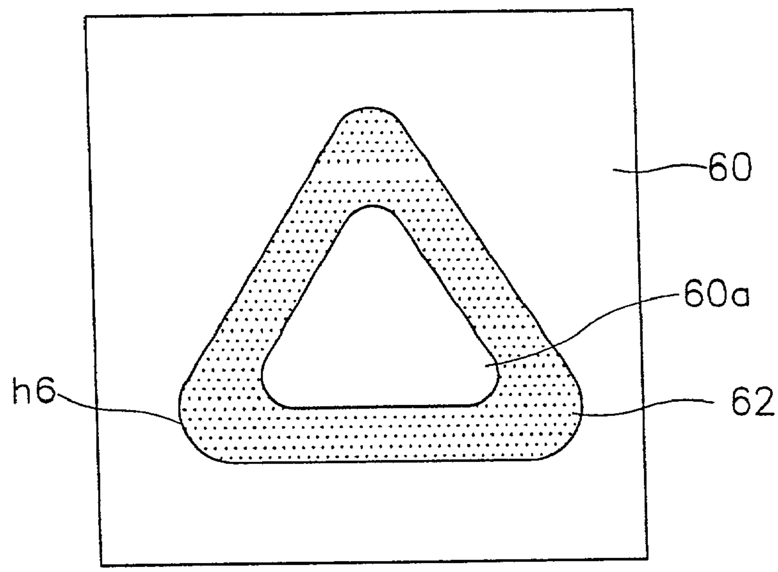


FIG. 6

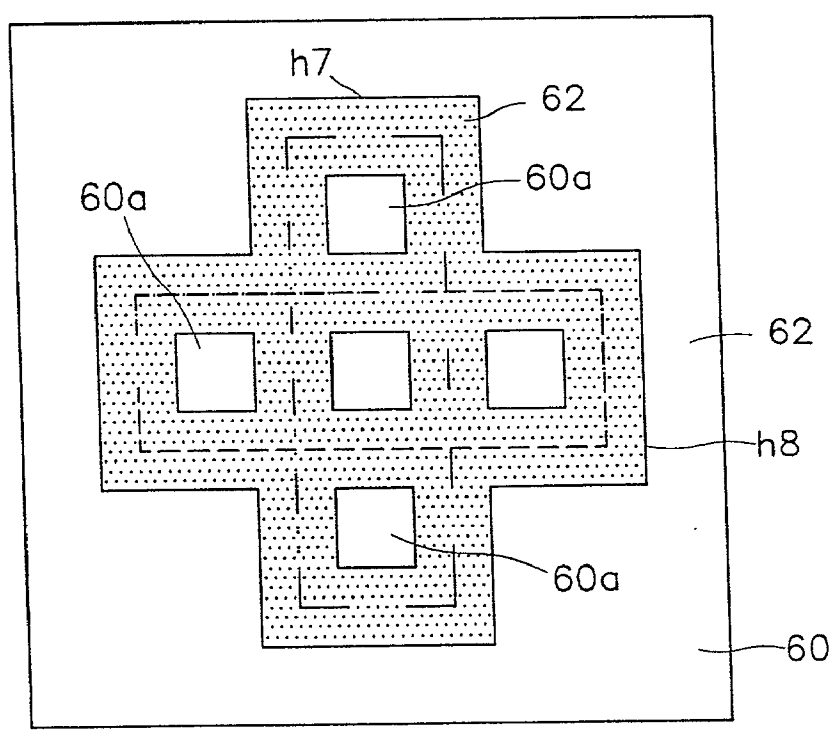


FIG. 7

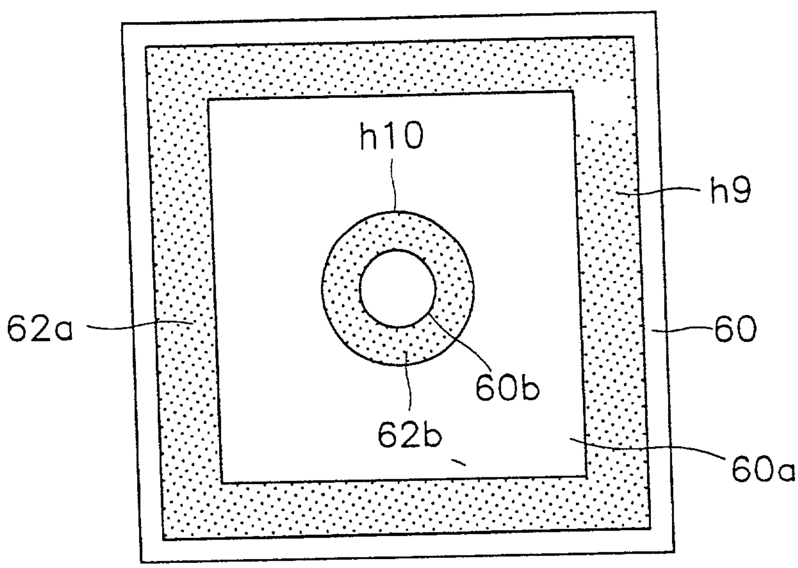


FIG. 8

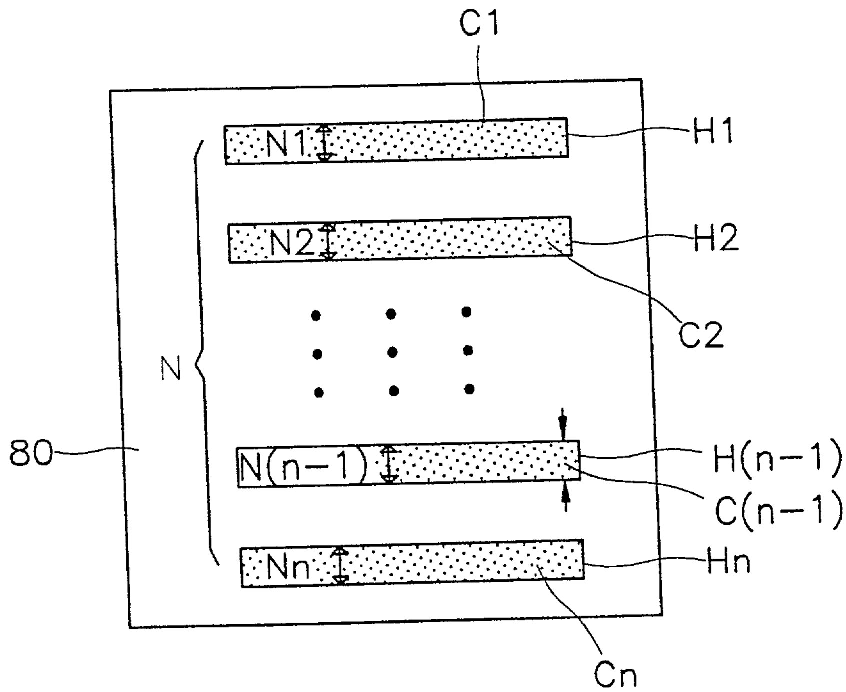
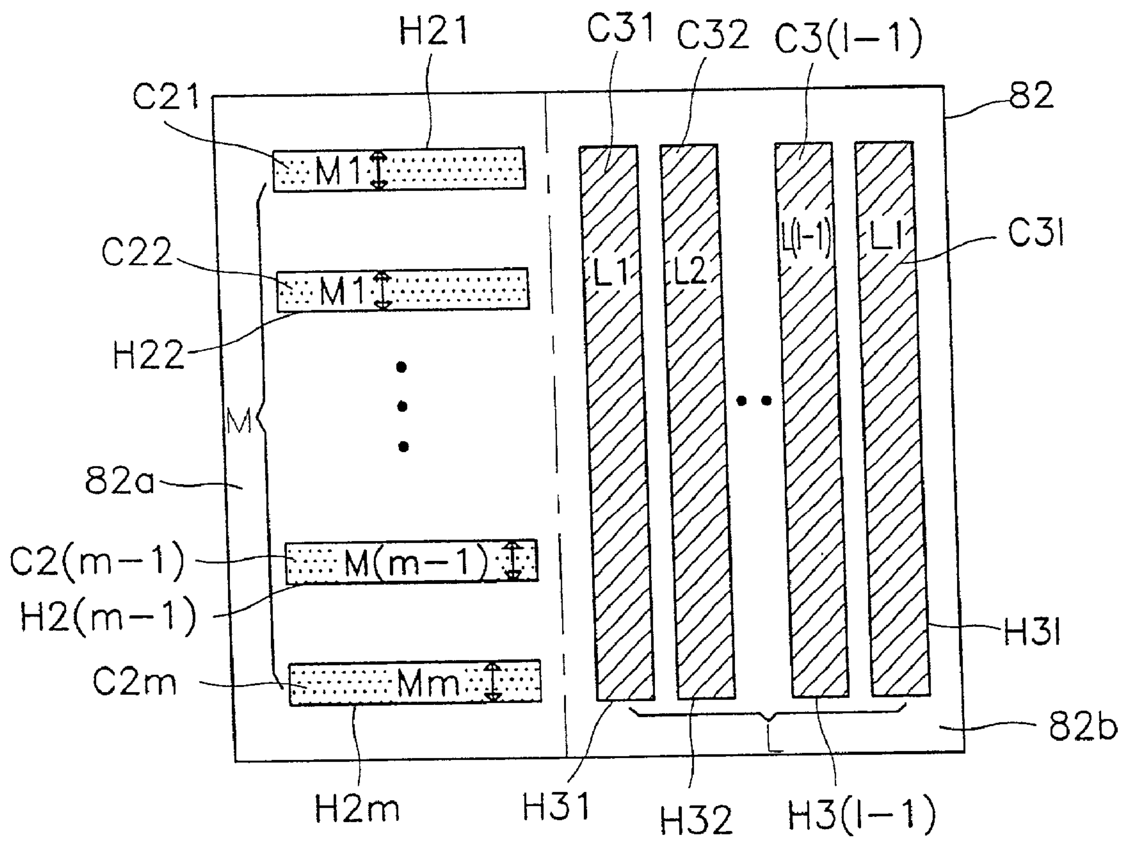


FIG. 9



H21
C31
C32
C3(l-1)
C21
82
M1
M1
C22
H22
L1
L2
L(l-1)
Ll
C3l
M
82a
C2(m-1)
M(m-1)
H2(m-1)
H3l
C2m
Mm
L
82b
H2m
H31
H32
H3(l-1)

FIG. 10

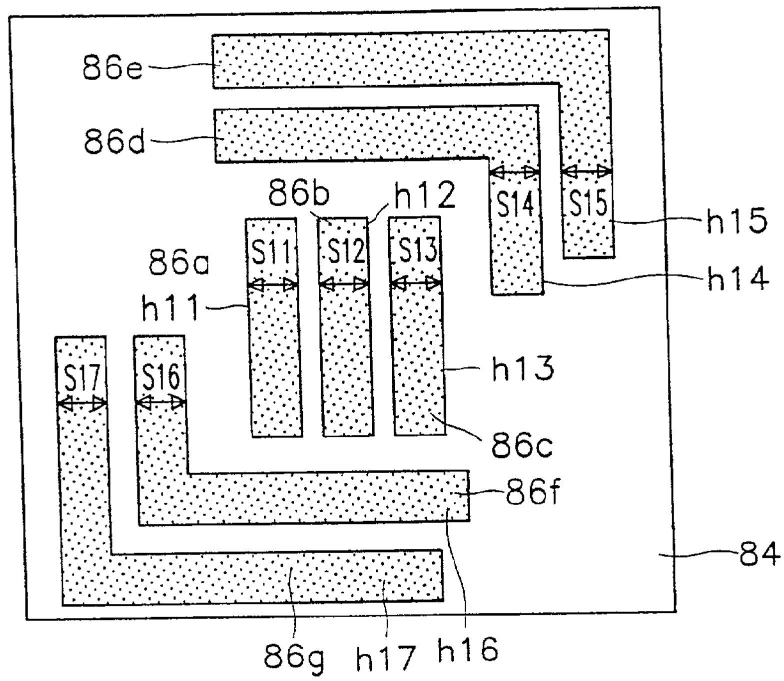

86e
86d
86b
h12
S14
S15
h15
86a
S11
S12
S13
h14
h11
S17
S16
h13
86c
86f
84
86g
h17
h16

FIG. 11

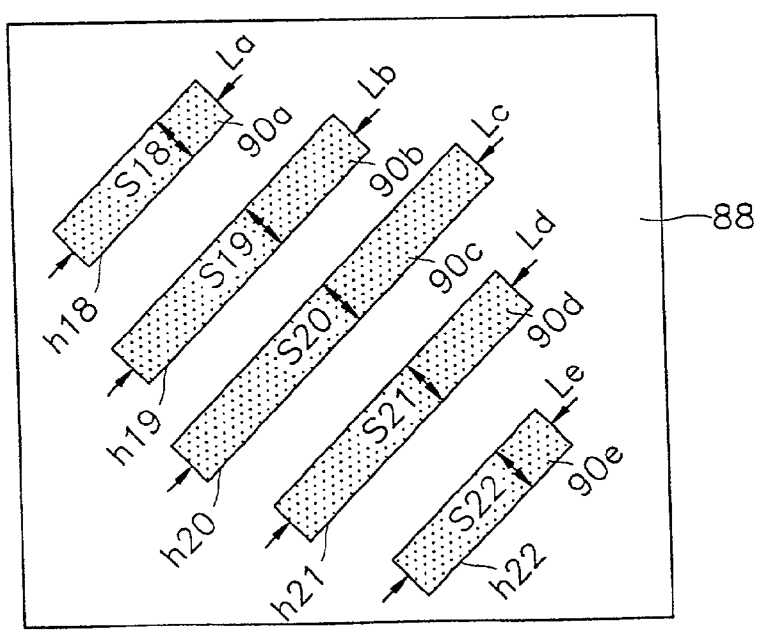

La
Lb
Lc
90a
S18
90b
88
S19
Ld
h18
90c
S20
90d
Le
S21
h19
90e
S22
h20
h22
h21

FIG. 12

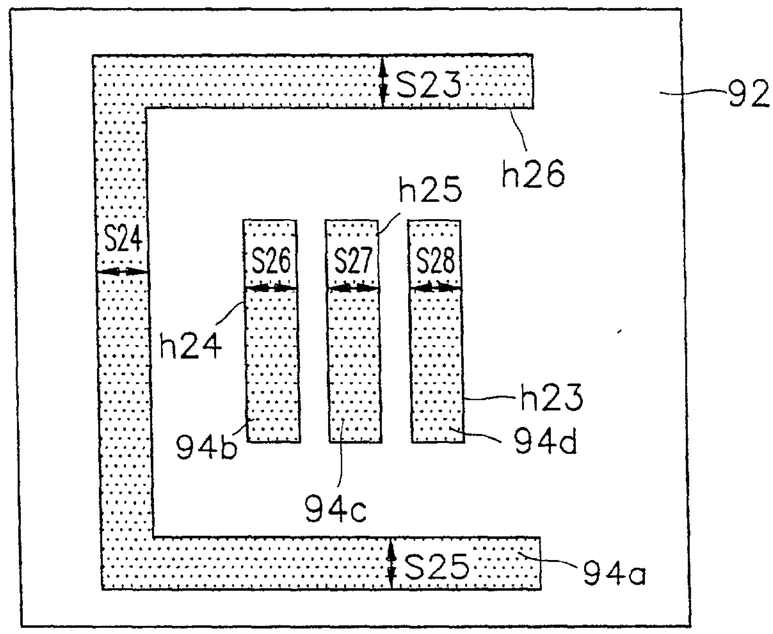

S23
92
h26
h25
S24
S26
S27
S28
h24
h23
94b
94d
94c
S25
94a

FIG. 13

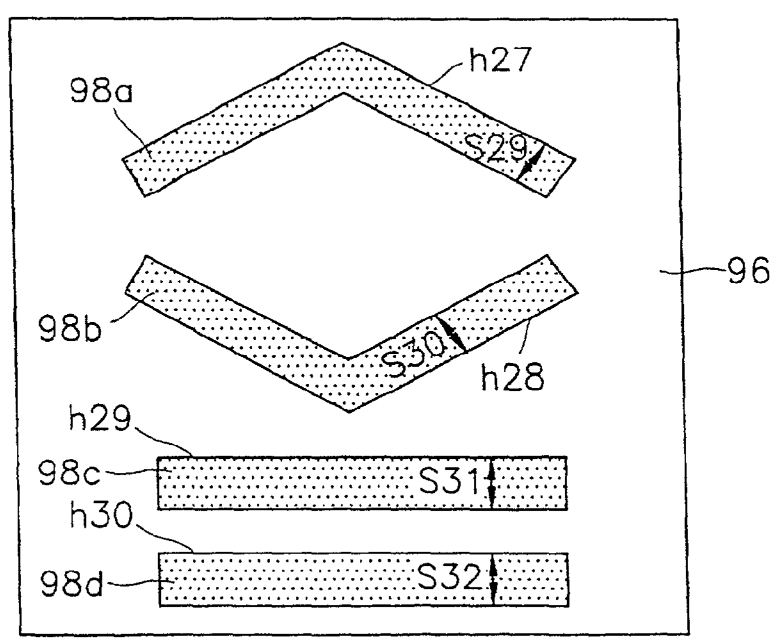

h27
98a
S29
96
98b
S30
h28
h29
98c
S31
h30
98d
S32

FIG. 14

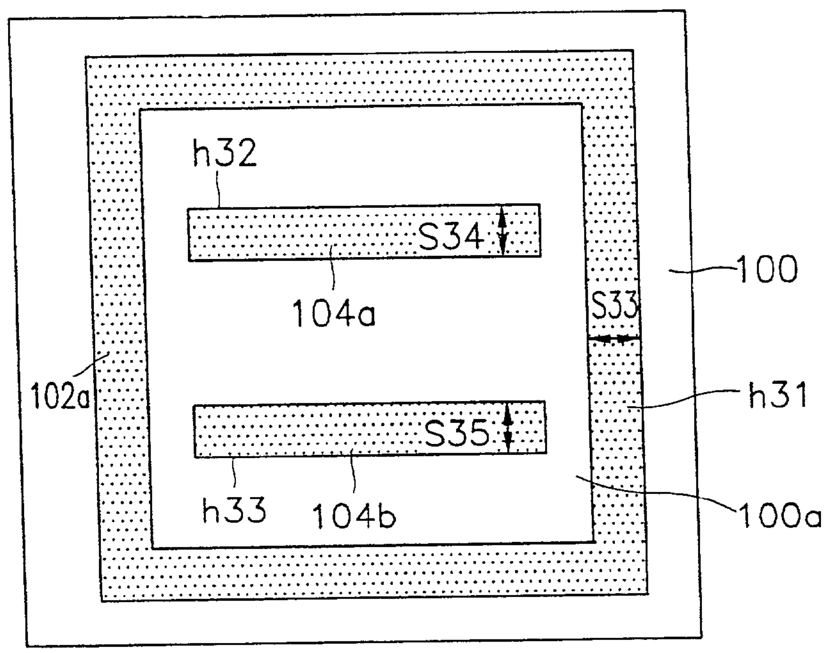

h32
S34
100
104a
S33
102a
h31
S35
h33
104b
100a

FIG. 15

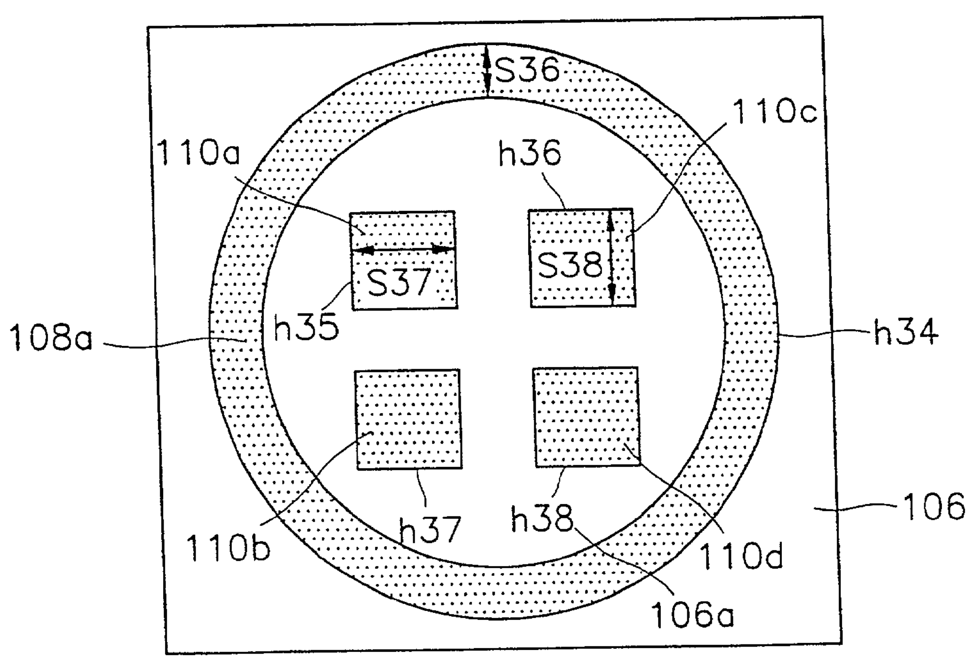

S36
110c
110a
h36
S38
S37
108a
h35
h34
106
110b
h37
h38
110d
106a

FIG. 16

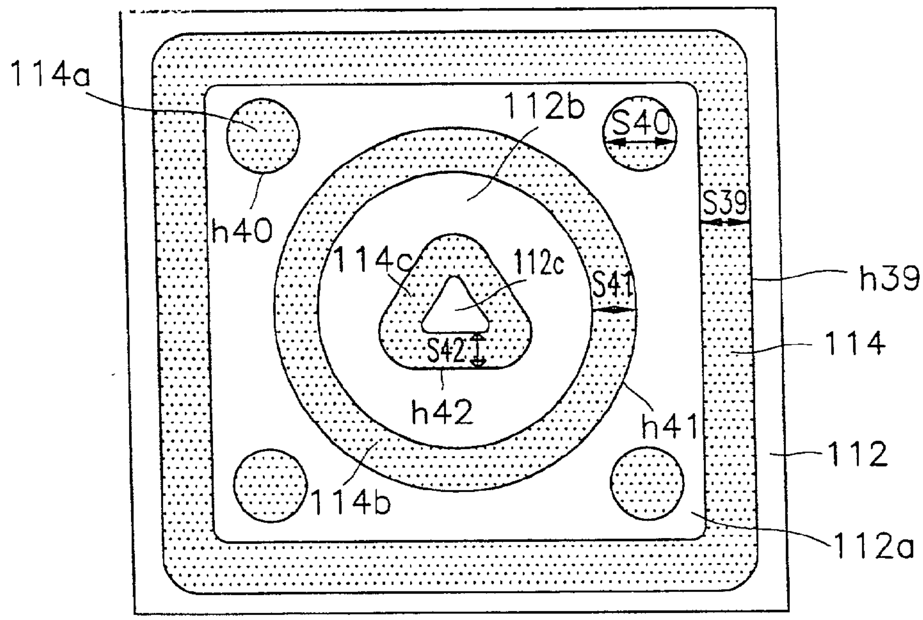


FIG. 17

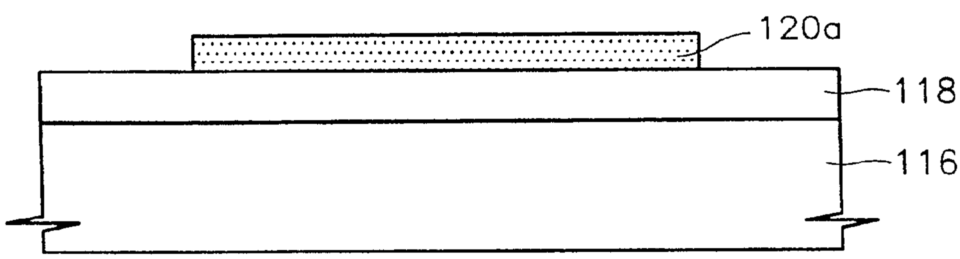


FIG. 18

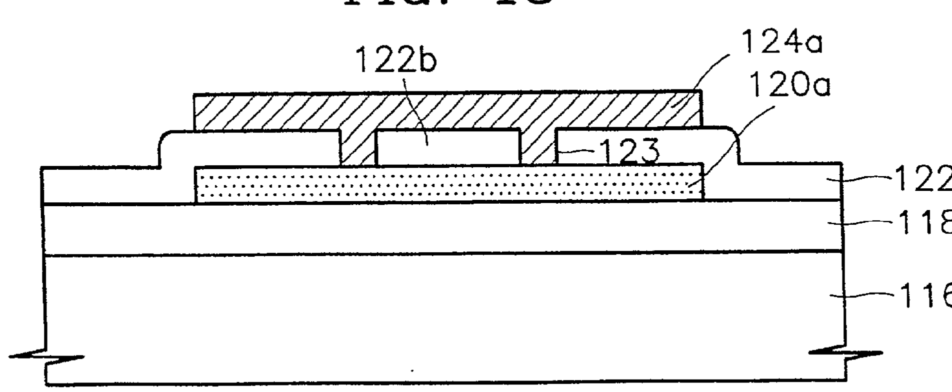


FIG. 19

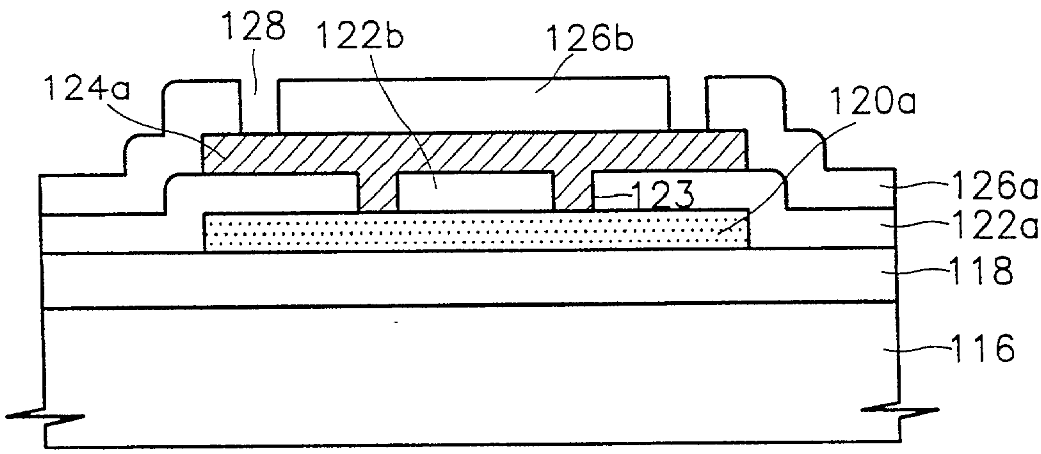

128
122b
126b
124a
120a
123
126a
122a
118
116

FIG. 20

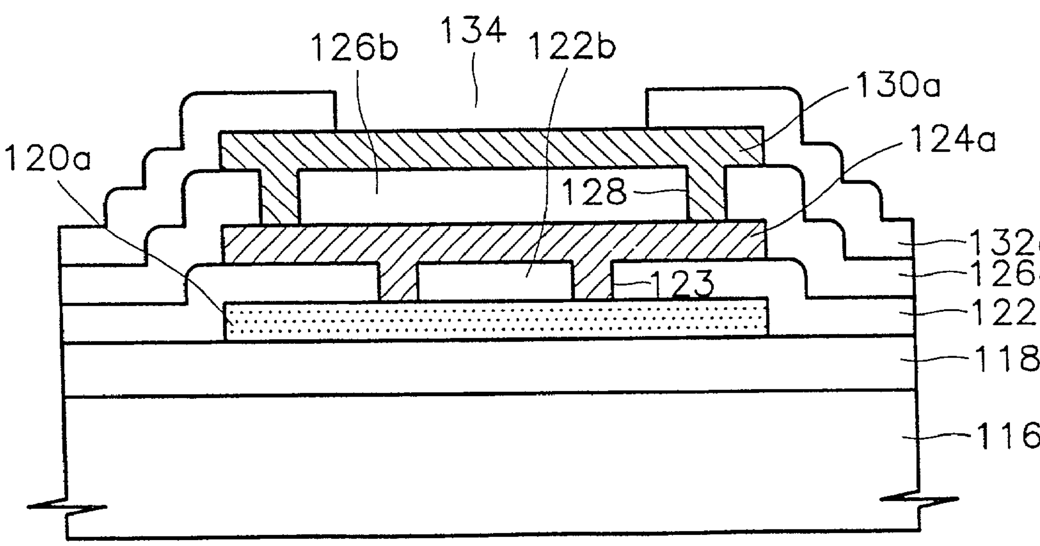
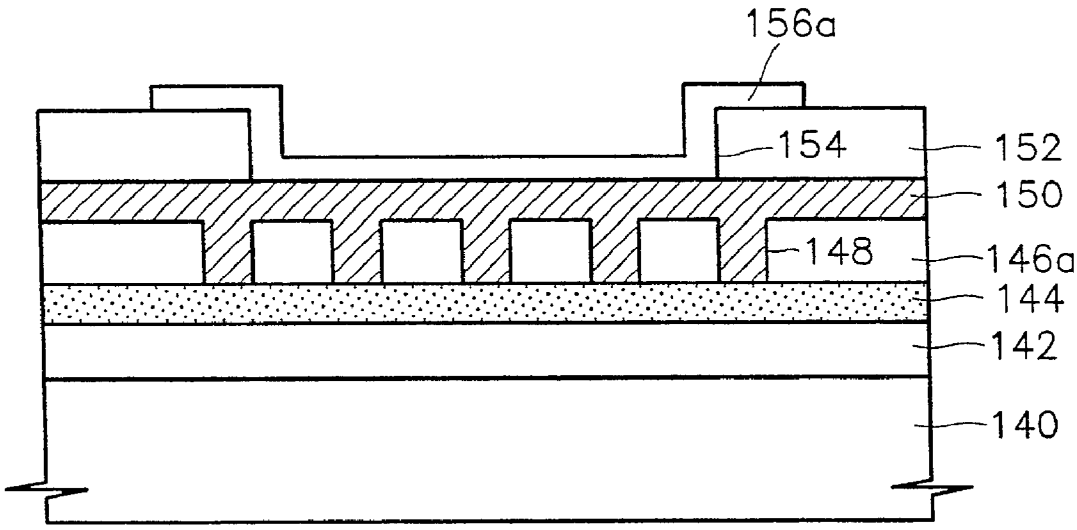

134
126b
122b
130a
120a
124a
128
132a
126a
123
122a
118
116

FIG. 21



METHOD OF FORMING INTEGRATED BONDING PADS INCLUDING CLOSED VIAS AND CLOSED CONDUCTIVE PATTERNS

FIELD OF THE INVENTION

[0001] This invention relates to integrated circuits and methods of forming the same, and more particularly to bonding pads for integrated circuits and methods of forming the same.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits, also referred to as "chips", are widely used in consumer and commercial electronic products. As is well known to those having skill in the art, an integrated circuit generally includes a substrate such as a semiconductor substrate and an array of bonding pads on the substrate. The bonding pads provide an electrical connection from outside the integrated circuit to microelectronic circuits in the integrated circuit.

[0003] In the design of high performance integrated circuits, it is generally desirable to provide a low electrical resistance in the bonding pads. Unfortunately, as the integration density of integrated circuits continues to increase, more bonding pads may be needed in the integrated circuit, so that the area of each bonding pad may be lowered. Unfortunately, as the bonding pad becomes smaller, the resistance thereof may increase.

[0004] Moreover, as the integrated circuit device becomes more highly integrated, a step between the bonding pad and an insulating layer around the bonding pad may be produced. Reaction residue that is generated during a process of forming a contact hole on the insulating layer in order to expose the bonding pad, may become stacked at the edge of the step. The reaction residue may increase the contact resistance of the bonding pad.

SUMMARY OF THE INVENTION

[0005] It is therefore an object of the present invention to provide improved bonding pads for integrated circuits and methods of forming the same.

[0006] It is another object of the present invention to provide bonding pads for integrated circuits that can have low contact resistance, and methods of forming the same.

[0007] These and other objects are provided, according to the present invention, by multilayer bonding pads for integrated circuits that include first and second spaced apart conductive patterns and a dielectric layer therebetween. A closed conductive pattern is included in the dielectric layer that electrically connects the first and second spaced apart patterns. The closed conductive pattern encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer. As is well known to those having skill in the art, a closed pattern is a curve that has no end points. The closed conductive pattern may be a circular, elliptical, polygonal or other conductive pattern.

[0008] A second closed conductive pattern may also be included in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns. An open conductive pattern having end points, may also be included in the dielectric layer. The open conductive pattern may be included in the inner portion of the dielectric layer, in the outer portion of the dielectric layer or both.

[0009] A third conductive pattern may also be provided that is spaced apart from the second conductive pattern. A second dielectric layer is included between the second and third conductive patterns, and a fourth conductive pattern is included in the dielectric layer, electrically connecting the second and third spaced apart conductive patterns. The fourth conductive pattern may be an open conductive pattern. Alternatively, the fourth conductive pattern may comprise a second closed conductive pattern in the second dielectric layer, electrically connecting the second and third spaced apart conductive patterns. The second closed conductive pattern encloses a second inner portion of the second dielectric layer and is enclosed by a second outer portion of the second dielectric layer. The second dielectric layer may also include additional open and closed conductive patterns therein, electrically connecting the second and third spaced apart conductive patterns.

[0010] In a preferred embodiment, the second and third conductive patterns are congruent to one another, and the closed conductive pattern and the second closed conductive pattern are of the same shape but of different sizes. In another preferred embodiment, the closed conductive pattern is an elliptical conductive pattern and the second closed conductive pattern is a polygonal closed conductive pattern.

[0011] By connecting conductive layer patterns with a closed conductive pattern in the dielectric layer, a step between an exposed region of the conductive pad and a dielectric layer covering an edge of the pad may be reduced. Reaction residue can therefore be reduced or prevented from being stacked on the step. Stacked residue can also be easily removed, to thereby lower the contact resistance of the pad.

[0012] Bonding pads according to the present invention may also be thought of as including first and second spaced apart conductive patterns and a dielectric layer therebetween, the dielectric layer including a closed via therein that extends between the first and second spaced apart conductive patterns. The closed via encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer. A closed conductive pattern is provided in the closed via, electrically connecting the first and second spaced apart conductive patterns. The closed conductive pattern preferably fills the closed via. Various forms of closed conductive patterns and combinations with open conductive patterns may be provided, as was described above.

[0013] Bonding pads according to the present invention are preferably included on an integrated circuit substrate, to provide improved integrated circuits. Bonding pads according to the present invention may be formed by forming a dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via therein that encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer. A conductive pattern is formed in the closed via and on the dielectric layer opposite the substrate. The conductive pattern preferably fills the closed via. The steps of forming a dielectric layer and forming a conductive pattern may be repeatedly performed, to form a multilayer bonding pad on the integrated circuit substrate. The closed vias may have various shapes and may be combined with open vias as was described above. Accordingly, high performance bonding pads, integrated circuits and forming methods may thereby be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** is a plan view of an integrated circuit device having a multilayer conductive pad according to a first embodiment of the present invention;

[0015] **FIG. 2** is a sectional view of an integrated circuit device taken along direction of **FIG. 1**;

[0016] **FIGS. 3 through 7** are plan views of various closed type via holes of the first embodiment of the present invention;

[0017] **FIGS. 8 through 13** are plan views of an integrated circuit device having a multilayer conductive pad according to a second embodiment of the present invention;

[0018] **FIGS. 14 through 16** are plan views of an integrated circuit device having a multilayer conductive pad according to a third embodiment of the present invention;

[0019] **FIGS. 17 through 20** are diagrams showing a method of manufacturing an integrated circuit device having a multilayer conductive pad according to embodiments of the present invention; and

[0020] **FIG. 21** is a sectional view of an integrated circuit device having a multilayer pad according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0021] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0022] Referring to **FIG. 1**, reference numerals **43***a*, **46***a* and **50***a* denote first, second and third conductive layer patterns stacked in sequence on an integrated circuit substrate such as a semiconductor substrate, for forming a multilayer conductive pad. Reference numerals h**1** and h**2** denote first and second vias, also referred to as via holes, exposing the first and second conductive layer patterns **43***a* and **46***a*. The first and second via holes h**1** and h**2** are closed via holes. The first via hole h**1** is a path connecting the first and second conductive layer patterns **43***a* and **46***a*, and the second via hole h**2** is a path connecting the second conductive layer pattern **46***a* to the third conductive layer pattern **50***a*.

[0023] Reference numeral **54** denotes a pad window. The pad window **54** is a bonding area in which an external connection to an integrated circuit is made to the multilayer conductive pad. Preferably, the pad window **54** is wide enough to increase a bonding process margin. An edge boundary of the pad window **54** of **FIG. 1** is disposed between the first and second via holes h**1** and h**2**.

[0024] Reference character d denotes a width of the pad window **54**. The widths s**1** and s**2** of the first and second via holes h**1** and h**2** may be the same or different from each other. Also, the widths of the first and second via holes h**1** and h**2** may be different per region on different sides thereof. For instance, the width of a portion of the first via hole h**1** may be different from other portions thereof.

[0025] Referring to **FIG. 2, a** first dielectric layer **42**, also referred to as an interdielectric layer, is formed on a semiconductor substrate **40**, and a first conductive layer pattern **43***a* is formed on the first interdielectric layer **42**. A second dielectric layer **44***a*, also referred to as a second dielectric layer, and a second interdielectric layer pattern **44***b* are formed on the first interdielectric layer **42** and the first conductive layer pattern **43***a*. A first via hole h**1** exposing the first conductive layer pattern **43***a* is formed between the second interdielectric layer **44***a* and the second interdielectric layer pattern **44***b*. It is preferable that the width s**1** of the first via hole h**1** is uniform.

[0026] A second conductive layer pattern **46***a*, preferably filling the first via hole h**1**, is formed on the second interdielectric layer **44***a* and the second interdielectric layer pattern **44***b*. The width of the second conductive layer pattern **46***a* preferably is the same as that of the first conductive layer pattern **43***a*.

[0027] In **FIG. 2**, the second conductive layer pattern **46***a* completely overlaps the first conductive layer pattern **43***a*, i.e. it is congruent thereto. However, the second conductive layer pattern **46***a* may partially overlap the first conductive layer pattern **43***a*.

[0028] The first via hole h**1** is filled with a conductive plug such as a tungsten plug, and a conductive layer may exist on the entire surface of the resultant structure. The third interdielectric layer **48***a* and the third interdielectric layer pattern **48***b* are formed on the second interdielectric layer **44***a* and the second conductive layer pattern **46***a*. Also, the second via hole h**2** exposing the second conductive layer pattern **46***a* is formed between the third interdielectric layer **48***a* and the third interdielectric layer pattern **48***b*. The third interdielectric layer **48***a* and the third interdielectric layer pattern **48***b* are separated from each other by a width s**2** of the second via hole h**2**. It is preferable that the width s**2** of the second via hole h**2** is the same as the width s**1** of the first via hole h**1**. The third interdielectric layer pattern **48***b* is preferably larger than the second interdielectric layer pattern **44***b*. The area of the third interdielectric layer pattern **48***b* may have an arbitrary value within the second conductive layer pattern **46***a*. A third conductive layer pattern **50***a* connected to the second conductive layer pattern **46***a* through the second via hole h**2** is formed on the third interdielectric layer **48***a* and the third interdielectric layer pattern **48***b*.

[0029] The second via hole h**2** is filled with a conductive plug such as a tungsten plug, and a conductive layer may be formed on the entire surface of the third interdielectric layer **48***a*, the third interdielectric layer pattern **48***b* and the conductive plug. Preferably, the thicknesses of the first through third conductive layer patterns **43***a*, **46***a* and **50***a* are the same. An upper insulating layer **52***a* having a pad window **54** exposing the third conductive layer pattern **50***a* is formed on the third interdielectric layer **48***a*. Preferably, the pad window **54** is smaller than the third interdielectric layer pattern **48***b*, and larger than the second interdielectric layer pattern **44***b*.

[**0030**] As described above, if desired, various types of via holes, for instance, closed or open via holes may be further formed in the second and third interdielectric layers **44***a* and **48***a* or the second and third interdielectric layer patterns **44***b* and **48***b*. Various closed or open via holes may be formed in an arbitrarily selected interdielectric layer. The shape of the closed via hole may be circular, elliptical or polygonal.

[**0031**] The various closed holes may be formed independently or overlapping with each other in the second or third interdielectric layer **44***a* and **48***a*. Also, open via holes may be formed independently or together with the closed via hole in the second and third interdielectric layers **44***a* and **48***a*.

[**0032**] The shape of the via holes formed in the second and third interdielectric layers **44***a* and **48***a* will now be described. More specifically, the plane forms of the interdielectric layer patterns surrounded by the closed via holes will be described.

[**0033**] Referring to **FIG. 3**, an interdielectric layer pattern **60***a* is formed in an interdielectric layer **60**. The shape of the interdielectric layer pattern **60***a* is a circle. A third closed via hole h**3** is formed between the interdielectric layer **60** and the interdielectric layer pattern **60***a*. A width s**3** of the third closed via hole h**3** indicates a distance between the interdielectric layer pattern **60***a* and the interdielectric layer **60**. A conductive material **62** filling the third closed via hole h**3** contacts conductive layers formed on and under the interdielectric layer **60**. An interdielectric layer pattern **60***b* is formed in the interdielectric layer pattern **60***a*. The interdielectric layer pattern **60***b* is surrounded by a fourth closed via hole h**4**. A width s**4** of the fourth closed via hole h**4** indicates a distance between the interdielectric layer patterns **60***a* and **60***b*. It is preferable that the widths s**3** and s**4** of the third and fourth closed via holes h**3** and h**4** are the same.

[**0034**] Other shapes of closed via holes may be provided. For example, an elliptical formed closed via hole h**5** is shown in **FIG. 4**. A triangular closed via hole h**6** is shown in **FIG. 5**. A closed via hole h**7** obtained by intersecting two rectangular closed via holes may be formed in the interdielectric layer **60** as shown in **FIG. 6**. Also, as shown in **FIG. 7**, two different closed via holes, for instance, a rectangular closed via hole h**9** and a circular closed via hole h**10**, may be formed in the interdielectric layer **60**.

[**0035**] Referring to **FIG. 8, N** linear open via holes H**1**, H**2**, . . . , H(n-**1**), Hn extend parallel with each other in an interdielectric layer **80**. The lengths of the open via holes are preferably the same. Also, it is preferable that the widths N**1**, N**2**, . . . , N(n-**1**), Nn of the open via holes H**1**, H**2**, . . . , H(n-**1**), Hn are the same. The open via holes H**1**, H**2**, . . . , H(n-**1**), Hn may be filled with conductive materials C**1**, C**2**, . . . C(n-**1**), Cn. It is preferable that the conductive materials C**1**, C**2**, . . . , C(n-**1**), Cn are the same.

[**0036**] In **FIG. 8**, it is preferable that the open via holes H**1**, H**2**, . . . , H(n-**1**), Hn are arranged in the longitudinal direction. Also, intervals among the open via holes H**1**, H**2**, . . . , H(n-**1**), Hn may be the same or different.

[**0037**] Referring to **FIG. 9**, an interdielectric layer **82** is divided into first and second regions **82***a* and **82***b*. M linear open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m of the first region **82***a* are in the longitudinal direction. L linear open via holes H**31**, H**32**, . . . , H**3**(**1**-**1**), H**31** of the second region **82***b* are arranged in the latitudinal direction. It is preferable that lengths of the open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m arranged in the first region **82***a* are the same. The widths M**1**, M**2**, . . . , M(m-**1**), Mm of the open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m of the first region **82***a* may be different. Preferably, intervals among the open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m of the first region **82***a* are the same.

[**0038**] M open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m arranged on the first region **82***a* are filled with conductive materials C**21**, C**22**,. . . , C**2**(m-**1**), C**2**m. Open via holes H**31**, H**32**, . . . , H**3**(**1**-**1**), H**31** of the second region **82***b* are also filled with conductive materials. Reference numerals L**1**, L**2**, . . . , L(**1**-**1**), L**1** of the second region **82***b* denote widths of the open via holes H**31**, H**32**, . . . , H**3**(**1**-**1**), H**31**, respectively. Also, reference numerals C**31**, C**32**,. . . , C**3**(**1**-**1**), C**31** denote conductive materials filling the open via holes H**31**, H**32**, . . . , H**3**(**1**-**1**), H**31** of the second region **82***b*, respectively.

[**0039**] Preferably, the conductive materials C**21**, C**22**, . . . , C**2**(m-**1**), C**2**m filling the open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m arranged on the first region **82***a* and the conductive materials C**31**, C**32**,. . . , C**3**(**1**-**1**), C**31** filling the open via holes H**31**, H**32**, . . . , H, H**3**(**1**-**1**), H**31** arranged on the second region **82***b* are the same. Also, the lengths of the open via holes H**21**, H**22**, . . . , H**2**(m-**1**), H**2**m arranged on the first region **82***a* may be different from those of the open via holes H**31**, H**32**, . . . , H**3**(**1**-**1**), H**31** arranged on the second region **82***b*.

[**0040**] Referring to **FIG. 10**, first through third open via holes serially arranged in the latitudinal direction and having a predetermined length in the longitudinal direction are formed in the center of an interdielectric layer **84**. The lengths of the first through third open via holes h**11**, h**12** and h**13** are preferably the same. The widths s**11**, s**12** and s**13** of the first through third open via holes h**11**, h**12** and h**13** also preferably are the same. The first through third open via holes h**11**, h**12** and h**13** are filled with conductive materials **86***a*, **86***b* and **86***c*. Fourth and fifth open via holes h**14** and h**15** are arranged in the right upper portion of the interdielectric layer **84**. Each of the fourth and fifth open via holes h**14** and h**15** includes horizontal and vertical components, where the horizontal components of the fourth and fifth open via holes h**14** and h**15** are parallel with each other and the vertical components thereof are parallel with each other. The widths s**14** and s**15** of the fourth and fifth open via holes h**14** and h**15** preferably are the same. In another embodiment, the widths of the horizontal and vertical components of the fourth and fifth open via holes h**14** and h**15** may be different from each other.

[**0041**] Sixth and seventh open via holes h**16** and h**17** are arranged in the left lower portion of the interdielectric layer **84**. The sixth and seventh open via holes h**16** and h**17** preferably have the same structure as the fourth and fifth open via holes h**14** and h**15** except that longitudinal components may differ. It is preferable that the widths **s11**, . . . , **s17** of the first through seventh open via holes **h11**, . . . , **h17** are the same.

[**0042**] In **FIG. 10**, reference numerals **86***d*, **86***e*, **86***f* and **86***g* denote conductive materials filling the fourth through seventh open via holes h**14**, h**15**, h**16** and h**17**, respectively.

[**0043**] Referring to **FIG. 11, a** plurality of open via holes, for example first through fifth open via holes h**18**, h**19**, h**20**, h**21** and h**22** serially and diagonally arranged in an interdielectric layer **88**. The widths s**18**, s**19**, s**20**, s**21** and s**22** and lengths La, Lb, Lc, Ld and Le of the first through fifth open via holes h**18**, h**19**, h**20**, h**21** and h**22** preferably are the same. However, other embodiments may have different widths and lengths. The first through fifth open via holes h**18**, h**19**, h**20**, h**21** and h**22** are arranged in the diagonal direction. The characteristics of the first through fifth open via holes h**18**, h**19**, h**20**, h**21** and h**22** may differ. The widths of the first through fifth open via holes h**18**, h**19**, h**20**, h**21** and h**22** are preferably the same. However, the widths also may be different from each other.

[**0044**] **FIGS. 12 and 13** is plan views presenting embodiments in which open via holes of different forms exist together.

[**0045**] Referring to **FIG. 12, a** plurality of open via holes, for example first through third linear open via holes h**23**, h**24**, and h**25** having a predetermined latitudinal length are arranged parallel with each other in the center of the interdielectric layer **92**. The horizontal widths s**26**, s**27** and s**28** of the first through third open via holes h**23**, h**24** and h**25** preferably are the same. Also, intervals among the first through third open via holes h**23**, h**24** and h**25** preferably are also the same. The first through third open via holes h**23**, h**24** and h**25** are filled with conductive materials **94***b*, **94***c* and **94***d*. A fourth open via hole h**26**, having a predetermined width, surrounding the first through third open via holes h**22**, h**23**, h**24** and h**25** is also formed in an interdielectric layer **92**.

[**0046**] The fourth open via hole h**26** includes a longitudinal component and two latitudinal components connected to both ends of the longitudinal component. As a result, the fourth open via hole h**26** is positioned independently from the first through third open via holes h**23**, h**24** and h**25**. The fourth open via hole h**26** is filled with a conductive material **94***a*. The latitudinal and longitudinal widths s**23**, s**24** and s**25** of the fourth open via hole h**26** are the same. Also, it is preferable that the widths of the first through third open via holes h**23**, h**24** and h**25** are equivalent to that of the fourth open via hole h**26**.

[**0047**] Referring to **FIG. 13**, first and second open via holes h**27** and h**28** are symmetrically provided in a predetermined region of an interdielectric layer **96**. The first and second open via holes h**27** and h**28** have a bent point, respectively. The widths s**29** and s**30** of the first and second open via holes h**27** and h**28** preferably are the same. However, the widths s**29** and s**30** of the first and second open via holes h**27** and h**28** may be different from each other. The first and second open via holes h**27** and h**28** are filled with conductive materials **98***a* and **98***b*.

[**0048**] The third and fourth open via holes h**29** and h**30** having a predetermined latitudinal length, are arranged under the first and second open via holes h**27** and h**28** of the interdielectric layer **96**. The third and fourth open via holes h**29** and h**30** are arranged independently from the first and second open via holes h**27** and h**28**. The widths s**31** and s**32** and lengths of the third and fourth open via holes h**29** and h**30** preferably are the same. In other embodiments, the widths s**31** and s**32** of the third and fourth open via holes h**29** and h**30** may be different from each other.

[**0049**] The third and fourth open via holes h**29** and h**30** which are shown parallel with each other, may also have a predetermined angle therebetween. Also, the third and fourth open via holes h**29** and h**30** may be arranged in the longitudinal or diagonal direction. The position of the first and second open via holes h**27** and h**28** may be changed to that of the third and fourth open via holes h**29** and h**30**. The third and fourth open via holes h**29** and h**30** are filled with conductive materials **98***c* and **98***d*.

[**0050**] **FIG. 14** is a plan view illustrating an embodiment in which a closed via hole and an open via hole exist together. Referring to **FIG. 14**, an interdielectric layer pattern **110***a* is formed in an interdielectric layer **100**. A closed via hole h**31** of a predetermined width s**33** surrounding the interdielectric layer pattern **100***a* is positioned between the interdielectric layer **100** and the interdielectric layer pattern **100***a*. The width s**33** of the closed via hole h**31** preferably is uniform. However, in other embodiments, the width s**31** of the closed via hole h**31** may be different. The closed via hole h**31** is filled with a conductive material **102***a* contacting conductive layer patterns formed on and under the interdielectric layer **100**.

[**0051**] Also, the first and second open via holes h**32** and h**33** are formed in the interdielectric layer pattern **100***a*. The first and second open via holes h**32** and h**33** extend latitudinally, and have predetermined widths s**34** and s**35** in the longitudinal direction. The first and second open via holes h**32** and h**33** may extend latitudinally within the interdielectric layer pattern **100***a*. The lengths of the first and second open via holes h**32** and h**33** preferably are the same. It is also preferable that the widths s**34** and s**35** of the first and second open via holes h**32** and h**33** are the same. The first and second open via holes h**32** and h**33** are filled with conductive materials **104***a* and **104***b*.

[**0052**] In other embodiments, the first and second open via holes h**32** and h**33** extend latitudinally and parallel with each other arranged in the interdielectric layer pattern **100***a*. Also, the first and second open via holes h**32** and h**33** may be arranged in the diagonal direction of the interdielectric layer pattern **100***a*. In this case, the lengths of the first and second open via holes h**32** and h**33** preferably are different from each other. Also, the positions of the closed via hole h**31** and the first and second open via holes h**32** and h**33** may be changed relative to each other. That is, the first and second open via holes h**32** and h**33** may be positioned outside the closed via hole h**31**.

[**0053**] Referring to **FIG. 15**, an interdielectric layer pattern **106***a* is formed in an interdielectric layer **106**. A closed via hole h**34** surrounding the interdielectric layer pattern **106***a* and having a predetermined width s**36**, is disposed between the interdielectric layer **106** and the interdielectric layer pattern **106***a*. The width s**36** of the closed via hole h**34** preferably is uniform. The closed via hole h**34** is filled with a conductive material **108***a* contacting a conductive layer pattern formed on and under the interdielectric layer **106**.

[0054] First through fourth open via holes h35, h36, h37 and h38 are formed in the interdielectric layer pattern 106*a*. The first through fourth via holes h35, h36, h37 and h38 are square. The first through fourth open via holes h35, h36, h37 and h38 formed in the interdielectric layer pattern 106*a* also are arranged in the form of a square. The first through fourth open via holes h35, h36, h37 and h38 preferably are spaced apart from each other by the same interval in the latitudinal or longitudinal direction. The first through fourth open via holes h35, h36, h37 and h38 may be arranged in an arbitrary form instead of the form of a square. In other embodiments, the latitudinal and longitudinal widths s37 and s38 of the first through fourth open via holes h35, h36, h37 and h38 may be different. The first through fourth open via holes h35, h36, h37 and h38 preferably are filled with the same conductive materials 110*a*, 110*b*, 110*c* and 110*d*.

[0055] The positions of the first through fourth open via holes h35, h36, h37 and h38 may be changed relative to that of the closed via hole h34. That is, the first through fourth open via holes h35, h36, h37 and h38 may be formed in the interdielectric layer 106 outside the closed via hole h34.

[0056] **FIG. 16** is a plan view presenting an embodiment according to the present invention in which various closed and open via holes exist together in a interdielectric layer. Referring to **FIG. 16, a** first interdielectric layer pattern 112*a* is formed in an interdielectric layer 112. The shape of the first interdielectric layer pattern 112*a* is a rectangle, preferably a square. A first closed via hole h39 having a predetermined width s39 along the first interdielectric layer pattern 112*a* is disposed between the first interdielectric layer pattern 112*a* and the interdielectric layer 112. The interdielectric layer 112 and the first interdielectric layer pattern 112*a* are separated from each other by the width of the first closed via hole h39.

[0057] The width of the first closed via hole h39 preferably is uniform. The first closed via hole h39 is filled with a conductive material 114. A second interdielectric layer pattern 112*b* is formed in the first interdielectric layer pattern 112*a*. The second interdielectric layer pattern 112*b* preferably is circular. Also, a second closed via hole h41 of a predetermined width s41 is between the first interdielectric layer pattern 112*a* and the second interdielectric layer pattern 112*b*. The second interdielectric layer pattern 112*b* is separated from the first interdielectric layer pattern 112*a* by the width s41 the second closed via hole h41. A width s41 of the second closed via hole h41 along the second interdielectric layer pattern 112*b* preferably is uniform.

[0058] The second closed via hole h41 is filled with a conductive material 114*b*. It is referable that the conductive material 114*b* is the same as the conductive material 114 filling the first closed via hole h39.

[0059] A third interdielectric layer pattern 112*c* is formed in the second interdielectric layer pattern 112*b*. The shape of the third interdielectric layer pattern 112*c* is a triangle. A third closed via hole h42 of a predetermined width s42 surrounds the closed surface of the third interdielectric layer pattern 112*c*. The third interdielectric layer pattern 112*c* is separated from the second interdielectric layer pattern 112*b* by the width s42 of the third closed via hole h42. The width s42 of the third closed via hole h42 preferably is uniform along the closed surface of the third interdielectric layer pattern 112*c* like the first and second closed via holes h39 and h41. However, the width h42s of the third closed via hole h42 may be nonuniformly wide or narrow. It is preferable that the widths s39, s41, and s42 of the first through third closed via holes h39, h41 and h42 are the same.

[0060] The third closed via hole h42 is filled with a conductive material 114*c*. It is preferable that the conductive material 114*c* is the same as the conductive materials 114 and 114*b* filling the first and second closed via holes h39 and h41.

[0061] Four fourth open via holes h40 exist between the first closed via hole h39 and the second closed via hole h41. The form of the fourth open via hole 40 is a circle. The fourth open via holes h40 are arranged in the form of a square. It is preferable that the diameters of the fourth open via hole h40 are the same. In other embodiments, the fourth open via holes h40 may be arranged in a form different from a square. The form of the fourth open via holes h40 may be different from a circle, for example, a rectangle, ellipse or a line.

[0062] An open via hole may be formed in the second interdielectric layer pattern 112*b* between the second closed via hole h41 and the third closed via hole h42. Also, fifth and sixth closed or open via holes may be provided in the third interdielectric layer pattern 112*c*. The fourth open via hole h40 is filled with a conductive material 114*a*.

[0063] As described above, an interdielectric layer shown in **FIGS. 3 through 16** may be used for any of the interdielectric layers between the conductive layer patterns forming the multilayer pad. Thus, the interdielectric layer shown in FIGS. 3 through 16 may be the second and/or third interdielectric layers between the first through third conductive layer patterns composing the multilayer pad of **FIG. 1**.

[0064] For instance, the second interdielectric layer 44*a* between the first and second conductive layer patterns 43*a* and 46*a* of **FIG. 2** may be selected from the interdielectric layers shown in **FIGS. 3 through 16**, and the third interdielectric layer 48*a* existing between the second and third conductive layer patterns 46*a* and 50*a* of **FIG. 2** may be the interdielectric layer shown in **FIG. 14**. The second and third interdielectric layers 44*a* and 48*a* may be selected from the interdielectric layers of **FIGS. 3 through 16**. Also, there may be modifications to the embodiments shown in **FIG. 3** through 16. For instance, the closed via holes h7 and h8 intersecting with each other of **FIG. 6** may be elliptical or one of them may be elliptical.

[0065] A method of manufacturing an integrated circuit having a multilayer pad according to the first embodiment of the present invention will be described.

[0066] **FIG. 17** shows the step of forming a first conductive layer pattern on a substrate. In detail, a first interdielectric layer 118 is formed on a semiconductor substrate 116. Semiconductor devices such as transistors and capacitors and a conductive interconnections such as bit lines or gate lines are formed between the first interdielectric layer 118 and the semiconductor substrate 116. A first conductive layer is formed on the first interdielectric layer 118. A photosensitive layer (photoresist) is coated on the first conductive layer, and then the first conductive layer is patterned through a photolithography process. As a result, a photosensitive layer pattern defining a predetermined region of the first conductive layer is formed on the first conductive layer. The entire surface of the first conductive layer is anisotropically etched using the photosensitive layer pattern as a mask until a surface of the first interdielectric layer **118** is exposed. As a result, the first conductive layer pattern **120***a* is formed on the first interdielectric layer **118**.

[**0067**] **FIG. 18** shows the step of forming a second conductive layer pattern **124***a*. In detail, the photosensitive layer pattern is removed, and then a second interdielectric layer **122***a* is formed on the entire surface of the first interdielectric layer **118** and on the first conductive layer pattern **120***a*. A photosensitive layer is coated on the second interdielectric layer **122***a*, and a photosensitive layer pattern exposing a portion covering the first conductive layer pattern **120***a* of the second interdielectric layer **122***a* is formed on the second dielectric layer **122***a*. A closed or open via hole is formed on the exposed region of the second interdielectric layer **122***a*. The photosensitive layer is patterned according to the form of the via hole to be formed on the second interdielectric layer **122***a*, to thereby define a closed or open exposed region exposing the second interdielectric layer **122***a*.

[**0068**] The second interdielectric layer **122***a* is anisotropically etched using the photosensitive layer pattern as a mask until a surface of the first conductive layer pattern **120***a* is exposed. The photosensitive layer pattern is removed, and a first closed via hole **123** and a second interdielectric layer pattern **122***b* having a closed circumference surrounded by the first closed via hole **123** are formed on the second interdielectric layer **122***a*. The photosensitive layer may be patterned in various patterns, so that a multitude of closed or open via holes may be formed outside the first closed via hole **123** of the second interdielectric layer **122***a*. The open via hole may be shaped in the form of a line or curve. Additional closed via holes may be formed on the second interdielectric layer **122***a* and the second interdielectric layer pattern **122***b*. At this time, the additional closed via holes may be elliptical or polygonal.

[**0069**] A second conductive layer pattern **124***a* filling the first closed via hole **123** is formed on the second interdielectric layer **122***a*. The second conductive layer pattern **124***a* is formed parallel to the second interdielectric layer **122***a*. Thus, there preferably is no step between the center of the second conductive layer pattern **124***a* and the edge thereof. It is preferable that the first and second conductive layer patterns **120***a* and **124***a* are formed of the same conductive material. It is also preferable that the thicknesses of the first and second conductive layer patterns **120** and **124***a* are the same.

[**0070**] **FIG. 19** shows the step of forming a third interdielectric layer **126***a* including a second closed via hole **128**. In detail, a third interdielectric layer **126***a* is formed on the entire surface of the second interdielectric layer **122***a* and on the second conductive layer pattern **124***a*. A photosensitive layer pattern exposing a portion covering the second conductive layer pattern **124***a* of the third interdielectric layer **126***a* is formed on the third interdielectric layer **126***a*. The photosensitive layer pattern preferably is formed such that the exposed portion of third interdielectric layer **126***a* becomes a closed path. Other closed or open exposed regions may be formed in the photosensitive layer pattern.

[**0071**] The third interdielectric layer **126***a* is anisotropically etched using the photosensitive layer pattern as a mask until the second conductive layer pattern **124***a* is exposed. The photosensitive layer pattern is removed, the second closed via hole **128** and the third interdielectric layer pattern **126***b* surrounded by the second closed via hole **128** are formed on the third interdielectric layer **126***a*. The second closed via hole **128** may be shaped in various forms like the first closed via hole **123**.

[**0072**] If necessary, other closed or open via holes may be further formed on the third interdielectric layer **126***a*. It is preferable that via holes of the same form are shaped in the second and third interdielectric layers **122***a* and **126***a*. However, via holes having other shapes may be used. The first and second closed via holes **123** and **128** may be formed according to the same pattern.

[**0073**] **FIG. 20** shows the step of forming a pad window **134**. In detail, a third conductive layer pattern **130***a* filling the second closed via hole **128** is formed on the third interdielectric layer **126***a*. The third conductive layer pattern **130***a* is connected to the second conductive layer pattern **124***a* through the second closed via hole **128**. It is preferable that the third conductive layer pattern **130***a* is formed of the same conductive material as the first or second conductive layer pattern **120***a* or **124***a*. It is also preferable that the third conductive layer pattern **130***a* has the same thickness as the first or second conductive layer pattern **120***a* or **124***a*.

[**0074**] As shown in **FIGS. 20 and 1**, it is preferable that the first through third conductive layer patterns **120***a*, **124***a* and **130***a* are formed of the same thickness. Also preferably, the first and second closed via holes **123** and **128** and other open and closed via holes are filled with a conductive plug such as a tungsten plug, and then the second and third conductive layer patterns **124***a* and **130***s* may be formed on the resultant structure.

[**0075**] Subsequently, an upper insulating layer **132***a* is formed on the entire surface of the entire surface of the third conductive layer pattern **130***a*. A photosensitive layer pattern exposing a portion covering the third conductive layer pattern **130***a* of the upper insulating layer **132***a* is formed on the upper insulating layer **132***a*. The entire surface of the exposed upper insulating layer **132***a* is anisotropically etched using the photosensitive layer pattern as an etching mask until the third conductive layer pattern **130***a* is exposed. Then, the photosensitive layer pattern is removed, the pad window exposing the surface of the third conductive layer pattern **130***a* is formed in the upper insulating layer **132***a*.

[**0076**] The pad window **134** becomes a bonding area of a multilayer pad comprising the first through third conductive layer patterns **120***a*, **124***a*, **130***a*. It is preferable that the pad window **134** is formed wide enough to reduce contact resistance of the pad window **134** within a range of the third conductive layer pattern **130***a*. An interdielectric layer and a conductive layer pattern can be formed before forming the pad window **134**. If necessary, the pad window **134** may be formed in the second conductive layer pattern **124***a* without forming the third conductive layer pattern **130***a*, to thereby reduce the thickness of the multilayer pad.

[**0077**] With reference to **FIG. 1**, the pad window **134** preferably is formed as a rectangle. However, the pad window **134** may be shaped in various forms, for example, the pad window **134** may be a polygon, a circle or an ellipse.

[0078] FIG. 21 is a sectional view of a semiconductor device having a multilayer pad according to a second embodiment of the present invention. In detail, a first interdielectric layer **142** and a first conductive layer pattern **144** are in sequence formed on a semiconductor substrate **140**. A second interdielectric layer **146***a* including a first via hole **148** is formed on the first conductive layer pattern **144**. The first via hole **148** is a closed or open via hole. A second conductive layer pattern **150** filling the first via hole **148** exists on the second interdielectric layer **146***a*. A third interdielectric layer **152** having a second via hole **154** exists on the second conductive layer pattern **150**. The second via hole **154** is a single open via hole. A third conductive layer pattern **156***a* connected to the second conductive layer pattern **150** through the second via hole **154** exists on the third interdielectric layer **152**.

[0079] As described above, in a semiconductor device having a multilayer pad according to the second embodiment of the present invention, a closed via hole exists in one of the interdielectric layers between the first through third conductive layer patterns **144**, **150** and **156***a*, and an open via hole exists in another interdielectric layer.

[0080] According to the present invention, a bonding pad is composed of multilayer conductive layer patterns, and an interdielectric layer having a closed via hole exists between the multilayer conductive layer patterns. Also, an interdielectric layer pattern having a closed circumference surrounded by the closed via hole exists in the same plane as the interdielectric layer. The conductive layer patterns and the interdielectric layers are parallel with each other, so that there is little or no step between the center and the edge of the conductive layer pattern. Thus, reaction residues generated in the process of etching the interdielectric layer or the conductive layer can be prevented from being stacked between the conductive layer patterns. Alternatively, some reaction residues may be stacked, but the stacked residues can be easily removed during a cleaning process, to thereby lower the resistance of the bonding pad.

[0081] In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A bonding pad for an integrated circuit comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween; and

a closed conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns, the closed conductive pattern enclosing an inner portion of the dielectric layer, and being enclosed by an outer portion of the dielectric layer.

2. A bonding pad according to claim 1 wherein the closed conductive pattern is at least one of a circular, elliptical and polygonal conductive pattern.

3. A bonding pad according to claim 1 further comprising a second closed conductive pattern in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

4. A bonding pad according to claim 1 further comprising an open conductive pattern in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

5. A bonding pad according to claim 1 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns; and

a fourth conductive pattern in the dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

6. A bonding pad according to claim 5 wherein the fourth conductive pattern comprises a second closed conductive pattern in the second dielectric layer, electrically connecting the second and third spaced apart conductive patterns, the second closed conductive pattern enclosing a second inner portion of the second dielectric layer, and being enclosed by a second outer portion of the second dielectric layer.

7. A bonding pad according to claim 6 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

8. A bonding pad according to claim 6 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

9. A bonding pad for an integrated circuit comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween, the dielectric layer including a closed via therein that extends between the first and second spaced apart conductive patterns, the closed via enclosing an inner portion of the dielectric layer, and being enclosed by an outer portion of the dielectric layer; and

a closed conductive pattern in the closed via, electrically connecting the first and second spaced apart conductive patterns.

10. A bonding pad according to claim 9 wherein the closed conductive pattern fills the closed via.

11. A bonding pad according to claim 9 wherein the closed via is at least one of a circular, elliptical and polygonal via.

12. A bonding pad according to claim 9 further comprising a second closed via in the inner portion of the dielectric layer; and

a second closed conductive pattern in the second closed via, electrically connecting the first and second spaced apart conductive patterns.

13. A bonding pad according to claim 9 further comprising:

an open via in the inner portion of the dielectric layer; and

an open conductive pattern in the open via, electrically connecting the first and second spaced apart conductive patterns.

14. A bonding pad according to claim 9 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns, the second dielectric layer including a second via therein that extends between the second and third spaced apart conductive patterns; and

a fourth conductive pattern in the second via, electrically connecting the second and third spaced apart conductive patterns.

15. A bonding pad according to claim 14:

wherein the second via comprises a second closed via in the second dielectric layer that encloses an inner portion of the second dielectric layer, and is enclosed by a second outer portion of the second dielectric layer; and

wherein the fourth conductive pattern is a second closed conductive pattern in the second via.

16. A bonding pad according to claim 15 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

17. A bonding pad according to claim 15 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

18. An integrated circuit comprising:

an integrated circuit substrate; and

a bonding pad on the integrated circuit substrate, the bonding pad comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween, on the integrated circuit substrate; and

a closed conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

19. An integrated circuit according to claim 18 wherein the closed conductive pattern is at least one of a circular, elliptical and polygonal conductive pattern.

20. An integrated circuit according to claim 18 further comprising a second closed conductive pattern within the closed conductive pattern, electrically connecting the first and second spaced apart conductive patterns.

21. An integrated circuit according to claim 18 further comprising an open conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

22. An integrated circuit according to claim 18 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns; and

a fourth conductive pattern in the dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

23. An integrated circuit according to claim 22 wherein the fourth conductive pattern comprises a second closed conductive pattern in the second dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

24. An integrated circuit according to claim 23 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

25. An integrated circuit according to claim 23 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

26. An integrated circuit comprising:

an integrated circuit substrate; and

a bonding pad on the integrated circuit substrate, the bonding pad comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween on the integrated circuit substrate, the dielectric layer including a closed via therein that extends between the first and second spaced apart conductive patterns; and

a closed conductive pattern in the closed via, electrically connecting the first and second spaced apart conductive patterns.

27. An integrated circuit according to claim 26 wherein the closed conductive pattern fills the closed via.

28. An integrated circuit according to claim 26 wherein the closed via is at least one of a circular, elliptical and polygonal via.

29. An integrated circuit according to claim 26 further comprising:

a second closed via in the dielectric layer, within the closed via; and

a second closed conductive pattern in the second closed via, electrically connecting the first and second spaced apart conductive patterns.

30. An integrated circuit according to claim 26 further comprising an open via in the dielectric layer; and

an open conductive pattern in the open via, electrically connecting the first and second spaced apart conductive patterns.

31. An integrated circuit according to claim 26 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns, the second dielectric layer including a second via therein that extends between the second and third spaced apart conductive patterns; and

a fourth conductive pattern in the second via, electrically connecting the second and third spaced apart conductive patterns.

32. An integrated circuit according to claim 31:

wherein the second via comprises a second closed via in the second dielectric layer; and

wherein the fourth conductive pattern is a second closed conductive pattern in the second via.

33. An integrated circuit according to claim 32 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

34. An integrated circuit according to claim 32 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

35. A method of forming bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and

forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

36. A method according to claim 35 wherein the step of forming a conductive pattern comprises the step of forming a conductive pattern filling the closed via and on the dielectric layer opposite the substrate.

37. A method according to claim 35 wherein the steps of forming a dielectric layer and forming a conductive pattern are repeatedly performed to form a multilayer bonding pad on the integrated circuit substrate.

38. A method according to claim 35 wherein the closed via is at least one of a circular, elliptical and polygonal via.

39. A method according to claim 35:

wherein the step of forming a dielectric layer comprises the step of forming a dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein; and

wherein the step of forming a conductive pattern comprises the step of forming a conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

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