United States Patent [19]

Jamet et al.

[11] **3,810,098**

[45] **May 7, 1974**

[54] **EMITTER AND RECEIVER DEVICES FOR REMOTE CONTROL OF MINING MACHINES**

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[22] Filed: **Oct. 2, 1972**

[21] Appl. No.: **294,192**

[30] **Foreign Application Priority Data**

June 26, 1972 France 72.23059

[52] **U.S. Cl.** .... **340/170,** 178/66 R

[51] **Int. Cl.** **H04b 1/00,** H04q 9/00

[58] **Field of Search** .... 340/170, 167 R; 328/94; 325/37, 60; 178/66 R

[56] **References Cited**

UNITED STATES PATENTS

3,361,978	1/1968	Fiorini	328/94 X
3,577,187	5/1971	Benson	340/167 R
3,582,783	6/1971	Hendrickson	340/167 R
3,609,662	9/1971	Grimm	340/167 R X
3,619,503	11/1971	Ragsdale	178/66 R
3,443,229	5/1969	Becker	325/60
3,518,680	6/1970	McAuliffe	325/60 X

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[57] **ABSTRACT**

A transmitter device is provided which includes a serial encoder which transforms input control data into a series of binary signals which are subsequently coded into a second series of binary signals. An ascending transition between levels in the second series, e.g., a transition between a binary "zero" and a binary "one", represents one of the levels of the binary signals of the first series and a descending transition represents the other of the levels. The transmitter device also includes a modulator for modulating the signals of the second series with two distinct modulating frequencies.

10 Claims, 4 Drawing Figures

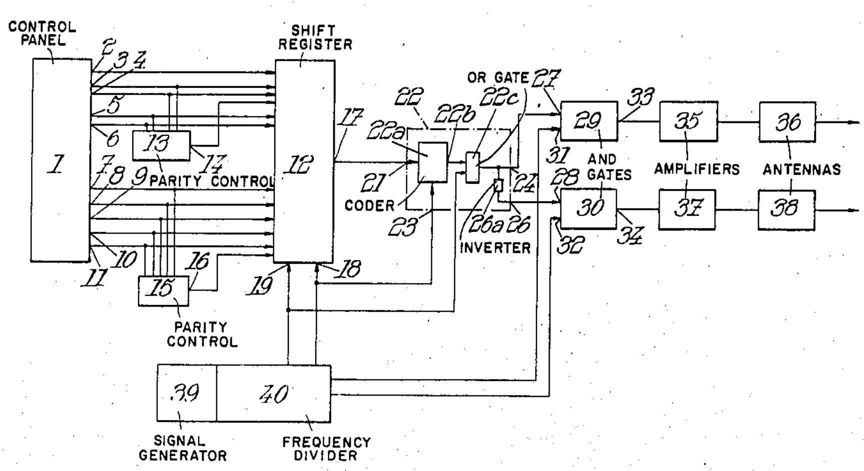
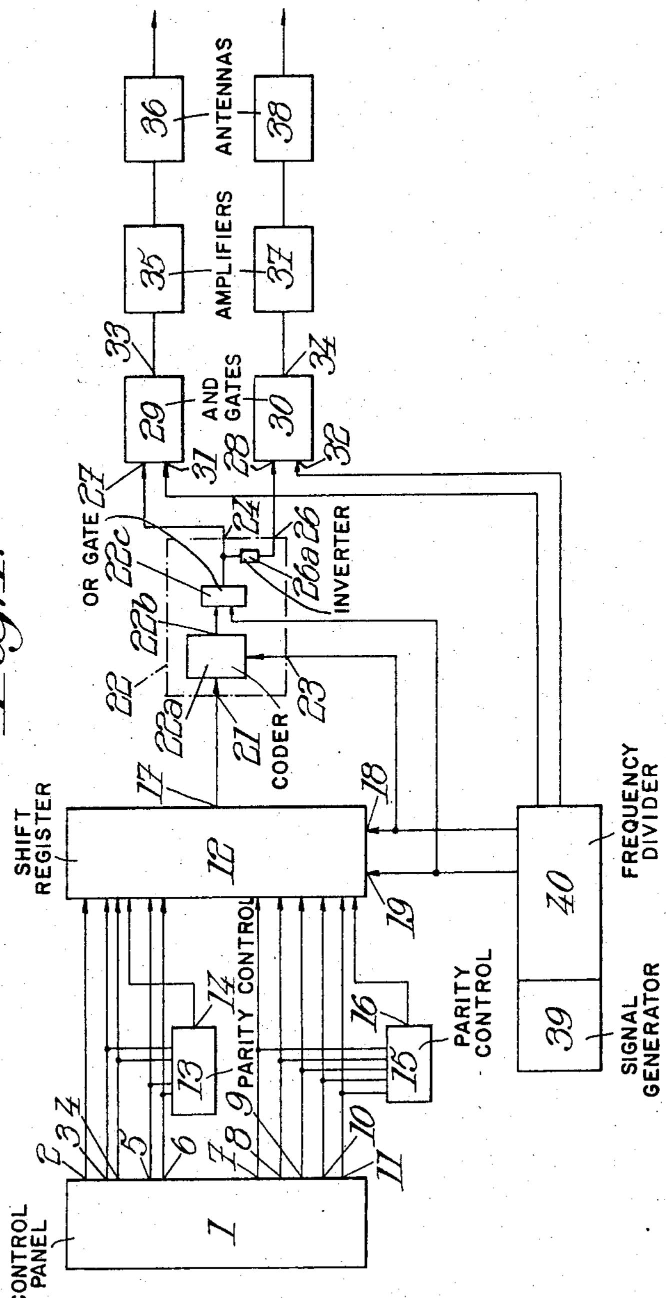


Fig.1.


CONTROL PANEL
SHIFT REGISTER
PARITY CONTROL
PARITY CONTROL
CODER
OR GATE
INVERTER
AND GATES
AMPLIFIERS
ANTENNAS
FREQUENCY DIVIDER
SIGNAL GENERATOR

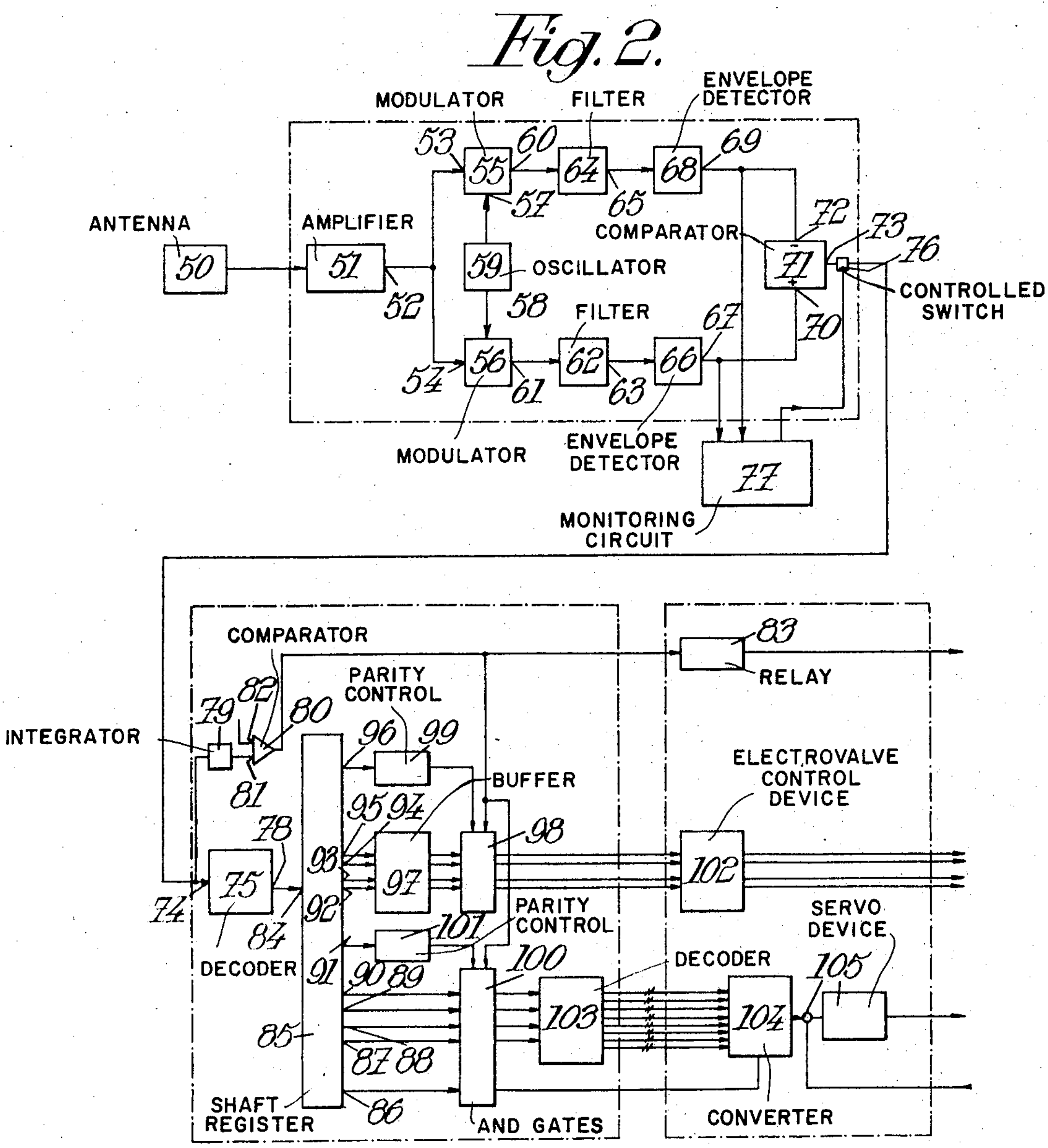


Fig. 2.
MODULATOR
FILTER
ENVELOPE DETECTOR
ANTENNA
AMPLIFIER
OSCILLATOR
COMPARATOR
CONTROLLED SWITCH
FILTER
MODULATOR
ENVELOPE DETECTOR
MONITORING CIRCUIT
COMPARATOR
PARITY CONTROL
INTEGRATOR
BUFFER
RELAY
ELECTROVALVE CONTROL DEVICE
PARITY CONTROL
SERVO DEVICE
DECODER
DECODER
SHAFT REGISTER
AND GATES
CONVERTER

Fig. 3.

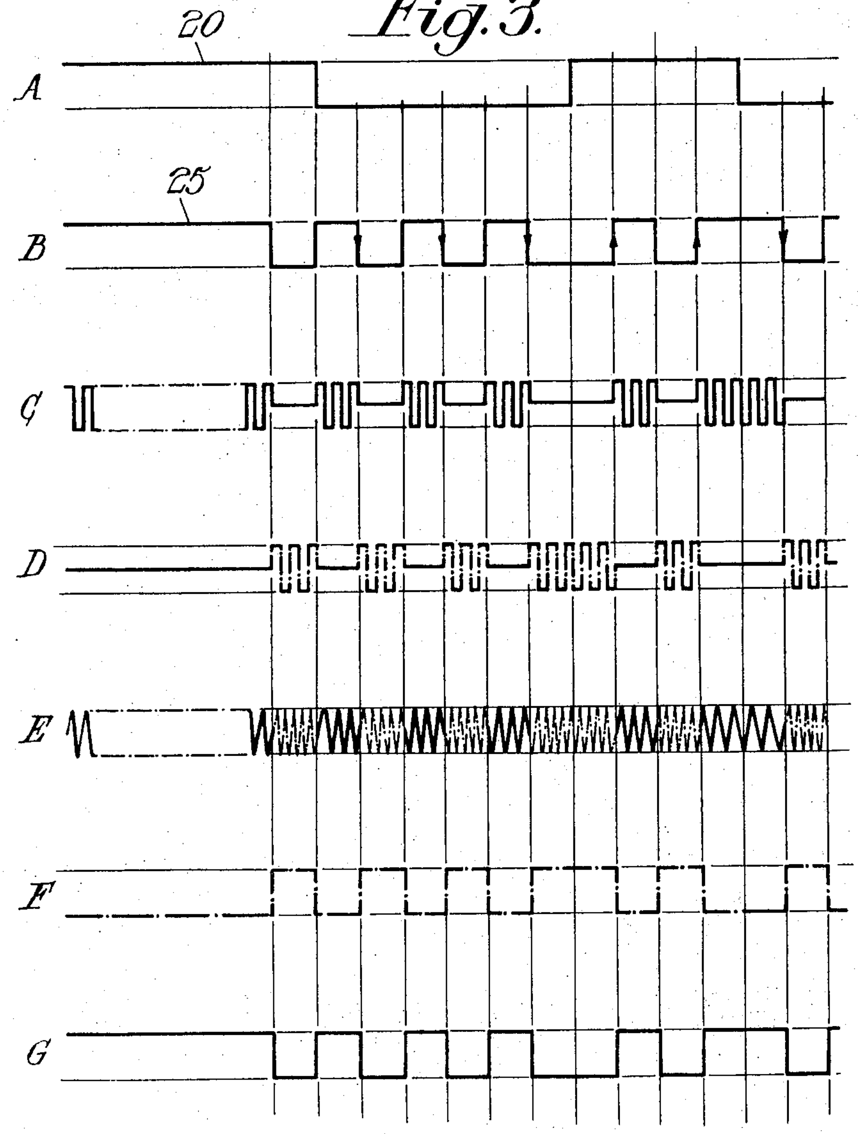
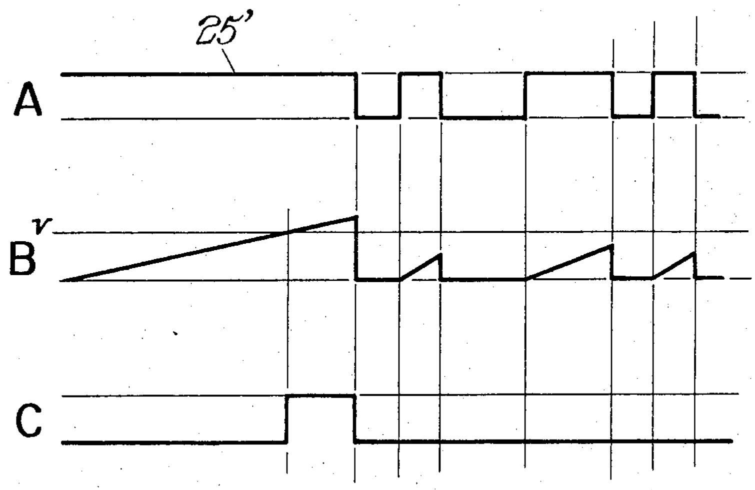


Fig. 4.



EMITTER AND RECEIVER DEVICES FOR REMOTE CONTROL OF MINING MACHINES

The invention relates to devices for transmitting operating control information, at a distance to a machine adapted to effect a predetermined number of operations. It relates particularly to a transmitter device, normally separate from the machine, and a receiver device, normally affixed to the machine, and adapted to receive the information transmitted by the emitter device.

The invention relates, more particularly, because it is in this case that its application seems to be most advantageous, but not exclusively, to those relating to remote control of extraction machines (such as mineral cutters) or transporting machines used in mines.

A first object of the invention is the construction of transmitter and receiver devices, for the remote control of machines of the above-mentioned type, which are simple and easy to construct.

A second object of the invention is the construction of such devices which enables transmission of information to the machine which is free of errors due to the presence of external interference.

A third object of the invention is to enable the production of transmitter and receiver devices which cause the stopping of the operation of the machine as soon as the transmitter device reaches a distance greater than a given distance from the receiver device installed on the machine.

The transmitter device of the present invention comprises, in combination, operator-controlled serial coding means for transforming control information into a first group of sequential binary signals of substantially equal duration, two-phase coding means, responsive to the output of said serial coding means, for transforming the first group of binary signals into a second group of binary signals wherein binary signals in the first group of a first level are transformed into signals which are characterized by an ascending transition between the two levels in the second group and binary signals of a second level in the first group are transformed into signals which are characterized by a descending transition between the two levels of the second group, modulator means for transforming, in sequence, all of the binary signals of the second group of a first level into a first periodic signal of a constant frequency f_1 having a period which is short as compared with the said duration of said binary signals and for transforming, in sequence, all of the signals of said second group of a second level into a second period signal of a constant frequency f_2 having a period which is short as compared with the said duration of said binary signals, and at least one antenna for transmitting said first and second periodic signals to the receiver device of the machine.

Preferably, the serial coding means comprises a control panel including a plurality of operator-controlled switch means, each of said switch means being associated with a respective output of the control panel so that binary signals representing the positions of the switch means associated therewith appear simultaneously at corresponding ones of said outputs, a parallel-in, serial-out shift register having a plurality of parallel inputs connected to the outputs of said control panel, synchronizing inputs, and a series output, oscillator means for providing a word synchronizing signal and a binary signal synchronizing signal at respective of

said synchronizing inputs of said shift register so that the binary signals of said first group all have the same duration and so that said first group is divided into words all containing the same number N of binary signals, each of said words comprising a speed control signal formed from a number n of successive binary signals of predetermined levels, the other binary signals of each word constituting said predetermined binary signals of said first group, said two-phase coding means including an input for receiving said binary signals synchronizing signal and providing that the second group of binary signals comprises second speed control signals of a duration substantially equal to of a duration substantially equal to that of the speed control signal of the first group.

The receiver device according to the invention is preferably used to receive signals transmitted by a transmitter device as described above and comprises, in combination, a antenna for detecting a first periodic signal of frequency f_1 and a second periodic signal of frequency f_2, first decoding means for transforming the first periodic signal into binary signals of a first level and the second periodic signal into binary signals of a second level, second decoding means, having an input connected to the output of the first decoding means, for transforming the group of binary signals applied to the input thereof into a fourth group of binary signals so that each ascending transition between the different levels of the two successive binary input signals corresponds to a binary signal of one level and each descending transition between the different levels of two successive binary input signals corresponds to a binary signal of the other level of said fourth group and third decoding means, having a series input and parallel output, for transforming the serial binary signals of the fourth group into a group of binary signals which simultaneously appear at the outputs of said third decoding means.

In a preferred embodiment of the receiver device, wherein the receiver is adapted to receive signals such that the fourth group of binary signals appearing at the output of the second decoding means of the receiver is divided into words composed of a same number N of binary signals, each of these words comprising a third speed signal of substantially constant duration, the second decoding means comprises first and second distinct outputs, said first output of said second decoding means delivering binary signals representative of the third speed signals and the second output of said second decoding means delivering the other binary signals of each word forming said fourth group, said third decoding means comprising a shift register with a serial input and parallel outputs, said serial input being connected to the second output of the second decoding means and the first output of the second decoding means controlling stopping of the operation of the machine when the said speed signal is absent.

Other features, advantages and characteristics of the invention will appear also in the course of the more detailed description of a preferred embodiment of the invention which follows and in which reference is made to the accompanying drawings in which:

FIG. 1 represents one embodiment of a transmitter device according to the invention;

FIG. 2 shows one embodiment of a receiver device according to the invention, and

FIGS. 3 and 4 are diagrams illustrating the operation of the devices shown in FIGS. 1 and 2, the axis of abscissae representing time in all these diagrams.

The type of application of the invention which will now be described relates to remote control of a mineral cutter (not shown).

This mineral cutter is driven by a hydraulic winch and its position is adjustable by means of two jacks which can confer, by their intervention, several positions (or inclinations) to the cutter. The hydraulic winch and the jacks have not been shown either in the drawings.

All the elements of the transmitter device which have been shown in FIG. 1 are enclosed in a case (not shown). Only the control switches (not shown) extend outside this case and these enable an operator to program, by the position of these switches, a certain number of operations that the cutter must execute; in the example shown, these operations are: arrest of the machine, lifting of the first jack, descent of the first jack, lifting of the second jack, descent of the second jack, direction of rotation and speed of rotation of the hydraulic winch of the machine. The control switches are two position switches or rotary contacts having a certain number of distinct positions. Panel 1 comprises at least one outer surface at the case on which are arranged said switches or contacters. On the outputs of these switches or contacters appear the signals or binary numbers whose value (0 or 1) depends on the position of the control switches. Each output or group of outputs of the control panel 1 corresponds therefore to a certain control signal to be transmitted to the machine. These outputs which have been, respectively, numbered 2, 3, 4, 5, 6, 7 and 8 to 11 thus correspond, in the order specified, to the aforementioned operations which machine must carry out.

Informations relating to the speed of rotation of the winch are hence represented by four binary numbers appearing at the outputs 8 to 11. The operator will hence be able to choose sixteen different speeds for this winch rotation. Each of the outputs 2 to 11 on the panel 1 is connected to a parallel input of a parallel-series shift register or memory 12 the storage capacity of which is sixteen bits (binary numbers). A first parity control device 13 comprises an output 14 connected also to a parallel input of the memory 12; the binary signal which appears at this output 14 is a control signal enabling checking of the compatibility between the lifting or the lowering orders of the jacks. Moreover, there is provided a second parity control device 15 comprising an output 16 connected to a parallel input of the memory 12 and which is capable of producing a binary signal whose value provides control information relative to the compatability between the speed control signals and the direction of rotation of the winch of the machine.

The shift register 12, known in itself, comprises a series output 17 at which there is made to appear in succession, in a predetermined order, the binary signals appearing at its parallel inputs. Said register 12 comprises two synchronising inputs 18 and 19. Rectangular wave signals of 250 Hz frequency are applied at the input 18. This bit synchronising signal fixes the frequency and the duration of appearance of the binary signals delivered at the output 17. A second rectangular wave signal is applied at the input 19; this signal is a word synchronising signal whose frequency is: (250/16) = 15.6 Hz and which enables delivery at said output 17 of the memory 12 of a speed signal composed in the example of three equal binary signals; this speed signal enables separation into "words" of the succession of binary signals appearing at the output 17 and which is representative of the binary signals applied at the parallel inputs of the register 12.

The group of binary signals which is delivered at the output 17 is shown in the diagram of FIG. 3A. In this diagram the line 20 represents the above-mentioned speed signal. Following the speed signal 20 appear successively, in a pre-set order, the binary signals representing, on one hand, positions of the control switches and, on the other hand, parity control signals.

The output 17 is connected to the input 21 of a two-phase coder 22 which comprises a second input 23 on which is applied the same bit synchronising signals as on the input 18 of the memory 12.

The two-phase coder 22 enables transformation of the group of binary signals applied at its input 21 and shown by FIG. 3A, into a second group of binary signals represented by the diagram of FIG. 3B and produced at an output 24 of this device. Comparison of the diagrams of FIGS. 3A and 3B shows, firstly, that there corresponds to a second speed signal 25 to the speed signal 20 of each word. In addition, correspondence between binary signals which are different from those which compose the speed signals 20 and 25, is a signal-transition correspondence which can be defined as follows:

in the middle of the duration of appearance of each binary signal of the diagram of FIG. 3A corresponds the transition between two binary signals of different values of FIG. 3B. More specifically, for a binary 0 (zero) of FIG. 3A (shown by the lower level on this diagram) is made to correspond a descending transition (from 1 to 0, or from high level to low level) and a binary 1 (one) of FIG. 3B (represented by the high level in this diagram) is made to correspond an ascending transition (from 0 to 1) in FIG. 3B.

This type of "signal-transition" coding has the advantage of associating a transition with each binary number and hence of avoiding the use of a clock signal at the receiver, the signal transmitted bearing itself its own synchronisation. It will be noted that, when a succession of binary signals of the same value appears at the input 21, the binary signals delivered at the output 24 have a frequency of appearance double of that (250 Hz) of the input signals; on the contrary, when two successive input signals have different values, the frequency of the output signals is the same as that of the input signals.

The coder 22 is, according to the invention, constructed in the following manner: it comprises, in the first place, a coder 22*a* known in itself, and comprising two inputs 21 and 23; this coder 22*a* delivers at its output 22*b* a group of binary signals corresponding to "transition" coding of all the binary signals of each word presented at the input 21. The coder 22 comprises, in the second place, an OR gate 22*c* with two inputs of which the first is connected to the output 22*b* and the second receives the speed signal 20. The output of this OR gate 22*c* is connected, on one hand, to the output 24 of the coder 22 and, on the other hand, to a second output 26 of said coder 22 by means of an inverter 26*a*.

There hence appears at this second output **26** a group of complementary binary signals (i.e., signals out of phase by 180°) from those appearing at the output **24.** In other words, to each binary 0 appearing at the output **24,** there corresponds a binary 1 appearing at the output **26** and conversely.

The outputs **24** and **26** of the coder **22** are connected, respectively, to the first inputs **27** and **28** of AND gates, **29** and **30** respectively. There is applied to the second input **31** of the AND gate **29** square wave signals of frequency $f_1 = 20$ kHz and there is applied to the second input **32** of the AND gate **30** square wave signals of frequency $f_2 = 21.3$ kHz.

It is seen in FIG. 3C that, when a binary "one" appears at the output **24** of the coder **22,** the AND gate **29** transmits to its output **33** square wave signals of a frequency $f_1 = 20$ kHz. On the other hand, when a binary "zero" appears at the output **24,** AND gate **29** does not transmit the said signal of frequency f_1 and a signal of constant level at the output **33;** however, in this case, when a binary one appears at the output **26** of coder **22** the AND gate **30** enables the transmission to its output **34** of square wave signals of frequency f_2. The condition of the output **34** is represented by diagram shown in FIG. 3C. It is seen in this latter diagram that, as in the case of the output **33,** the signal appearing at the output **34** has a constant level when the output **26** delivers a binary "zero." The pulse trains of frequency f_2 have been shown in mixed chain and solid lines in FIG. 3D in order to differentiate them from the pulse trains of frequency f_1 which are shown in full lines in FIG. 3C.

It will be noted that the AND gates **29** and **30** are, in fact, modulators since each of them enables the transformation of a binary signal of a given level into a periodic signal having a predetermined frequency.

The signals produced at the output **33** of the AND gate **29** are amplified by means of a first amplifier **35** and the so-amplified signals are applied to a first antenna **36.** In the example, the first amplifier **35** is constituted by a frequency multiplier amplifier, the frequency multiplying coefficient of this amplifier being three; the antenna **36** radiates therefore signals whose frequency is 60 kHz; these signals are only, of course, emitted when binary "ones" appear at the output **24** of the coder **22.**

In the same way, the signals produced at the output **34** of the AND gate **30** are amplified by means of a second amplifier **37** and these signals so amplified are delivered to a second antenna **38.** As previously, the amplifier **37** is constituted by a frequency multiplying amplifier whose frequency multiplier coefficient is equal to three. The antenna **38** radiates therefore a signal whose frequency is equal to 64 kHz when binary signals of value 1 appear at the output **26** of the coder **22.**

In the embodiment shown, the various square signals are provided by a signal generator **39** delivering signals of frequency 640 kHz to frequency divider means **40** comprising four outputs. The first of these outputs provides a signal whose frequency is 15.6 Hz; the duration of each pulse of this signal is equal to the duration of the pulse **20** (3 bits); this first output is connected to the input **19** of the register **12** and to the second input of the OR gate **22***c*. The second of these outputs delivers a signal of frequency 250 Hz and is connected, on one hand, to the input **18** of the register **12** and, on the other hand, to the input **23** of the coder **22.** The third of these outputs delivers a frequency signal $f_1 = 20$ kHz and is hence connected to the second input **31** of the AND gate **29.** The fourth output delivers a square wave signal of frequency $f_2 = 21.3$ kHz and is therefore connected to the second input **32** of the AND gate **30.**

It should be noted that it is not indispensible to arrange two antennae to radiate signals of frequency **60** and 64 kHz, a single antenna being sufficient to transmit these signals. Thus, in a modification (not shown), the outputs of the AND gates **29** and **30** are each connected to an input of an OR gate and it is the output of this OR gate which supplies, if necessary through an amplifier, a single antenna.

The antennae **36** and **38** are advantageously constituted in such a way that they radiate a magnetic field whose amplitude diminishes rapidly with its distance from these antennae. These transmitter antennae are for example constituted by simple frames. It can also be constituted by a metallic wire winding on a ferrite core as described in French patent No. 1,522,272 filed 7 Feb. 1967 for "Device for Remote Control by Alternating or Pulsating Magnetic Field".

It will be appreciated with this arrangement, the receiver device installed on the machine no longer receives signals coming from the transmitter device carried by an operator when this operator is at a distance greater than a predetermined length (for example 15 metres). The receiver device can then be arranged in such a way that, when its antenna does not receive a signal, a stopping of the operation of the machine is triggered. In this way, the cutter can only operate when the operator who carries the transmitter device can supervise it to avoid any accident as regards personnel or material.

There will now be described, with reference to FIG. **2,** a preferred embodiment of the receiver device which is adapted to be installed on the cutter. This receiver device contained in a flame-protecting case of steel and fixed in front of the winch (not shown), on the chassis of the cutter.

As already indicated, and as shown in FIG. **2,** the receiver device comprises an antenna **50** adapted to detect periodic signals of frequency 60 kHz and 64 kHz; this antenna **50** will hence preferably be tuned to the frequency of 62 kHz. It can advantageously constitute a metallic wire coil wound on a ferrite core as described in the above-said French Pat. No. 1,522,272. The signals detected by the antenna **50** are applied to the input of an amplifier **51.**

This amplifier **51** has a wide band-pass centered, preferably, at the frequency of 62 kHz. Moreover, said amplifier is of the peak limiter type so that the signals that it delivers to the output **52** all have the same amplitude.

Said signals which appear at the output **52** of the amplifier **51** have been shown in the diagram of FIG. 3E. It is seen in this diagram that the signals are composed of successive alternate sinusoidal wave trains; the signals represented in full lines have the frequency 60 kHz and those represented in broken or chain lines have the frequency 64 kHz.

The output **52** is connected to the first inputs **53** and **54** of frequency modulator circuits, **55** and **56** respectively. As applied to the second inputs **57** and **58** of the frequency modulator circuits **55** and **56** respectively, a periodic signal, advantageously sinusoidal, whose frequency is 68 kHz. This signal of frequency 68 kHz is generated, in the example, by an oscillator **59**.

The frequency changing circuits **55** and **56**, known in themselves, are of the type which deliver at their outputs, **60** and **61** respectively, a signal with several components. Among these components figures that which has the frequency which is the difference between those of the signals applied to its two inputs. In other words, there appears on the outputs **60** and **61** signals whose frequency is 68 − 64 = 4 kHz and 68 − 60 = 8 kHz.

The signal produced at the output **61** of the circuit **56** is filtered by a band-pass filter **62**; the band-pass of this filter **62** is centered around 8 kHz and is sufficiently narrow to remove signals of frequency 4 kHz. There hence only appears signals at the output **63** of the filter **62** when the antenna **50** receives signals whose frequency is 60 kHz.

The output **60** of the circuit **55** is connected to the input of a filter **64** of which the band-pass is centered around the frequency 4 kHz and is sufficiently narrow to eliminate entirely the frequency 8 kHz. There also appears therefore a signal at the output **65** of the filter **64** only when the antenna **50** detects a signal whose frequency is 64 kHz.

An envelope detector circuit **66** enables transformation of the periodic signals of frequency 8 kHz, produced at the output **63** of the filter **62**, into their envelopes. There is hence obtained at the output **67** of the circuit **66** a continuous signal having a non-zero value when the antenna **50** detects a signal of which the frequency is 60 kHz, that is to say when the binary signals represented in the diagram of FIG. 3B have the value **1**. Said signal provided at the output **67** of circuit **66** is represented in full lines in the diagram of FIG. 3G.

In the same way, the signals produced at the output **65** of the filter **64** are applied at the input of an envelope detector circuit **68** whose output **69** delivers a signal which is the envelope of that provided at its input. The signal appearing at the output **69** is represented in broken lines in the diagram of FIG. 3F. It is seen that there appears at the output **69** a continuous signal of non-zero level when the antenna **50** detects a periodic signal of frequency 64 kHz, that is to say when the binary signals represented in the diagram of FIG. 3B have the value 0.

The output **67** of the circuit **66** is connected to the positive input **70** of a comparator **71**. In the same way, the output **69** of the circuit **68** is connected to the negative input **72** of said comparator **71**. This comparator **71** which is, for example, a differential amplifier, delivers at its output **73** a continuous signal of a first level when the amplitude of the signal which appears at its positive input **70** is greater than the amplitude of the signal which appears at its negative input **72**; there appears a continuous signal of a given second level, different from the first, in the opposite case, that is to say when the signal which appears at the input **70** has a lower amplitude than that of the signal which appears at the input **72**. The signals which will thus be generated at the output **73** will be similar to those which are shown in the diagram of FIG. 3G.

The comparator **71** hence enables the forming of signals delivered at the outputs **67** and **69** of the envelope detector circuits **66** and **68**. The comparator **71** thus restores binary signals substantially identical to those which are represented in the diagram of FIG. 3B.

It is to be noted here that the choice of the two signals of different frequencies f_1 and f_2 to modulate, respectively, the 0 and the 1 of the signals to be transmitted enables a transmission to be obtained scarcely sensitive to interference. In fact, interference detected by the antenna **50** will weaken or strengthen, generally in the same proportions, the signals presented at the inputs **70** and **72** of the comparator **71**.

In a modification (not shown), only a single frequency changing circuit is provided, the circuit **55** for example, and the inputs of the filters **62** and **64** are both connected to the output **60** of the circuit **55**.

In the embodiment of the receiver device shown in FIG. **2**, the output **73** of the comparator **71** is connected to the input **74** of a decoder **75** by means of a controlled switch **76**. This controlled switch **76** provides a control input which, according to the value of the signal which is applied to it, will or will not allow interruption of the connection between the output **73** and the input **74**. The control of the switch **76** is effected by a reception monitoring circuit **77**. This circuit **77** comprises two inputs, the first being connected to the output **67** of the circuit **66**, the second of these inputs being connected to the output **69** of the circuit **68**. The circuit **77** enables cut-off of the connection between the points **73** and **74** when the levels of the signals applied at its inputs have too high or, too low values or again, where the amplitudes are distinctly different in average value.

The role of the decoder **75** is to transform the signals such as represented in the diagram of FIG. 3B into binary signals such as represented in the diagram of FIG. 3A. It hence plays an inverse role to that played by the coder **22** of the transmitter device represented in FIG. **1**. In other words, to an ascending transition between a 0 and a 1 of the binary signals presented at the input **74**, there is made to correspond, at the output **78** of this decoder **75**, a binary signal of value 1; similarly, a descending transition between a 1 and a 0 of the binary signals at the input **74** corresponds a binary signal of value 0 at the output **78**.

According to a feature of the invention, the absence of the speed signal **25'** (shown in the diagram FIG. **4A**) in the assembly of binary signals appearing at the output **73** of the comparator **71** is used to control the stopping of operation of the cutter. For this purpose there is used an integrator **79** and a second comparator **80**. The input of the integrator **79** is connected to the output **73** of the comparator **71** through the controlled switch **76**; the output of this integrator **79** is connected to the first input **81** of the comparator **80**. The second input **82** of said comparator **80** receives a signal of constant level *v*. The output of the comparator **80** is connected to the control input of a relay **83**. This relay **83** is constructed in such a way that it enables actuation of the arrest of operation of the cutter when it does not receive a signal at its control input during the length of a word.

The diagrams of FIGS. **3A** to **3C** illustrate the operation of the integrator **79** and of the comparator **80**. The diagram B' represents the assembly of binary signals which appear at the output **73** of the comparator **71**. The diagram of FIG. 3B represents the signal obtained at the output of the integrator **79**; it is seen in this diagram that at each succeeding binary "one" in the signal represented in the diagram of FIG. **3A** corresponds to a ramp or saw-tooth signal represented in the diagram of FIG. 3B. The maximum value (final) of each of these saw-teeth is dependent on the duration of the corresponding binary "one" so that the greater the duration the greater the maximum value. The value v of the level of the signal presented at the input **82** of the comparator **80** is selected in such a way that it is greater than the maximum value of the saw-tooth which corresponds to the longest of the sequential binary "ones", different from the speed signal **25'**, in the group of signals represented in the diagram of FIG. 4A; moreover, this value v is selected so that it is less than the maximum value of the saw-tooth of the diagram of FIG. 4B which corresponds to said signal **25'**. The comparator **80** being arranged in such a way that it only produces a signal at its output if the value of a signal presented at its input **81** exceeds the value of the signal presented at its input **82,** this output signal then represents the presence of the speed signal **25'** and its absence, during the length of a word, can thus be used to cause the stopping of the operation of the cutter.

The output **78** of the decoder **75** is connected to the series input **84** of a shift register **85** with a series input and parallel outputs. This shift register **85** has a storage capacity at least equal to sixteen bits; however, the three parallel outputs of this register on which appear the binary signals corresponding to the speed signal **25'** are not used, this signal being already utilized by relay **83.** At the output **86** of the register **85** appears the binary signal representing the direction of rotation of the winch; at the outputs **87** to **90** appear the binary signals representing the speed of rotation selected for the winch; at the output **91** appears the binary signal representing the compatability between the speed and the direction of rotation of the winch; at the outputs **92** to **95** appear the binary signals which represent the lifting or lowering information of the jacks; at the output **96,** lastly, appears the binary signal indicating the compatability between the orders of lifting and of lowering of said jacks.

According to a further feature of the invention, certain of the control information is only transmitted to the cutter if they remain identical with themselves during a limited and pre-set time t. In the embodiment shown, there is selected for said time t, that which corresponds to the length of four words; in other words, an information of control is only transmitted to the cutter if it has remained identical with itself during four successive words, that is to say for about 0.26 second.

This feature enables further improvement of the quality, and hence of the safety, of the transmission between the emitter device and the cutter. In fact, if interference should disturb the transmission during the length of a word, this interference being capable of falsifying the control orders transmitted to the outputs of the register **85,** the erroneous control signals will not then be cited upon by the machine.

In the embodiment shown, this feature is applied to information relative to the lifting and lowering of the jacks. Each binary signal presented at the outputs **92** to **95** is transmitted to control circuits of the cutter through a buffer circuit effecting the abovesaid function. The buffer circuit have been shown in FIG. **2** by a single block **97.**

A circuit **98** comprising, for example, four AND gates with three inputs enables the transmission to the control circuits of the cutter of the signals produced at the outputs of the buffer members, represented by the

block **97,** if, in the course of each word, the output of the comparator **80** produces a signal and if the binary signal produced at the output **96,** and converted by a parity control device **99,** indicates that there is compatability between the jack lifting and lowering orders.

In the same way, a member **100** composed, for example, itself also, of five AND gates with three inputs enables the transmission to the corresponding control circuits of the cutter of the binary signals appearing at the outputs **86** to **90** of the register **85** if, on one hand, in the course of each word, a signal is produced at the output of the comparator **80** and if, on the other hand, in the course of each word, the binary signal produced at the output **91,** and converted by a parity control device **101,** indicates that there is compatability between the information relative to the speed and to the sense of rotation of the winch.

The outputs of the member **98** are applied to the inputs of an electrovalve control device **102** whose outputs control directly the jacks of the cutter.

A decoder **103** enables transformation of the binary signals representing the desired speed for the winch of the cutter in sixteen signals each of which represents a speed of the said winch.

Of course, the signals produced at the output of the device **103** are utilized by a digital-to-analog converter **104** which delivers a positive or negative signal, according to the value of the binary signal appearing at the output **86** of the register **85,** and this signal, produced at the output of the converter **104,** is utilized by speed servo devices **105.**

The operation of the transmitter and receiver devices which have just been described is sufficiently clear from the foregoing so that it is unnecessary to dwell further on this subject. It will be noted however, always for an operation providing maximum safety for the personnel, that the starting of the cutter is effected manually, whilst the stopping can be remote controlled.

The transmitter and receiver devices which have just been described are advantageously used for controlling, with a limited range, mine working machines, especially coal mining.

As is self-evident and as is already evident from the foregoing, the invention is in no way limited to the types of applications described, nor to those embodiments of its various parts, which have been more especially considered; it encompasses, on the contrary, all modifications.

We claim:

1. A transmitter device for transmitting control information, at a distance, to a machine which is adapted to effect a predetermined number of operations in a mine, the transmitter device being remote from the machine and the machine including a receiver device associated therewith for receiving the control information transmitted by the transmitter device, said transmitter device comprising operator-controlled serial coding means for transforming control information into a first group of sequential binary signals of substantially equal duration, two-phase coding means, responsive to the output of said serial coding means, for transforming the first group of binary signals into a second group of binary signals wherein binary signals in the first group of a first level are transformed into signals which are characterized by an ascending transition between the two levels in the second group and binary signals of a second level in the first group are transformed into signals

which are characterized by a descending transition between the two levels of the second group, modulator means for transforming, in sequence, all of the binary signals of the second group of a first level into a first periodic signal of a constant frequency f_1 having a period which is short as compared with the said duration of said binary signals and for transforming, in sequence, all of the signals of said second group of a second level into a second periodic signal of a constant frequency f_2 having a period which is short as compared with the said duration of said binary signals, and at least one antenna for transmitting said first and second periodic signals to the receiver device of the machine.

2. A transmitter device according to claim 1 wherein said serial coding means comprises a control panel including a plurality of operator-controlled switch means, each of said switch means being associated with a respective output of the control panel so that binary signals representing the positions of the switch means associated therewith appear simultaneously at corresponding ones of said outputs, a parallel-in, serial-out shift register having a plurality of parallel inputs connected to the outputs of said control panel, synchronizing inputs, and a series output, oscillator means for providing a word synchronizing signal and a binary signals synchronizing signal at respective of said synchronizing inputs of said shift register so that the binary signals of said first group all have the same duration and so that said first group is divided into words all containing the same number N of binary signals, each of said words comprising a speed control signal formed from a number n of successive binary signals of predetermined levels, the other binary signals of each word constituting said predetermined binary signals of said first group, said two-phase coding means including an input for receiving said binary signals synchronizing signal, and providing that the second group of binary signals comprises second speed control signals of a duration substantially equal to that of said speed control signals of the first group.

3. A transmitter device according to claim 2 wherein said two-phase coding means comprises transition coding means, having an input which constitutes the input of said two-phase coding means, for transforming the first group of binary signals into a further group of binary signals wherein the binary signals of said first group of a first level correspond to a descending transition between the two levels of the binary signals of the further group and the binary signals of said first group of a second level correspond to an ascending transition between the two levels of the binary signals of said further group, an OR gate having first and second inputs, said first input of said OR gate being connected to the output of said transition coding means and said second input of said OR gate receiving a signal whose frequency corresponds to the frequency of appearance of said words, and which is formed from a number n of successive binary signals of the same level, the output of said OR gate constituting the output of said two-phase coding means.

4. A transmitter device according to claim 1 wherein said two-phase coding means comprises first and second outputs, said first output delivering the second group of binary signals and said second output delivering a third group of binary signals identical to the second group of binary signals but of opposite phase, said modulator means comprising a first modulator, having an input connected to the first output of the two-phase coding means, for delivering at the output thereof, responsive to binary signals of the second group of a first level, said first periodic signal of frequency f_1 and, responsive to binary signals of the second group of a second level, a signal of constant level, and a second modulator, having one input connected to the second output of the two-phase coding means, for delivering at the output thereof, responsive to signals of the first group of a first level corresponding to a second level of the second group, said second periodic signal of frequency f_2, and responsive to the binary signals of the third group of a second level corresponding to the first level of the second group, a constant level signal.

5. A transmitter as claimed in claim 4 wherein said at least one antenna comprises a first antenna for transmitting a signal representative of the first periodic signal and a second antenna for transmitting a signal representative of the second periodic signal.

6. A transmitter device according to claim 1 wherein said at least one antenna is arranged so that the periodic signal radiated thereby has a negligible amplitude beyond a given distance from said antenna.

7. In combination with a transmitter device according to claim 1, a receiver device comprising an antenna for detecting a first periodic signal of frequency f_1 and a second periodic signal of frequency f_2, first decoding means for transforming the first periodic signal into binary signals of a first level and said second periodic signal into binary signals of a second level, second decoding means, having an input connected to an output of the first decoding means, for transforming the group of binary signals applied to the input thereof into a fourth group of binary signals so that each ascending transition between the different levels of two successive binary signals corresponds to a binary signal of one level and each descending transition between different levels of the two successive binary input signals corresponds to a binary signal of the other level of said fourth group and third decoding means, having a series input and parallel outputs, for transforming the serial binary signals of the fourth group into a group of binary signals which simultaneously appear at the outputs of said third decoding means.

8. The combination claimed in claim 7 wherein said first decoding means further comprises at least one oscillator for providing at the output thereof a third periodic signal of constant frequency f_3, at least one frequency modulator having a first input connected to the output of said oscillator and a second input for receiving signals detected by said receiver antenna, said frequency modulator producing at the output thereof fourth and fifth periodic signal, the frequency of the fourth periodic signal being the difference $f_3 - f_1$ between the frequencies of the third and first periodic signals, and the frequency of the fifth periodic signal being the difference $f_3 - f_2$ between the frequencies of the third and second periodic signals, a first bandpass filter, having an input connected to the output of said frequency modulator, for delivering at the output thereof only the fourth periodic signal, a second bandpass filter, having an input connected to the output of said frequency modulator, for delivering at the output thereof only the fifth periodic signal, a first envelope detector means having an input connected to the output of said first bandpass filter, a second envelope detector means having an input connected to the output

of said second bandpass filter, and a comparator having first and second inputs, the first input of said comparator being connected to the output of said first envelope detector means and the second input of said comparator being connected to the output of said second envelope detector means, the output of said comparator constituting the output of said first decoding means and the signal appearing at said output of said comparator being a binary signal which is of a first level when the level of the signal appearing at the first input of said comparator is greater than that appearing at the second input thereof and is of a second level when the level of the signal appearing at the second input of said comparator is greater than that appearing at the first input thereof.

9. The combination according to claim **8** wherein said serial coding means of said transmitter device comprises a control panel including a plurality of operator-controlled switch means, each of said switch means being associated with a respective output of the control panel so that binary signals representing the positions of the switch means associated therewith appear simultaneously at corresponding ones of said outputs, a parallel-in, serial-out shift register having a plurality of parallel inputs connected to the outputs of said control panel, synchronizing inputs, and a series output, oscillator means for providing a word synchronizing signal and a binary signal synchronizing signal at respective of said synchronizing inputs of said shift register so that the binary signals of said first group all have the same duration and so that said first group is divided into words all containing the same number N of binary signals, each of said words comprising a speed control signal formed from a number *n* of successive binary signals of predetermined levels, the other binary signals of each word constituting said predetermined binary signals of said first group, said two-phase coding means including an input for receiving said binary signals synchronizing signal and providing that the second group of binary signals comprises second speed control signals of a duration substantially equal to that of said speed control signals of the first group, the transmitter signals being such that the fourth group of binary signals appearing at the output of the second decoding means of the receiver device is divided into words composed of a same number N of binary signals, each of said words comprising a third speed signal of substantially constant duration, said second decoding means comprising first and second distinct outputs, said first output of said second decoding means delivering binary signals representative of the third speed signals and the second output of said second decoding means delivering the other binary signals of each word forming said fourth group, said third decoding means comprising a shift register with a serial input and parallel outputs, the said serial input being connected to the second output of said second decoding means, and the first output of said second decoding means controlling stopping of the operation of the machine when said speed control signal is absent.

10. The combination as claimed in claim **8** wherein said receiver further comprises at least one safety buffer circuit having an input connected to the output of the third decoding means, for delivering at the output thereof, the binary signal at the input thereof only if said binary signal remains unchanged during a preset time period *t*.

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