

[54] **SELECTING APPARATUS AND METHOD FOR PHONOGRAPH**
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[22] Filed: **Sept. 11, 1970**
[21] Appl. No.: **71,501**

Related U.S. Application Data

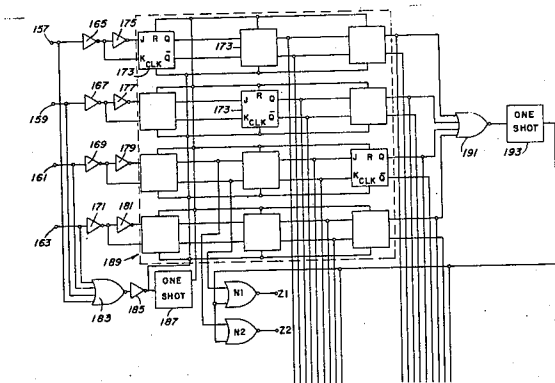
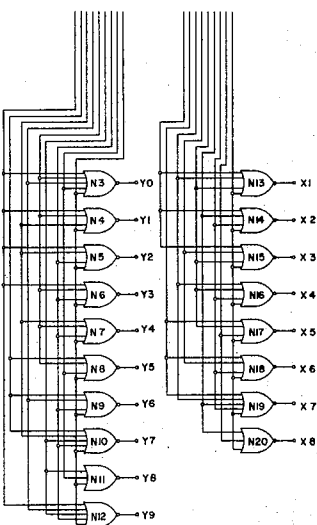
[63] Continuation-in-part of Ser. No. 862,624, Sept. 11, 1969, abandoned.
[52] U.S. Cl.....**340/162, 194/15**
[51] Int. Cl.....**G11b 19/08, G07f 11/00**
[58] Field of Search.....**340/162, 168, 164, 152; 194/10, 15; 178/2, 17, 17.5**

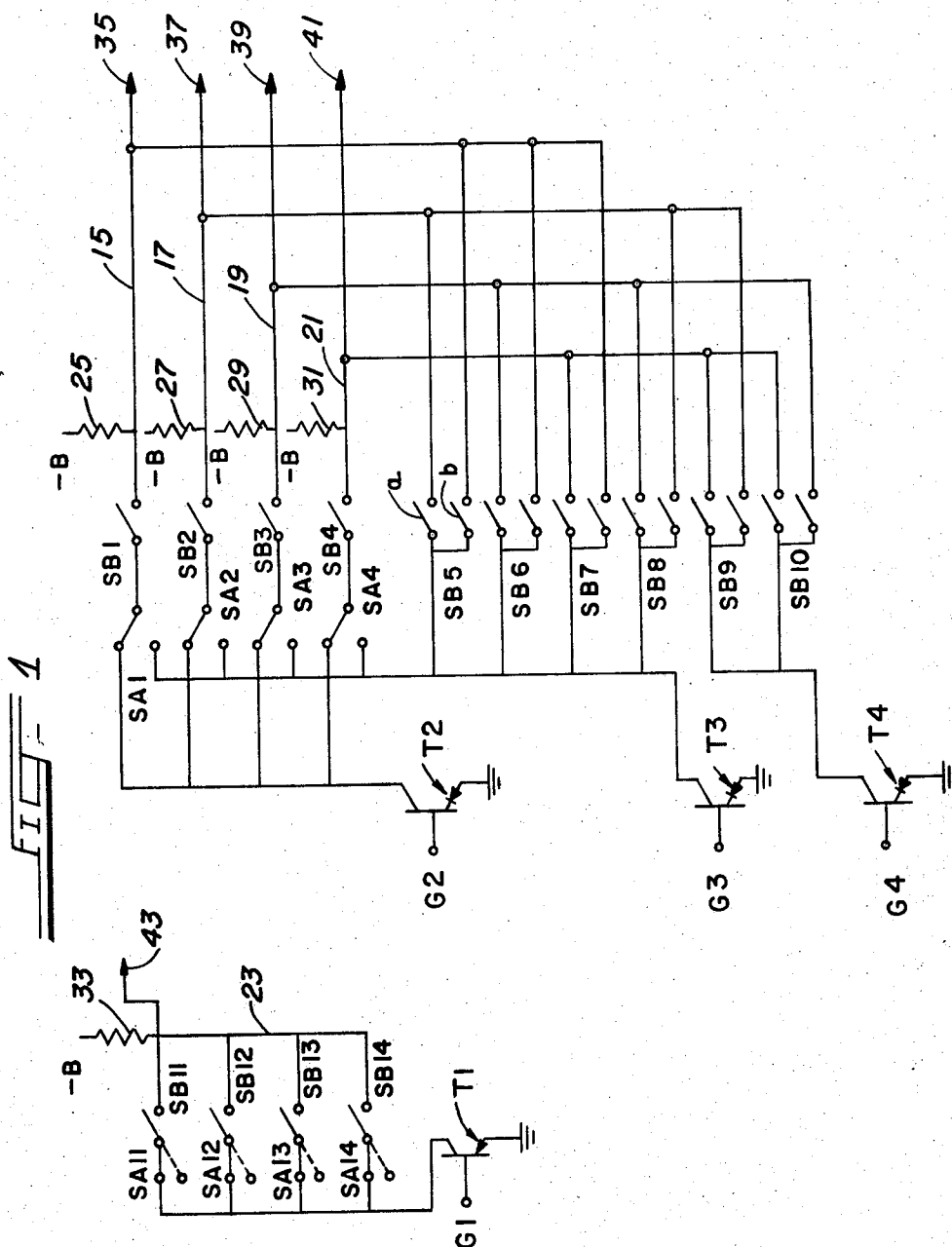
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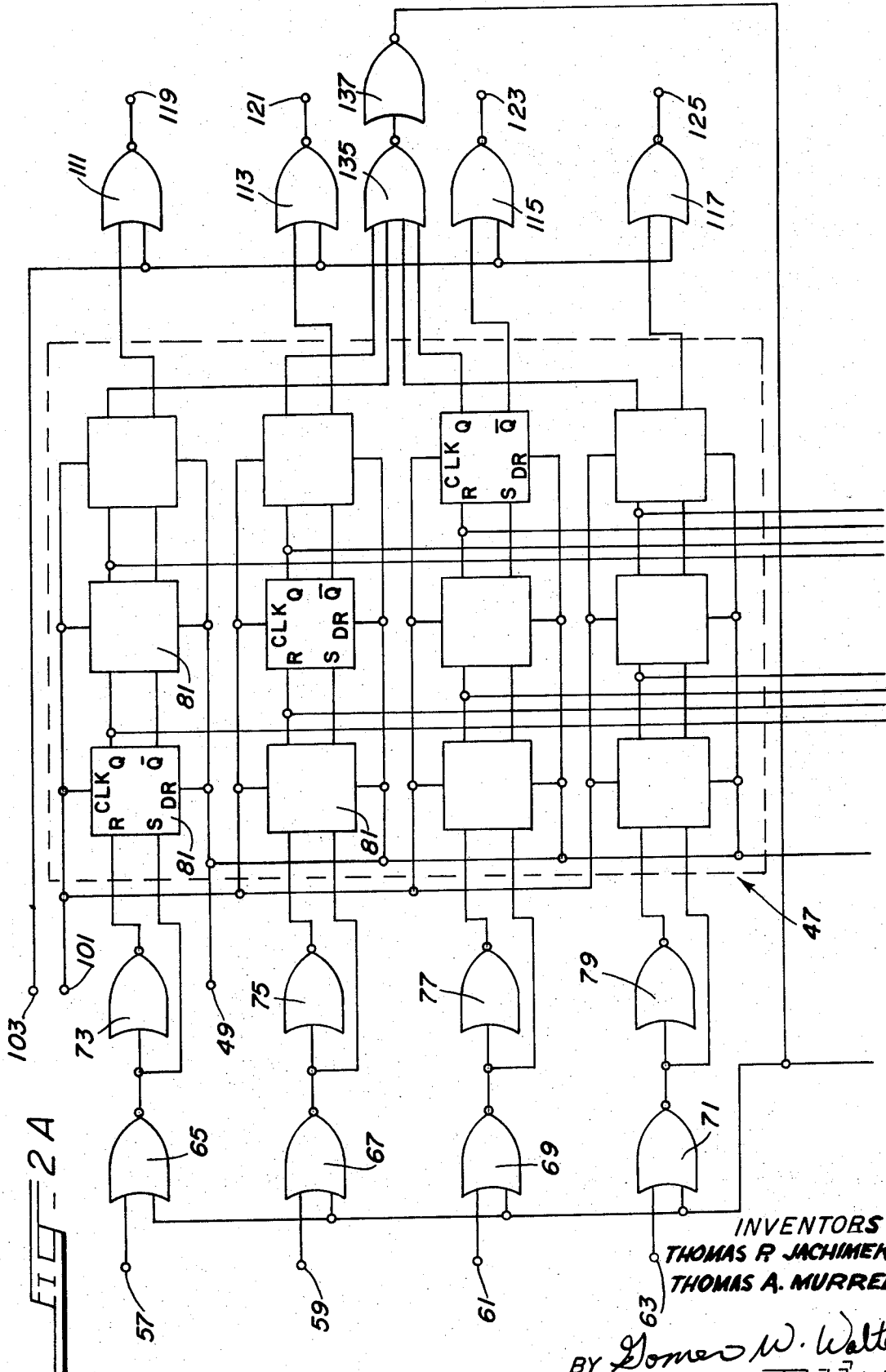
[57] **ABSTRACT**
Vending selections are identified by a character format. Selections are chosen by sequentially actuating switches representing the characters. The characters of the selection identifying format are coded and stored until the entire format has been coded and stored, at which time the coded format is transmitted for subsequent reception, storage and decoding. Integrated circuitry is utilized.

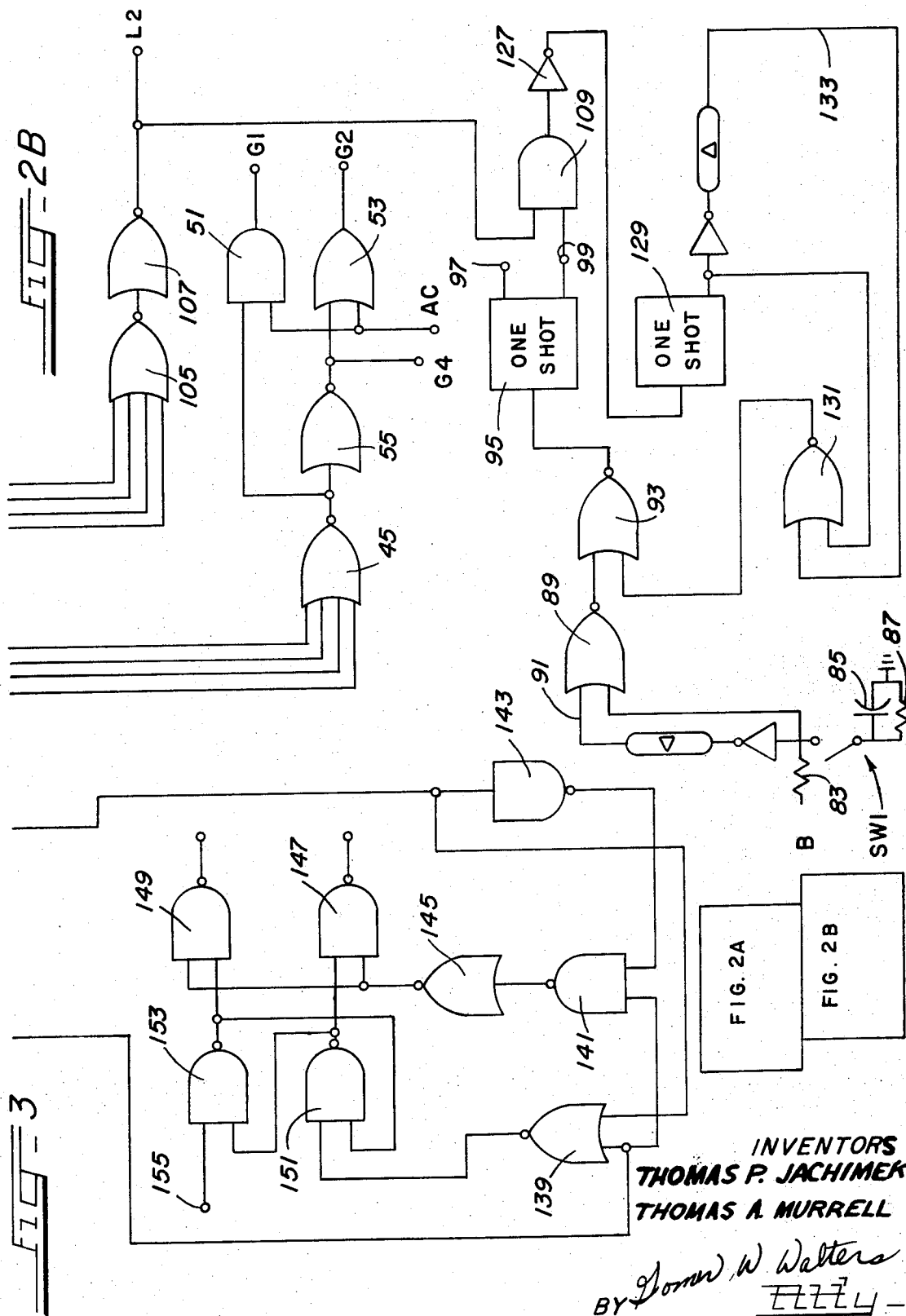
10 Claims, 42 Drawing Figures





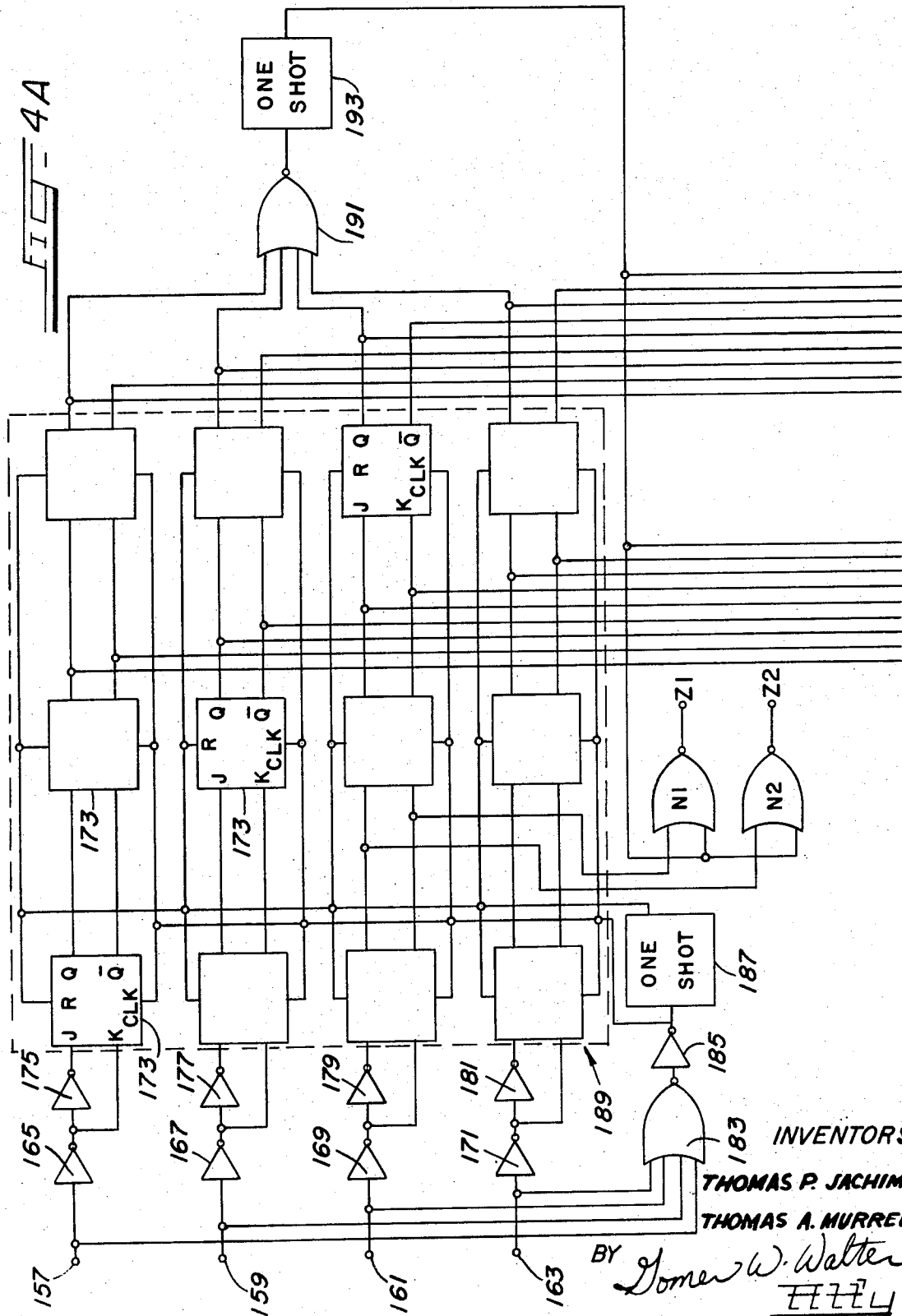
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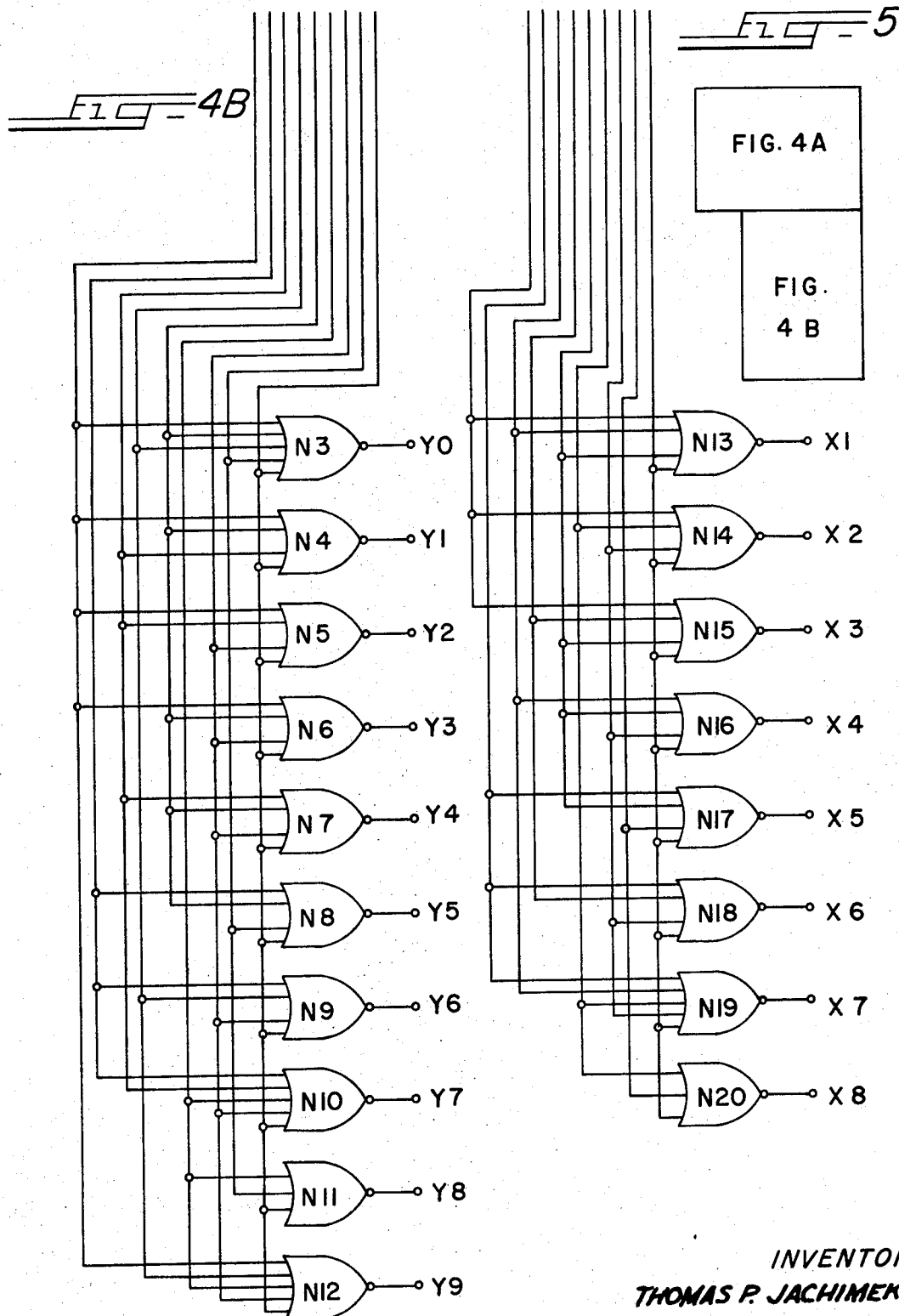
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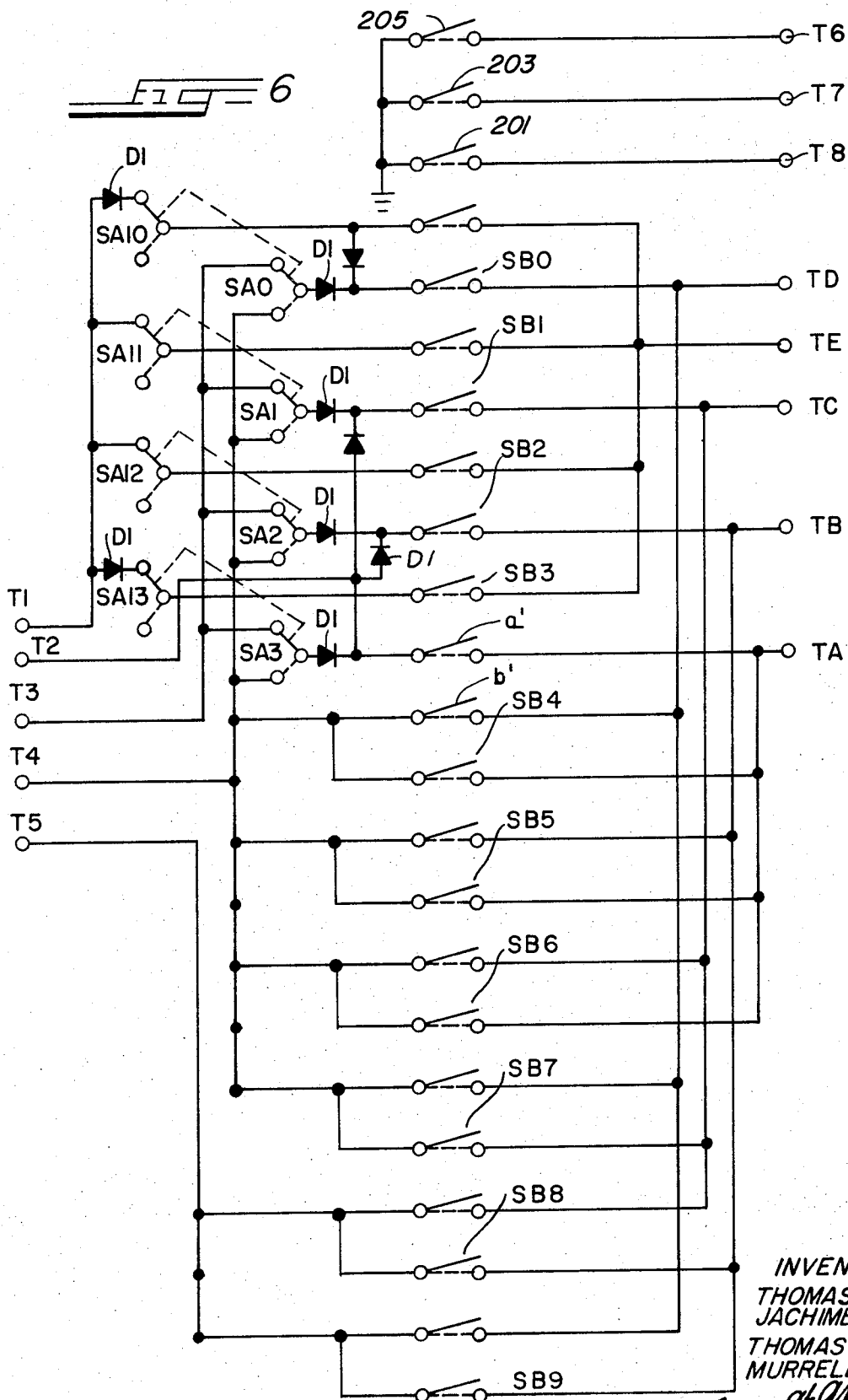


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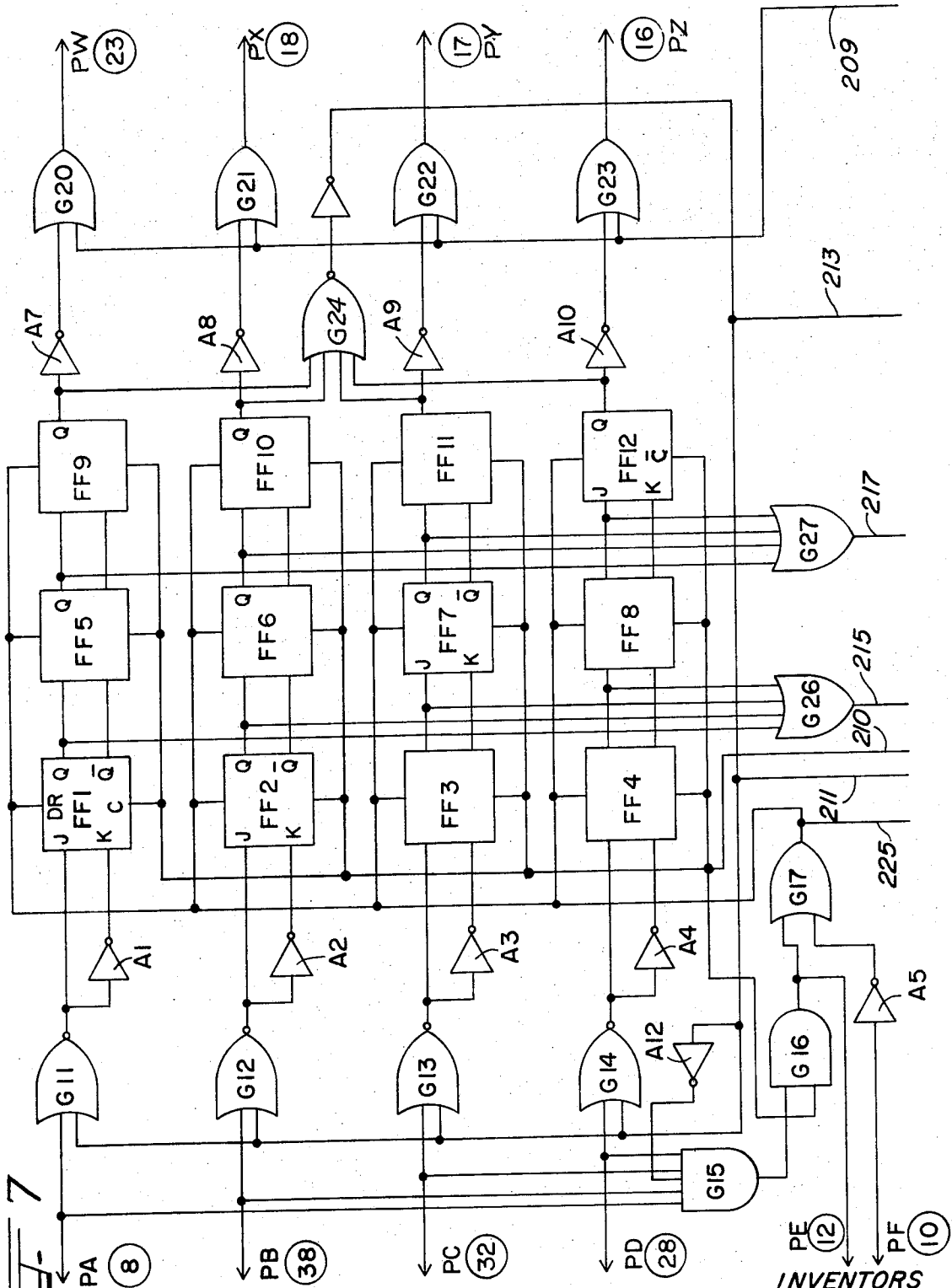
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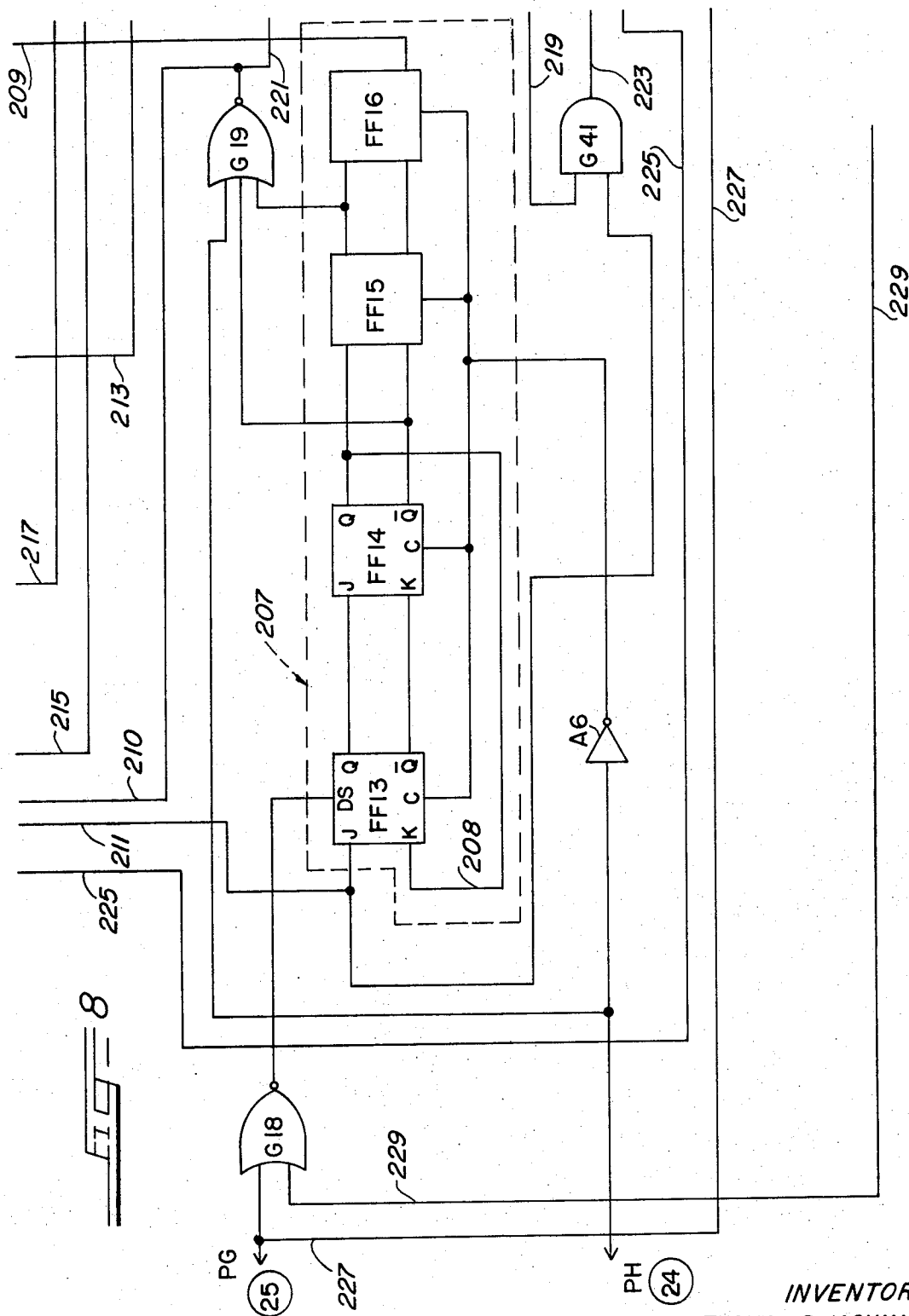
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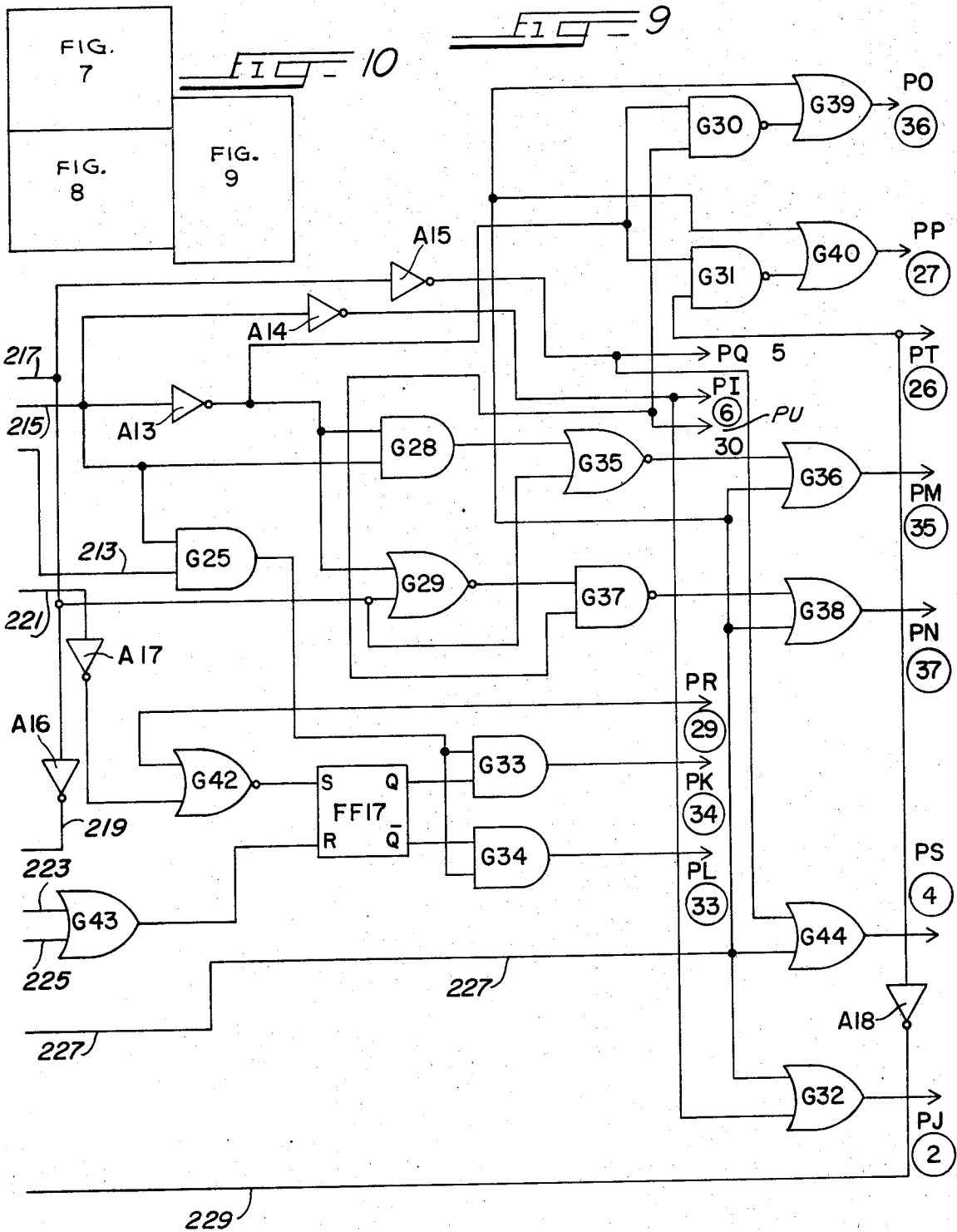
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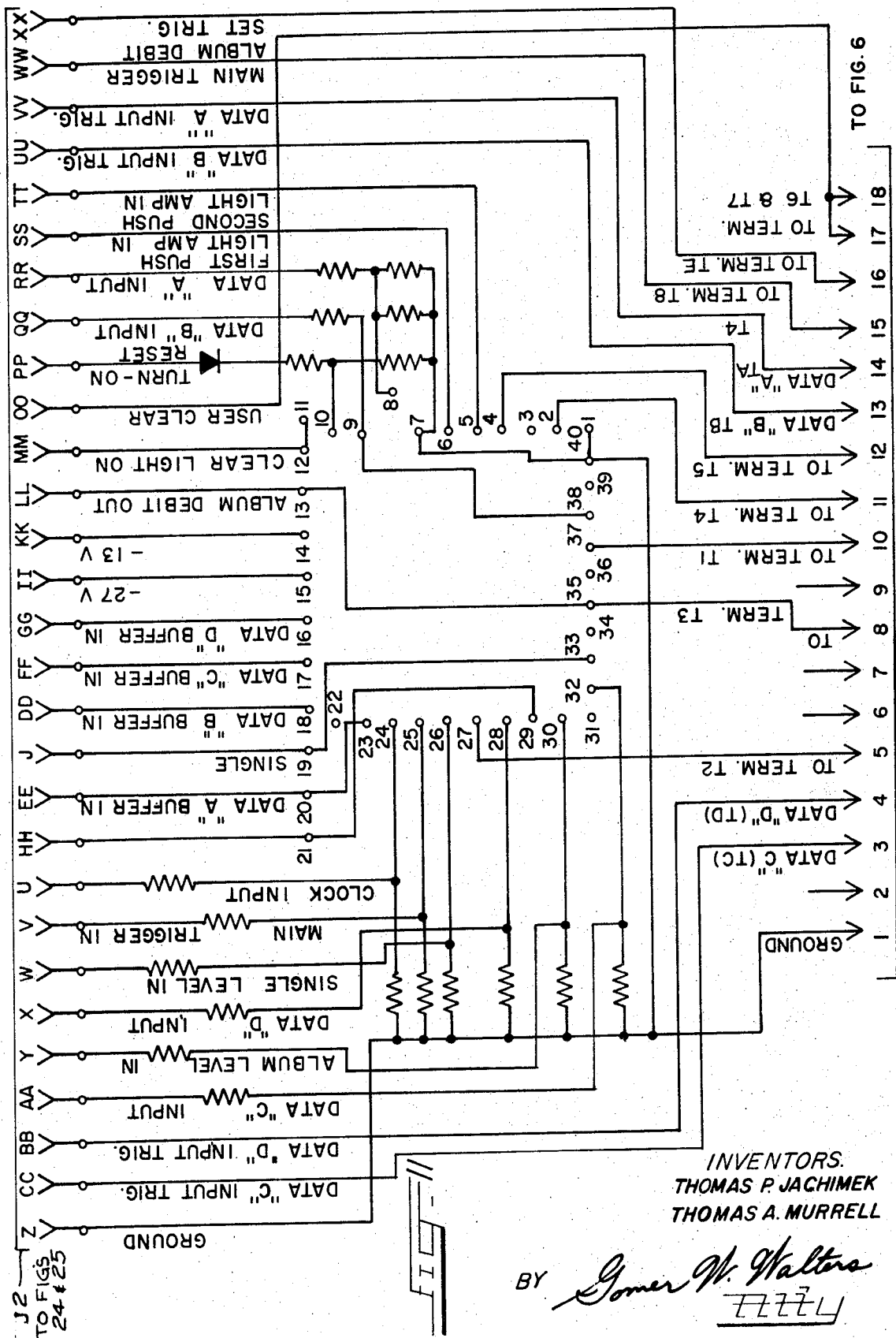
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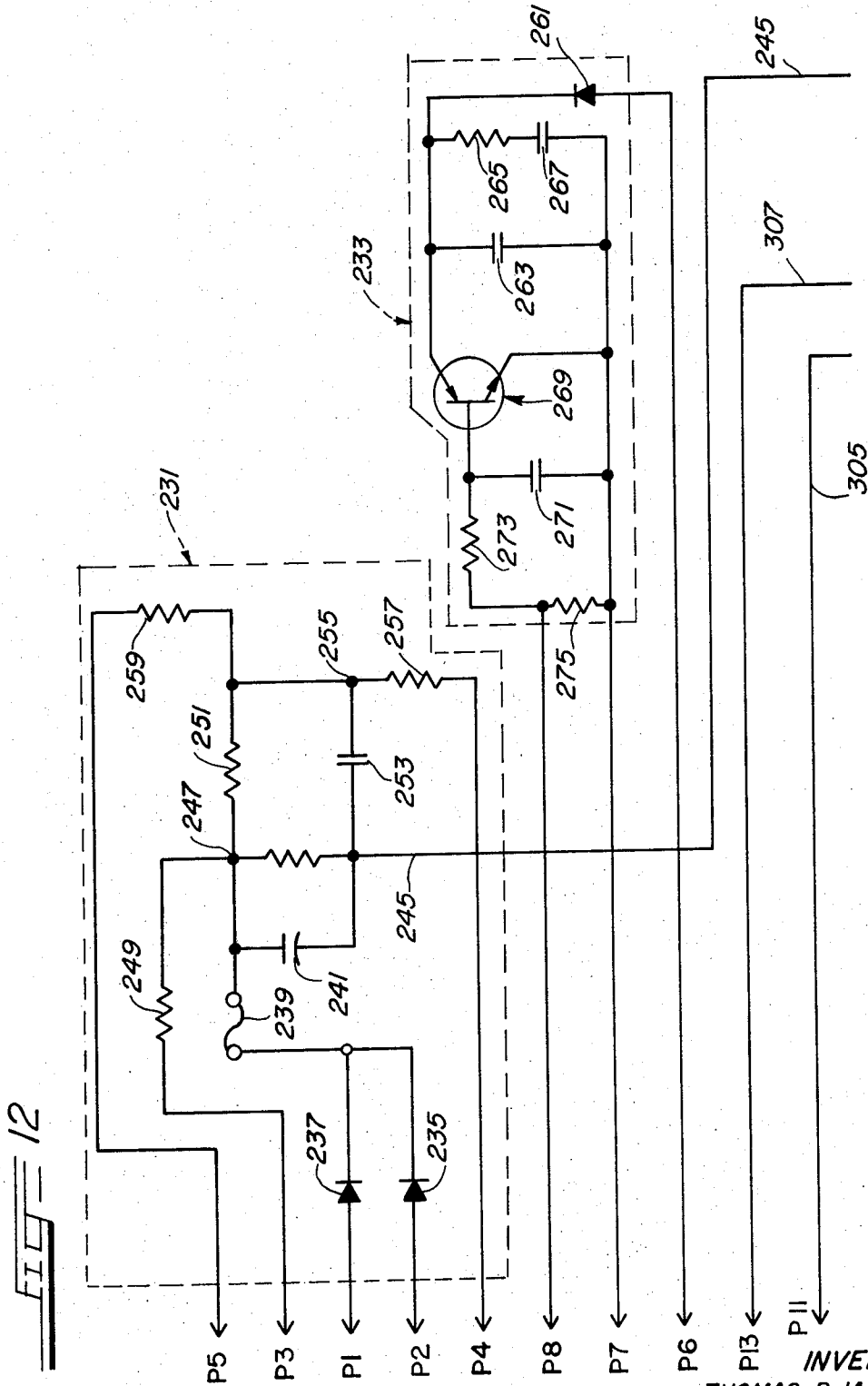
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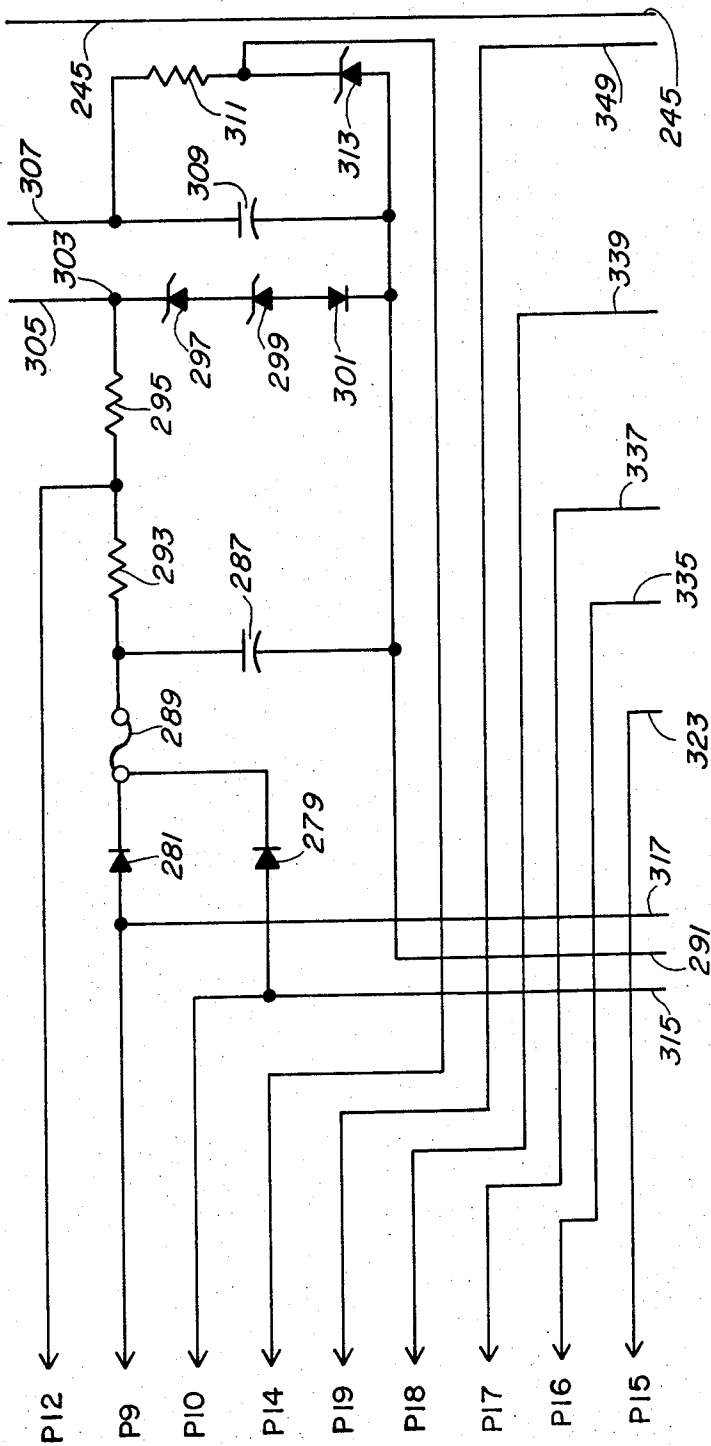
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FIG. 13



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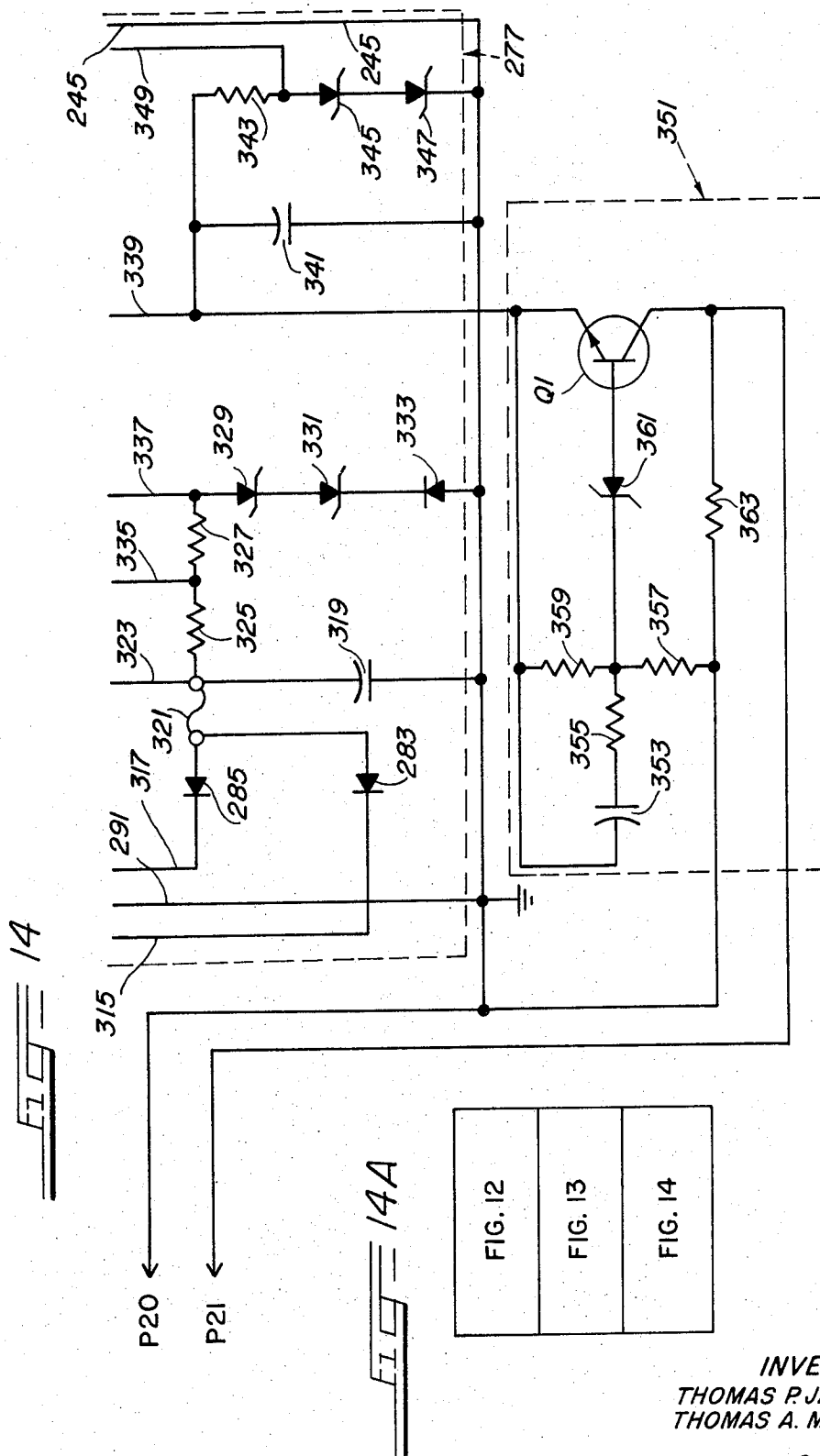


FIG. 12
FIG. 13
FIG. 14

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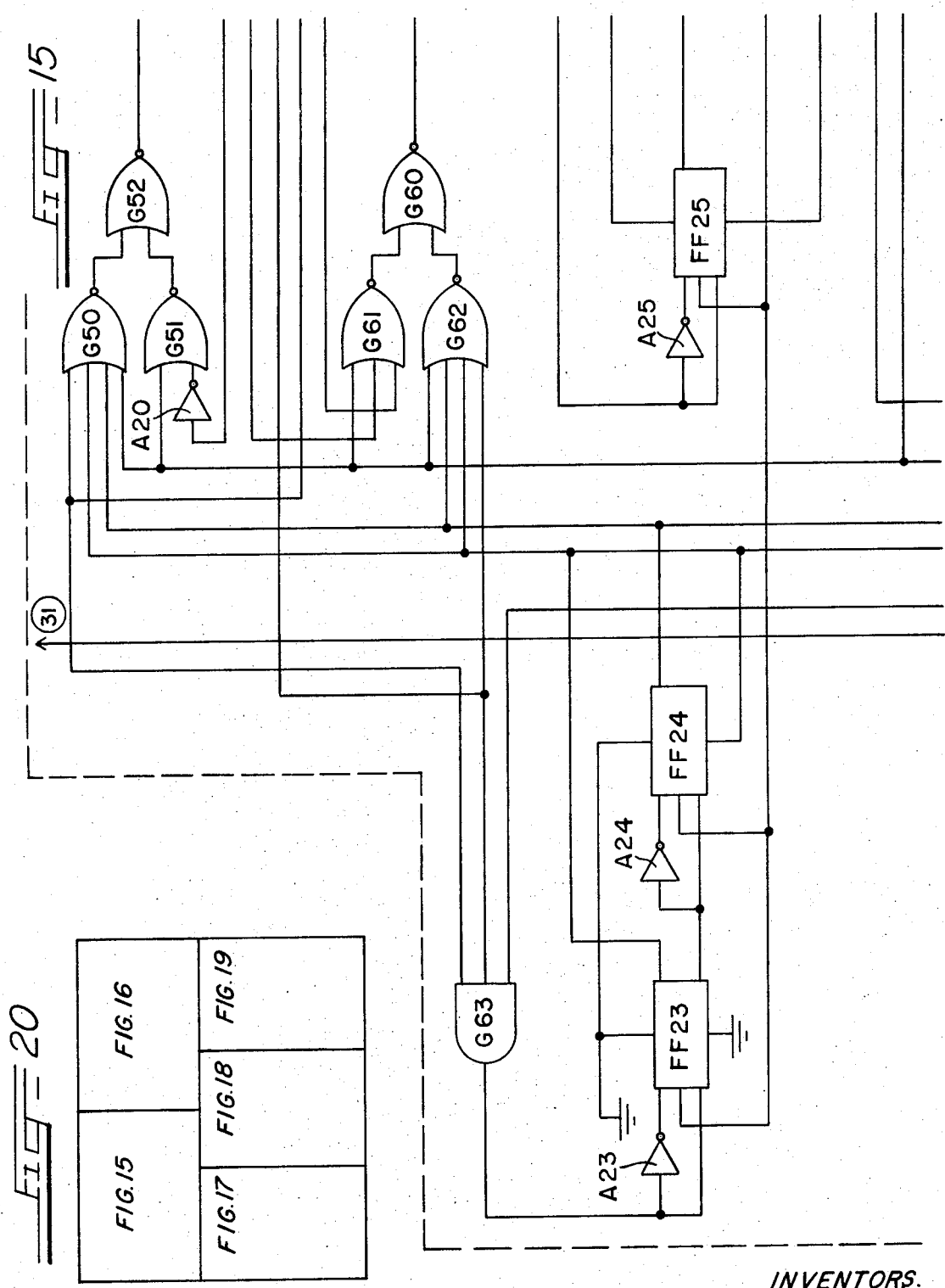


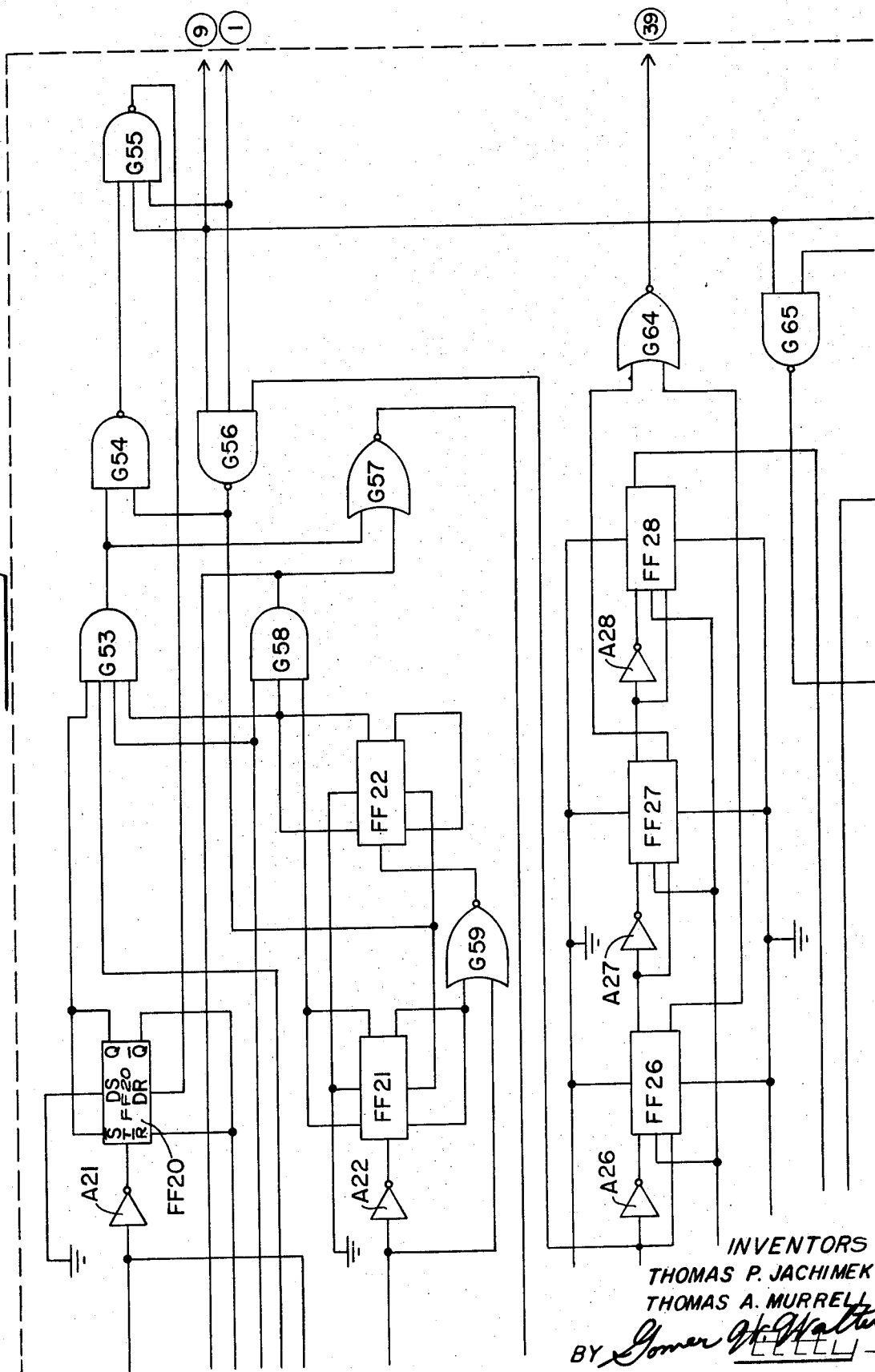
FIG. 20

FIG. 15	FIG. 16	FIG. 17	FIG. 18	FIG. 19
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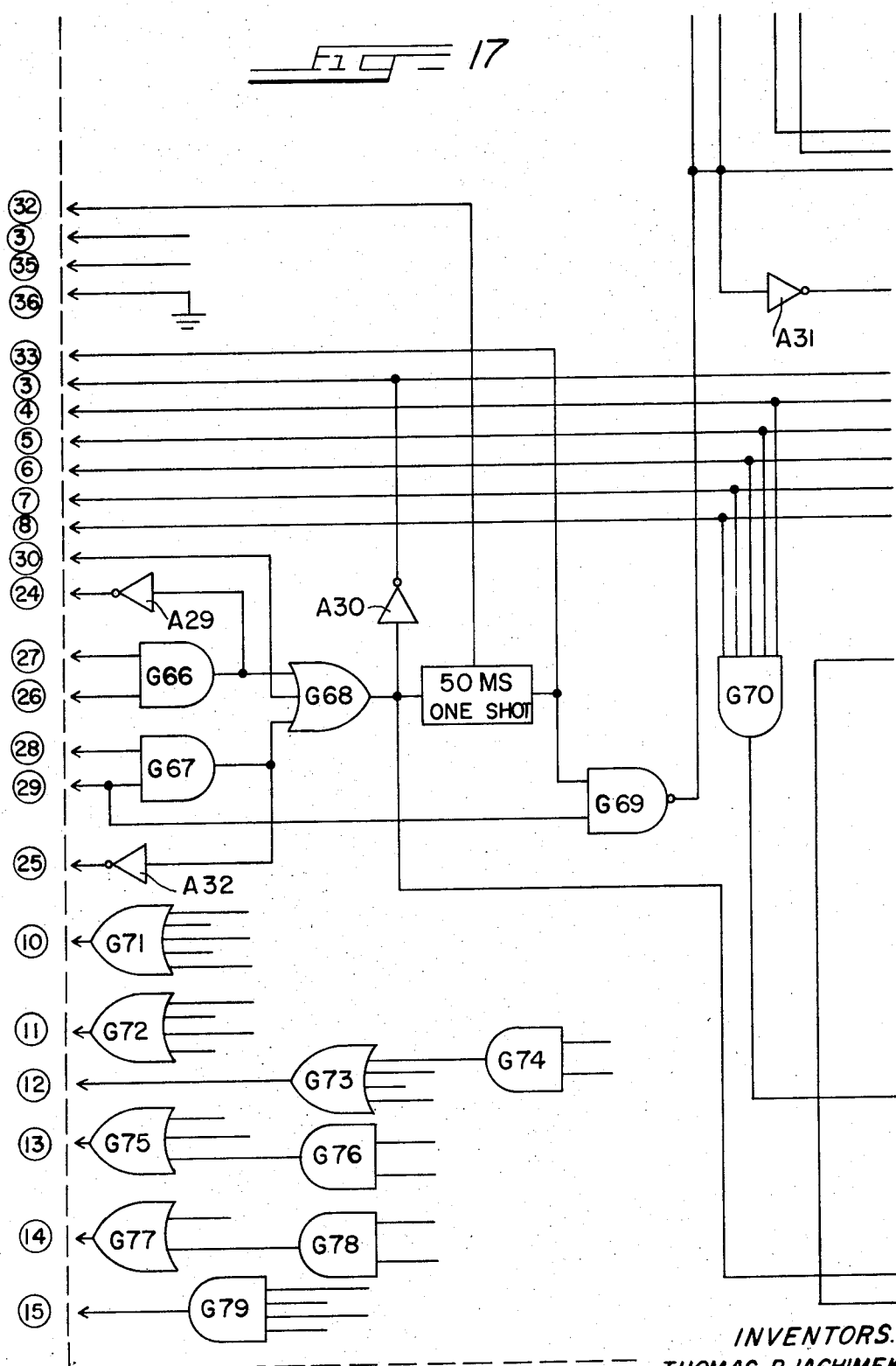
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FIG. 16

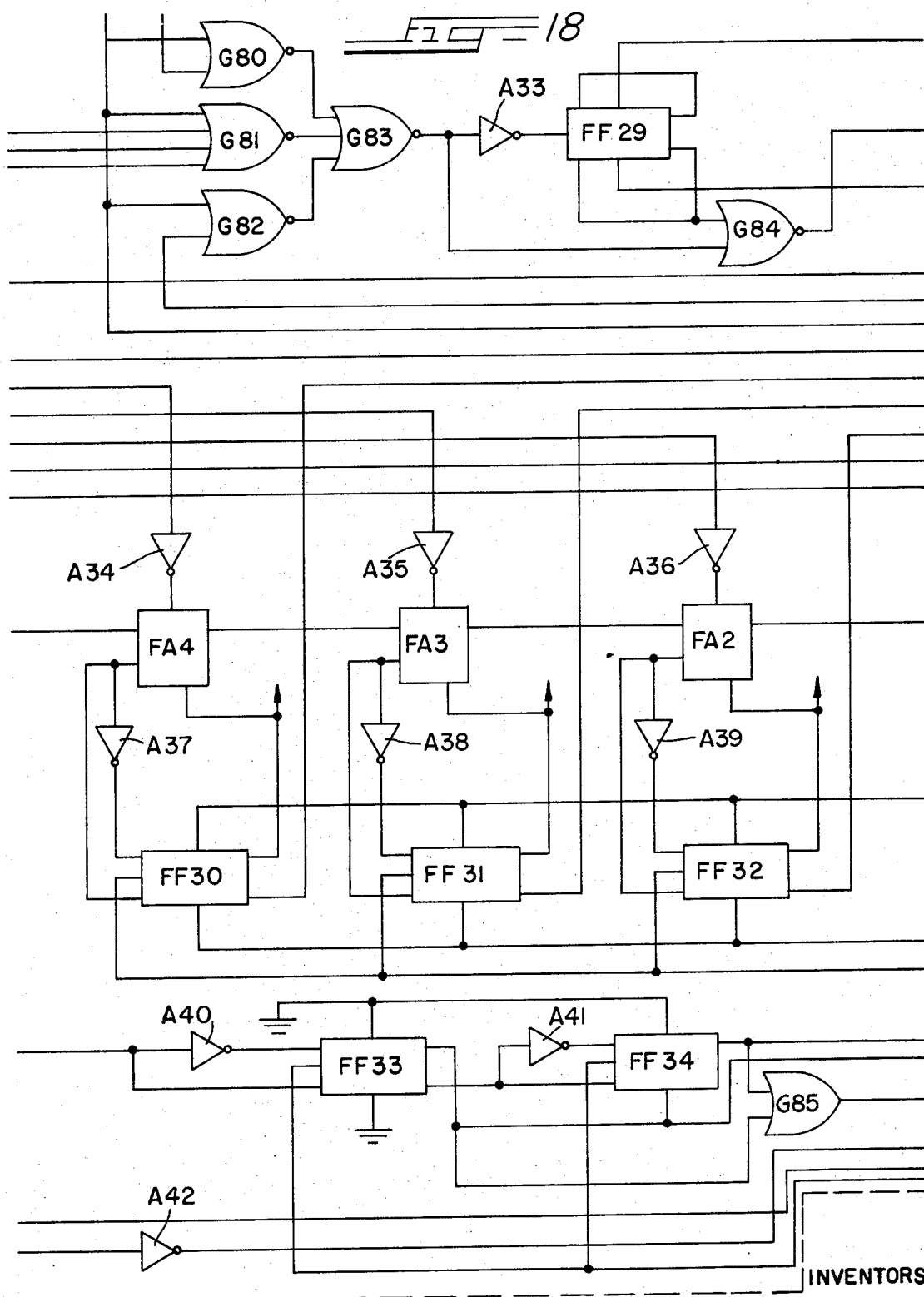


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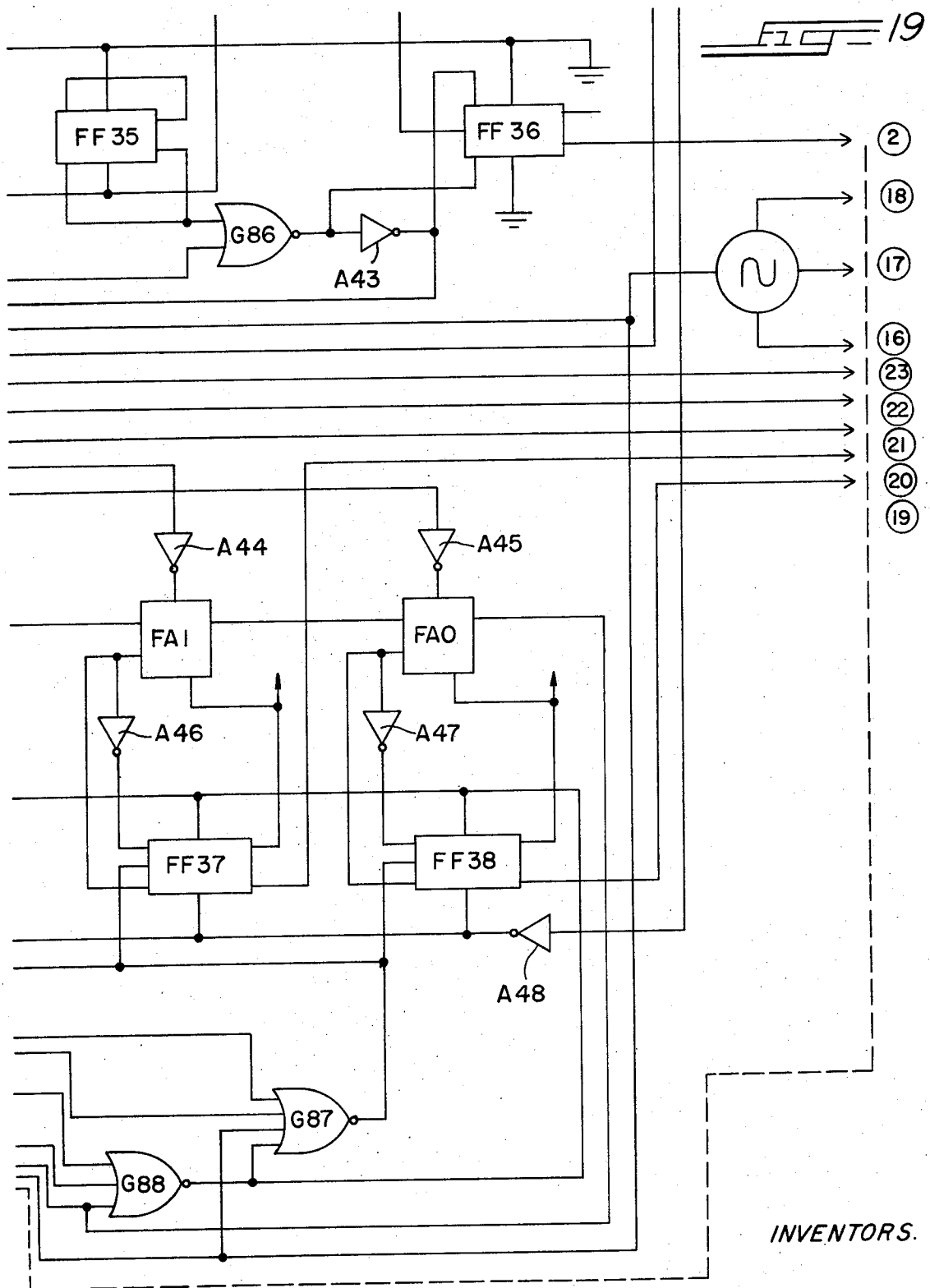
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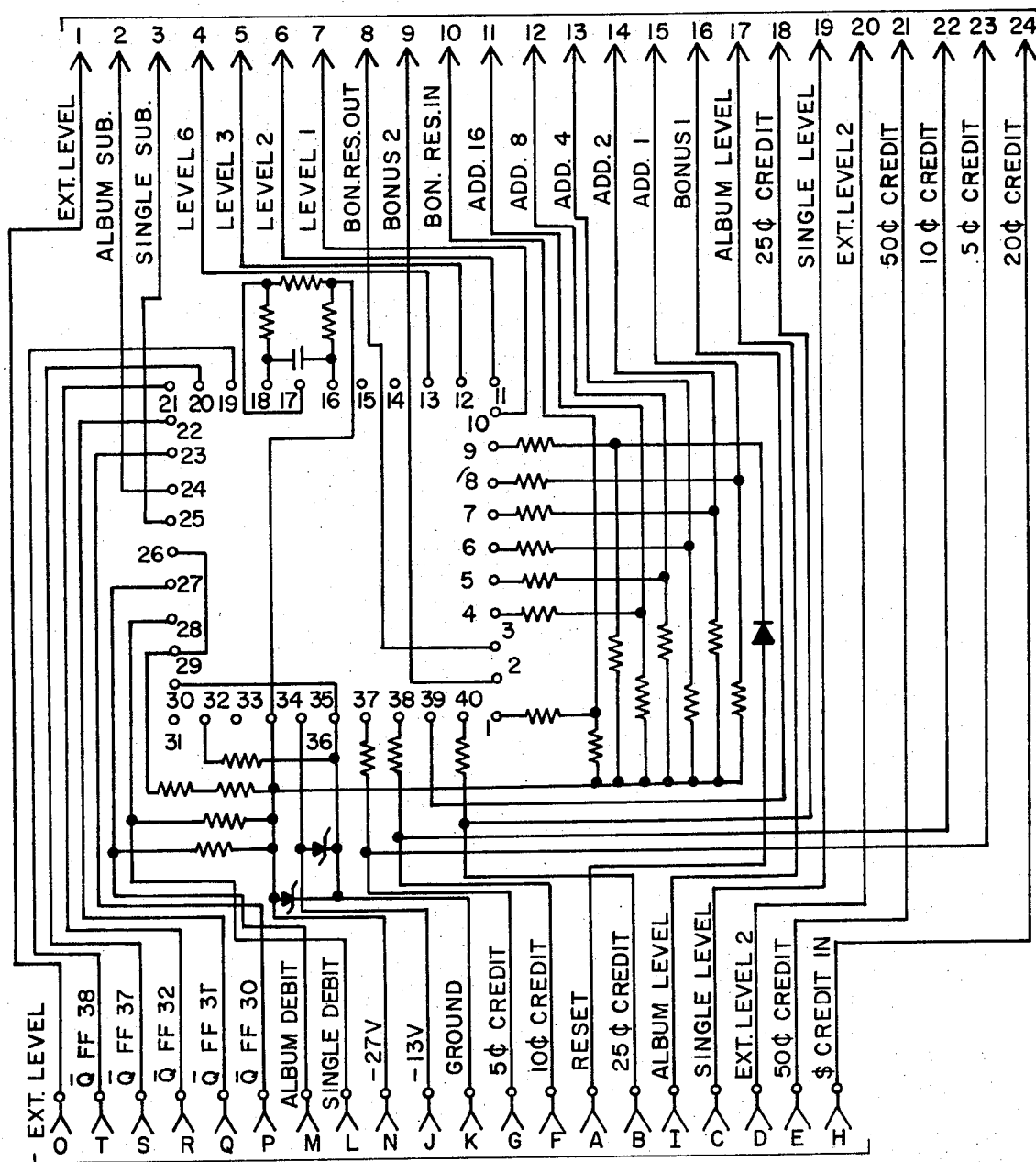


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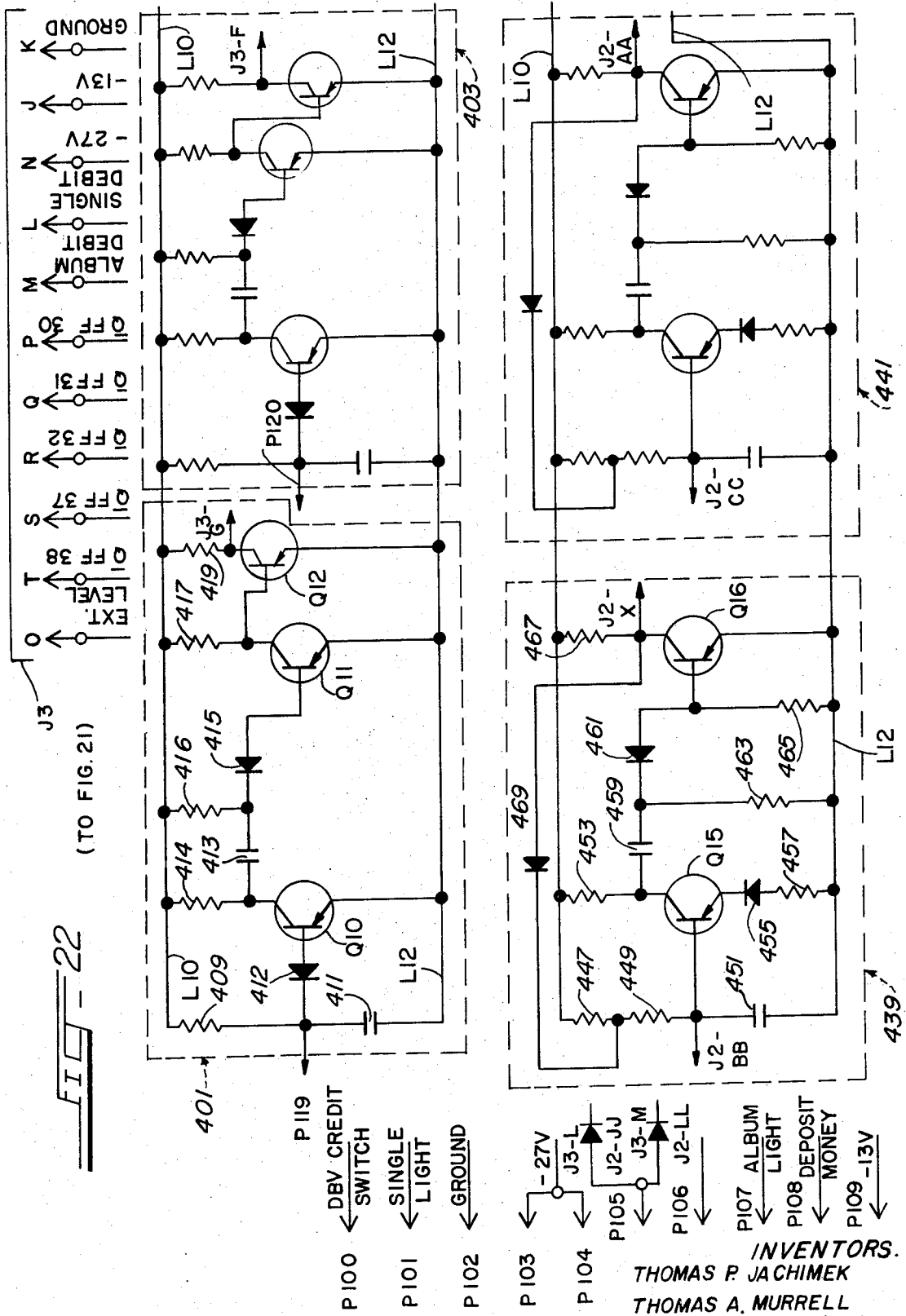
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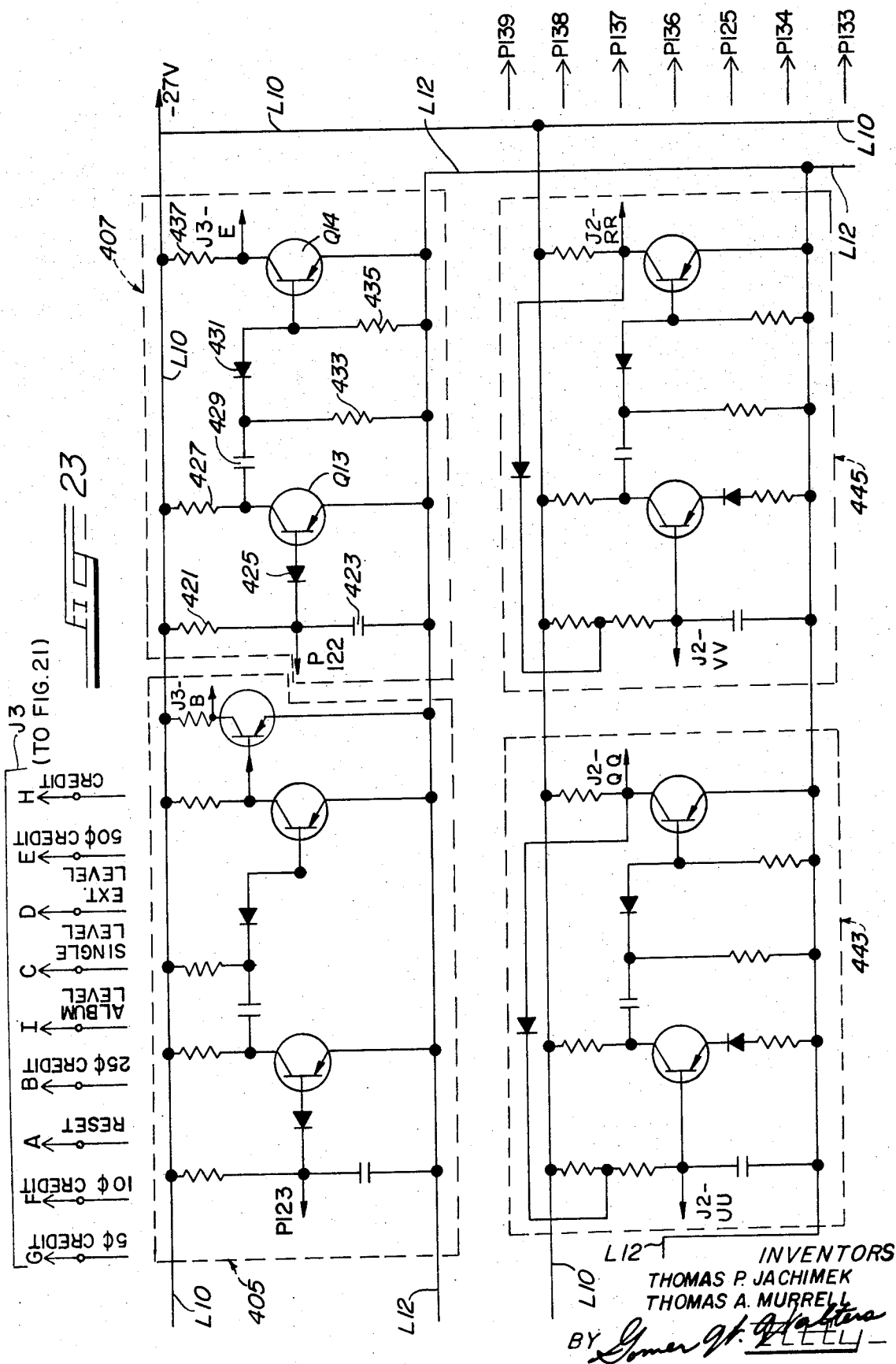
FIG. 21

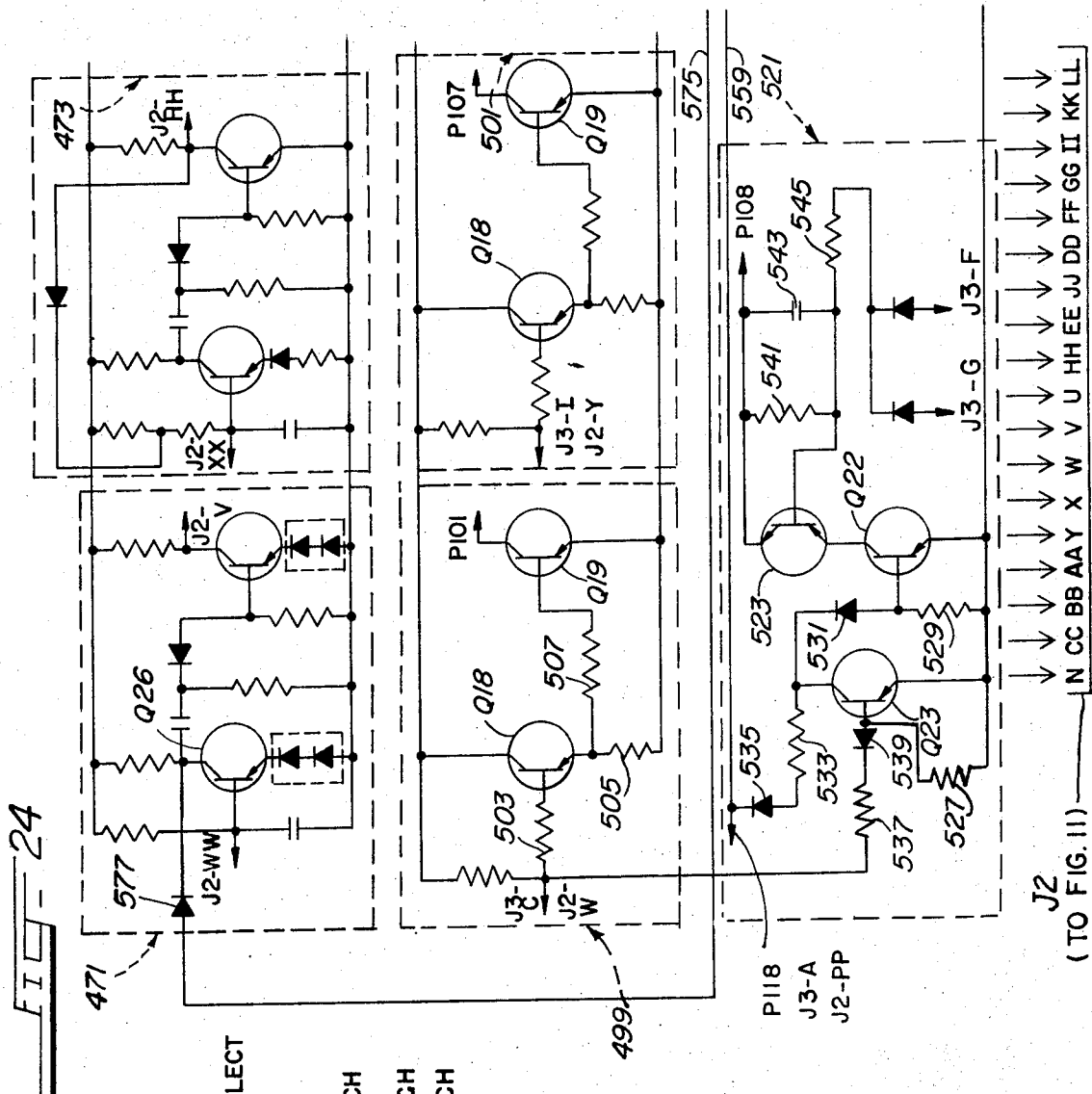


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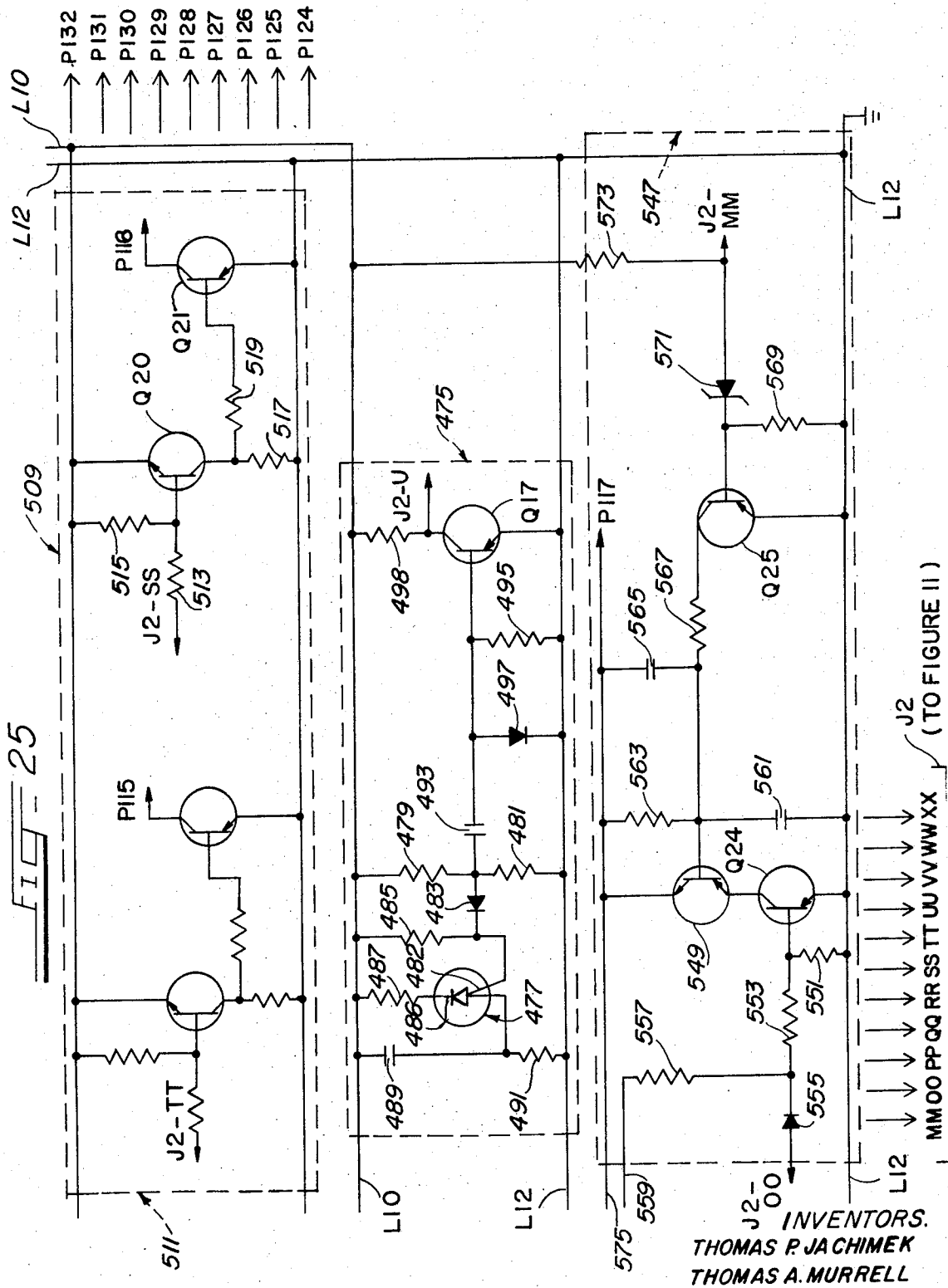
- FIG. 24
- PI10 C BUFFER IN
 - PI11 B BUFFER IN
 - PI12 A BUFFER IN
 - PI13 D BUFFER IN
 - PI14 KEY
 - PI15 SECOND LAMP
 - PI16 FIRST LAMP
 - PI17 RESET AND RESELECT
 - PI18 RESET
 - PI19 5¢ COIN SWITCH
 - PI20 10¢ COIN SWITCH
 - PI21 50¢ COIN SWITCH
 - PI22 50¢ COIN SWITCH
 - PI23 25¢ COIN SWITCH

FIG. 22	FIG. 23
FIG. 24	FIG. 25

FIG. 26

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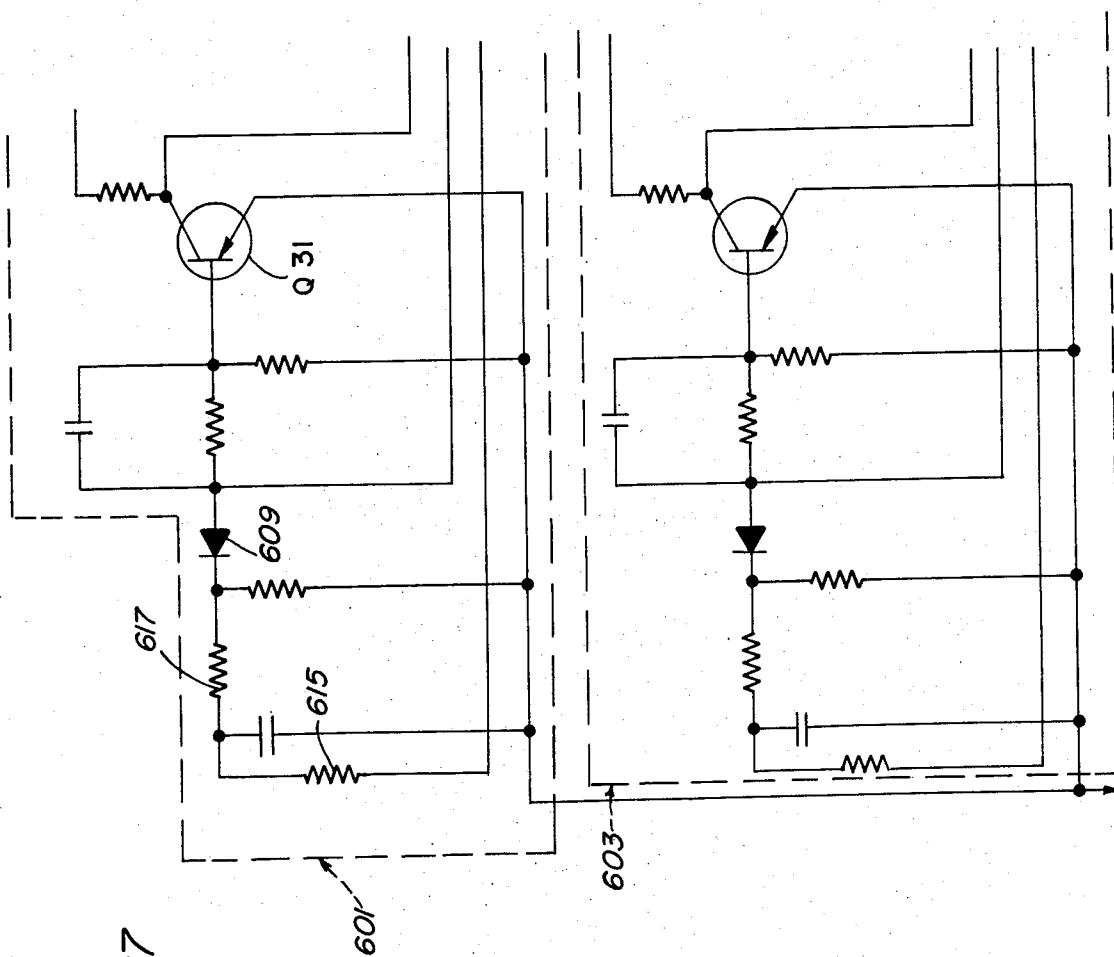


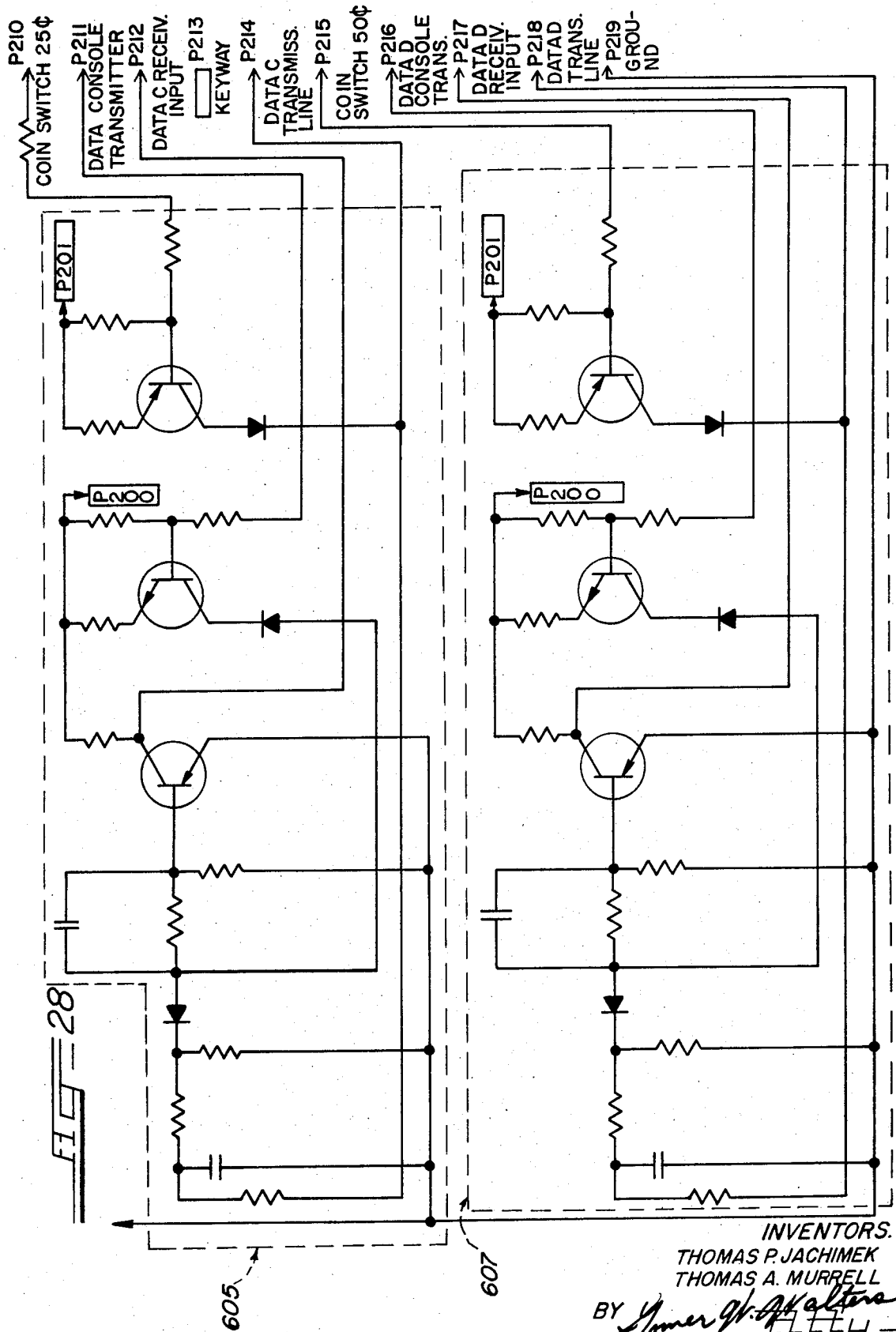
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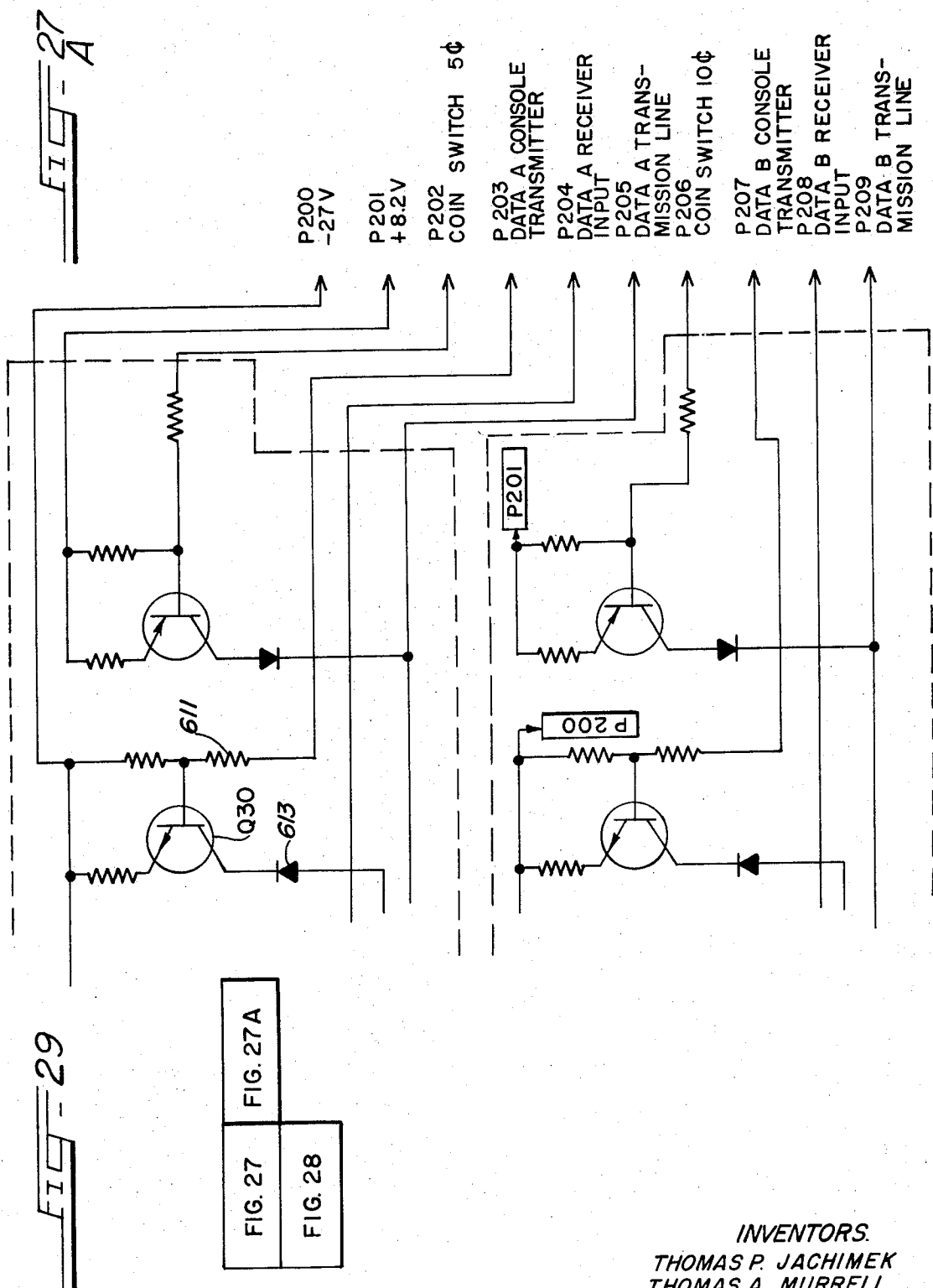
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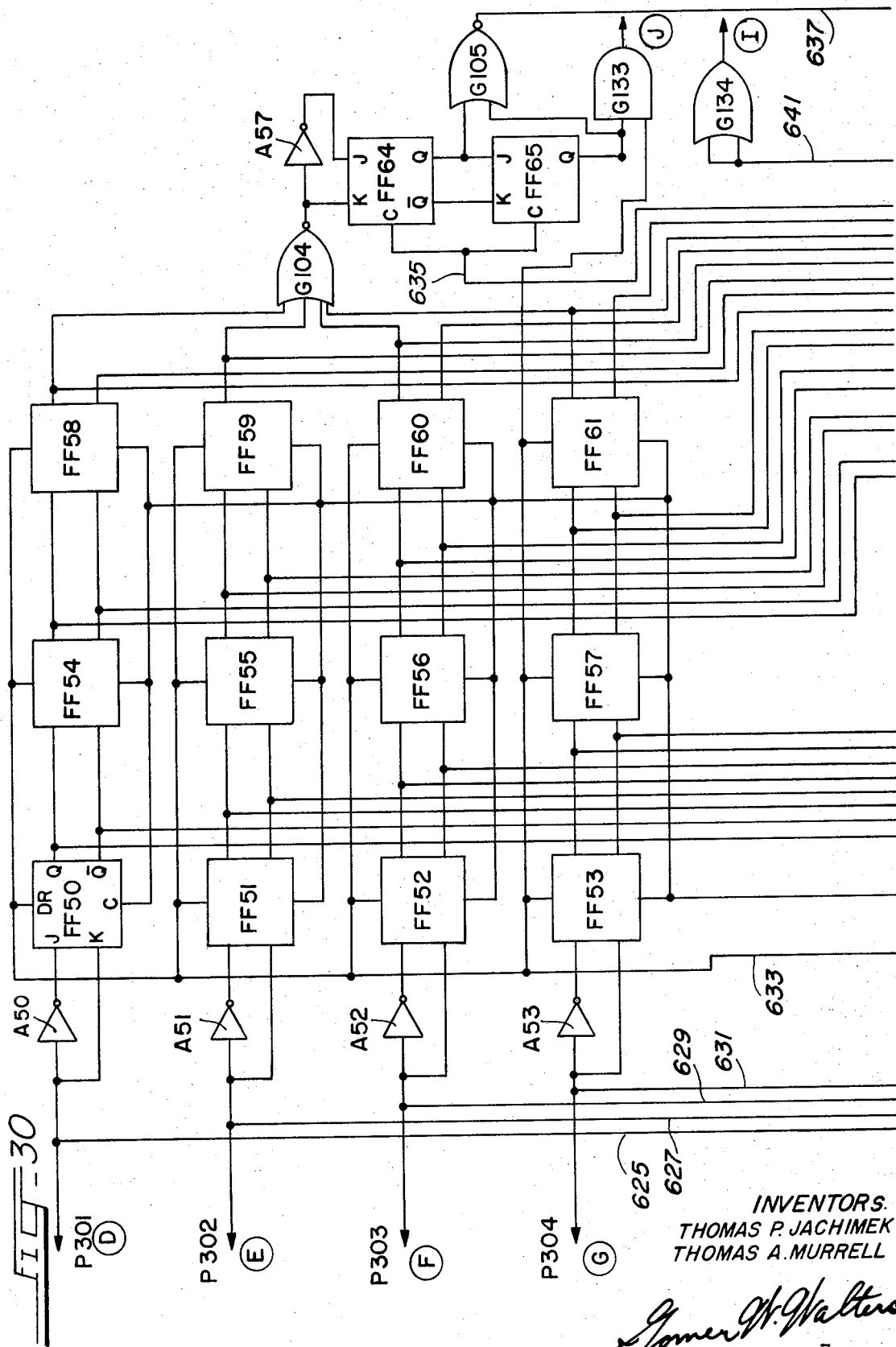
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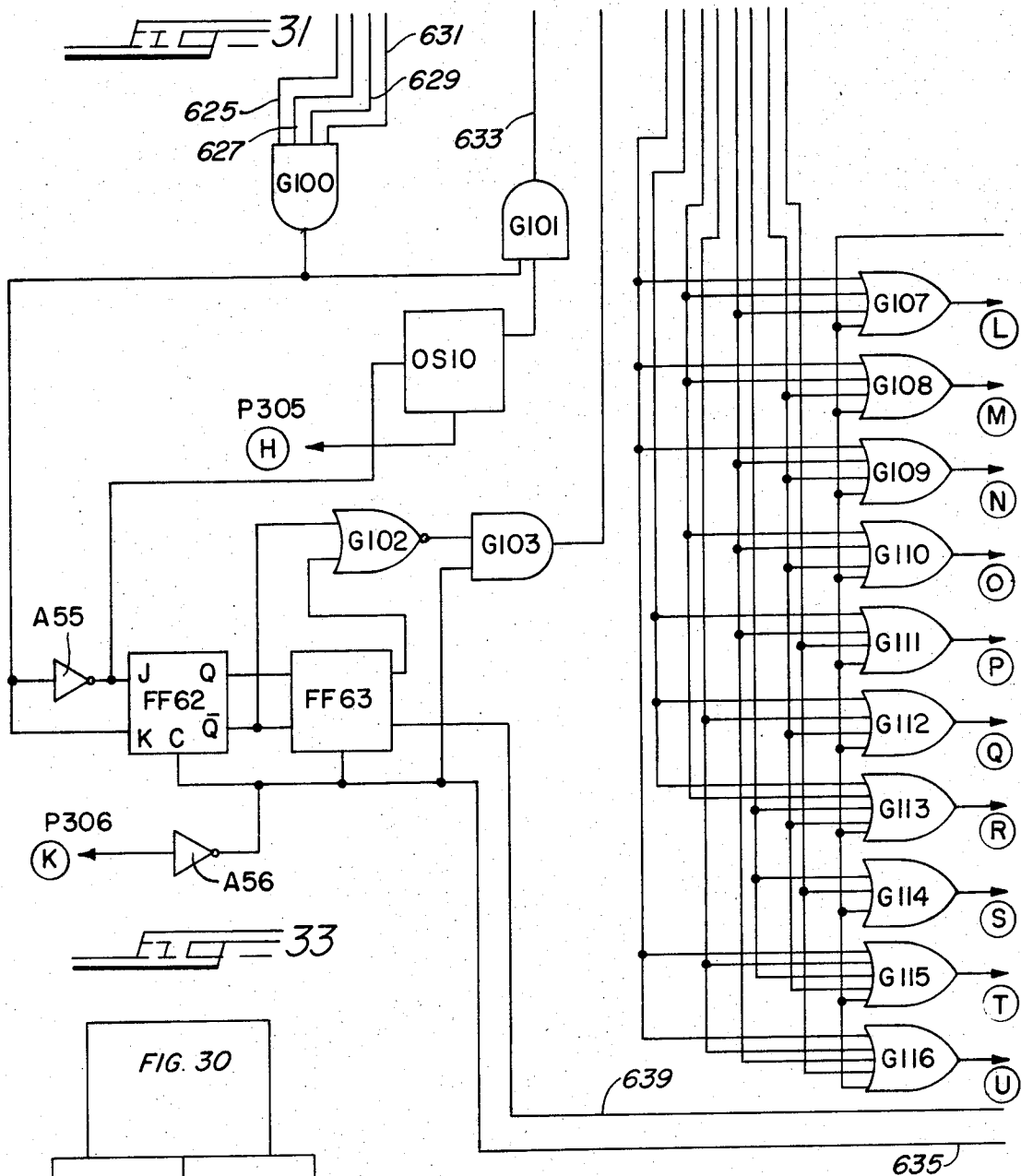
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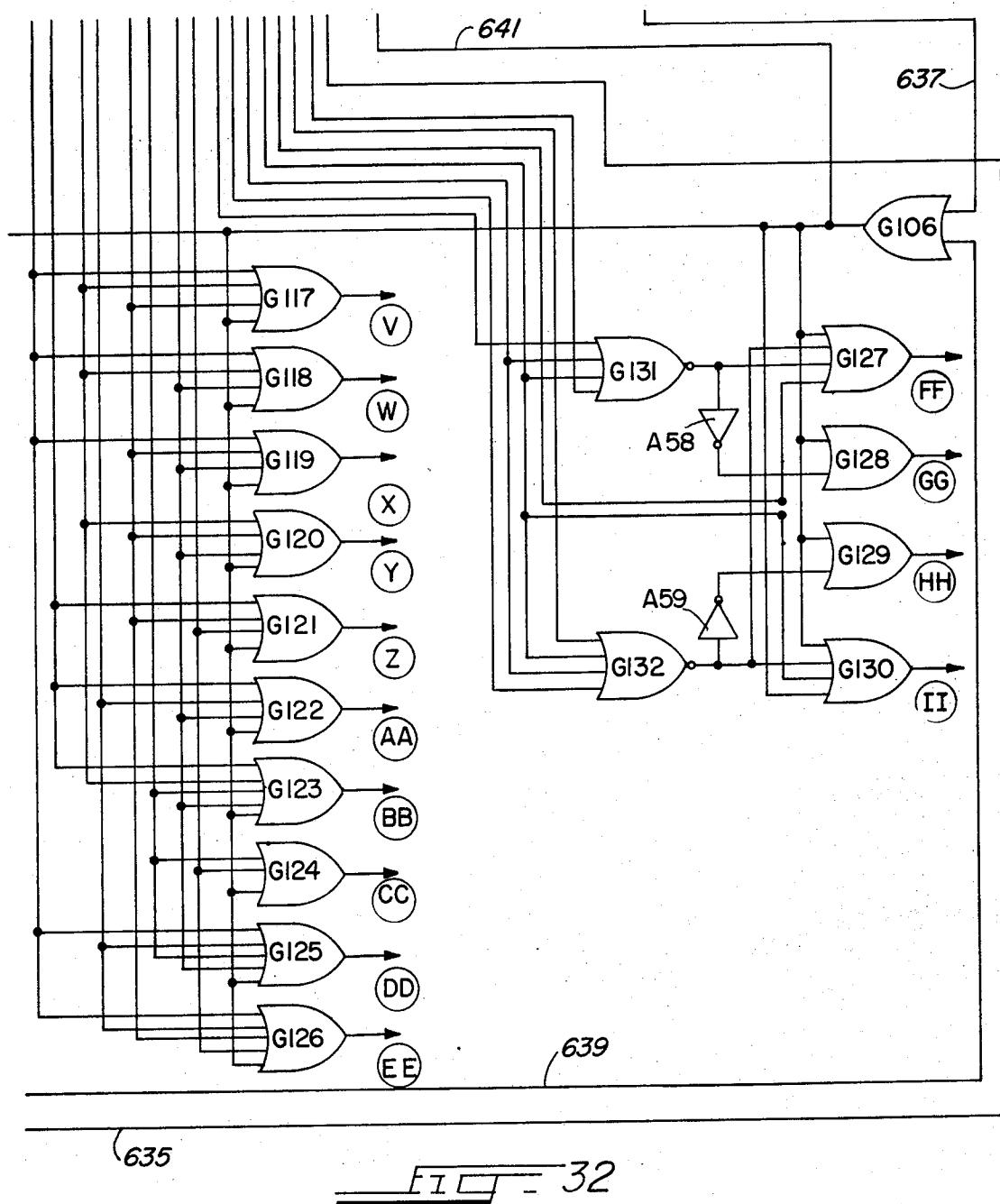
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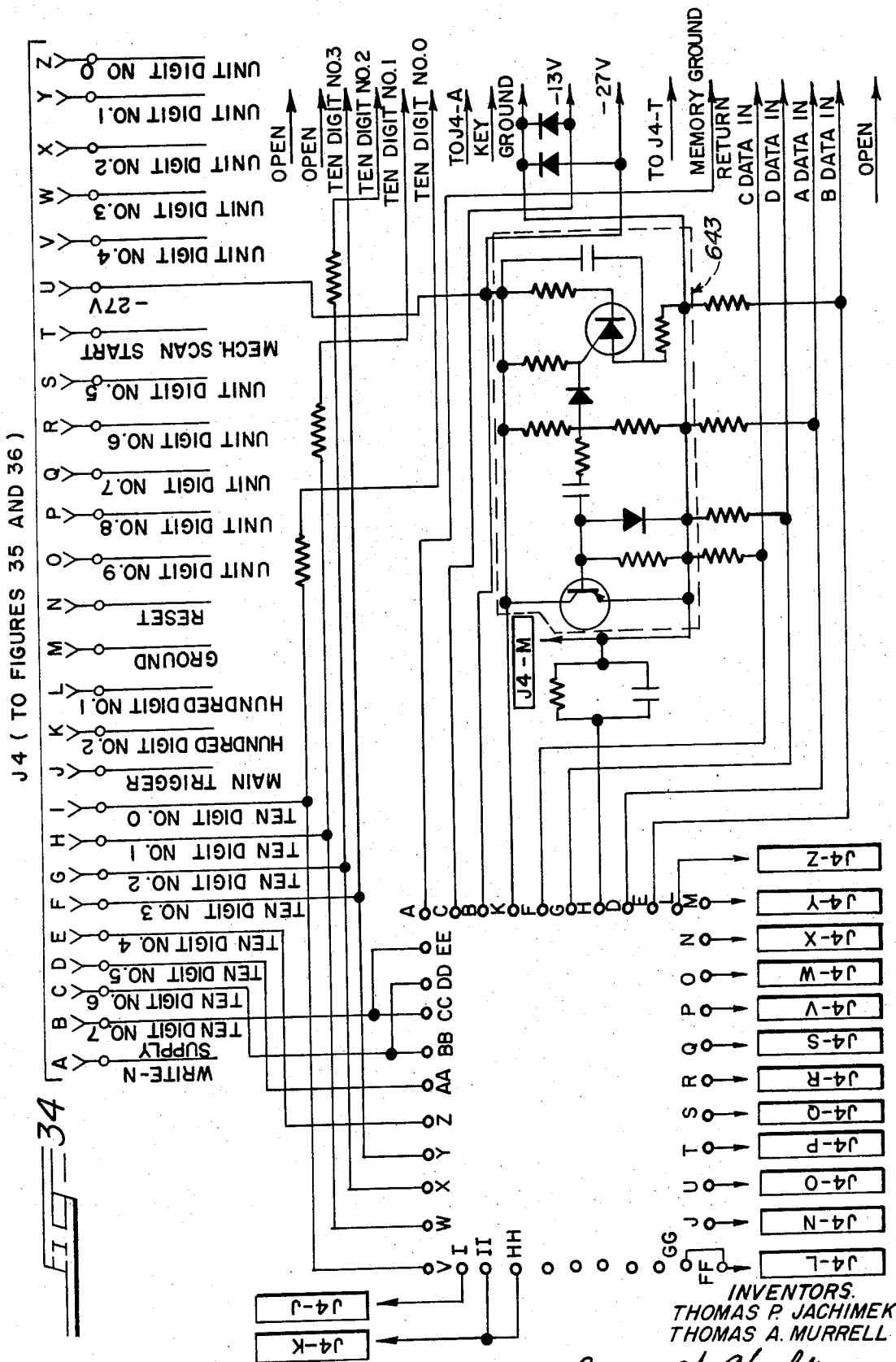
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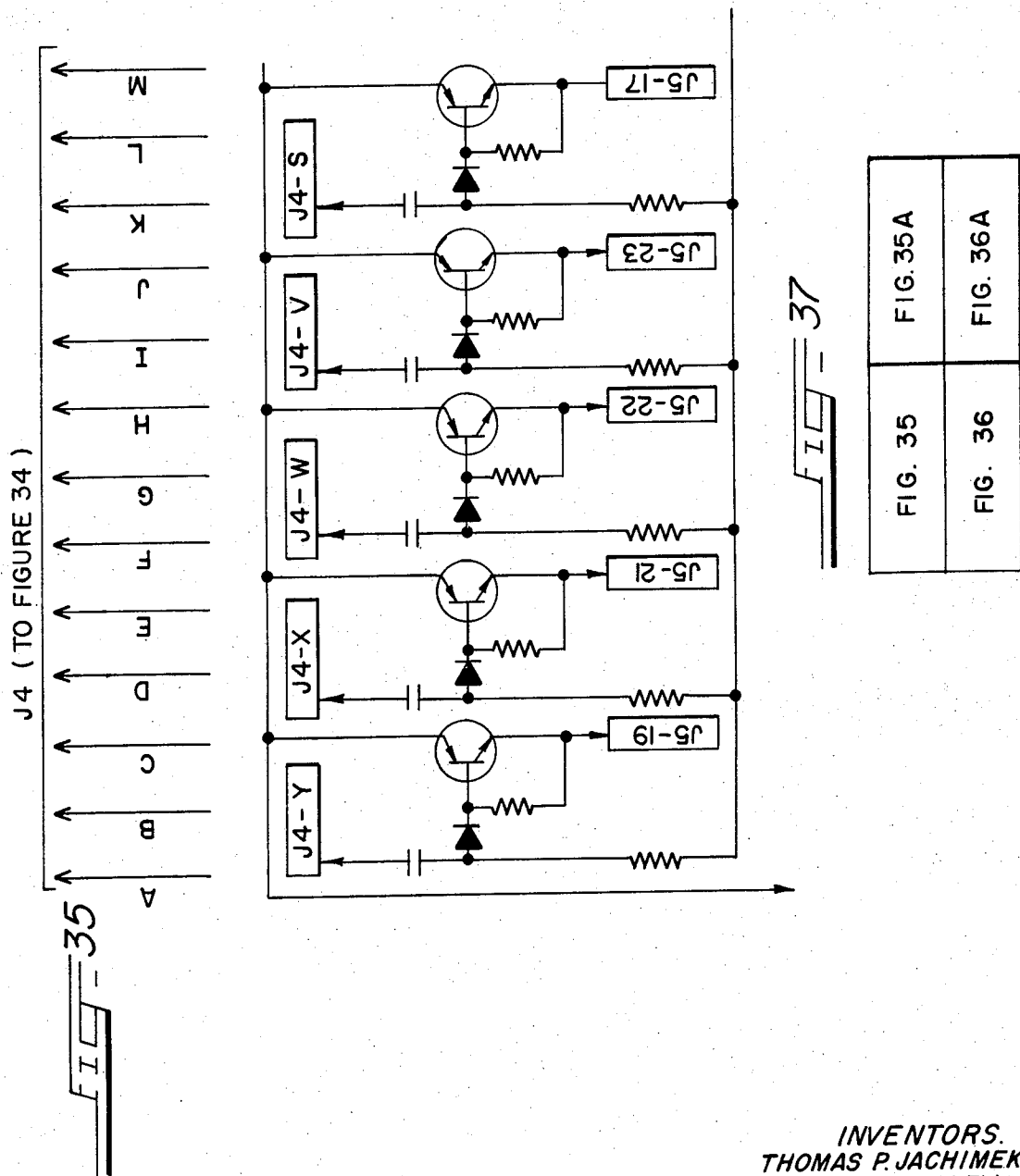
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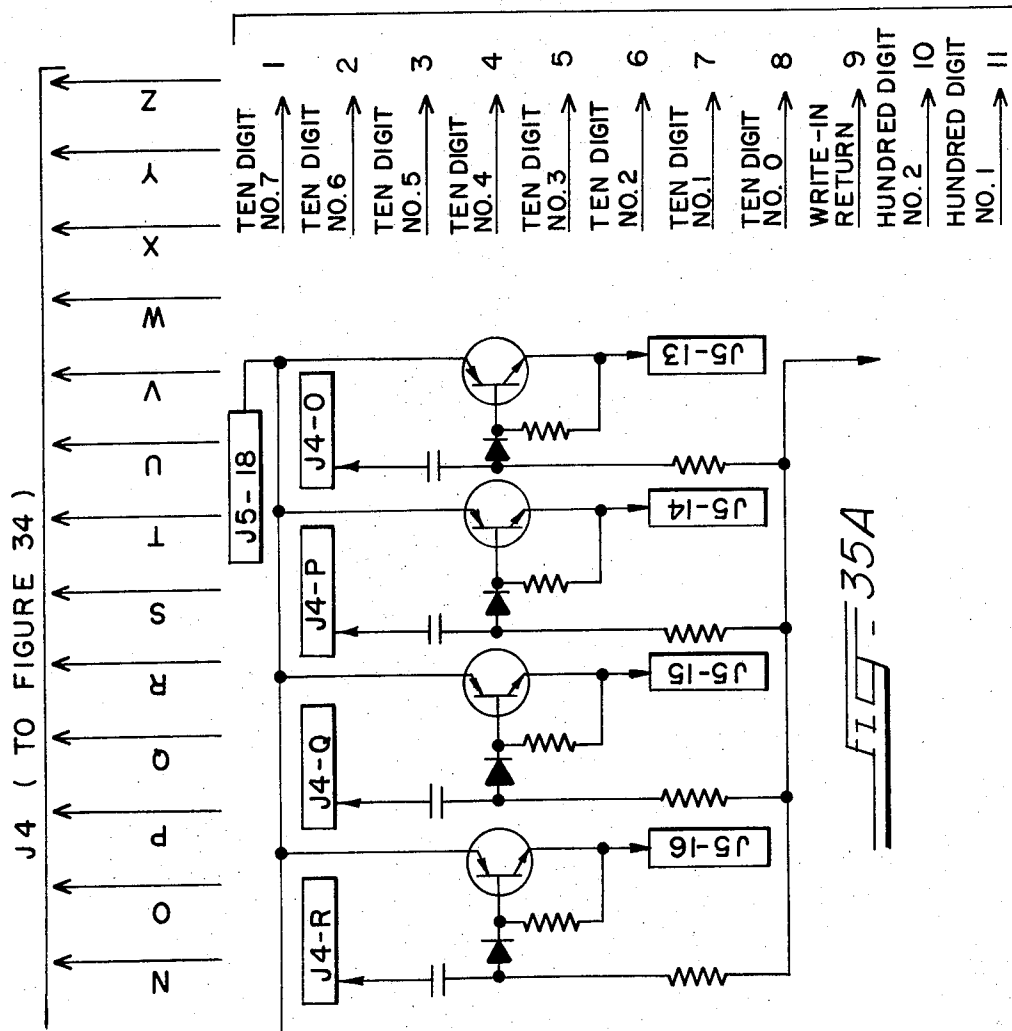
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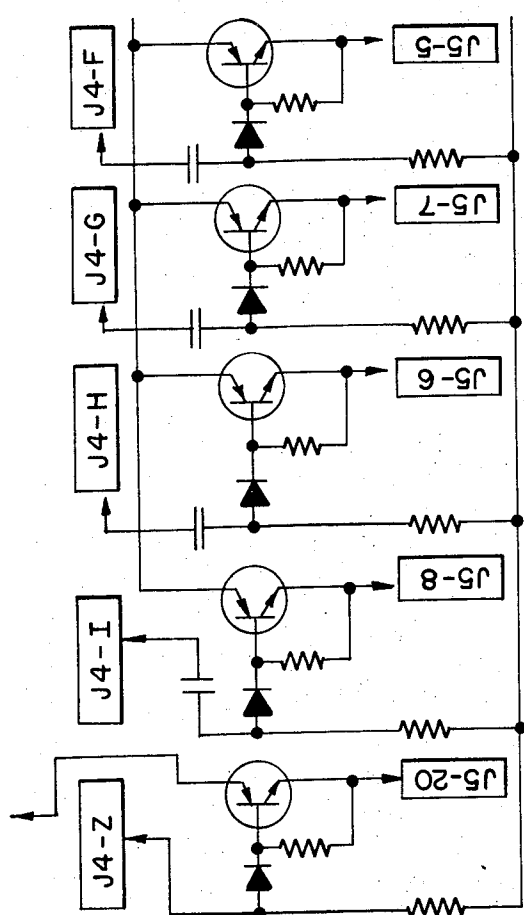
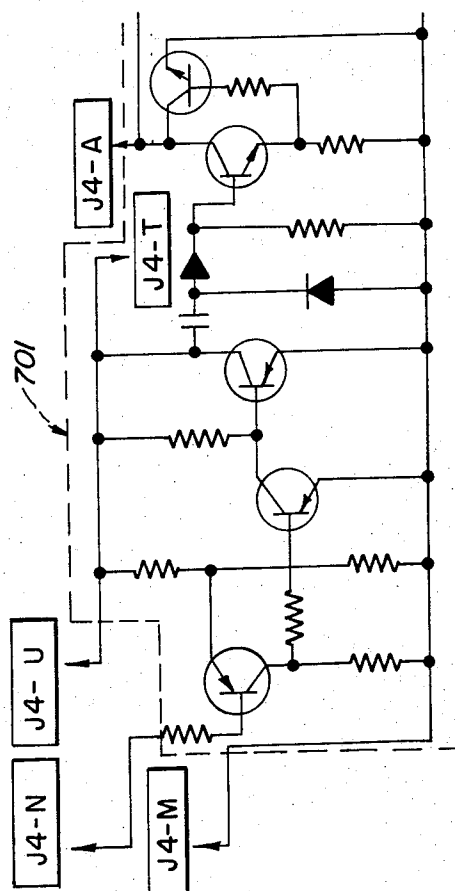


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FIG. 36



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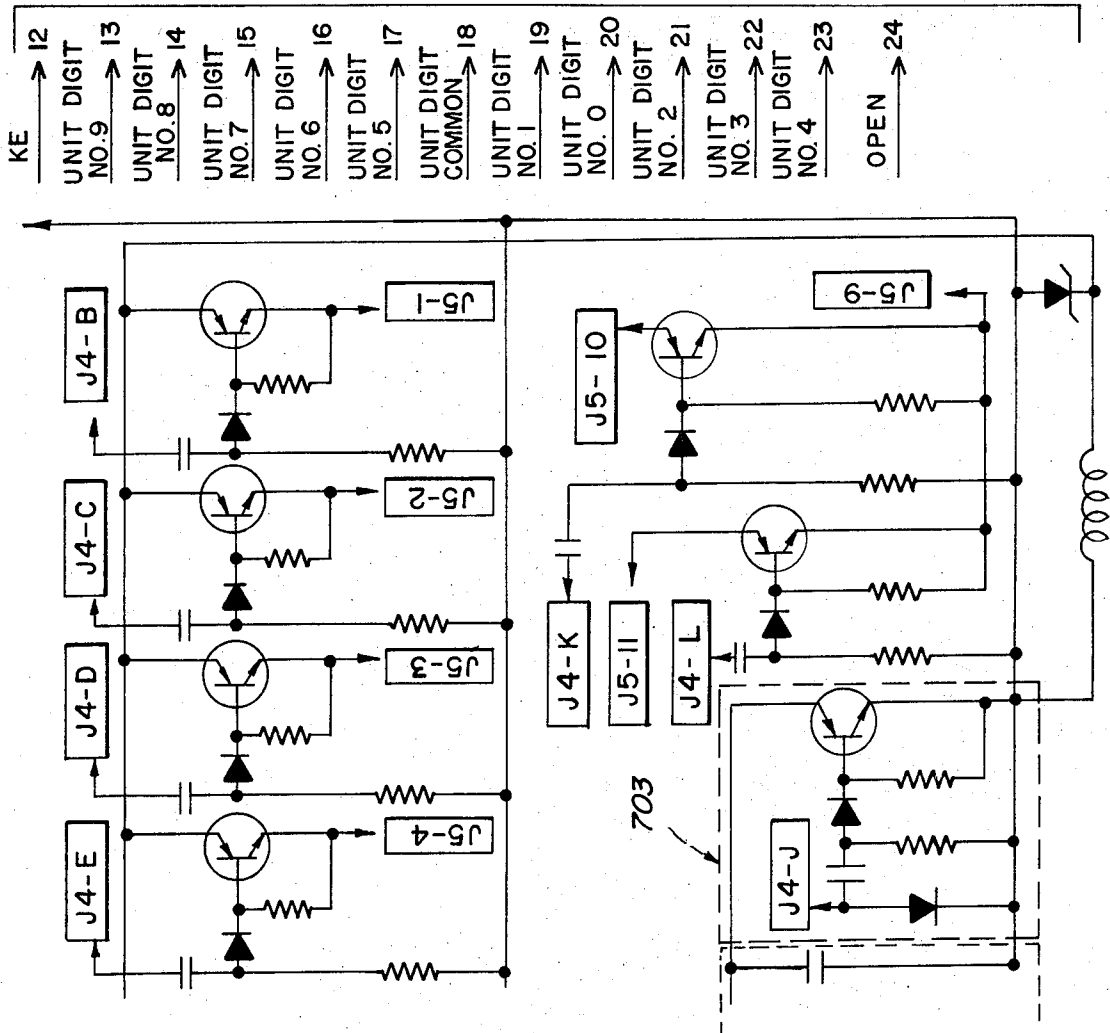


FIG. 36A

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SELECTING APPARATUS AND METHOD FOR PHONOGRAPH

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. Pat. Application Ser. No. 862,624 of Thomas P. Jachimek et al., filed on Sept. 11, 1969 for "Selecting Apparatus and Method for Phonograph," now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to a vender selecting arrangement utilizing sequential character selecting, and more particularly this invention relates to an integrated circuit phonograph selecting arrangement in which selection identifying character formats are encoded for sequential transmission and decoded upon reception for controlling record selecting.

2. Description of the Prior Art

Prior art phonograph selecting arrangements utilize letter-number combinations to identify selections. When making a choice of a particular selection both a letter and a number button must be simultaneously maintained in a depressed position to have the choice recorded for future play. During the time that the buttons are depressed and the choice of a selection is being recorded, no other choice, such as a choice from a second remote selector, can be recorded, or else there is a possibility of interference between two separate choices. This factor is a significant problem when a coin-operated phonograph ("juke-box") is controlled by a number of remote selection units, such as the so-called "wall boxes."

Due to the fact that both the number and letter button must be simultaneously depressed, prior art phonographs have a "memory" function built into the selector unit. As a result of this memory factor, expansion of the selector unit becomes quite difficult as the addition of selections requires new buttons and the corresponding switches.

Another disadvantage of one type of prior art selecting arrangement is that the information conveyed from remote selecting stations to the central phonograph unit requires a considerable number of electrical leads. Thus, a large amount of wire is needed and the resultant connecting cable is large and unwieldy. This problem has been overcome by more recent prior art devices that utilize pulse sequences of differing lengths to provide character identification. However, these devices need on the order of 2.5 seconds of transmission time, which necessitates either the lock-out of other choices or running the risk of having interfering choices during this time. Both of these conditions result in loss of income to the operator. In addition, this relatively lengthy transmission time provides a greater opportunity to "cheat" the machine, a constant problem in all vending areas.

SUMMARY OF THE INVENTION

To overcome the above and other disadvantages of prior art devices, the present invention was developed.

Briefly, the present invention involves a vender selecting arrangement, such as a phonograph selecting arrangement, utilizing integrated circuits. Individual

selections are identified by character formats, such as multi-digit numerals. A customer chooses a selection by sequentially actuating a selector switching arrangement similar to a telephone push-button selector. The switching arrangement is constructed as an encoding device to produce patterns of pulses representative of the particular characters. In the present invention, the selection identifying character formats (selection identifying numbers) have three characters (digits) and the patterns of signals for each character (digit) include four signals of the binary type, i.e., yes - no or on - off information. For ease of reference, the following description of applicant's invention shall refer to the preferred embodiment form of numerals for the character formats and digits for the characters.

As the digits are encoded, the patterns of signals appear at the inputs of a register. A shift circuit produces clock pulses to enter the first pattern of signals into the register. Subsequent patterns are also entered until the register contains the complete encoded identifying numeral.

At this time the shift circuit is activated by a control circuit to transmit the coded digits in the register in the same sequence as that in which the customer designated them. These sequential signals are transmitted to the input of a second register. A second shift circuit causes the signals to be entered into the second register. If the signals are all received within an allotted time period, they are accepted and are then decoded while stored in the second register to provide control currents for a memory circuit. The decoded signals are then conveyed to a selecting control memory for temporary storage until the player mechanism is actuated to play that selection.

With this arrangement, the same selector switching arrangement can be utilized for virtually an unlimited number of selections, while the necessary circuit modifications can be made quite simply in the integrated circuit chips, which preferably are a more advanced generation, or "large scale" integrated circuits. Also, the transmittal of the entire coded numeral at one time and the very short time for which the receiver is captured (approximately 0.0025 second) permits the use of one receiver for a large number of transmitters without getting the interference or lost choices that occur in prior art arrangements, thus increasing operator income. Further, the rapid transmission time of about 0.0025 second (2.5 millisecond) greatly reduces, if it does not eliminate, the cheating problem, since the time during which tampering could take place exceeds the human reaction time. In addition, the number of leads needed for transmitting a large number of selection choices is considerably reduced over some prior art devices.

In the preferred embodiment wherein the character format is a numeral, the selector has a much more global significance due to the universally accepted significance of numerals, as opposed to the letters of the various alphabets.

Accordingly, it is a primary object of this invention to provide a vender selecting arrangement utilizing a character format to identify vend selections.

A further object of this invention is to provide a phonograph selecting arrangement utilizing a character format to identify record selections.

Another object of this invention is to provide a phonograph selecting arrangement that utilizes universally meaningful numerals to identify record selections.

Yet another object of this invention is to reduce the transmission time needed to record the choice of a record selection.

Still another object of this invention is to limit or eliminate interference between choices from different selector locations.

These and other objects, advantages, and features of this invention will hereinafter appear, and for purposes of illustration, but not of limitation, exemplary embodiments of the subject invention are shown in the appended drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic circuit diagram of a switching arrangement utilized in one embodiment of the present invention.

FIGS. 2A and 2B illustrate the transmitter portion of one embodiment of the present invention.

FIG. 3 illustrates the relative placement of FIGS. 2A and 2B.

FIGS. 4A and 4B illustrate the receiver portion of one embodiment of the present invention.

FIG. 5 illustrates the relative placement of FIGS. 4A and 4B.

FIG. 6 is schematic circuit diagram of a switching arrangement utilized in a second embodiment of the subject invention.

FIGS. 7—9 illustrate the transmitter portion of the second embodiment of this invention.

FIG. 10 illustrates the relative placement of FIGS. 7—9.

FIG. 11 is a schematic diagram illustrating the circuit board connections for the transmitter of FIGS. 7—9.

FIGS. 12—14 are a schematic diagram of the DC power supply utilized in the second embodiment of this invention.

FIG. 14A illustrates the relative placement of FIGS. 12—14.

FIGS. 15—19 are a schematic diagram of the coin and credit arrangement utilized in the second embodiment of this invention.

FIG. 20 illustrates the relative placement of FIGS. 15—19.

FIG. 21 is a schematic diagram illustrating the circuit board connections for the coin and credit arrangement of FIGS. 15—19.

FIGS. 22—25 are a schematic diagram of interface circuitry for the transmitter of FIGS. 7—9 and the coin and credit arrangement of FIGS. 15—19.

FIG. 26 illustrates the relative placement of FIGS. 22—25.

FIGS. 27; 27A and 28 are a schematic diagram of buffer circuitry between the transmitter and receiver portions of the second embodiment of this invention.

FIG. 29 illustrates the relative placement of FIGS. 27, 27A and 28.

FIGS. 30—32 are a schematic diagram of the receiver portion of the second embodiment of this invention.

FIG. 33 illustrates the relative placement of FIGS. 30—32.

FIG. 34 is a schematic diagram of the circuit board connections for the receiver of FIGS. 30—32.

FIGS. 35; 35A and 36; 36A are a schematic diagram of the interface circuitry leading to the memory circuit of the second embodiment of this invention.

FIG. 37 illustrates the relative placement of FIGS. 35, 35A and 36, 36A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although it should be recognized that this invention may be utilized in any type of vending arrangement, or even in selecting systems outside of the vending field, this description is undertaken of a preferred embodiment utilized in a coin-operated phonograph.

With reference to FIG. 1, it may be seen that the illustrated switching arrangement has two banks of switches: SA1—SA4 and SA11—SA14; and SB1—SB14. The switches in the "A" bank are all preset, the setting depending upon whether the closure of a single one of the switches SB1—SB4 is to represent an album or a single selection. As illustrated in FIG. 1, all of these switches are located in the album select position.

Each of the switches SB1—SB10 is actuated by a push button and represents the corresponding digit (1—0). The arrangement of the push button actuators is similar to that of a push button telephone, while the structure of the switch and associated structure is depicted and claimed in an application of Leon R. Britton and Joseph K. Semerjian entitled VENDING MACHINE SELECTING APPARATUS, which is assigned to the same assignee as this application. Switches SA1—SA4 are ganged with switches SA11—SA14 and switches SB11—SB14 are ganged with switches SB1—SB4 for use when any of the switches SA1—SA4 is in the album position.

Switches SB5—SB8 each have two blades a and b adapted to be moved to a closed position when a particular switch is actuated. Closure of these switches connects a pair of lines from the group of lines 15—21 to the collector of a transistor T3, each pair of connections being different from each other pair. In a similar fashion switches SB9 and SB10 connect respective pairs of lines from among lines 15—21 to the collector of a transistor T4. Further, if any of switches SA1—SA4 are placed in the single selection position, the corresponding switch SB1—SB4 will, when closed, connect an associated line from among lines 15—21 to the collector of transistor T3. Any of the switches SA1—SA4, when located in the album position, will connect the associated line to the collector of a transistor T2 when the corresponding switch from among SB1—SB4 is closed. Finally, if any of the switches SA11—SA14 is in the album position, closure of the corresponding SB11—SB14 switch will connect a line 23 to the collector of a transistor T1.

Each of the lines 15, 17, 19, 21, and 23 (hereinafter 15—23) is connected to a negative supply -B through a respective resistor 25, 27, 29, 31, or 33 (hereinafter 25—33). During inactivated status, the lines 15—23 are at or near the -B potential. However, upon closure of an appropriate SB switch when the transistor to which that switch is connected is conducting, the line will be grounded. Therefore, a positive-going pulse is produced on that line. Lines 15—23 have outputs 35, 37, 39, 41, and 43 (hereinafter 35—43), respectively.

Transistors T1—T4 have biasing signals applied to respective terminals G1—G4. The signal applied to ter-

terminal G3, in this embodiment, is an indication that sufficient credit has been deposited to make a single selection. If not used for this purpose, the signal applied to G3 would have to be provided to initiate operation of the device. When the signal is applied to terminal G3, a first digit can be designated by closing one of the switches SB5-SB8 (and SB1-SB4 if set for single selection). Upon closing of the SB switch, an identifying pattern of signals is formed on lines 15-21.

Referring now to FIG. 2B, it should be noted that the NOR gate 45 will produce an output when there is no information stored in register 47 (FIG. 2A). Upon initiation of operation a signal is applied to terminal 49 (FIG. 2A) to completely reset register 47, and thus NOR gate 45 would always produce an output at this time. If an album credit signal AC is also present, AND gate 51 will produce a biasing signal for terminal G1. Therefore, actuation of any switch SB11-SB14 (when SA11-SA14 are all in album position as shown) will produce an output on line 43. Of course, switches SB11-SB14 are ganged to switches SB1-SB4 and any actuation of a switch SB11-SB14 also means that a switch SB1-SB4 has been actuated. If an album credit signal AC is present, OR gate 53 will produce a signal at terminal G2, so that switches SB1-SB4 will produce an output signal if closed.

After a first digit has been designated and entered into register 47, the output of NOR gate 45 goes from a "1" to a "0". Thus, transistor T1 will become nonconducting. At the same time, the "0" appearing at the input to NOR gate 55 will result in a "1" appearing at the output thereof, and hence a signal will be applied to terminal G2 permitting an additional two digits to become available. In the embodiments disclosed herein, this invention utilizes three digit selection identifying numerals for choosing form among 160 record selections. To achieve the 160 combinations, two numbers are available for one digit of the identifying numeral, eight numbers are available for a second digit, and the full ten are available for the third digit. Therefore, it is not necessary to have SB9 and SB10 available for the first digit, and the signal appearing on G4 can be utilized to indicate that the first digit representation has entered register 47.

Upon closing one of the SB switches that is connected to a conducting transistor, a certain pattern of signals appears on outputs 35-41 of the switching arrangement. This pattern of signals consists of four binary signals which have a different pattern for each of the ten digits represented by switches SB1-SB10.

The signals on outputs 35-41 of the switch arrangement are conveyed to terminals 57, 59, 61, and 63 (hereinafter 57-63), shown in FIG. 2A. Terminals 57-63 are connected, respectively, to NOR gates 65, 67, 69, and 71 (hereinafter 65-71). The outputs of NOR gates 65-71 are connected, respectively, to a second set of NOR gates 73-79 and also to the S terminals of information storing and transferring units 81. The outputs of NOR gates 73-79 are conveyed to the R terminals of the respective units 81.

Each of the units 81 has R and S input terminals and Q and Q output terminals to which the R and S information is transferred. A direct reset terminal DR is provided to permit the unit to be returned to the stand-by state by application of an appropriate signal. It should

be noted that all of the DR terminals are connected to the "clear" terminal 49. There is also a clock terminal CLK. When a signal is applied to the clock terminal the data on the R and S terminals is transferred to the Q and Q terminals.

In the initial or quiescent state after a signal has been applied to terminal 49 to directly reset all the storage and transfer units 81, all of the NOR gates 57-63 have nothing but "0's" at the inputs thereof. Therefore, the outputs of these gates are "1's", which are connected to the S terminals of units 81. The NOR gates 73-79 convert the "1's" into "0's" which are supplied to the R terminals of units 81.

When a pattern of signals is supplied to terminals 57-63, a "1" on one of these terminals will reverse the signals applied to the corresponding R and S terminals.

All of the SB switches are ganged to switch SW1. When switch SW1 is closed, a current runs from a DC source B through a resistor 83 to a capacitor 85. A resistor 87 in parallel with capacitor 85 assists in regulating the charging rate of capacitor 85 and in providing a shunt path for discharging the capacitor when SW1 is open. The signal produced by this action is applied directly to a NOR gate 89, and to NOR gate 89 through a parallel path 91. The output of NOR gate 89 is passed to a NOR gate 93, which controls a one-shot multivibrator 95 to produce a clock signal on terminal 97 thereof and a "not clock" signal (i.e., the inverse of the clock signal) on terminal 99. Terminals 97 and 99 are connected to terminals 101 and 103, respectively, in FIG. 2A.

When a clock signal is produced by one-shot 95, the data on the R and S terminals of the units 81 in the first stage of the register 47 is transferred to the Q and Q terminals thereof. Thus, the coded first digit of the selection identification numeral is stored in the first stage of register 47. Due to the fact that there will have to be at least one "1" produced on a Q terminal of the units in this stage, the previously described operation of NOR gate 45 and the following elements will take place. Also, if there was no album credit signal AC initially, a signal would appear on terminal G2 at this time to permit utilization of switches SB1-SB4. Further, a check may be instituted at this time to determine if appropriate data has been recorded, and if not, a clear signal can be supplied to terminal 49.

When the next SB switch is actuated, the same sequence of operation occurs except that the data in the first stage (appearing on the R and S terminals of the second stage) is shifted to the Q and Q terminals of the second stage. The Q terminals of the second stage of register 47 are connected as inputs to a NOR gate 105. The output of NOR gate 105 is connected to the input of NOR gate 107. When the first digit data is transferred to the second stage, NOR gate 105 will cause NOR gate 107 to produce an output at terminal L2. This output is connected to an AND gate 109 and may also be utilized to indicate entry of the second digit. Again the register may be cleared if incorrect information has been entered.

Upon designation of the third digit by actuation an SB switch the same sequence is once again repeated with the data on the Q and Q terminals of the first and second stages being transferred to the Q and Q terminals of the second and third stages respectively. The

data on the Q terminals of units 81 in the last stage of the register is conveyed to NOR gates 111-117. These NOR gates also have an input from the "not clock" terminal 103. Thus, after the clock signal from one-shot 95 has subsided, the data in the last stage of the register will appear on output terminals 119-125.

At this time the "not clock" signal at terminal 99, together with the L2 signal, cause AND gate 109 to apply a signal to inverting amplifier 127. The signal from inverting amplifier 127 causes one-shot 129 to be activated. The output of one-shot 129 is conveyed directly to a NOR gate 131, and to NOR gate 131 through a parallel path 133. NOR gate 131 produces a signal which causes NOR gate 93 to actuate one-shot 95 to produce a clock pulse. This process is repeated to sequentially transfer the data from the register 47 to the output terminals 119-125. When the signal at L2 disappears, the process is terminated after one more clock pulse to clear the last data from the register.

All of the Q terminals of the last stage of the register are connected to a NOR gate 135, which in turn is connected to a NOR gate 137. Since at least one of the Q terminals must have a "1" on it, an output signal is produced by NOR gate 137. This signal is applied to NOR gates 65-71 to lock out the introduction of any additional data. In addition, this signal is supplied to a NOR gate 139 and a NAND gate 141.

NOR gate 139 and NAND gate 141 are located in a credit subtract circuit. NOR gate 139 also has an input from the clear line, while NAND gate 141 has another input from a NAND gate 143, which also has an input from the clear line. The output of NAND gate 141 is connected to a NOR gate 145, which is connected to NAND gates 147 and 149. NAND gate 147 provides a single selection subtract pulse, while NAND gate 149 provides an album subtract pulse. NAND gates 151 and 153 are also included in the circuit. A terminal 155 receives an output on line 43 from the SB11-SB14 switch arrangement. In operation, this circuit provides an album subtract signal from NAND gate 149 if a signal is applied to terminal 155, while a single selection subtract signal is obtained from NAND gate 147 if there is no signal 43 on terminal 155.

Referring now to FIG. 4A, it may be seen that the signals appearing on the terminals 119-125 are conveyed to terminals 157-163 of the receiver. These signals are conveyed through respective inverting amplifiers 165-171. The outputs of amplifiers 165-171 are conveyed to the K terminals of storage and transfer units 173 and to a second set of inverting amplifiers 175-181.

The input signals on terminals 157-163 are also conveyed to a NOR gate 183. At the output of NOR gate 183 there is an inverting amplifier 185. From inverting amplifier 185 signals are conveyed to the clock terminals of units 173 and to a one-shot multivibrator 187. Output signals from one-shot 187 are supplied to the reset terminals of units 173. This one-shot 187 automatically clears register 189 upon initial energization of the system and locks units 173 in the reset state. Also, one-shot 187 is actuated upon the arrival of data to unlock units 173, and has a time delay before returning to the lock condition that is sufficiently long to permit a regular data sequence to be registered and recorded.

As each coded digit arrives at terminals 157-163 it is entered into the first stage of register 189 and the other digits already entered are shifted by action of NOR gate 183 and inverting amplifier 185. If all three digits are not entered into register 189 within the time permitted by one-shot 187, register 189 is reset prior to recording of the data.

When all the data has been entered into register 189, a NOR gate 191 is actuated by the outputs from the last stage of the register. The NOR gate 191 in turn triggers a one-shot multivibrator 193, which unlocks a plurality of NOR gates N1-N20. One-shot 193 has a time duration less than that remaining on one-shot 187 if the code was properly entered.

Upon actuation of one-shot 193 the NOR gates N1-N20 decode the information stored in register 189 during the time provided by one-shot 193. The decoding is arranged to provide a control current for a memory circuit. This memory circuit may be identified as a selecting memory arrangement, such as that disclosed in U.S. Letters Pat. No. 2,923,553, issued on Feb. 2, 1960, in the name of Schultz et al. and assigned to the same assignee as the present invention.

With respect to FIGS. 6-40, a detailed description of the complete system utilizing the present invention will be undertaken. The embodiment of the invention utilized in this system differs somewhat from that described in the immediately preceding sections, but involves the same basic approach.

In FIG. 6 a slightly modified form of the elector switching apparatus depicted in FIG. 1 as illustrated. There are still the two banks of switches SB and SA, designated as SA0-SA3 and SB0-SB9. As previously described, the switches SA0-SA3 are album selecting switches that are ganged with switches SA10-SA13 respectively. All of the SA bank switches are illustrated in the album position so that album credit must be deposited in order to utilize switches SB0-SB3 for certain selecting operations.

As some switch combinations could provide a feedback problem, diodes D1 have been included for isolation purposes. Also, the input signals appearing on terminals T1-T5 are derived from the transmitter circuit, as will be described in more detail.

A common or master switch 201 is closed with each actuation of a switch in the SB bank. Switches 203 and 205 are operator actuated and serve to reset the transmitter when actuated by an operator. Thus, terminals T6 and T7 will be grounded when an operator desires to reset or clear the transmitter, and terminal T8 will be grounded with every actuation of a SB switch. The grounding of terminal T8 provides a main trigger signal for the transmitter circuit.

Terminals TA-TD will have signals appearing thereon representative of the SB switch that has been actuated. For ease of reference, the signals appearing on each of these terminals will hereinafter be referred to as "Data" and identified by the designated secondary letters (i.e., the signals appearing on terminal TA will be termed "Data A", the signals appearing on terminal TB will be termed "Data B", etc.). Terminal TE has a signal appearing thereon only when the SA switches are in the album select position.

Reference will now be made to FIGS. 7-10, which illustrate the transmitter. As in the embodiment illus-

trated in FIGS. 2A and 2B, this embodiment of the transmitter incorporates a register having flip-flops FF1-FF12. The flip-flops FF1-FF12 operate in the same fashion as flip-flops 81 in FIGS. 2A and 2B and hence will not be described again at this point. Data A, Data B, Data C, and Data D appear at pins PA, PB, PC, and PD, respectively, after passing through "one-shot" oscillators to provide fixed duration pulses. Data A is conveyed to terminal J of flip-flop FF1 through a NOR gate G11 and to terminal K of FF1 through NOR gate G11 and an inverting amplifier A1. In a similar fashion Data B is conveyed to terminals J and K of flip-flop FF2 through a NOR gate G12 and (to K) inverting amplifier A2, while Data C and Data D are conveyed to flip-flops FF3 and FF4 in a similar fashion.

Pins PA-PD are all connected to an AND gate G15, the output of which is conveyed to an AND gate G16. The output of AND gate G16 is conveyed to OR gate G17, the output of which is applied to the direct reset terminals DR of flip-flops FF1-FF12. The output of AND gate G16 is also applied to pin PE, which has a "1" thereon if an erroneous first digit is selected. A second input for OR gate G17 comes from pin PF through inverting amplifier A5, pin PF having a reset pulse thereon when the power is turned on, thus resetting all of the flip-flops in the register. This is accomplished by the "0" pulse appearing on pin PF being inverted by A5 and passed through OR gate G7 to the direct reset terminals of the flip-flops.

A main trigger signal, in the form of a pulse of definite duration, appears on pin PG from a main trigger one shot activated by closure of switch 201. This main trigger signal must be present for all future operations to occur and its presence will be assumed in the following description. This signal is applied to a NOR gate G18, the output of which is conveyed to the direct set terminal DS of the first flip-flop FF13 in a clock register 207.

Clock register 207 is a four-stage register comprising flip-flops FF13-FF16. A clock signal is supplied to pin PH from where it is conveyed to the clock terminals C of flip-flops FF13-FF16 through an inverting amplifier A6. The Q terminal of flip-flop FF14 is connected back to the K terminal of FF13 by a line 208. In the quiescent state, the J AND Q terminals would have "0's" thereon, while the K and Q terminals would have "1's" thereon. However, due to a feedback line 208 the K terminal of flip-flop FF13 would have the "0" from the Q terminal of flip-flop FF14 thereon, which causes the clock register to automatically reset itself. When the main trigger signal appears on pin PH the Q and Q terminals of FF13 will change to a "1" and an "0", respectively. On the next clock pulse the same change will be occasioned in FF14. In this fashion, the Q and Q terminals of FF14 will change state every two clock pulses supplied to pin PH, while the Q and Q terminals of FF15 will change state every third clock pulse on pin PH. Thus, a clock pulse will be supplied to the clock terminals of flip-flops FF1-FF12 two clock pulse periods after a selection button is pushed to close switch 201.

The clock signal on terminal PH is also conveyed to a NOR gate G19, which also receives input signals from the Q output of flip-flop FF14 and the Q output of flip-flop FF15. The output of NOR gate G19 is connected

to the clock terminals of flip-flops FF1-FF12 through line 210. As a result of the feedback line 208 and the reapplication of a main trigger signal on pin PG, a clock pulse will be applied to flip-flops FF1-FF12 for every four clock pulses appearing on pin PH.

The Q output of flip-flop FF16 is conveyed to OR gates G20-G23 via a line 209. OR gates G20-G23 also have inputs from the Q terminals of flip-flops FF9-FF12 which are passed through inverting amplifiers A7-A10, respectively. The outputs of OR gates G20-G23 are connected pins PW, PX, PY, and PZ, respectively.

The Q outputs of flip-flops FF9-FF12 are also applied to a NOR GATE G24, the output of which is passed through an inverting amplifier A11 and connected to NOR gates G11-G14. The signal from inverting amplifier A11 is also passed through another inverting amplifier A12 and applied to AND gate G15. In addition, the signal from inverting amplifier A11 is conveyed by line 211 to the J terminal of flip-flop FF13. Further, the signal at the output of A11 is conveyed by line 213 to an AND gate G25.

The outputs of the Q terminals of flip-flops FF1-FF4 are all connected to an OR gate G26, while the signals appearing on the Q terminals of flip-flops FF5-FF8 are all connected to an OR gate G27. The output of OR gate G26 is connected by line 215 to an inverting amplifier A13, an inverting amplifier A14, AND gate G25, and an AND gate G28. Inverting amplifier A13 is connected to AND gate G28, a NOR gate G29, and AND gates G30 and G31. Inverting amplifier A14 is connected to a pin PI and an OR gate G32. The output of OR gate G32 is connected to a pin PJ.

AND gate G25 has its output connected to a pair of AND gates G33 and G34. The output of AND gate G33 appears on a pin PK, while the output of AND gate G34 appears on a pin PL.

AND gate G28 is connected to a NOR gate G35, which is in turn connected to an OR gate G36. The output of OR gate G36 appears on a pin PM.

NOR gate G29 has its output connected to a NAND gate G37, the output of which is conveyed to an OR gate G38. The output of OR gate G38 appears on a pin PN.

The output of NAND gate G30 is connected to an OR gate G39, while the output of NAND gate G31 is connected to an OR gate G40. The output of OR gate G39 appears on pin PO, while the output of OR gate G40 appears on pin PP.

In a fashion similar to that discussed in connection with OR gate G26, the output of OR gate G27 is conveyed via line 217 to an inverting amplifier A15, an inverting amplifier A16, NOR gate G29, and NOR gate G35. Inverting amplifier A15 is connected to a pin PQ and an OR gate G44. The output of inverting amplifier A16 is conveyed via line 219 to an AND gate G41. AND gate G41 also has an input from an inverting amplifier A11 via line 211.

The output of NOR gate G19, which provides the clock pulse for flip-flops FF1-FF12 is also connected to an inverting amplifier A17 by means of a line 221. The output of inverting amplifier A17 is conveyed to a NOR gate G42, which has also an input from pin PR. The output of NOR gate G42 is connected to the S terminals of a pricing level register FF17. An input for the

R terminal of flip-flop FF17 is attained from OR gate G43. The Q terminal of flip-flop FF17 is connected to AND gate G33, while the $\bar{Q}$ terminal is connected to AND gate G34.

The inputs for OR gate G43 are obtained from AND gate G41 (via line 223) and from OR gate G17 (via line 225). OR gate G17 provides a direct reset pulse to flip-flops FF1-FF12. An OR gate G44, whose output appears on pin PS, has an input from pin PQ. The other input of OR gate G44 is the main trigger signal that appears on pin PG, which is conveyed through line 227. It should also be noted that the main trigger signal is applied to OR gate G32, OR gate G38, OR gate G36, OR gate G40, and OR gate G39.

The signal appearing on terminal PT is connected to the input of a NAND gate G31 and to an inverting amplifier A18. The output of inverting amplifier A18 is conveyed through line 229 to the input of NOR gate G18, which is connected to the direct set terminal of flip-flop FF13 in the clock register 207.

To follow the various pin connections referred to in connection with FIGS. 7-10, reference may be made to FIG. 11 wherein the pin connections are illustrated in some detail. The numerical pin designations in FIG. 11 have been noted in FIGS. 7-9 and are enclosed in circles. For example, pin PA has a circle number "8" adjacent thereto, and from FIG. 11 it may be seen that pin 8 is connected to a jack terminal RR through a resistor and that the signal appearing on jack terminal RR is the Data A input.

The operation of the transmitter portion of this embodiment of the invention can now be followed in some detail. Upon turning on of power to the system, a reset circuit (described in more detail hereinafter) supplies a pulse to pin PF. The pulse appearing on pin PF is a "0" which is converted to a "1" by inverting amplifier A5 and applied to OR gate G17, which then provides a "1" to the direct reset terminals DR of flip-flops FF1-FF12, in order to place all of these flip-flops in the initial or reset state.

The preferred embodiment of the invention disclosed herein is that of a vending machine, specifically a coin-operated phonograph. Operation of the selecting apparatus in such an environment is dependent upon the insertion of money or other credit indicia into the apparatus to obtain vending of the desired object or service. One type of coin and credit arrangement particularly useful in the present invention is that disclosed in the copending application of Edwin J Meixner entitled Credit Accumulating Arrangement, U.S. Pat. Application Ser. No. 759,407, filed on Sept. 12, 1968, and assigned to the same assignee as this application. The basic circuitry of this arrangement is illustrated in FIGS. 15-20.

The information obtained from the coin and credit system is applied to pins PT and PU. The information on pin PT relates to a lower level of credit, such as the price of a single selection in a phonograph, while the information on pin PU relates to a higher credit level, such as the cost of an album in a phonograph. Until a certain minimum credit level is reached, on pin PT, such as the price of a single selection of a phonograph, the system will be inoperative. This is true because the "0" on PT in the initial state, converted to a "1" by inverting amplifier A18, will be applied to NOR gate G18

to maintain a "0" on the direct set terminal DS of flip-flop FF13. Thus, the clock register 207 will not be energized and any Data supplied to pins PA-PD will not be entered into flip-flops FF1-FF4, since no clock pulse will be provided for these flip-flops from NOR gate G19. On the other hand, if sufficient minimum credit has been awarded, a "1" will appear on pin PT, which will be converted to a "0" at the input of NOR gate G18 by inverting amplifier A18. Therefore, if a selector button is pushed, the common switch 201 will be closed and the master trigger signal (a "0") will also be applied to NOR gate G18 so that a "1" will be applied to the direct set terminal DS of flip-flop FF13 to initiate operation of clock register 207.

If the minimum credit level has been reached, a "1" will appear on terminal PT and be applied to NAND gate G31. Since the other input of NAND gate G31 is normally a "1", derived by inverting (by means of inverting amplifier A13) the "0" appearing on the output of OR gate G26, NAND gate G31 will apply a "0" to OR gate G40. If a selector switch is pushed, the common switch 210 will supply a main trigger "0" to the other terminal of OR G40 so that an output signal (a "0") will be provided on pin PP. As previously indicated, all of the operations to be discussed hereinafter will depend upon existence of the main trigger signal, and thus in the subsequent discussion it will be assumed that a switch has been pushed in an appropriate fashion to close the common switch 201 and that a main trigger signal is present.

As may be seen from FIG. 11, a signal appearing on pin PP is connected to terminal T2 in FIG. 6, thus grounding the lower sides of switches SB1 and SB2, which are connected to terminals TC and TB, respectively. Since these switches correspond to the numerals 1 and 2 in the selecting nomenclature, depression of the button labeled 1 or the button labeled 2 will produce a Data output on the corresponding terminal TC or TB. Since the signal on pin PN has not changed, there will be no data production by the other sides of the switches SB1 and SB2, which are connected to terminal T1 and hence to pin PN, as may be seen from FIGS. 11 and 9.

Depression of button 1 or button 2 will cause the Data to be applied to a "one-shot" oscillator and hence to the appropriate pin PA or PB in FIG. 7. The Data appearing on pin PA or pin PB will be passed to the Q and $\bar{Q}$ terminals of the appropriate one of flip-flops FF1 or FF2 upon application of a clock signal to those flip-flops. The clock signal is produced by NOR gate G18, flip-flops FF13-FF15, and NOR gate G19, as discussed above.

If a button other than 1 or 2 should be pushed at this time, a signal would be produced on pin PE to turn on a reset and reselect indicator light. This occurs because no Data would be introduced on pins PA-PD by depression of such a button, and thus the "1's" at the input of AND gate G15 would not be changed and the output of G15 would remain a "1". Therefore, the input to AND gate G16 would be a "1", and when the clock pulse is applied to AND gate G16 a "1" would be produced at the output thereof to provide the signal on pin PE. This "1" appearing at the output of gate G16 would also be applied to OR gate G17 to cause a "1" to be applied to the direct reset terminal DR of flip-flops FF1-FF12 to

reset terminal DR of flip-flops FF1-FF12 to reset the entire register. The pulse on pin PE also serves to disable the main trigger one shot, as will be described in more detail hereinafter.

When a "1" appears on pin PE, the transmitter will be inoperable until the system is reset or recleared by operator closure of switch 203 or switch 205. This same type of operation could occur on the second digit if button 8 or button 9 is pushed, since there will be no output on pin PS, which is connected to terminal T5, until a second digit has been entered and OR gate G27 produces a "1" to be converted by inverting amplifier A15 to a "0" and then applied to OR gate G44. In addition, the same sequence of operation would occur upon choice of the second digit if one of the buttons 0-3 were depressed and there was no album credit signal on pin PU. This latter statement is, of course, based upon the positioning of the SA switches in the album position illustrated in FIG. 6.

Selection of a proper digit will prevent the production of a "1" on pin PE, since there would be a Data input (a "0") on at least one of pins PA-PD. Thus, a "0" would be produced at the output of AND gate G15 to insure that the output of AND gate G16 would remain a "0". Assuming that the first digit was properly selected by closing switch SB1 or SB2 and that the Data has been appropriately entered into flip-flop FF1 or flip-flop FF2, the second digit may now be entered. At this point pin PP has been returned to the quiescent state as a result of the signal produced by OR gate G26 upon entry of Data in one of the flip-flops FF1 or FF2. Pins PM and PN remain unchanged due to the lack of an album credit, (and in the case of pin PM, no other changes in the applicable signals) while pin PS remains unchanged due to the lack of a signal from OR gate G27. However, pin PJ now has gone from the quiescent "1" to a "0", as a result of the inverted output of OR gate G26 applied to OR gate G32. Since pin PJ is connected to terminal T4 in FIG. 6, it is apparent that a number from among 4-7 may be selected (numbers 0-3 are allocated to albums by the switch positions shown). Depression of a button corresponding to an appropriate number from among 4-7 will supply the appropriate Data input to pins PA-PD, and the Data will then be clocked into the appropriate flip-flops FF1-FF4, while the Data of the first digit will be clocked from flip-flop FF1 or flip-flop FF2 to flip-flop FF5 or flip-flop FF6.

At this point pin PP remains in the quiescent state to which it was returned upon entry of the first digit, while pin PN remains in the quiescent state due to the lack of an album credit. However, pin PM has now changed from a quiescent "1" to a "0" as a result of the signal produced by OR gate G27 and applied to NOR gate G35 to produce a "0" at the output thereof and hence make the output of OR gate G36 go to "0". Similarly, pins PS and PJ have "0's" thereon as a result of the signals produced by OR gates G26 and G27. As a result of these conditions, the terminals T2-T5 in FIG. 6 are all energized and a selection may be made by closing any of the switches SB0-SB9 by pressing the buttons corresponding to the numerals 0-9. Upon selection of any numeral by pressing the appropriate button, the Data in the first two stages of the register is transferred to the second and third stages, while the Data represen-

tative of the third digit is entered into the first stage. At this point, all of the Data in the register is automatically transmitted by operation of the clock register 207.

At this point the Data in the third stage of the register causes the output of NOR gate G24 to go to a "0", which is converted into a "1" by inverting amplifier A11 and applied to the J terminal of flip-flop FF13 to initiate operation of the clock register 207. At the same time, this "1" is passed through inverting amplifier A12 where it is altered into a "0" and applied to AND gate G15, thus changing the output of AND gate G15 to a "0". The "0" at the output of AND gate G15 is then applied to AND gate G16 to preclude a reset and reselect signal from being transmitted when a clock signal is applied to the other input of AND gate G16. In this fashion, the reset and reselect operation is disabled in the same manner that it is disabled by an input signal on any of pins PA-PD. This action also prevents resetting of flip-flops FF1-FF12 by transmittal of a signal through OR gate G17.

In the meantime, the Q terminal of FF16 has gone to a "0", so that the data in flip-flop FF9-FF12 appears on the appropriate ones of pins PW-PZ. The Q terminal of flip-flop FF16 then returns to a "1" to disable the signals appearing on pins PW-PZ. At this time, the clock pulse initiated by the signal from NOR gate G24 clocks the Data in the first and second stages of the register into the second and third stages, respectively. This produces another output of NOR gate G24 that initiates the production of clock pulse from the clock register to 207. One clock period later the Q terminal of flip-flop FF16 again goes to a "0", and the second digit appears on pins PW-PZ. Two clock periods later the pins PW-PZ are again disabled by a "1" on the Q terminal of flip-flop FF16. At the same time, the Data in the second stage of the register is transferred into the third stage and the whole cycle is repeated once more. Upon disabling of pins PW-PZ after the third digit has appeared thereon, the third digit is clocked out of the register and the system is ready to accept another selection.

The pricing level register FF17 is used as a detector to determine if a single or album debit pulse should be generated and transmitted to the price and credit unit. Since we have been discussing the operation for selection of a single, a single debit pulse should be generated. FF17 has not changed state during this transmission cycle, so that when AND gate G25 goes a "1" as a result of the signal from inverting amplifier A11, a single debit pulse will be produced on pin PL, since the other input of AND gate G34 is a "1" in the quiescent state.

Essentially the same operation is followed if an album should be selected, except that the second digit shall be selected from among the numerals 0-3, as opposed to being among the digits 4-7 in the case of a single. Upon selection of an album, a debit set "one-shot" oscillator produces a "0" on pin PR. This "0", when combined with a "0" from inverting amplifier A17, which results from NOR gate G19 upon production of a clock pulse, produces a "1" on the S terminal of FF17, thus causing the Q terminal to go to a "1" and the Q terminal to go to "0". Thus, when a "1" is produced by AND gate G25 upon completion of a selection, the debit pulse will be applied to pin PK rather than to pin

PL, which results in an album debit. Pricing level register FF17 is reset to its original state by a signal from OR gate G27 passing through converting amplifier A16, AND gate G41, and OR gate G43.

Referring now to FIGS. 12-14, various portions of the power supply circuitry are illustrated. In FIG. 12 there is illustrated a read and write power supply 231 and a pulse detector circuit 233. Both of these circuits 231 and 233 are utilized in conjunction with the apparatus that removes and plays the record selected by a customer. A particular system of this nature is illustrated and described in U.S. Pat. No. 2,923,553 - Schultz et al., issued on Feb. 2, 1960, entitled SELECTORS FOR AUTOMATIC PHONOGRAPHS, and assigned to the same assignee as this application.

An AC signal appearing across pins P1 and P2 is conveyed through diodes 235 and 237 (which form a full-wave rectifier) and a fuse 239 to a parallel RC network having a capacitor 241 and a resistor 243. One side of the RC network is connected to ground through line 245, while the other side, denoted by the terminal 247, provides a source of power on pin P3 for the "write-in" circuitry through resistor 249. This is the supply utilized to enter information into the controlling matrix of magnetic cores at the playing apparatus, when a selection identifying numeral is decoded at the receiver.

The voltage at terminal 247 is also applied across the series connection of resistor 251 and capacitor 253. The potential appearing at terminal 255 at the midpoint of resistor 251 and capacitor 253 is conveyed through resistor 257 to pin P4 to provide a source of power for the "read-out" circuitry associated with the playing mechanism. This power source signal is utilized upon motion of the carriage in the playing apparatus to test the cores of the controlling matrix to determine if selecting information has been entered therein.

The potential at terminal 255 is also connected to pin P5 through a resistor 259. This voltage provides a source of power utilized in disabling the "read-out" circuitry in the playing apparatus under certain predetermined conditions.

If a magnetic core subjected to a "read-out" pulse was previously energized by a "write-in" pulse, the "read-out" pulse will cause a change of state of that core which results in a trip relay being actuated. Actuation of the trip relay is produced when a signal on pin P8 is conveyed to the pulse detector circuit 233. The signal on pin P8 is applied to the gate of a silicon controlled switch 269 through a resistor 273, the signal being taken from across resistor 275 and capacitor 271 in parallel. One power terminal of the silicon controlled switch 269 is connected to pin P6 through a diode 261, the other power terminal being connected to the ground of the magnetic core circuitry in the record playing apparatus, this ground appearing on pin P7. The signal obtained from silicon controlled switch 269 is formed across capacitor 263, which is connected in parallel with the series combination of a resistor 265 and capacitor 267. Capacitors 263 and 267 maintain the output signal in order to insure that the trip relay coil (not shown) is actuated by the signal on pin P6.

In FIG. 13 and portion 277 of FIG. 14, there are illustrated the various DC supply arrangements utilized to energize this embodiment of the invention. An AC line voltage is applied to pins P9 and P10. The AC voltage

on pins P9 and P10 is applied to diodes 279, 281, 283, and 285, which provide a full-wave rectifying function. The positive portions of the rectified signal passing through diodes 279 and 281 are applied to a capacitor 287 through a fuse 289. The other side of capacitor 287 is connected to the chassis ground on pin P20 through line 291.

The signal appearing across capacitor 287 also appears across a series combination of resistor 293, resistor 295, Zener diode 297, Zener diode 299, and diode 301. Zener diodes 297 and 299 each have a breakdown voltage of 13 volts and diode 301 has a voltage drop of 0.7 volts, so that the regulated potential at point 303 is 26.7 volts. This 26.7 volt potential is connected to pin P11 via line 305 and then applied to the base of a first power transistor (not shown). The potential on the collector of the first power transistor is obtained from the midpoint of resistors 293 and 295 and appears on pin P12. The emitter of the first power transistor is connected to pin P13 and constitutes a regulated voltage of +27 volts. This positive supply of 27 volts is connected by line 307 to a combination of a capacitor 309, a resistor 311 and a Zener diode 313, resistor 311 and Zener diode 313 being connected in series across capacitor 309. Zener diode 313 has a breakdown voltage of 8.2 volts, and hence a regulated voltage of 8.2 volts is obtained from between resistor 311 and Zener diode 313 from where it is conveyed to pin P14.

What amounts to practically a mirror image of the circuit thus described is illustrated in FIG. 14 to obtain the negative supply voltages. The AC line voltage appearing on lines 315 and 317 has the negative portions thereof passed through diodes 283 and 285 to a capacitor 319. A fuse 321 is connected between diodes 283 and 285 on the one hand and capacitor 319 on the other. The potential appearing across capacitor 319 is an unregulated -27 volts that is conveyed to pin P15 by line 323.

The unregulated -27 volt potential on pin P15 is also connected across the series combination of resistor 325, resistor 327, Zener diode 329, Zener diode 331, and diode 333. The potential appearing at the midpoint of resistors 325 and 327 is conveyed via line 335 to pin P16, from where it is connected to the collector of a second power transistor (not shown). Zener diode 329 and 331 each have a voltage breakdown of 13 volts, and diode 333 has a voltage drop of 0.7 volts, so that a potential of 26.7 volts (negative) is conveyed to pin P17 through line 337. Pin P17 is also connected to the base of the second power transistor. The emitter on the second power transistor is connected to pin P18 and then, via line 339, to a capacitor 341. A series combination of resistor 343 and Zener diodes 345 and 347 is connected in parallel with capacitor 341. Zener diode 345 has a breakdown voltage of 6.8 volts, while Zener diode 347 has a breakdown voltage of 6.2 volts, so that a regulated negative potential of 13 volts is conveyed to pin P19 via line 349.

It should be noted that the chassis ground is obtained from a pin P20.

At the bottom of FIG. 14 there is illustrated a reset circuit 351. This reset circuit is the source of the signal applied to pin PF in FIG. 7 to insure that all of the flip-flops FF1-FF12 are set to the initial or quiescent state upon power being connected to the system.

When the system is turned on, the -27 volt supply voltage is connected to the emitter of the transistor in the reset circuit 351. The negative supply potential on pin P18 and line 339 is also connected to a capacitor 353, which charges through resistors 355 and 357. The bias voltage for the base of transistor Q1 is obtained from the midpoint of the resistors 357 and 359, which are connected in series from line 339 to ground. The potential at the midpoint of resistors 357 and 359 is connected to the base of transistor Q1 through a Zener diode 361. Another resistor 363 connects the emitter of transistor Q1 to ground. Since resistor 357, along with resistor 355 and the size of the capacitor 353, determines the charging rate of capacitor 353, and since resistor 357 in conjunction with resistor 359 determines the base bias voltage on transistor Q1, resistor 357 must be carefully chosen to adequately perform both functions.

When the -27 volts appears on line 339 as a result of turning on the system, capacitor 353 begins to charge through resistors 355 and 357. After capacitor 353 has charged to the point that the voltage drop across resistor 359 is approximately 20.7 volts, Zener diode 361 will break down and begin to conduct. This initiates conduction of transistor Q1, which in turn produces a voltage of approximately -26.6 volts across resistor 363. This negative reset voltage is passed to pin P21 and subsequently conveyed to pin PF to reset all of the flip-flops FF1-FF12.

If the potential on line 339 drops below 20 volts, Zener diode 361 will again block current flow and thus cause transistor Q1 to turn off. With transistor Q1 turned off, no voltage appears across resistor 363 and the reset signal is removed from pin PF. As soon as the potential on line 339 returns to its correct level of -27 volts, Zener diode 361 will again be caused to break down and the reset voltage will appear across resistor 363 and be conveyed to pin PF.

FIGS. 15-20 illustrate the price and credit arrangement utilized in conjunction with the present invention. The structure and operation of this circuitry will not be discussed at this point, as it is fully described in the co-pending applications of Edwin J. Meixner, entitled CREDIT ACCUMULATING ARRANGEMENT, U.S. Pat. Application Ser. No. 759,407, filed on Sept. 12, 1968, and of Casimer J. Dabrowski, entitled BONUS CREDITING SYSTEM, U.S. Pat. Application Ser. No. 759,270, filed on Sept. 12, 1968, both of which are assigned to the same assignee as this application. However, reference will be made to FIG. 21 in order to describe the interconnections of this arrangement with the remainder of the system.

The pin designations in FIG. 21 are indicated by the circled numerals in FIGS. 15-19.

Of primary importance with respect to the present invention are the arrangements for providing single and album credit signals to the transmitter and the handling of the debit pulses produced by flip-flop FF17 in FIG. 9. With respect to the single and album credit level controls, it may be noted in FIG. 17 that the outputs of the OR and AND gate combinations which indicate when a specified credit level has been reached are connected to pins 10-15 in FIG. 21. All of the signals appearing on these pins are conveyed to a pricing board. Circuitry at the pricing board will determine the amount of credit needed to make a single or album

selection. As a simple example, it could be determined that a single may be purchased for 10 cents, so that the second credit level is needed as a minimum credit level. If a dime is deposited, this would be indicated on the output of OR gate G72, which is connected to pin 11 in FIG. 21. This pulse would be passed through the pricing board circuitry and then conveyed to pin PT at the transmitter (FIG. 9) to permit operation of the transmitter. In a similar fashion, the selected album pricing information would be conveyed to pin PU in FIG. 9.

With respect to the debit pulses produced on pins PK and P1 in FIG. 9, they are conveyed to pins 28 and 27 in the FIG. 21 structure. As may be seen in FIG. 17, pins 27 and 28 are connected to AND gates G66 and G67, respectively. When the debit pulses cause AND gate G66 to produce an output, it is conveyed through inverting amplifier A29 to pin 24, while AND gate G67 similarly will supply a signal to pin 25 through inverting amplifier A32, if it is actuated. The signals appearing on pins 24 and 25 are conveyed to the pricing board, where the debit pulses are conveyed through appropriate circuitry to provide the appropriate inputs for completing a complementary addition function. Thus, the signals from the pricing board will be conveyed to appropriate pin or pins 4-8 in FIG. 21.

Referring now to FIGS. 22-25, a number of different circuits utilized to provide a variety of functions are illustrated. This circuitry is the so-called "interface" circuitry for the transmitting and pricing portions of the system.

At the top of FIGS. 22 and 23 there are illustrated credit monostable multivibrator oscillator circuits ("one-shots") 401, 403, 405 and 407. These "one shots" serve to shape the pulses coming from the coin switches before being applied to the credit arrangement illustrated in FIGS. 15-19. Also, the "one shots" are designed to prevent coin "bounce" from causing unwarranted awarding of credit due to false switch closures or noise effects. Such a feature is necessary as a result of the sensitivity and fast acting capabilities of the credit arrangement used herewith.

The particular coins utilized will, of course, depend upon the currency involved and upon the price levels desired. However, for purposes of this particular description, it will be assumed that nickels, dimes, quarters, and half dollars are being utilized.

A negative 27 volt supply potential is connected throughout the system on line L10. This 27 volt potential may be obtained from pin P18 in the DC power supply of FIG. 13. Similarly, a chassis ground is provided throughout the system on line L12, and one possible connection for such a ground would be to pin P20 in the DC power supply in FIG. 14.

"One shot" 401 is the nickel or 5 cent "one shot," and a coin pulse is applied to pin P119 from an appropriate coin switch. The pulse appearing on pin P119 is connected to a midpoint of series connected resistor 409 and capacitor 411. This pulse is also supplied to a diode 412, which is connected from the midpoint of resistor 409 and capacitor 411 to the base of a transistor Q10. The emitter of Q10 is connected to ground, while the collector thereof is connected to the negative 27 vote potential through a resistor 414. The collector of transistor Q10 is also connected to a capacitor 413, the other side of which is connected to a diode 415 and a

resistor 416. Diode 415 is also connected to the base of a transistor Q11. Transistor Q11 has a collector load resistor 417, and the collector is connected to the base of another transistor Q12. Transistor Q12 has a collector load resistor 419, and the collector of a transistor Q12 is connected to pin J3-G.

In the quiescent state transistors Q10 and Q11 are normally conducting, while transistor Q12 is in a non-conducting state. Upon application of a positive going pulse to pin P119, transistor Q10 will be cut off, which will cause the collector voltage of transistor Q10 to go to approximately -27 volts. The -27 volts appearing on the collector of transistor Q10 will cause capacitor 413 to charge through diode 415 and the base of transistor Q11, thereby driving transistor Q11 further into saturation. After the coin switch opens for a period of time determined by capacitor 411 and resistor 409 (3 milliseconds in this example), Q10 turns on and capacitor 413 discharges through transistor Q10. Discharge of capacitor 413 removes the driving voltage from the base of transistor Q11, thus turning it off.

As transistor Q11 ceases to conduct, its collector potential will go toward the negative supply voltage of -27 volts, thus turning on transistor Q12. As transistor Q12 begins to conduct, its collector potential will go from -27 volts to ground, thus producing a positive going of "0" pulse on pin J3-G. An output will continue to be taken from the collector of transistor Q12 as long as transistor Q11 is turned off, which depends upon the discharge rate of capacitor 413 through transistor Q10. Thus, a definite duration pulse is produced at pin J3-G.

By reason of the delay before transistor Q10 returns to a conducting state, erroneous credit awards due to coin "bounce" or stray noise are greatly reduced. Therefore, a monostable oscillator that does not depend upon regeneration is provided to develop standard duration credit pulses while eliminating most of the coin "bounce" and noise problems.

Each of the "one shots" thus produces a credit pulse upon closure of an associated coin switch. "One shot" circuit 403 responds to a dime pulse on pin P120 to produce an output on pin J3-F, "one shot" circuit 405 responds to a quarter pulse on pin P123 to produce an output on pin J3-B, and "one shot" circuit 407 responds to a half dollar pulse on pin P122 to produce an output on pin J3-E. The output pulses on pins J3-G, J3-F, J3-B, and J3-E, together with a dollar credit signal on J3-H, are conveyed to appropriate ones of the pins 4-8 in FIG. 17 for insertion in the credit arrangement.

It should be noted that "one shot" circuit 407 differs slightly from the other "one shot" circuits, but that the operation is essentially identical except for the AC coupling between stages. In this arrangement the signal from the half dollar coin switch is applied to the junction of series connected resistor 421 and capacitor 423 and passed to the base of a transistor Q13 through a diode 425. Transistor Q13 has a collector load resistor 427, and the collector of transistor Q13 is connected to the base of a transistor Q14 through a capacitor 429 and a diode 431. The juncture of capacitor 429 and diode 431 is connected to ground through a resistor 433. The base of transistor Q14 is also connected to ground by a resistor 435, while a collector load resistor 437 is connected to the negative supply. In this circuit,

turning off of transistor Q13 by a credit switch input causes transistor Q14 to conduct until capacitor 429 is charged through the base of transistor Q14, diode 431, and resistor 427, thus producing a shaped pulse output on pin J3-E, while still preventing the coin "bounce" and noise problems.

Illustrated at the bottoms of FIGS. 22 and 23 are Data "one shots" 439, 441, 443, and 445. "One shot" 439 is the Data D "one shot", "one shot" 441 is the Data C "one shot", "one shot" 443 is the Data B "one shot", and "one shot" 445 is the Data A "one shot." As all of these "one shots" utilize the same circuit, the operation of only one circuit will be described in detail.

It should be noted that each of these "one shot" circuits is virtually identical to "one shot" 407, except for a diode connected from an input voltage divider to the collector of the output transistor. Specifically, each of the Data "one shots" includes a pair of transistors Q15 and Q16. Each of the "one shots" has an input derived from the selector switch arrangement illustrated in FIG. 6, the Data D one shot 439 obtaining its signal from pin J2-BB. In the Data D one shot 439, a series combination of resistor 447, resistor 449, and a capacitor 451 is connected between the negative supply and ground. The Data D input signal is connected to the point between resistor 449 and capacitor 451, which is tied to the base of transistor Q15.

Transistor Q15 has a collector load resistor 453, while the emitter thereof is connected to ground through diode 455 and resistor 457. The collector of transistor Q15 is connected to the base of transistor Q16 through a capacitor 459 and a diode 461. The midpoint of capacitor 459 and diode 461 is connected to ground through a resistor 463. The base of transistor Q16 is also connected to ground by resistor 465.

Transistor Q16 has a collector load resistor 467, and its collector output appears on pin J2-X. A diode 469 is connected between the collector of transistor Q16 and the midpoint of resistors 447 and 449. This connection of diode 469 assists in driving the collector of Q16 toward ground potential when it is turned on, thus speeding up the leading edge of the pulse applied to pin J2-X.

As the operation of this "one shot" is essentially the same as that previously discussed, no further description is necessary at this time. It should merely be noted that when transistor Q16 is caused to conduct, a "0" appears on pin PD in FIG. 7. Data C "one shot" 441, Data B "one shot" 443, and Data A "one shot" 445 produce similar outputs on the pins as noted, so that "0's" are applied to the appropriate pins PA, PB, or PC in FIG. 7 when the corresponding "one shot" is activated. The inputs for these "one shot" circuits are obtained from the appropriate switches in the selecting switch arrangement illustrated in FIG. 6.

Referring now to FIG. 24, there is illustrated a main trigger "one shot" 471 and a debit set "one shot" 473. As these "one shot" circuits are essentially the same as the credit and Data "one shots", they will not be discussed in detail at this point. It should merely be noted that the main trigger signal from switch 201 in FIG. 6 is applied to "one shot" 471 (the main trigger signal appears on pin J2-WW). One shot 471 shapes the main trigger signal to one which is conveyed to pin PG in FIG. 8 (from pin J2-B in FIG. 24). Similarly,

debit set "one shot" 473 obtains an input signal from terminal TE in FIG. 6 upon selection of an album. This signal is shaped and applied to pin J2-HH in FIG. 24, from where it is conveyed to pin PR in FIG. 9 and applied to NOR gate G42 to activate flip-flop FF17 for production of an album debit pause upon completion of an album selection.

Referring now to FIG. 25, there is illustrated a clock circuit 475 for producing clock pulses on pin J2-U, which are then conveyed to pin PH in FIG. 8 to be applied to the clock register 207. This clock oscillator circuit 475 is based on a programmable unijunction transistor 477. This programmable unijunction transistor is essentially the same as a conventional unijunction transistor, except that the "eta" thereof can be controlled by means of the voltage divider comprising resistors 479 and 481. The midpoint of the voltage divider formed of resistors 479 and 481 is connected to terminal 482 of the programmable unijunction transistor 477 by means of a diode 483, this terminal also being connected to a negative potential source by a resistor 485. Terminal 486 of the unijunction transistor 477 is connected to the negative source by a resistor 487. The gate terminal of programmable unijunction transistor 477 is connected between a capacitor 489 and a resistor 491, which are connected in series between the negative source and ground.

When power is applied to the system, capacitor 489 begins charging through resistor 491. When capacitor 489 has charged sufficiently, programmable unijunction transistor 477 is fired, which causes a current through resistor 481, diode 483, programmable unijunction transistor 477, and resistor 487. This causes the potential at the midpoint of resistors 479 and 481 to go toward the negative supply potential. The negative going pulse is passed through capacitor 493 and developed across a resistor 495 in parallel with the base of transistor Q17 to ground. A diode 497 serves to discharge capacitor 493 when programmable unijunction transistor 477 is turned off, thus sharpening the trailing edge of the pulse. The negative pulse appearing at the base of transistor Q17 causes transistor Q17 to conduct and produce a positive going "0" across transistor Q17. The positive going pulse across transistor Q17 is conveyed to pin J2-U, from whence it is conveyed to the transmitter. After capacitor 489 has discharged sufficiently, programmable unijunction transistor 477 is returned to its quiescent state and the cycle is repeated. In this fashion, a free running clock oscillator is produced to provide clock pulses to the clock register.

As money is deposited and credit awarded, lights are lit to indicate whether the credit accumulated is sufficiently great to select a single or album. The circuitry for controlling these lights is illustrated in FIG. 24, wherein circuit 499 is a single light controlling circuit, while circuit 501 is an album light controlling circuit. These circuits are identical and comprise a pair of transistors Q18 and Q19. Inputs for these circuits are obtained from the corresponding single level and album level inputs (appearing on pin J3-C and J3-I respectively). As referred to above, the amount of credits necessary to give a single level indication is determined by the pricing board, and when appropriate credits have been deposited, a signal will appear at the input to single light controlling circuit 499.

The incoming signal is conveyed through a resistor 503 to the base of transistor Q18. The signal applied to the base of transistor Q18 causes this transistor to begin conduction, thereby causing a voltage drop across resistor 505. The drop across resistor 505 brings the emitter potential of transistor Q18 to essentially -27 volts, and this potential is applied to the base of transistor Q19 through resistor 507. The signal applied to the base of transistor Q19 causes transistor Q19 to begin conduction, and a signal is produced on pin P101 which is then conveyed to the single light. Exactly the same operation occurs with respect to the album light controlling circuit 501, except that the output signal is applied to pin 107 to be conveyed to the album light.

It is also helpful to inform the customer when he has failed to deposit enough money to make any selection. This is accomplished by a "deposit more money" light controlling circuit 521 illustrated in FIG. 24. Circuit 521 utilizes a silicon controlled switch 523, one side of which is connected to ground through transistor Q22. A bias for the base of transistor Q22 is obtained from diode 535, resistor 533, diode 531 and resistor 529. The base of transistor Q22 is also connected to the collector of transistor Q23 by a diode 531. The collector of transistor Q23 is connected to pin P118 through a resistor 533 and a diode 535. Pin P118 receives a reset signal from pin P21 in FIG. 14.

The base of transistor Q23 is connected to pin J3-C through a resistor 537 and a diode 539, and to ground through resistor 527. Pin J3-C has a signal applied thereto from the single level output of the pricing board, which indicates that credit equal to or greater than the price of a single has been deposited.

The gate of the silicon controlled switch 523 is connected to one of the power terminals of the switch by a parallel arrangement of a resistor 541 and a capacitor 543. The gate of SCS 523 is also connected to appropriate credit level indicators by a resistor 545. In this particular embodiment, it will be assumed that the lowest level at which a selection may be made is two for a quarter. Thus, it will be necessary to inform the customer that he cannot make a selection until this amount of money is deposited, and if he should deposit less than that amount the indicator light will come on to inform him that he must deposit more money before making a selection. With this particular example, the gate of the silicon controlled switch 523 is connected to pins J3-G and J3-F, which have signals thereon from the credit arrangement illustrated in FIGS. 15-19 representing the deposit of a 5 cent credit increment and a 10 cent credit increment, respectively.

When the system is first turned on, transistor Q22 is in a non-conducting state, thus insuring that silicon controlled switch 523 is also maintained in an off state. After the delay built into the reset circuit, the negative supply potential of -27 volts appears on pin P118. This negative voltage initiates conduction of transistor Q22. If a nickel or dime is now deposited, the resulting pulse on pin J3-G or pin J3-F will trigger silicon controlled switch 523 to conduct, thus producing an output on pin P108 which is conveyed to the "deposit more money" light. When sufficient credit has been awarded to exceed the minimum necessary credit, the single level signal on pin J3-C will initiate conduction of transistor Q23, thus removing the base drive from transistor Q22. Removing the base drive from transistor Q22 causes it

to return to a non-conducting state, thus turning off silicon controlled switch 523 and the "deposit more money" indicator light.

In addition to indicating whether sufficient credit has been awarded to obtain singles or albums selections, or to obtain any selection, there are also indicator lights to let a customer know that individual characters or digits have been accepted, before entry of the complete selection identifying format or numeral. These circuits are illustrated in FIG. 25, where circuit 509 is a first digit light controlling circuit, and circuit 511 is a second digit light controlling circuit. As both of these circuits are identical, only the first digit light controlling circuit 509 will be described in detail.

First digit light controlling circuit 509 has a pair of transistors Q20 and Q21, with an input being supplied to the base of Q20 through a resistor 513. The input signal to the base of transistor Q20 is obtained from pin J2-SS. The signal occurring on pin J2-SS is derived from OR gate G26 in FIG. 7. It will be remembered that OR gate G26 produces an output when a digit has been inserted into the first stage of the transmitter register. A bias is obtained for the base of transistor Q20 through resistor 515. Further, the emitter of transmitter Q20 is biased through resistor 517. The emitter voltage on Q20 is connected to the base of transistor Q21 through a resistor 519.

When a first digit is entered into the transmitter register, OR gate G26 produces an output which is applied to the base of transistor Q20. This signal initiates conduction of transistor Q20 so that the emitter thereof goes essentially to the negative supply potential. This negative voltage on the emitter of transistor Q20 is conveyed to the base of transistor Q21 to initiate conduction of that transistor. Conduction of transistor Q21 results in a signal being applied to the first digit light via pin P116.

By giving this visual indication to the customer that his selection is being recorded as he selects each digit, rather than his having to wait until the entire selection is entered to determine if the appropriate information is being received, the apparatus is made much more appealing. Elimination of the frustration that results when a complete selection is made and nothing happens, without being able to tell what went wrong, increases the consumer appeal of such a machine. Further, such an arrangement assists a customer in determining where a mistake was made in entering his selection.

In view of the fact that certain numerals are not available for selection as the first and second digit of a selection identifying numeral, it is desirable to inform the customer if he makes an erroneous selection. Further, it is necessary to disable the system so that no further selections may be made until the system has reset at a proper number chosen. (An alternative approach is to automatically select at random a proper digit.) These functions are performed by the reset and reselect circuit 547 illustrated in FIG. 25.

This circuit employs a silicon controlled switch 549 connected in series with a transistor Q24. The base of transistor Q24 is biased through a resistor 551, connected to pin J2-OO through resistor 553 and diode 555, and connected to pin P118 through resistor 553, a resistor 557, and line 559.

The gate of SCS 549 is connected to ground through capacitor 561. In addition, the gate of SCS 549 is connected to one of the power terminals thereof through resistor 563 and capacitor 565, in parallel. The gate of SCS 549 is also connected to the collector of a transistor Q25 through a resistor 567.

A bias for the base of transistor Q25 is obtained from a series connection of resistor 569, Zener diode 571 and resistor 573. The juncture of resistor 569 and Zener diode 571 is connected to the base of transistor Q25, while the juncture of Zener diode 571 and resistor 573 is connected to pin J2-MM.

The power terminal of SCS 549 on the side opposite transistor Q24 is connected to a line 575, which is connected to pin P117 and the collector of the first transistor Q26 in the main trigger "one shot" circuit 471 through a diode 577.

When power is initially turned on, transistor Q24 will not be conducting and thus will prevent firing of the silicon controlled switch 549. However, after the delay built into the reset circuit shown in FIG. 14, a reset voltage will appear on pin P118, which is connected to the base of transistor Q24 through line 559, resistor 557, and resistor 553. This voltage will cause transistor Q24 to conduct and permit firing of SCS 549. If an erroneous number is selected at this time, the pulse produced at the output of AND gate G16 and applied to pin PE in FIG. 7 will appear at pin J2-MM and initiate conduction of transistor Q25. Conduction of transistor Q25 will fire SCS 549 to ground line 575 and pin P117 to energize the reset and reselect indicator light. In addition, grounding of line 575 disables transistor Q26 in the main trigger "one shot" 471 by grounding the collector thereof. By precluding the application of a main trigger pulse to line 227 in FIGS. 8 and 9, the transmitter is rendered inoperative.

In order to again enable the main trigger "one shot" 471, it is necessary for the customer to close switches 203 and 205 in FIG. 6, which will produce a signal on pin J2-OO. This signal shuts off transistor Q24, which in turn shuts off silicon controlled switch 549 to return the reset and reselect circuit to its quiescent state.

With reference now to FIGS. 27 and 28, there are illustrated buffer circuits 601, 603, 605, and 607. Each of these buffer circuits is associated with a particular Data line, buffer 601 being the Data A buffer, buffer 603 being the Data B buffer, buffer 605 being the Data C buffer, and buffer 607 being the Data D buffer.

All of the buffer circuits are identical, and since they consist of conventional circuitry will not be discussed in detail at this point. However, it should be noted that the Data outputs of the console transmitter (pins PW, PX, PY, and PZ in FIG. 7) are connected to the anode of a diode 609 through a resistor 611, a transistor Q30, and a diode 613. On the other hand, Data being transmitted from a remote selector is connected to the cathode of diode 609 through resistors 615 and 617. This approach is utilized in order to maintain operation of the console if the remote transmission line should become grounded or otherwise malfunction.

The signals conveyed to the receiver from the collector of transistor Q31 are buffered to eliminate high frequency noise spikes and isolate the logic input circuitry from undesired transients.

The receiver of this selecting system may be described by reference to FIGS. 30-32. The Data A-Data D information arrives from the transmitter via the buffer circuits at pins P301-P304. The Data inputs are passed through inverting amplifiers A50-A-53 and conveyed to the receiver register comprising flip-flops FF50-FF61.

The Data inputs on pins P301-P304 are connected to an AND gate G100. The presence of a data input on any of pins P301-P304 will change the output of AND gate G100 from a "1" to a "0". This "0" is conveyed both directly to the K terminal of a flip-flop FF62 and also to the J terminal of flip-flop FF62 through an inverting amplifier A55. The "1" appearing at the output of inverting amplifier A55 is also conveyed to a "one shot" OS10. "One shot" OS10 is also connected to a pin P305. The "1" applied to "one shot" OS10 triggers the "one shot" and causes its output to go from a "1" to a "0". The "0" at the output of "one shot" OS10 is conveyed to an AND gate G101. Since the output of AND gate G101 is a "1" in the quiescent state, flip-flops FF50-FF61 are maintained in the reset condition by the signal applied to the direct reset terminals DR and by AND gate G101. Thus, the signal from "one shot" OS10 releases flip-flops FF50-FF61 so that they can be actuated to change state.

The signal output of "one shot" OS10 will be supplied to AND gate G101 for a definite time period determined by the circuitry to pin 305 of "one shot" OS10. If all three digits have not been entered in the receiver register by the end of the time period determined by "one shot" OS10, the transmitted numeral will not be accepted and the receiver flip-flops FF50-FF61 will be reset to the quiescent state.

Since the normal state of flip-flop FF62 is a "0" on the J terminal and a "1" on the K terminal, the signals from AND gate G100 prepare flip-flop FF62 for a change of state when clocked. A clock signal is obtained from pin P306 and passed through inverting amplifier A56 to the clock terminal of flip-flops FF62, and also to the clock terminal of a flip-flop FF63. Thus, upon the next clock pulse the "1" will be transferred to the Q terminal and the "0" will be transferred to the Q terminal of flip-flop FF62. The "0" on the Q terminal of flip-flop FF62 is conveyed to a NOR gate G102. Since the other input of NOR gate G102 is from the Q terminal of flip-flop FF63, which is normally a "0", it means that the output of NOR gate G102 will be changed from a "0" to a "1" when the Q terminal of FF62 goes to "0". Therefore, when the next clock pulse appears at AND gate G103, a "1" will be applied to the clock terminals C of flip-flops FF50-FF61. This clock pulse will cause the Data appearing on the pins P301-P304 to be entered into flip-flops FF50-FF53.

If the second digit does not arrive at pins P301-P304 before the end of the time period determined by "one shot" OS10, the receiver register flip-flops FF50-FF61 will all be reset to the quiescent state. However, if the second digit arrives before the expiration of the time period determined by "one shot" OS10, another clock pulse will be generated, the Data in the first stage of the receiver register will be transferred to the second stage, and the Data appearing on pins P301-P304 will be entered into the first stage of the register. The same sequence of events will occur to enter the third digit

into the receiver register, if it arrives before expiration of the time period determined by the "one shot" OS10.

If all three digits are entered into the receiver register before expiration of the time period determined by the "one shot" OS10, the resultant Data outputs from flip-flops FF58-FF61 will cause NOR gate G104 to produce a "0" output. The "0" output of NOR gate G104 is connected directly to the K terminal of a flip-flop FF64 while this same output is connected to the J terminal of flip-flop FF64 through inverting amplifier A57. Since in the quiescent state the K terminal is at a "1" and the J terminal is at a "0", the output of NOR gate G104 conditions flip-flop FF64 for a change of state upon the arrival of the next clock pulse on line 635.

When the "1" on the J terminal of flip-flop FF64 is transferred to the Q terminal thereof, it is applied to NOR gate G105, causing the output thereof to go from a "1" to a "0". The "0" at the output of NOR gate G105 is conveyed via line 637 to OR gate G106. OR gate G106 also has an input from the Q terminal of flip-flop FF63, which is conveyed on line 639 from FF63 to OR gate G106.

The Q terminal of flip-flop FF63 will change from a "1" to a "0" upon generation of the second clock pulse after arrival of data at pins P301-P304. Therefore, at that time (i.e., two clock pulses after the arrival of Data), OR gate G106 will have two "0's" at its inputs, and thus its output will go from a "1" to a "0".

The output of OR gate G106 is connected to the OR gates G107-G130. The OR gates G107-G130 each have a different predetermined combination of output signals from flip-flops FF50-FF61. The "1" that normally appears at the output of OR gate G106 is conveyed to all of the OR gates G107-G130, so that all of these OR gates have a "1" output regardless of the signals applied to them from the flip-flops in the receiver register. However, when the output of OR gate G106 goes to a "0", OR gates G107-G130 are released to produce outputs dependent upon the states of the flip-flop terminals to which they are connected. The outputs of OR gates G107-G130 are then conveyed to the memory system and phonograph playing mechanism to control playing of record selections, a particularly suitable arrangement being that disclosed in U.S. Pat. No. 2,923,553- Schultz et al. referred to above.

Two clock pulses after the Data appearing on pins P301-P304 has been entered into flip-flops FF50-FF53, the Q terminals of flip-flop FF63 will be returned to its quiescent state, a "1" output. When this "1" is applied to OR gate G106, the OR gates G107-G130 are then re-locked and inhibited from providing any output information.

After the expiration of the time period determined by "one shot" OS10, flip-flops FF50-FF61 are returned to their quiescent state. Since the reset signal on the direct reset terminals DR of flip-flops FF50-FF61 is also conveyed to an AND gate G133, the AND gate G133 will have one input at "1". The other input of AND gate G133 is derived from the Q terminal of flip-flop FF65. Since the one appearing at the J terminal of flip-flop FF64 will be conveyed to the Q terminal of flip-flop FF65 after two clock pulses, a "1" will also appear at this input of AND gate G133 at this

time. Therefore, a "1" output will be derived from AND gate G133. Since the reset of flip-flops FF50-FF61 means that the input to the J terminal of flip-flop FF64 is now a "0," the Q terminal of flip-flop FF65 will return to a "0" after application of two more clock pulses.

The output of OR gate G106 is also conveyed to both inputs of OR gate G134. Due to this connection, the output of OR gate G35 will go to a "0" when the output of OR gate G106 goes to a "0".

Reference may be made to FIG. 34 to illustrate the various interconnections of the receiver register, both internal and external. The pin members of FIG. 34 are shown encircled at the pins of FIGS. 30-33.

In FIGS. 35 and 36, the so-called memory address interface circuit arrangements are illustrated. Each of the outputs from OR gates G107-G130 is conveyed to a silicon controlled switch, which they fire to produce a signal in the magnetic core matrix memory. The various interconnections for these signals may be determined from FIGS. 35 and 36, in conjunction with FIG. 34 and FIGS. 30-32.

At the bottom of FIG. 36 there is illustrated a reset and mechanism scan circuit 701 that is utilized to control the mechanical movement of the movable carriage in the record playing mechanism. Further, a main trigger circuit 703 for utilization in providing "write-in" pulses to the memory matrix is illustrated.

It should be recognized that while this description has been conducted in terms of a coin operated phonograph, the selecting mechanism disclosed herein has broad application in the whole vending field, as well as in numerous other areas outside of the vending area. In fact, wherever it is desired to automatically select one of a relatively large number of choices, this system has applicability. In addition, it should be understood that various modifications, changes, and variations may be made in the arrangements, operations, and details of construction of the elements disclosed herein without departing from the spirit and scope of the present invention.

What is claimed is:

1. Vending machine apparatus comprising:

a plurality of selector switches each adapted to be manually actuated by a customer, actuation of a selector switch causing a predetermined pattern of signals representative of a character of a selection identifying format to be generated, the characters of said selection identifying format having a sequential order that identifies the corresponding selection;

disabling means for rendering said selector switches inoperative until a minimum amount of credit has been established, said disabling means also rendering certain of said selector switches inoperative for particular characters of said selection identifying format;

a first register adapted to store patterns of signals sequentially entered therein;

first shift means for causing the patterns of signals representative of the characters of said selection identifying format to be successively entered into said first register in the sequential order determined by the customer;

reset and indicating means for resetting said first register to its initial state and for indicating the necessity of reactivating the selector switches corresponding to the characters of the selection chosen by the customer after a selector switch rendered inoperative by said disabling means is actuated;

control means for automatically activating said first shift means to cause the patterns of signals stored in said first register to be rapidly transmitted in the sequential order determined by the customer when the patterns of signals representative of all of the characters in said selection identifying format have been entered into said first register;

a second register adapted to store the patterns of signals transmitted from said first register;

second shift means for causing the patterns of signals transmitted from said first register to be successively entered into said second register in the sequential order determined by the customer; and decoding means for converting the patterns of signals in said second register into vend control functions, whereby vend selection information is conveyed from the selector actuated by the customer to a selecting arrangement of a central vending apparatus.

2. Apparatus as claimed in claim 1 wherein:

each of the selection identifying formats is a three digit numeral; separate

each of the digits is represented by a pattern of four binary signals each formed on a separate line;

said first and second registers comprise a plurality of bistable devices arranged in a series of three stages with four bistable devices in each stage; and

said first shift means comprises a clock circuit adapted to activate said bistable devices to change state when appropriate portions of said patterns of signals are applied thereto.

3. Apparatus as claimed in claim 1 wherein said disabling means also renders said first shift means inoperative if credit equal to or greater than said minimum credit level has not been established.

4. Apparatus as claimed in claim 1 and further comprising means for individually indicating that the characters of said selection identifying format have been properly entered.

5. Apparatus as claimed in claim 1 and further comprising means for disabling said second register if the patterns of signals transmitted from said first register are not entered into said second register within a predetermined time limit.

6. Selecting apparatus comprising:

means for generating a predetermined character signal for each character of a selection identifying format in response to choice of the corresponding selection, the characters of said selection identifying format having a sequential order that identifies the corresponding selection;

disabling means for rendering said generating means inoperative until a minimum amount of credit has been established, said disabling means also rendering certain portions of said generating means inoperative for particular characters of said selection identifying format;

a first register adapted to store character signals sequentially entered therein;

means for causing character signals representative of the characters of said selection identifying format to be successively entered into said first register in the sequential order determined by the chosen selection;

reset and indicating means for resetting said first register to its initial state and for indicating the necessity of reactivating said generating means after a portion of said generating means rendered inoperative by said disabling means has been actuated;

control means for automatically causing the character signals stored in said first register to be transmitted in the sequential order determined by the chosen selection when the character signals representative of all of the characters in said selection identifying format have been entered into said first register;

a second register adapted to store signals transmitted from said first register;

means for causing signals transmitted from said first register to be successively entered into said second register in the sequential order determined by the chosen selection; and

means for converting the signals in said second register in the selection control functions, whereby selection information is conveyed from the selector to an arrangement controlling fulfillment of the desired selection.

7. Coin-operated phonograph apparatus comprising: a plurality of selector switches each adapted to be manually actuated by a customer, actuation of a selector switch causing a predetermined pattern of signals representative of a digit of a selection identifying numeral to be generated, the digits of said selection identifying numeral having a sequential order that identifies the corresponding selection;

disabling means for rendering said selector switches inoperative until a minimum amount of credit has been established, said disabling means also rendering certain of said selector switches inoperative for particular digits of said selection identifying numeral;

a first register adapted to store patterns of signals sequentially entered therein;

first shift means for causing the patterns of signals representative of the digits of said selection identifying numeral to be successively entered into said first register in the sequential order determined by the customer;

reset and indicating means for resetting said first register to its initial state and for indicating the necessity of reactivating the selector switches corresponding to the characters digits of the selection chosen by the customer after a selector switch rendered inoperative by said disabling means is actuated;

control means for automatically activating said first shift means to cause the patterns of signals stored in said first register to be transmitted in the sequential order determined by the customer when the patterns of signals representative of all of the digits in said selection identifying numeral have been entered into said first register;

a second register adapted to store the patterns of signals transmitted from said first register;

second shift means for causing the patterns of signals transmitted from said first register to be successively entered into said second register in the sequential order determined by the customer; and decoding means for converting the patterns of signals in said second register into memory circuit control currents,

whereby record selection information is conveyed from the selector actuated by the customer to a selecting memory arrangement at a central record playing apparatus.

8. Apparatus as claimed in claim 7 and further comprising means for indicating whether the credit established by the customer is sufficient to permit choice of a single selection or an album selection.

9. Apparatus as claimed in claim 7 wherein said disabling means also renders said first shift means inoperative if the credit established by a customer does not exceed a predetermined minimum credit level.

10. Apparatus as claimed in claim 7 wherein said disabling means prevents choice of certain predetermined numbers as digits of said selection identifying numeral unless credit sufficient to make an album selection has been established.

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