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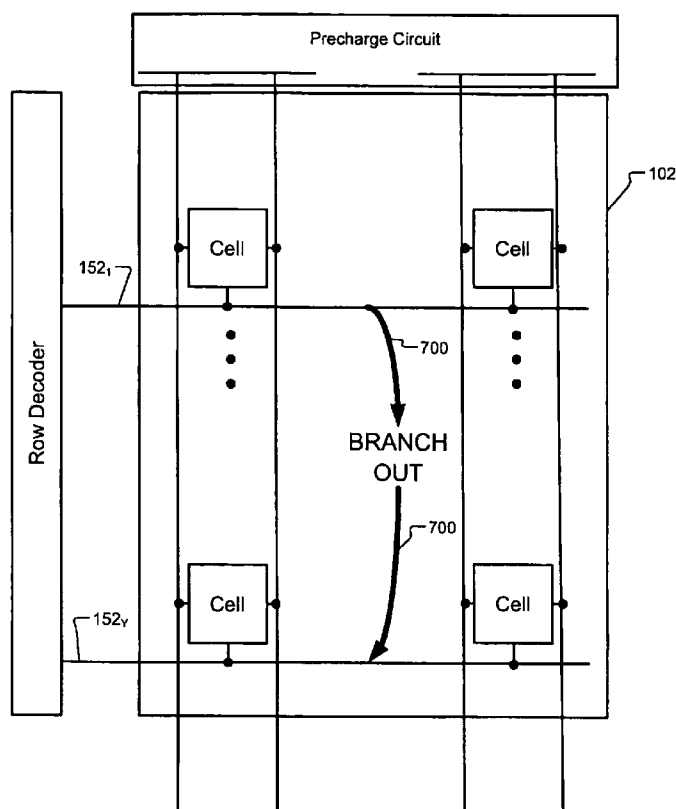


FIG. 12

(57) Abstract: A processor includes a cache memory that has an array, word lines, and bit lines. A control module accesses cells of the array during access cycles to access instructions stored in the cache memory. The control module performs one of a first discrete read and a first sequential read to access instructions in a first set of cells of the array that are connected to a first word line and selectively performs one of a second discrete read and a second sequential read based on a branch instruction to access instructions in a second set of cells of the array that are connected to a second word line. The second word line is different than the first word line.



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PROCESSOR INSTRUCTION CACHE WITH DUAL-READ MODES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Utility Application No. 12/061,296, filed April 2, 2008; and is a continuation-in-part application of U.S. Non-provisional Application No. 11/870,883, filed October 11, 2007, which
5 claims the benefit of U.S. Provisional Application No. 60/829,438, filed October 13, 2006. The disclosure of the above application is incorporated herein by reference in its entirety.

FIELD

10 **[0002]** The present disclosure relates to processors, and more particularly to processor and memory access techniques.

BACKGROUND

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently
15 named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Memory in computing devices may be arranged in a memory
20 hierarchy, which includes memory devices of different speeds, types and sizes. The type, size and proximity of a memory device to a processor affect processing speed of the memory device. Higher levels of the hierarchy generally correspond to higher speed/lower capacity memory devices while lower levels of the hierarchy generally correspond to lower speed/higher capacity devices. For
25 example, cache may be at the highest level, RAM and ROM may be at middle levels, and non-volatile memory such as a hard disk drive may be at the lowest level.

[0005] Cache may be used to store copies of highly used data and instructions to improve performance. The cache may be implemented using high

speed memory such as static random access memory (SRAM) instead of slower dynamic RAM (DRAM), which may be used for main memory. The cache may be arranged on the same integrated circuit (IC) as the processor and may be referred to as Level 1 (L1) cache.

5 **[0006]** During operation, the processor executes instructions. More particularly, the processor fetches an instruction having a location identified by a program counter (PC). After fetching the instruction, the processor decodes the instruction, which may include an opcode and an operand. The opcode indicates the operation to be performed while the operand may include
10 information for the operation to be performed. After the fetch and decode steps are performed, the processor executes the instruction. Finally, the processor writes back the results to memory. After completing the instruction, the program counter may be incremented by the length of the instruction word.

[0007] Some types of instructions may be called branches or jumps that may be used to directly manipulate the program counter. For example, the branch may be used to facilitate behavior similar to loops, conditional decisions and other program functions. Alternately, the branch may occur as a result of register values, which may represent flags.

[0008] The cache may be accessed as a word; each including R instructions, where R is an integer greater than one. Each instruction may include I bits, where I is an integer greater than one. To access the word of instructions, multiple read cycles may be executed. Each read cycle accesses one of the instructions. During the read cycle, memory cells associated with an instruction are accessed by asserting toggling both a row path (a word line) and multiple column paths (bit lines) of the array for the corresponding instruction. The asserting of row and column paths may be accompanied by decoding row and column addresses, generating a word line signal, precharging bit lines, sensing-amplification of stored bit information, and latching data.

30 SUMMARY

[0009] In one embodiment, a processor is provided and includes a cache memory that has an array, word lines, and bit lines. A control module

accesses cells of the array during access cycles to access instructions stored in the cache memory. The control module performs one of a first discrete read and a first sequential read to access instructions in a first set of cells of the array that are connected to a first word line and selectively performs one of a second
5 discrete read and a second sequential read based on a branch instruction to access instructions in a second set of cells of the array that are connected to a second word line. The second word line is different than the first word line.

[0010] In other features, the control module, when performing the first sequential read, enables the first word line of the cache memory to access a first
10 cell in the first word line, disables the first word line, and maintains the first word line in a disabled state when accessing a second cell in the first word line.

[0011] In other features, the control module, when performing the first sequential read, generates a first word line pulse associated with the first word line for a first access cycle of the bit lines and selectively refrains from
15 generating a second word line pulse for the first word line for a second access cycle of the bit lines.

[0012] In other features, the control module determines bit line separation based on a number of the access cycles to be performed along a first word line. The control module precharges the bit lines connected to the first
20 word line to provide the bit line separation when accessing the first set of cells.

[0013] In other features, the control module precharges a set of the bit lines connected to the first word line to provide the bit line separation when accessing a first set of cells of the array. The control module selectively refrains from precharging at least one of the set of the bit lines when accessing a second
25 set of cells of the array based on connections between the second set of cells and the first word line.

[0014] In other features, the control module refrains from precharging the at least one of the set of the bit lines when the second set of cells is connected to the first word line.

[0015] In other features, the control module precharges the at least
30 one of the set of bit lines when the second set of cells is connected to a word line other than the first word line.

[0016] In other features, the control module adjusts precharge timing of the bit lines based on a rate of a clock signal. In other features, the control module delays precharging of the bit lines when a rate of a clock signal is less than a predetermined rate.

5 **[0017]** In other features, the control module generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal. In other features, the control module generates a sequential read signal to enable a sequential read mode and precharges the bit lines based on the sequential read signal.

10 **[0018]** In other features, the control module, when in a discrete mode, performs row address decoding, word line enablement, and bit line precharging for each access of each of the cells.

[0019] In other features, the control module, when accessing cells in a first mode, precharges the bit lines and performs row address decoding for each
15 read cycle. The control module, when accessing cells in a second mode, precharges the bit lines, performs row address decoding for a first read cycle, does not precharge the bit lines, and does not perform row address decoding for a second read cycle.

[0020] In other features, a column decoder is included that selects
20 cells of the array via a column select signal. The control module generates a latch signal to latch bit information in the selected cells based on the column select signal. In other features, an amplification module is included that detects and amplifies bit information in the first and second set of cells.

[0021] In other features, a row decoder is included. The control
25 module generates a word line signal via the row decoder to access the first set of cells. In other features, the word line signal defines an extended period to increase the bit line separation. In other features, the extended period increases bit line separation time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined
30 number of read cycles.

[0022] In other features, a column decoder is included. The control module generates bit line signals via the column decoder to access the first set

of cells. In other features, a sense-amplifier is included that has common lines and that receives a precharge signal to precharge the common lines before latching bit information in the first and second set of cells.

5 **[0023]** In other features, the control module precharges the bit lines based on a precharge flag that indicates when a precharge has been performed. In other features, the control module precharges the bit lines based on timing of a previous precharge of the bit lines.

10 **[0024]** In other features, the control module, when performing the second sequential read, enables the second word line of the cache memory to access a cell in the second word line, disables the second word line, and maintains the second word line in a disabled state when accessing another cell in the second word line. In other features, the control module performs in a discrete read mode based on the branch instruction.

15 **[0025]** In other features, the processor pre-fetches and decodes subsequent instructions in a pipeline. A branch prediction module predicts whether one of the subsequent instructions that is a second branch instruction is likely to be taken. The branch prediction module selectively performs one of a discrete read and a sequential read on the branch instruction based on the prediction and on whether the branch instruction involves multiple reads along a
20 same word line. The branch prediction module includes a branch history module that outputs branch prediction data based on an address of the second branch instruction. The branch prediction module bases the prediction on the branch prediction data.

25 **[0026]** In other features, a method is provided and includes providing a cache memory that has an array of cells, word lines, and bit lines. Cells of the array are accessed during access cycles to access instructions stored in the cache memory. One of a first discrete read and a first sequential read is performed to access instructions in a first set of cells of the array that are connected to a first word line. One of a second discrete read and a second
30 sequential read is selectively performed based on a branch instruction to access instructions in a second set of cells of the array that are connected to a second word line. The second word line is different than the first word line.

[0027] In other features, when performing the first sequential read, the first word line of the cache memory is enabled to access a first cell in the word line, the first word line is disabled, and the first word line is maintained in a disabled state when accessing a second cell in the first word line.

5 **[0028]** In other features, when performing said first sequential read, the method includes generating a first word line pulse associated with said first word line for a first access cycle of the bit lines and selectively refrains from generating a second word line pulse for said first word line for a second access cycle of said bit lines.

10 **[0029]** In other features, the method includes determining bit line separation based on a number of the access cycles along a first word line and precharging the bit lines connected to the first word line to provide the bit line separation when accessing the first set of cells.

[0030] In other features, the method includes: precharging a set of the
15 bit lines connected to the first word line to provide the bit line separation when accessing a first set of cells of the array, and refraining from precharging at least one of the set of the bit lines when accessing a second set of cells of the array based on connections between the second set of cells and the first word line.

[0031] In other features, the method includes refraining from
20 precharging the at least one of the set of the bit lines when the second set of cells is connected to the first word line.

[0032] In other features, the method includes precharging the at least one of the set of bit lines when the second set of cells is connected to a word line other than the first word line.

25 **[0033]** In other features, the method includes adjusting precharge timing of the bit lines based on a rate of a clock signal. In other features, the method includes delaying precharging of the bit lines when a rate of a clock signal is less than a predetermined rate.

[0034] In other features, the method includes selectively operating in a
30 discrete read mode and a sequential read mode. In other features, the method includes generating a sequential read signal to enable a sequential read mode and generating a word line signal based on the sequential read signal.

[0035] In other features, the method includes generating a sequential read signal to enable a sequential read mode and precharging the bit lines based on the sequential read signal.

[0036] In other features, when in a discrete mode, the method includes
5 performing row address decoding, word line enablement, and bit line precharging for each access of each of the cells.

[0037] In other features, when accessing cells in a first mode, the method includes precharging the bit lines and performing row address decoding for each read cycle. When accessing cells in a second mode, the method
10 includes precharging the bit lines, performing row address decoding for a first read cycle, refraining from precharging the bit lines, and refraining from performing row address decoding for a second read cycle.

[0038] In other features, the method includes selecting cells of the array via a column select signal and generating a latch signal to latch bit
15 information in the selected cells based on the column select signal. In other features, the method includes detecting and amplifying bit information in the first and second set of cells.

[0039] In other features, the method includes generating a word line signal via the row decoder to access the first set of cells. In other features, the
20 word line signal defines an extended period to increase the bit line separation. In other features, the extended period increases bit line separation time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0040] In other features, the method includes generating bit line
25 signals via the column decoder to access the first set of cells.

[0041] In other features, the method includes receiving a precharge signal to precharge common lines of a sense-amplifier before latching bit information in the first and second set of cells.

[0042] In other features, the method includes precharging the bit lines
30 based on a precharge flag that indicates when a precharge has been performed. In other features, the method includes precharging the bit lines based on timing of a previous precharge of the bit lines.

[0043] In other features, when performing the second sequential read, the method includes enabling the second word line of the cache memory to access a cell in the second word line, disabling the second word line, and maintaining the second word line in a disabled state when accessing another cell
5 in the second word line. In other features, the method includes performing in a discrete read mode based on the branch instruction.

[0044] In other features, the method includes pre-fetching and decoding subsequent instructions in a pipeline; and predicting whether one of said subsequent instructions that is a second branch instruction is likely to be
10 taken.

[0045] In other features, the method includes selectively performing one of a discrete read and a sequential read on said branch instruction based on said prediction and on whether said branch instruction involves multiple reads along a same word line.

[0046] In other features, the method includes generating branch prediction data based on an address of said second branch instruction; and basing said prediction on said branch prediction data.
15

[0047] In other features, a processor is provided and includes a cache memory that has an array, word lines, and bit lines. Control means accesses
20 cells of the array during access cycles to access instructions stored in the cache memory. The control means performs one of a first discrete read and a first sequential read to access instructions in a first set of cells of the array that are connected to a first word line and selectively performs one of a second discrete read and a second sequential read based on a branch instruction to access
25 instructions in a second set of cells of the array that are connected to a second word line. The second word line is different than the first word line.

[0048] In other features, the control means, when performing the first sequential read, enables the first word line of the cache memory to access a first cell in the first word line, disables the first word line, and maintains the first word
30 line in a disabled state when accessing a second cell in the first word line.

[0049] In other features, the control means, when performing the first sequential read, generates a first word line pulse associated with the first word

line for a first access cycle of the bit lines and selectively refrains from generating a second word line pulse for the first word line for a second access cycle of the bit lines.

5 **[0050]** In other features, the control means determines bit line separation based on a number of the access cycles along a first word line. The control means precharges the bit lines connected to the first word line to provide the bit line separation when accessing the first set of cells.

10 **[0051]** In other features, the control means precharges a set of the bit lines connected to the first word line to provide the bit line separation when accessing a first set of cells of the array. The control means selectively refrains from precharging at least one of the set of the bit lines when accessing a second set of cells of the array based on connections between the second set of cells and the first word line.

15 **[0052]** In other features, the control means refrains from precharging the at least one of the set of the bit lines when the second set of cells is connected to the first word line.

[0053] In other features, the control means precharges the at least one of the set of bit lines when the second set of cells is connected to a word line other than the first word line.

20 **[0054]** In other features, the control means adjusts precharge timing of the bit lines based on a rate of a clock signal. In other features, the control means delays precharging of the bit lines when a rate of a clock signal is less than a predetermined rate.

25 **[0055]** In other features, the control means selectively operates in a discrete read mode and a sequential read mode. In other features, the control means generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal.

30 **[0056]** In other features, the control means generates a sequential read signal to enable a sequential read mode and precharges the bit lines based on the sequential read signal. In other features, the control means, when in a discrete mode, performs row address decoding, word line enablement, and bit line precharging for each access of each of the cells.

[0057] In other features, the control means, when accessing cells in a first mode, precharges the bit lines and performs row address decoding for each read cycle. The control means, when accessing cells in a second mode, precharges the bit lines, performs row address decoding for a first read cycle,
5 does not precharge the bit lines, and does not perform row address decoding for a second read cycle.

[0058] In other features, column decoder means for selecting cells of the array via a column select signal is included. The control means generates a latch signal to latch bit information in the selected cells based on the column
10 select signal. In other features, amplification means for detecting and amplifying bit information in the first and second set of cells is included.

[0059] In other features, row decoder means for decoding is included. The control means generates a word line signal via the row decoder means to access the first set of cells. In other features, the word line signal defines an
15 extended period to increase the bit line separation. In other features, the extended period increases bit line separation time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0060] In other features, column decoder means for decoding is included. The control means generates bit line signals via the column decoder
20 means to access the first set of cells.

[0061] In other features, sense-amplifier means for providing common lines and for receiving a precharge signal to precharge the common lines before latching bit information in the first and second set of cells is included.

[0062] In other features, the control means precharges the bit lines based on a precharge flag that indicates when a precharge has been performed. In other features, the control means precharges the bit lines based on timing of a
25 previous precharge of the bit lines.

[0063] In other features, the control means, when performing the second sequential read, enables the second word line of the cache memory to
30 access a cell in the second word line, disables the second word line, and maintains the second word line in a disabled state when accessing another cell

in the second word line. In other features, the control means performs in a discrete read mode based on the branch instruction.

[0064] In other features, the processor pre-fetches and decodes subsequent instructions in a pipeline. Branch prediction means predicts whether one of the subsequent instructions that is a second branch instruction is likely to be taken. The branch prediction means selectively performs one of a discrete read and a sequential read on the branch instruction based on the prediction and on whether the branch instruction involves multiple reads along a same word line. The branch prediction means includes branch history means for generating branch prediction data based on an address of the second branch instruction and wherein the branch prediction means bases the prediction on the branch prediction data.

[0065] In other features, a processor is provided and includes a cache memory and a control module. The cache memory includes an array, word lines, and bit lines. The control module accesses cells of the array during access cycles to access instructions stored in the cache memory. The control module determines bit line separation based on a number of the access cycles along a first word line. The control module precharges a set of the bit lines connected to the first word line based on the bit line separation when accessing a first set of cells of the array. The control module selectively refrains from precharging one of the set of bit lines when accessing a second set of cells of the array based on connections between the second set of cells and the first word line.

[0066] In other features, the control module selectively refrains from precharging the one of the set of bit lines when the second set of cells is connected to the first word line. In other features, the control module precharges the one of the set of bit lines when the second set of cells is connected to a word line other than the first word line.

[0067] In other features, the control module adjusts precharge timing of the set of bit lines based on a rate of a clock signal. In other features, the control module delays precharging of the set of bit lines when a rate of a clock signal is less than a predetermined rate.

[0068] In further features, the control module enables the first word line of the cache memory to access a first cell in the word line, disables the first word line, and maintains the first word line in a disabled state when accessing a second cell in the first word line.

5 **[0069]** In other features, the control module generates a word line pulse associated with one of the word lines for a first access cycle of the set of the bit lines. The control module selectively refrains from generating a word line pulse for a second access cycle of the set of said bit lines.

[0070] In yet other features, the control module selectively operates in
10 a discrete read mode and a sequential read mode. In other features, the control module generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal. In other features, the control module generates a sequential read signal to enable a sequential read mode and precharges the set of bit lines based on the sequential
15 read signal. In other features, the control module, when in a discrete mode, performs row address decoding, word line enablement, and bit line precharging for each cycle associated with access of each of the cells.

[0071] In still other features, control module, when accessing cells during s first mode, precharges the set of bit lines and performs row address
20 decoding for each read cycle. The control module, when accessing cells during s second mode, precharges the set of bit lines, performs row address decoding for a first read cycle, does not precharge the set of bit lines, and does not perform row address decoding for a second read cycle.

[0072] In further features, the processor further includes a column
25 decoder that selects cells of the array via a column select signal. The control module generates a latch signal to latch bit information in the selected cells based on the column select signal.

[0073] In other features, the processor further includes an amplification
30 module that detects and amplifies bit information in the first and second set of cells.

[0074] In still other features, the processor further includes a row decoder. The control module generates a word line signal via the row decoder to

access the first set of cells. In other features, the word line signal defines an extended period to increase the bit line separation. In other features, the extended period increases bit line separation time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0075] In further features, the processor further includes a column decoder. The control module generates bit line signals via the column decoder to access the first set of cells. In other features, the processor further includes a sense-amplifier that has common lines and that receives a precharge signal to precharge the common lines before latching bit information in the first and second set of cells. In other features, the control module precharges the one of the set of bit lines based on a branch instruction.

[0076] In other features, the control module detects a precharge error and precharges the at least one of the set of bit lines based on the precharge error. In other features, the control module precharges the at least one of the set of bit lines based on a precharge flag that indicates when a precharge has been performed. In other features, the control module precharges the at least one of the set of bit lines based on timing of a previous precharge of the at least one of the set of bit lines.

[0077] In yet other features, a method is provided and includes providing a cache memory. The cache memory includes an array of cells, word lines, and bit lines. Cells of the array are accessed during access cycles to access instructions stored in the cache memory. Bit line separation is determined based on a number of the access cycles along a first word line. A set of the bit lines connected to the first word line is precharged based on the bit line separation when accessing a first set of cells of the array. Precharging of at least one bit line of the set of bit lines is refrained from being performed when accessing a second set of cells of the array based on connections between the second set of cells and the first word line.

[0078] In still other features, the method further includes refraining from precharging the at least one bit line of the set of bit lines when the second set of cells are connected to the first word line. In other features, the method

further includes precharging the at least one bit line of the set of bit lines when the second set of cells are connected to a word line other than the first word line.

5 **[0079]** In other features, the method further includes adjusting precharge timing of the set of bit lines based on a rate of a clock signal. In other features, the method further includes delaying precharging of the set of bit lines when a rate of a clock signal is less than a predetermined rate.

10 **[0080]** In further features, the method further includes enabling the first word line of the cache memory to access a first cell in the word line. The first word line is disabled. The first word line is maintained in a disabled state when accessing a second cell in the first word line.

[0081] In yet other features, the method further includes generating a word line pulse associated with one of the word lines for a first access cycle of the set of the bit lines and selectively refraining from generating a word line pulse for a second access cycle of the set of said bit lines.

15 **[0082]** In still other features, the method further includes selectively operating in a discrete read mode and a sequential read mode. In other features, the method further includes generating a sequential read signal to enable a sequential read mode. A word line signal is generated based on the sequential read signal. In other features, the method further includes generating
20 a sequential read signal to enable a sequential read mode. The set of bit lines is precharged based on the sequential read signal.

[0083] In other features, the method further includes operating in a discrete mode, which includes: performing row address decoding; enabling a word line; and precharging a bit line for each cycle associated with access of
25 each of the cells.

[0084] In further features, when accessing cells during a first mode, the set of bit lines is precharged and row address decoding is performed for each read cycle. When accessing cells during a second mode, the set of bit lines is precharged, row address decoding for a first read cycle is performed,
30 precharging the set of bit lines is refrained from being performed, and row address decoding for a second read cycle is performed.

[0085] In yet other features, the method further includes selecting cells of the array via a column select signal and generating a latch signal to latch bit information in the selected cells based on the column select signal. In other features, the method further includes detecting and amplifying bit information in
5 the first and second set of cells.

[0086] In still other features, the method further includes generating a word line signal via a row decoder to access the first set of cells. In other features, the word line signal includes an extended period to increase the bit line separation. In other features, the extended period increases bit line separation
10 time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0087] In other features, the method further includes generating bit line signals via a column decoder to access the first set of cells. In other features,
15 the method further includes receiving a precharge signal to precharge common lines of a sense-amplifier before latching bit information in the first and second set of cells. In other features, the method includes precharging the one of the set of bit lines based on a branch instruction.

[0088] In further features, a processor is provided and includes a
20 cache memory with an array, word lines, and bit lines and control means. The control means accesses cells of the array during access cycles to access instructions stored in the cache memory. The control means determines a bit line separation based on a number of the access cycles along a first word line. The control means precharges a set of the bit lines connected to the first word
25 line based on the bit line separation when accessing a first set of cells of the array. The control means selectively refrains from precharging at least one of the set of bit lines when accessing a second set of cells of the array based on connections between the second set of cells and the first word line.

[0089] In other features, the method further comprises detecting a
30 precharge error and precharging the at least one of the set of bit lines based on the precharge error. In other features, the method includes precharging the at least one of the set of bit lines based on a precharge flag that indicates when a

precharge has been performed. In other features, the method includes precharging the at least one of the set of bit lines based on timing of a previous precharge of the at least one of the set of bit lines.

5 **[0090]** In yet other features, the control means selectively refrains from precharging the at least one of the set of bit lines when the second set of cells is associated with the first word line. In other features, the control means precharges the at least one of the set of bit lines when the second set of cells are associated with a word line other than the first word line.

10 **[0091]** In other features, the control means adjusts precharge timing of the set of bit lines based on a rate of a clock signal. In other features, the control means delays precharging of the set of bit lines when a rate of a clock signal is less than a predetermined rate.

15 **[0092]** In other features, the control means enables the first word line of the cache memory to access a first cell in the word line, disables the first word line, and maintains the first word line in a disabled state when accessing a second cell in the first word line.

20 **[0093]** In further features, the control means generates a word line pulse associated with one of the word lines for a first access cycle of the set of the bit lines. The control means selectively refrains from generating a word line pulse for a second access cycle of the set of said bit lines.

25 **[0094]** In yet other features, the control means selectively operates in a discrete read mode and a sequential read mode. In other features, the control means generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal. In other features, the control means generates a sequential read signal to enable a sequential read mode and precharges the set of bit lines based on the sequential read signal.

30 **[0095]** In other features, the control means, when in a discrete mode, performs row address decoding, word line enablement, and bit line precharging for each cycle associated with access of each of the cells.

[0096] In still other features, the control means, when accessing cells during a first mode, precharges the set of bit lines and performs row address

decoding for each read cycle. The control means, when accessing cells during a second mode, precharges the set of bit lines, performs row address decoding for a first read cycle, does not precharge the set bit lines, and does not perform row address decoding for a second read cycle.

5 **[0097]** In further features, the processor further includes column decoding means that selects cells of the array via a column select signal. The control means generates a latch signal to latch bit information in the selected cells based on the column select signal. In other features, the processor further includes amplification means for detecting and amplifying bit information in the
10 first and second set of cells.

[0098] In yet other features, the processor further includes row decoding means for generating a word line signal to access the first set of cells. In other features, the word line signal defines an extended period to increase the bit line separation. In other features, the extended period increases bit line
15 separation time and sets the bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0099] In still other features, the processor further includes column decoding means for generating bit line signals to access the first set of cells. In
20 other features, the processor further includes sense-amplifying means for receiving a precharge signal to precharge common lines before latching bit information in the first and second set of cells. In other features, the control means precharges the one of the set of bit lines based on a branch instruction.

[0100] In other features, a processor is provided that includes a cache
25 memory. The cache memory includes an array of cells, word lines and bit lines. A control module enables a word line of the word lines to access a first cell in the enabled word line. The control module disables the word line and maintains the word line in a disabled state to access a second cell in the word line.

[0101] In further features, the control module accesses multiple cells in
30 the array through separate cycled selection of the bit lines. The control module generates a single word line pulse associated with one of the word lines. In

other features, the control module operates in a discrete read mode and a sequential read mode.

[0102] In yet other features, the control module generates a sequential read signal to enable a sequential read mode and generates a word line signal
5 based on the sequential read signal.

[0103] In still other features, the control module generates a sequential read signal to enable a sequential read mode and precharges the bit lines based on the sequential read signal.

[0104] In other features, the control module, when in a discrete mode,
10 performs row address decoding for each cycle associated with access of each of the cells.

[0105] In further features, the control module, when in a sequential mode, performs address decoding for a single row and enables a word line for column cell sets. The control module selects, senses and amplifies a column
15 cell set of the column cell sets for column address decoding. The control module disables the word line for column address decoding and access of column cell sets of the column cell sets other than the column cell set.

[0106] In yet other features, the control module operates in a first mode and in a second mode. The control module, when in the first mode,
20 precharges the bit lines and performs row address decoding for each read cycle. The control module, when in the second mode, precharges the bit lines and performs row address decoding for a first read cycle and does not precharge the bit lines and does not perform row address decoding for a second read cycle. The control module, when in the second mode, enables an address counter that
25 is associated with pointing a column address to a next location after each column access. The address counter, when the column address is associated with an end of a word, is reset and memory access is permitted for a next discrete or sequential read access.

[0107] In other features, the control module precharges the bit lines
30 when accessing a first set of cells of the array and does not precharge the bit lines when accessing a second set of cells of the array.

[0108] In yet other features, the cache memory includes at least one of an instruction cache and a static random access memory (SRAM).

[0109] In other features, a column decoder is further included and selects the second cell via a column select signal. The control module
5 generates a latch signal to latch bit information in the second cell based on the column select signal. In other features, latches are included and latch bit information in the first and second cells. In other features, a sensing-amplification module is included and detects and amplifies bit information in the first and second cells.

10 [0110] In still other features, a row decoder is included. The control module generates a word line signal via the row decoder to access a first set of cells.

[0111] In other features, the word line signal includes an extended period to increase bit line signal separation and to compensate for leakage. In
15 other features, the extended period increases bit line separation time and sets bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0112] In other features, a column decoder is included. The control module generates bit line signals via the column decoder to access a first set of
20 cells.

[0113] In further features, the control module precharges bit lines after a word line extended period. In other features, the control module precharges the bit lines once for multiple cell access cycles.

[0114] In other features, a sense-amplifier is included that has
25 common lines and that receives a precharge signal to precharge the common lines before latching bit information between accesses to sets of cells.

[0115] In other features, an integrated circuit is provided that includes the processor. In other features, the integrated circuit further includes an external memory that is in communication with the processor.

30 [0116] In still other features, a cellular phone is provided that includes the processor. In other features, the cellular phone further includes an external memory that is in communication with the processor.

[0117] In yet other features, a communication system is provided that includes the processor. In other features, the communication system further includes an external memory that is in communication with the processor.

5 [0118] In other features, a method is provided and includes providing a cache memory with an array of cells, word lines, and bit lines. A word line of the word lines is enabled to access a first cell in the word line. The word line is disabled. The word line is maintained in a disabled state to access a second cell in the word line.

10 [0119] In other features, the method further includes accessing multiple cells in the array through separate cycled selection of the bit lines. A single word line pulse associated with one of the word lines is generated. In other features, the method includes operating in a discrete read mode and a sequential read mode.

15 [0120] In other features, the method further includes generating a sequential read signal to enable a sequential read mode. A word line signal is generated based on the sequential read signal.

[0121] In further features, the method further includes generating a sequential read signal to enable a sequential read mode. The bit lines are precharged based on the sequential read signal.

20 [0122] In still other features, the method further includes performing row address decoding for each cycle associated with access of each of the cells when in a discrete mode.

25 [0123] In yet other features, the method further includes, when in a sequential mode, performing address decoding for a single row and enabling a word line for column cell sets. A column cell set of the column cell sets is selected, sensed and amplified for column address decoding. The word line is disabled for column address decoding and accessing of column cell sets of the column cell sets other than the column cell set.

30 [0124] In other features, the method further includes precharging the bit lines and performing row address decoding for each read cycle when in a first mode. When in the second mode, the method further includes precharging the bit lines and performing row address decoding for a first read cycle and

refraining from precharging the bit lines and refraining from performing row address decoding for a second read cycle. When in the second mode, an address counter is enabled that is associated with pointing a column address to a next location after each column access. When the column address is associated with an end of a word, the address counter is reset and permitted access to memory for a next discrete or sequential read access.

[0125] In other features, the method further includes precharging the bit lines when accessing a first set of cells of the array. The method further includes refraining from precharging the bit lines when accessing a second set of cells of the array.

[0126] In other features, the method further includes selecting the second cell via a column select signal and generating a latch signal to latch bit information in the second cell based on the column select signal. In other features, the method further includes latching bit information in the first and second cells. In other features, the method further includes detecting and amplifying bit information in the first and second cells. In other features, the method further includes generating a word line signal via a row decoder to access a first set of cells.

[0127] In further features, the word line signal includes an extended period to increase bit line signal separation and to compensate for leakage. In other features, the extended period increases bit line separation time and sets bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles. In other features, the method further includes generating bit line signals via a column decoder to access a first set of cells.

[0128] In still other features, the method further includes precharging bit lines after a word line extended period. In other features, the method further includes precharging the bit lines once for multiple cell access cycles.

[0129] In yet other features, the method further includes receiving a precharge signal via a sense-amplifier to precharge common lines before latching bit information between accesses to sets of cells.

[0130] In other features, a processor is provided and includes a cache memory with an array of cells, word lines, and bit lines. Control means for enabling a word line of the word lines to access a first cell in the word line is included. The control means disables the word line and maintains the word line
5 in a disabled state to access a second cell in the word line.

[0131] In other features, the control means accesses multiple cells in the array through separate cycled selection of the bit lines and generates a single word line pulse associated with one of the word lines. In other features, the control means operates in a discrete read mode and a sequential read mode.

10 **[0132]** In other features, the control means generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal.

[0133] In other features, the control means generates a sequential read signal to enable a sequential read mode and precharges the bit lines based
15 on the sequential read signal.

[0134] In other features, the control means, when in a discrete mode, performs row address decoding for each cycle associated with access of each of the cells.

[0135] In still other features, the control means, when in a sequential
20 mode, performs address decoding for a single row and enables a word line for column cell sets. The control means selects, senses and amplifies a column cell set of the column cell sets for column address decoding. The control means disables the word line for column address decoding and access of column cell sets of the column cell sets other than the column cell set.

25 **[0136]** In yet other features, the control means operates in a first mode and a second mode. The control means, when in the first mode, precharges the bit lines and performs row address decoding for each read cycle. The control means, when in the second mode, precharges the bit lines and performs row address decoding for a first read cycle and does not precharge the bit lines and
30 does not perform row address decoding for a second read cycle. The control means, when in the second mode, enables an address counter that is associated with pointing a column address to a next location after each column

access. The address counter, when the column address is associated with an end of a word, is reset and memory access is permitted for a next discrete or sequential read access.

5 **[0137]** In further features, the control means precharges the bit lines when accessing a first set of cells of the array and that does not precharge the bit lines when accessing a second set of cells of the array.

[0138] In other features, the cache memory includes at least one of an instruction cache and a static random access memory (SRAM).

10 **[0139]** In other features, column decoding means for selecting the second cell via a column select signal is further included. The control means generates a latch signal to latch bit information in the second cell based on the column select signal. In other features, latching means for latching bit information in the first and second cells is further included. In other features, sensing-amplification means for detecting and amplifying bit information in the
15 first and second cells is further included. In other features, the control means generates a word line signal via a row decoder to access a first set of cells.

[0140] In yet other features, the word line signal includes an extended period to increase bit line signal separation and to compensate for leakage. In other features, the extended period increases bit line separation time and sets bit
20 line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles. In other features, the control means generates bit line signals via a column decoder to access a first set of cells.

[0141] In still other features, the control means precharges multiple bit
25 lines after a word line extended period. In other features, the control means precharges the bit lines once for multiple cell access cycles.

[0142] In other features, sense-amplifier means for receiving a precharge signal to precharge common lines of the sense-amplifier means prior to latching bit information between accesses to sets of cells is further included.

30 **[0143]** In other features, an integrated circuit is provided that includes the processor. In other features, the integrated circuit further includes an external memory that is in communication with the processor.

[0144] In other features, a cellular phone is provided and includes the processor. In other features, the cellular phone further includes an external memory that is in communication with the processor.

5 [0145] In other features, a communication system is provided that includes the processor. In other features, the communication system further includes an external memory that is in communication with the processor.

10 [0146] In further features, a processor is provided and includes a cache memory with an array of cells, word lines, and bit lines. A control module accesses cells associated with instructions stored in the cache memory during access cycles. The control module precharges the bit lines when accessing a first set of cells of the array and does not precharge the bit lines when accessing a second set of cells of the array.

15 [0147] In still other features, the control module enables a word line of the cache memory to access a first cell in the word line. The control module disables the word line and maintains the word line in a disabled state when accessing a second cell in the word line.

20 [0148] In yet other features, the control module accesses multiple cells in the array through separate cycled selection of the bit lines and generates a single word line pulse associated with one of the word lines. In other features, the control module operates in a discrete read mode and a sequential read mode.

[0149] In other features, the control module generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal.

25 [0150] In other features, the control module generates a sequential read signal to enable a sequential read mode and precharges the bit lines based on the sequential read signal.

30 [0151] In other features, the control module, when in a discrete mode, performs row address decoding for each cycle associated with access of each of the cells.

[0152] In other features, the control module, when in a sequential mode, performs row address decoding for the first set of cells and maintains the word line in a disabled state to access the second set of cells.

5 [0153] In still other features, the control module operates in a first mode and a second mode. The control module, when in the first mode, precharges the bit lines and performs row address decoding for each read cycle. The control module, when in the second mode, precharges the bit lines and performs row address decoding for a first read cycle and does not precharge the bit lines and does not perform row address decoding for a second read cycle.

10 [0154] In yet other features, the cache memory includes at least one of an instruction cache and a static random access memory (SRAM).

[0155] In further features, a column decoder that selects the second cell via a column select signal is further included. The control module generates a latch signal to latch bit information in the second set of cells based on the column select signal. In other features, latches are further included that latch bit information in the first and second set of cells. In other features, a sensing-amplification module is further included that detects and amplifies bit information in the first and second set of cells. In other features, a row decoder is further included. The control module generates a word line signal via the row decoder to access the first set of cells.

20 [0156] In other features, the word line signal includes an extended period to increase bit line signal separation. In other features, the extended period increases bit line separation time and sets bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles.

[0157] In other features, a column decoder is further included. The control module generates bit line signals via the column decoder to access the first set of cells.

30 [0158] In other features, the control module precharges bit lines after a word line extended period. In other features, the control module precharges the bit lines once for multiple cell access cycles.

[0159] In still other features, a sense-amplifier is further included that has common lines and that receives a precharge signal to precharge the common lines before latching bit information in the first and second set of cells.

5 [0160] In other features, an integrated circuit is provided and includes the processor. In other features, the integrated circuit further includes an external memory in communication with the processor.

[0161] In yet other features, a communication device is provided and includes the processor. In other features, the communication device further includes an external memory in communication with the processor.

10 [0162] In further features, a method is provided and includes providing a cache memory with an array of cells, word lines, and bit lines. The method includes accessing cells associated with instructions stored in the cache memory during access cycles. The bit lines are precharged when accessing a first set of cells of the array. Precharging of the bit lines is not performed when accessing a
15 second set of cells of the array.

[0163] In other features, the method further includes enabling a word line of the cache memory to access a first cell in the word line. The word line is disabled and is maintained in a disabled state when accessing a second cell in the word line.

20 [0164] In other features, the method further includes accessing multiple cells in the array through separate cycled selection of the bit lines. A single word line pulse associated with one of the word lines is generated. In other features, the method further includes operating in a discrete read mode and a sequential read mode.

25 [0165] In other features, the method further includes generating a sequential read signal to enable a sequential read mode. A word line signal based on the sequential read signal is generated.

[0166] In other features, the method further includes generating a sequential read signal to enable a sequential read mode. The bit lines are
30 precharged based on the sequential read signal.

[0167] In further features, the method further includes performing row address decoding for each cycle associated with access of each of the cells when in a discrete mode.

5 **[0168]** In yet other features, the method further includes performing row address decoding for the first set of cells. The word line is maintained in a disabled state to access the second cell when in a sequential mode.

[0169] In still other features, the method further includes precharging the bit lines and performing row address decoding for each read cycle when in a first mode. When in a second mode, the bit lines are precharged and row
10 address decoding is performed for a first read cycle and precharging of the bit lines and row address decoding is not performed for a second read cycle.

[0170] In other features, the method further includes selecting the second cell via a column select signal. A latch signal is generated to latch bit information in the second set of cells based on the column select signal. In
15 other features, the method further includes latching bit information in the first and second set of cells. In other features, the method further includes detecting and amplifying bit information in the first and second set of cells. In other features, the method further includes generating a word line signal via a row decoder to access the first set of cells.

20 **[0171]** In other features, the word line signal includes an extended period to increase bit line signal separation. In other features, the extended period increases bit line separation time and sets bit line separation at a predetermined voltage. In other features, the extended period is based on a predetermined number of read cycles. In other features, the method further
25 includes generating bit line signals via the column decoder to access the first set of cells.

[0172] In other features, the method further includes precharging bit lines after a word line extended period. In other features, the method further includes precharging the bit lines once for multiple cell access cycles.

30 **[0173]** In further features, the method further includes receiving a precharge signal to precharge common lines of a sense-amplifier prior to latching bit information in the first and second set of cells.

[0174] In other features, a processor is provided and includes a cache memory with an array of cells, word lines, and bit lines. The control means accesses cells associated with instructions stored in the cache memory during access cycles. The control means precharges the bit lines when accessing a first set of cells of the array and does not precharge the bit lines when accessing a second set of cells of the array.

[0175] In still other features, the control means enables a word line of the cache memory to access a first cell in the word line. The control means disables the word line and maintains the word line in a disabled state when accessing a second cell in the word line.

[0176] In yet other features, the control means accesses multiple cells in the array through separate cycled selection of the bit lines and generates a single word line pulse associated with one of the word lines. In other features, the control means operates in a discrete read mode and a sequential read mode.

[0177] In other features, the control means generates a sequential read signal to enable a sequential read mode and generates a word line signal based on the sequential read signal.

[0178] In other features, the control means generates a sequential read signal to enable a sequential read mode and precharges the bit lines based on the sequential read signal.

[0179] In other features, the control means, when in a discrete mode, performs row address decoding for each cycle associated with access of each of the cells.

[0180] In other features, the control means, when in a sequential mode, performs row address decoding for the first set of cells and maintains the word line in a disabled state to access the second set of cells.

[0181] In other features, the control means operates in a first mode and a second mode. The control means, when in the first mode, precharges the bit lines and performs row address decoding for each read cycle. The control means, when in the second mode, precharges the bit lines and performs row address decoding for a first read cycle and does not precharge the bit lines or perform row address decoding for a second read cycle.

[0182] In still other features, the cache memory includes at least one of an instruction cache and a static random access memory (SRAM).

[0183] In further features, column decoding means for selecting the second set of cells via a column select signal is included. The control means
5 generates a latch signal to latch bit information in the second set of cells based on the column select signal. In other features, latching means for latching bit information in the first and second set of cells is included. In other features, sensing-amplification means for detecting and amplifying bit information in the first and second set of cells is included. In other features, the control means
10 generates a word line signal via a row decoder to access the first set of cells.

[0184] In yet other features, the word line signal includes an extended period to increase bit line signal separation. In other features, the extended period increases bit line separation time and sets bit line separation at a predetermined voltage. In other features, the extended period is based on a
15 predetermined number of read cycles. In other features, the control means generates bit line signals via a column decoder to access the first set of cells.

[0185] In other features, the control means precharges bit lines after a word line extended period. In other features, the control means precharges the bit lines once for multiple cell access cycles.

[0186] In other features, sense-amplifier means is included for receiving a precharge signal to precharge common lines of the sense-amplifier means prior to latching bit information in the first and second set of cells.

[0187] In other features, an integrated circuit is provided and includes the processor. In other features, the integrated circuit further includes an
25 external memory in communication with the processor.

[0188] In other features, a communication device is provided and includes the processor. In other features, the communication device further includes an external memory in communication with the processor.

[0189] In still other features, the systems and methods described
30 above are implemented by a computer program executed by one or more processors. The computer program can reside on a computer readable medium

such as but not limited to memory, non-volatile data storage and/or other suitable tangible storage mediums.

[0190] Further areas of applicability of the present disclosure will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the disclosure, are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0191] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0192] FIG. 1 is a signal timing diagram illustrating operation of a discrete read access system for a processor memory;

[0193] FIG. 2 is a functional block diagram of a central processing unit (CPU) with a multi-mode accessing control module in accordance with an embodiment of the present disclosure;

[0194] FIG. 3 is a functional block diagram of a computer incorporating a CPU with a multi-mode accessing control module in accordance with an embodiment of the present disclosure;

[0195] FIG. 4 is a functional block diagram of a multi-mode processor in accordance with an embodiment of the present disclosure;

[0196] FIG. 5 is a block and schematic diagram of a portion of the processor of FIG. 4;

[0197] FIG. 6 is an exemplary storage cell and corresponding bit line precharge circuit in accordance with an embodiment of the present disclosure;

[0198] FIG. 7 is a schematic diagram of a sense-amplifier circuit and corresponding sense-amplifier precharge circuit in accordance with an embodiment of the present disclosure

[0199] FIG. 8 is a logic flow diagram illustrating a method of operating a multi-mode processor in accordance with an embodiment of the present disclosure;

[0200] FIG. 9 is a signal timing diagram illustrating operation of the multi-mode processor during a sequential read mode of FIG. 8 in accordance with an embodiment of the present disclosure;

5 [0201] FIG. 10 is a logic flow diagram illustrating a method of operating a multi-mode processor in accordance with another embodiment of the present disclosure;

[0202] FIG. 11 is a logic flow diagram illustrating precharging method in accordance with a embodiment of the present disclosure;

10 [0203] FIG. 12 is a block and schematic diagram of a portion of a memory of FIG. 4.

[0204] FIG. 13 is a is a signal timing diagram illustrating delayed precharging of bit lines of a processor memory;

[0205] FIG. 14 illustrates a CPU with a branch prediction module in accordance with an embodiment of the present disclosure;

15 [0206] FIG. 15A is a functional block diagram of a hard disk drive;

[0207] FIG. 15B is a functional block diagram of a DVD drive;

[0208] FIG. 15C is a functional block diagram of a high definition television;

20 [0209] FIG. 15D is a functional block diagram of a vehicle control system;

[0210] FIG. 15E is a functional block diagram of a set top box; and

[0211] FIG. 15F is a functional block diagram of a mobile device.

DETAILED DESCRIPTION

25 [0212] The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical or. It should be understood that steps within a method may be executed in different
30 order without altering the principles of the present disclosure.

[0213] As used herein, the term module may refer to an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared,

dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality. A processor may refer to a logic circuit that processes stored instructions.

5 **[0214]** In the following description, the terms assert and assertion may refer to the transitioning of a signal line from a first state to a second state. For example, a signal line may be transitioned from a LOW state to a HIGH state or vice versa. The terms assert and assertion may also refer to the enabling of one or more cells or cell lines for cell selection. The cell lines may include word lines
10 or bit lines.

[0215] In addition, many variables are disclosed herein. A variable used in one embodiment or context may have a different meaning in a different embodiment or context. For example, the variable T may refer to a transistor, to time, or to an integer value.

15 **[0216]** Traditionally, when reading the word of instructions from the cache, memory cells associated with each instruction are individually accessed and latched. The word may include multiple instructions, two or more of which may be located along a single word line. The word may also include instructions that are located along different word lines. Multiple read cycles are executed to
20 access each word of instructions.

[0217] During each read cycle, the row path and multiple column paths associated with a particular instruction are asserted. Additional tasks include decoding row and column addresses, generating a word line signal, precharging associated bit lines, sensing-amplification and latching of the data. Each word
25 line of the array may include multiple instructions, which may be associated with the same or different words. For example only, four (4) to eight (8) instructions may be associated with one word line.

[0218] Referring now to FIG. 1, signal timing of a discrete read access mode for a processor memory is shown. Various signals that are based on a
30 clock signal 10 are generated. The timing diagram illustrates a word line signal 12, first and second bit line signals 14 and 16, a sense-amplification signal 18, column select signals 20₁-20_M and an instruction output signal 22.

[0219] Normally when reading an instruction during a read cycle, the word line signal 12 is asserted as shown by word line pulse 24₁ (generally referred to as word line pulse 24). N-1 other instructions are read during word line pulses 24₂-24_N, respectively, where N is an integer value. In addition, 2*I bit lines of cells corresponding to the instruction are also precharged, where I is the number of cells in an instruction.

[0220] The word line pulse 24 is generated for each read cycle. Each read cycle also includes accessing and latching bit information in cells associated with a particular instruction. The word line signal pulses 24₁-24_N are generated based on the rising edges 26₁-26_N of the clock signal 10, as indicated by arrows 27₁-27_N. The word line signal pulse 24₁-24_N is generated for each of clock pulses 28₁-28_N, respectively.

[0221] Activation of a word line causes bit line separation between voltage levels of bit lines. Bit line separation refers to a difference between voltage potentials of the bit lines of the memory cell. For example only, bit line separation is shown by varying gap 30 between the bit line signals 14, 16. Bit line separation may increase with the amount of time that the word line is enabled. Increase in bit line separation is shown by ramp portions 32₁-32_N of the second bit line signal 16 relative to the first bit line signal 14.

[0222] Bit lines associated with the word of instructions are precharged prior to the generation of the word line pulse and during a deactivation state. Bit line separation may return to minimum or no separation during precharging after the word line signal 12 is de-asserted, as illustrated by falling edges 38₁-38_N of the word line signal 12. A decrease in bit line separation is shown by ramp portions 40₁-40_N of the second bit line signal 16 relative to the first bit line signal 14.

[0223] Bit line separation occurs due to leakage of the memory cell. For example only, leakage can cause voltage potentials of bit lines to decrease or increase relative to each other, which may impact bit line separation. When bit line separation is too small, the ability to accurately read data from a cell decreases. When bit line separation is too large, access time may be decreased

and/or the amount of power needed to supply or remove from the bit lines to return the bit lines to a set separation may increase.

[0224] The sense-amplification signal 18 is generated to initiate acquiring, amplifying, and latching of bit information stored in a cell array. The sense amplification signal 18 is generated based on the rising edges 26, as denoted by arrows 41₁-41_N. The columns of the cell array that are associated with the instruction are selected. The selection may occur with the generation of the word line pulse. Five column selection signals are shown, which represent the selection of column sets associated with five instructions. The instructions may be associated with one or more words of instructions. The sense-amplification signal 18 is generated to detect bit line separation for the selected cells, which provides bit information.

[0225] The sense-amplification signal 18 may be generated with the falling edges of the word line signal 12 and the column selection signals 20₁-20_M, where M is an integer value. The bit information for each cell of the instruction is latched and provided as the instruction output signal 22 based on rising edges 42₁-42_N of the sense-amplification signal 18, as denoted by arrows 44₁-44_N. Four instructions of the instruction output signal 22 are shown and identified as Instruction [0]-Instruction[3].

[0226] When accessing the instruction, certain cells of the selected word line may be retrieved and latched. Other cells may be discarded where discarded refers to the non-selection and non-latching of bits within asserted cells. Since all of the cells along a word line are asserted for one read cycle and only one instruction is latched per word line assertion, bits of other asserted non-selected cells in that word line are discarded.

[0227] Power is wasted by asserting the same word line again for another instruction on the same word line.

[0228] According to the present disclosure, power consumption is reduced by reducing precharging events and/or assertion of the same word line when accessing instructions associated with the same word line.

[0229] Referring now to FIG. 2, an integrated circuit (IC) 45 includes a central processing unit (CPU) 46 that includes a multi-mode accessing control

module 50. The CPU may include one or more sets of inputs and outputs (I/O) such as those identified at 52 and 54, respectively.

[0230] The CPU 46 communicates with a memory 56, which may be implemented as part of the IC 45 or as a separate memory. The CPU 46 includes processor memory 59 that is integrated with the CPU 46. For example, the processor memory 59 may operate as cache for the CPU 46. The memory 59 may include RAM, SRAM or other high speed memory. The control module 50 operates in multiple read modes in association with the processor memory 59. A mass storage device 58 such as a hard disk drive may be provided to store data.

[0231] The control module 50 operates in a discrete read mode and a sequential read mode. During the discrete read mode, the control module precharges the bit lines and asserts the word line for each instruction. During the sequential read mode, the control module 50 reduces precharging of the bit lines and/or assertion of the word line when accessing multiple instructions along the same word line. As can be appreciated, the control module operates in discrete and sequential write modes as well using a similar approach.

[0232] Power can be saved reducing word line assertion and/or reducing precharging of bit lines. For example only, when two instructions are associated with the same word line, both instructions are accessed using a single word line assertion. For example only, when two or more instructions are associated with the same word line, the bit lines can be precharged once rather than two or more times. One or both of these approaches may be used to reduce power consumption as compared to the discrete read mode.

[0233] The memory 56 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, semiconductor memory, solid state memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 58 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD).

[0234] Referring now to FIG. 3, a functional block diagram of a computing device 60 is shown. The computing device 60 operates in the sequential read mode and the discrete read mode and/or the sequential write

mode and the discrete write mode. The computing device 60 may be a cellular phone, network switch, router or interface, a personal computer, such as a desktop or laptop computer, a personal data assistant, an MP3 player, a global positioning system (GPS) device, etc.

5 **[0235]** The computing device 60 includes a CPU 61 that has a multi-mode accessing control module 62 that controls access to the memory 59. The computing device 60 may also include a power supply 63, memory 64, a storage device 66, and a cellular network interface 67. The CPU 61 also includes processor memory 69. The processor memory 69 may be operated as cache.
10 The CPU 61 may also include a network interface 68, a microphone 70, an audio output 72 such as a speaker and/or output jack, a display 74, and a user input device 76 such as a keypad and/or pointing device. If the network interface 68 includes a wireless local area network interface, an antenna (not shown) may be included.

15 **[0236]** During the discrete read mode, the control module 62 precharges the bit lines and asserts the word line for each instruction. During the sequential read mode, the control module 50 reduces precharging of the bit lines and/or assertion of the word line when accessing multiple instructions along the same word line. Power can be saved by reducing word line assertion and/or
20 precharging of bit lines.

[0237] The processor 61 may receive input signals from other devices such as the cellular network interface 67, the network interface 68, the microphone 70, and/or the user input device 76. The processor 61 may process signals, including encoding, decoding, filtering, and/or formatting, and generate
25 output signals. The output signals may be communicated to one or more of the memory 64, the storage device 66, the cellular network interface 67, the network interface 68, and the audio output 72.

[0238] Referring now to FIG. 4, an exemplary multi-mode processor 100 is shown. The processor 100 may be used in the embodiments of FIGs. 2
30 and 3. The processor 100 includes a memory cell array 102, which includes rows and columns of memory cells. The memory cells are accessed through row and column selection. A row is selected by asserting a word line and a

column is selected by asserting or precharging a pair of bit lines. Word line signals are denoted as 104_{1-S} and bit line signals are denoted as 106_{1-T} where S and T are integer values.

5 **[0239]** An address and control signal latch 110 receives address information, which is used by a row decoder 112 and a column decoder 114 to select the rows and columns of the memory cell array 102. The address and control signal latch 110, as well as other elements of the processor 100, such as the row decoder 112 and the column decoder 114, may be considered part of a multi-mode control module 115.

10 **[0240]** The address and control signal latch 110 may include the multi-mode accessing control module 115 and/or a timing control module 116. The address and control signal latch 110 communicates with a bus and receives a signal that has data D0-DN that is stored on the memory cell array 102 during a write mode. The address and control signal latch 110 may also receive a
15 precharge (PCH) signal, a signal-to-quantization ratio (SQR) signal, a write enable signal (WEN), a chip enable signal (CEN), and an output enable signal (OEN) for respective improvement in SQR, enablement of the write mode, operation of the memory cell array, and generation of an output signal.

20 **[0241]** The SQR signal may indicate whether the processor 100 is operating in a sequential read mode or in a discrete read mode. The PCH signal may indicate when the processor is performing a precharge of bit lines.

25 **[0242]** The processor 100 further includes a bit line precharge circuit 120, a column multiplexer 122, a sense-amplifier/write driver module 124, and a data latch/output buffer module 126. The bit line precharge circuit 120 is used to precharge the bit lines of the memory cell array 102. The bit line precharge circuit 120 may include drivers, buffers, transistors and/or other bit line asserting elements. The bit line precharge circuit 120 may be coupled between the memory cell array 102 and the column multiplexer 122 or may be located on an opposite side of the memory cell array 102 as the column multiplexer 122, as
30 shown by dashed bit line precharge circuit 120'. The bit line precharge circuit may precharge all of the bit lines 106_{1-T} during each precharge event.

[0243] During a read mode, the column multiplexer 122 is used to select the columns of the memory cell array 102 for latch purposes via column selection signals 128_{1-U} , where U is an integer value. After precharging of the bit lines, the column decoder 114, via the column multiplexer 122, selects certain columns. Stored bits, associated with the selected columns, are provided to one or more sense amplifiers of the sense-amplifier/write driver module 124 for amplification prior to reception by the data latch/output buffer module 126. The stored bits are received as bit information signals 130_{1-V} , where V is an integer value.

[0244] The sense-amplifier/write driver module 124 receives a read/write mode signal 136, a sense-amplifier (SA) precharge signal 138, and a SA enable signal 140. The read/write mode signal 136 is a command signal for read or write operation. The SA precharge signal 138 and the SA enable signal 140 are generated to initiate and activate SA cells of the sense-amplifier/write driver module 124. The amplified data is latched and provided in the form of an output signal 134 by the data latch/output buffers module 126 based on a latch signal 142 from the address and control signal latch 110.

[0245] During the write mode, cells in the memory cell array 102 are similarly asserted via the row decoder 112 and the column decoder 114. The received data DO-DN is provided to the bit lines via write drivers in the sense-amplifier/write driver module 124.

[0246] Referring also to FIG. 5, a portion of the processor 100 is shown. The memory cell array 102 includes cells $150_{1-X, 1-Y}$, which each store a bit of information. The cells $150_{1-X, 1-Y}$ are asserted via word lines 152_{1-Y} by the row decoder 112 and via bit lines 154_{1-W} by the column decoder 114 and the bit line precharge circuit 120, where X , Y and W are integer values. Row decoding and column decoding is based on an address input signal 155. Each of the cells $150_{1-X, 1-Y}$ has an associated first bit line and a second bit line, such as first bit lines 156_{1-X} and second bit lines 158_{1-X} for cells 160_{1-Y} , 162_{1-Y} , respectively.

[0247] The first bit lines 156 are coupled together by a first common line 164 through respective transistors 166_{1-W} of the column multiplexer 122. The second bit lines 158_{1-X} are coupled together at a second common line 168

through respective transistors 170_{1-W} of the column multiplexer 122. The column decoder 114 selects the cells $150_{1-X, 1-Y}$ via the column multiplexer 122. The column multiplexer 122 may include transistors, as shown, or other bit line selection devices. The transistors may include p-channel metal-oxide-semiconductor field-effect (PMOS) transistors, as shown, or other transistors.

[0248] For the example embodiment shown, a sense-amplifier (SA) 180, a latch (shown as a D-flip flop) 182, and a write driver 184 are included. The SA 180 is coupled to the column multiplexer 122. The SA 180 and the write driver 184 are part of the sense-amplifier/write driver module 124. The SA 180 includes first and second inputs lines 186, 188, a SA enable input 190, a SA precharge input 192 and a SA output 194. The first input line 186 is coupled to the first common line 164 and the second input line 188 is coupled to the second common line 168. The first common line 164 and the second common line 168 have SA bit A and SA bit B signals, respectively. The SA enable input 190 and the SA precharge input 192 receive the SA enable signal 140 and the SA precharge signal 138, which may be generated by the control module 115 and/or the address and control signal latch 110.

[0249] Information on selected bit lines is provided via the column multiplexer 122 and detected and amplified by the SA 180. An SA output signal 196 from the SA output 194 is provided to the latch 182 at terminal D. Data at terminal D is latched and provided to data output terminal $\bar{Q}$ of the latch 182 and outputted as a data output signal 198. The data is latched based on the received latch signal 142. The received latch signal 142 may be generated by the control module 115 and/or the address and control signal latch 110. The SA 180 receives the SA precharge signal 138 and asserts the SA input lines 186, 188 (best seen in FIG. 6).

[0250] The latch 182 and the write driver 184 are respectively used for output and writing purposes. The latch 182 may be a D-flip flop as shown or some other latching device. The latch 182 acquires data on the SA output 194 and may be part of the data latch/output buffer module 126. The write driver 184 receives a data input signal 200 and provides data, which may be amplified, on

the common lines 164, 168. From the common lines 164, 168 the data may be provided to the appropriate column of bit lines.

[0251] Referring to FIG. 6, an exemplary storage cell 210 and a corresponding bit line precharge circuit 212 is shown. The cell 210 is provided to illustrate one example configuration of a cell, which may be incorporated in the memory cell array 102 described above. Other configurations may be used.

[0252] The cell 210, as shown, includes four storage transistors M1-M4 and two access transistors M5, M6. The four storage transistors M1-M4 form two-cross-coupled inverters that store a bit of information. The access transistors M5, M6 control access to the four storage transistors M1-M4, during read and write operations. The four storage transistors M1-M4 serve as a storage cell. The precharge circuit 212 includes transistors M7, M8, M9. The transistors M1-M9 may be PMOS or n-channel MOSFET (NMOS) transistors, as shown, or other transistors. In the embodiment shown, the transistors M2, M4, and M7-M9 are PMOS transistors and the transistors M1, M3, M5, M6 are NMOS transistors. The transistors M1-M9 have respective source terminals M_{S1} - M_{S9} , drain terminals M_{D1} - M_{D9} , and gate terminals M_{G1} - M_{G9} .

[0253] The cell 210 has a word line 214 and may have the first and second bit lines 156, 158. The first and second transistors M1, M2 are coupled in series and in parallel to the third and fourth transistors M3, M4, which are also coupled in series. The source terminals M_{S2} , M_{S4} are coupled to a positive power source terminal Vdd. The drain terminals M_{D2} , M_{D4} are coupled to source terminals M_{S1} , M_{S3} . The gate terminals M_{G1} , M_{G2} are coupled together and to source terminal M_{S3} . The gate terminals M_{G3} , M_{G4} are coupled together and to the drain terminal M_{D2} . The drain terminals M_{D1} , M_{D3} are coupled to a negative power source terminal Vss. The source terminal M_{S5} is coupled to the drain terminal M_{D2} . The source terminal M_{S6} is coupled to the drain terminal M_{D4} . The source terminal M_{S5} and the drain terminal M_{D7} are coupled together and to the first bit line 156. The source terminal M_{S6} and the drain terminal M_{D9} are coupled together and to the second bit line 158.

[0254] Capacitance devices 220, 222, are shown and represent respective capacitance of bit line storage circuits associated with the bit lines

156, 158. The capacitance devices 220, 222 may be discrete storage capacitors, as shown, or may represent capacitance measured at each of the bit lines 156, 158 relative to reference potentials.

5 **[0255]** The bit line precharge circuit 212 receives a bit line precharge signal 224 via the bit line precharge input 226, which is provided to the gates M_{G7} - M_{G9} . The sources M_{S7} , M_{S9} are coupled to the power source terminal Vdd. The drain M_{D7} is coupled to the source M_{S8} and the drain M_{D9} is coupled to the drain M_{D8} .

10 **[0256]** Access to the cell 210 is enabled by assertion of the word line 214, which controls the access transistors M5, M6. In general, voltage potential of the second bit line 158 may be an inverse of the voltage potential of the first bit line 156. The cell 210 has three modes of operation, standby, read and write. Bit values, such as a zero (0) and a one (1) that are stored at locations denoted Q and $\bar{Q}$. During standby mode the word line 214 is not asserted and the
15 transistors M1-M4 reinforce each other.

20 **[0257]** During the read mode, a read cycle is started by precharging both of the bit lines 156, 158. The word line 214 is then asserted, thereby enabling the transistors M5, M6. The stored values Q and $\bar{Q}$ are transferred to the bit lines 156, 158 by maintaining charge on one of the bit lines and discharging the other bit line. The bit line for which charge is maintained is pulled to Vdd. The bit line that is discharged is pulled to ground.

25 **[0258]** During the write mode, a value to be written is applied to the bit lines 156, 158. The word line 214 is then asserted and the value to be stored is latched into the cell 210. Write drivers override the previous state of the cross-coupled inverters.

30 **[0259]** Referring to FIG. 7, a schematic diagram of a SA circuit 230 including a SA precharge circuit 232 is shown. The SA circuit 230 and the SA precharge circuit 232 may be used as part of or in replacement of the SA 180. The SA circuit 230 includes five transistors T1-T4, which form an SA cell 234 and are cross-coupled, and a fifth transistor T5. The SA precharge circuit 232 includes three transistors T6-T8. The transistors T1-T8 may be PMOS or n-channel MOSFET (NMOS) transistors, as shown, or other transistors. In the

embodiment shown, the transistors T2, T4, and T6-T8 are PMOS transistors and the transistors T1, T3, T5 are NMOS transistors. Each of the transistors T1-T8 has respective source terminals T_{S1} - T_{S8} , drain terminals T_{D1} - T_{D8} , and gate terminals T_{G1} - T_{G8} .

5 **[0260]** The first and second transistors T1, T2 are coupled in series and in parallel to the third and fourth transistors T3, T4, which are also coupled in series. The source terminals T_{S2} , T_{S4} are coupled to a positive power source terminal Vdd. The drain terminals T_{D2} , T_{D4} are coupled to the source terminals T_{S1} , T_{S3} . The gate terminals T_{G1} , T_{G2} are coupled together and to the source terminal T_{S3} . The gate terminals T_{G3} , T_{G4} are coupled together and to the drain terminal T_{D2} . The drain terminals T_{D2} , T_{D4} may be respectively coupled to the common lines 186, 188, which may be referred to as SA common lines. The drain terminals T_{D1} , T_{D3} are coupled to the source terminal T_{S5} . The gate terminal T_{G5} may be coupled to the SA enable input 190. The drain terminal T_{D5} is coupled to a negative power source terminal Vss. The drain terminals T_{D2} , T_{D6} are coupled together. The drain terminals T_{D4} , T_{D8} are coupled together.

[0261] The SA precharge circuit 232 receives the SA precharge signal 138 via the SA precharge input 192, which is provided to the gate terminals T_{G6} - T_{G8} . The source terminals T_{S6} , T_{S8} are coupled to the power source terminal Vdd. The drain terminal T_{D6} is coupled to the source terminal T_{S7} and the drain terminal T_{D8} is coupled to the drain terminal T_{D7} .

[0262] Inverters 240, 242 are coupled to the common lines 186, 188. One of the common lines 186, 188 is provided to the data input D of the latch 182. Although the second common line 188 is shown as being coupled to the data input D, the first common line 186 may be coupled to the data input D.

[0263] Referring to FIGs. 8 and 9, flow and timing diagrams are shown. The timing diagram includes multiple signals that are based on a clock signal 300 and a sequential read signal 302. The sequential read signal 302 is indicative of a sequential read mode. For the example shown, when the sequential read signal 302 is HIGH, a processor is operated in a sequential read mode; otherwise the processor is operated in a discrete read mode. The timing diagram includes a word line signal 304, bit line signals (voltage levels) 306, 308,

a SA enable signal 310, a SA bit A signal 312, a SA bit B signal 314, column select signals 316_{1-M} and an instruction output signals 318. Although several of the steps of the flow diagram are described below with respect to the timing diagram, the flow diagram may be modified to apply to other timing diagrams and/or embodiments of the present disclosure.

[0264] The flow diagram may begin at step 399. In step 400, a read signal is generated to read a word of instructions from a processor memory, such as the processor memories 59, 69. In step 401, received addresses for the word of instructions are row and column decoded, such as by the row and column decoders 112, 114.

[0265] In step 402, the processor determines whether two or more of the instructions are located along a single word line. When two or more instructions are located along a single word line, the processor proceeds to step 403. When the processor is reading a single instruction along a word line, the processor proceeds to step 405. Steps 400-432 or any portion thereof may be repeated when reading instructions from multiple word lines.

[0266] In step 403, the processor generates the sequential read signal 302, illustrated by rising edge 320. In step 406, the processor prepares for a sequential read. Between the rising edge 320 and a rising edge 322 of the clock signal 300, the processor may perform tasks to prepare for the sequential read. The tasks may include initializing an instruction counter, setting parameters for generation of an extended word line signal, generating SA precharge signals for read cycles, precharging of bit lines, precharging of common lines, etc. The extended word line signal refers to a word line pulse that is increased in duration to increase bit line separation.

[0267] In step 405, the processor generates a discrete read signal. After performance of step 405 or 406, step 407 is performed.

[0268] In step 407, bit lines for cells along a word line and associated with the word of instructions are precharged. Steps 406 and/or 407 may be repeated when control does not have knowledge of a previous precharge of bit lines and/or timing of a precharge of bit lines is undetermined or improper. Control may not have knowledge of a previous precharge when control cannot

determine the current precharged state of the bit lines or the state of a current read sequence. The state of the read sequence may include the state of a word line, such as when a word line has been asserted.

5 **[0269]** The timing of a precharge of bit lines may be improper when the amount of time between precharge events exceeds a predetermined period. When the amount of time since the last precharge event exceeds the predetermined period, an accurate read may not be able to be performed due to an improper amount of bit line separation. Thus, a precharge may be performed before the predetermined period is exceeded. Steps 406 and 407 may not be
10 repeated when control does have knowledge of a previous precharge of bit lines and/or timing of a precharge is known and/or proper.

[0270] Control may perform a precharge, which may be in addition to a previous precharge, based on knowledge, timing, and state of a current precharge. A precharge instruction may be generated at any point in the
15 sequential read mode to perform a precharge. Thus, steps 406 and 407 may be repeated independently of prior precharging. For example, step 407 may be repeated and performed during or after step 424. In other words, another precharge event of the bit lines may be performed between steps 424 and 432, although instructions along a current word line have not all been received and/or
20 executed. A precharge command signal may be generated to perform a precharge.

[0271] Control parameters may be updated to account for the precharge performed based on the precharge command signal. When a precharge command signal is generated, control may continue to perform in the
25 current operating mode, such as a sequential read mode or a discrete read mode, or may change operating modes. For example, when operating in a sequential read mode and upon generation of a precharge command signal, control may perform a precharge and continue operating in the sequential read mode or begin operating in a discrete read mode.

30 **[0272]** In step 408, the processor generates the word line signal 304, illustrated by rising edge 324 of the word line signal 304, in the middle of a clock pulse 326 based on the row decoded addresses. The word line signal 304 is in

the form of a pulse, which is generated for a first instruction, Instruction [0]. The word line signal 304 may not be generated for subsequent instructions, which are accessed along the same or a single word line. The word line signal 304 remains in an active or HIGH state until after detection of a falling edge 328 of the clock signal 300 and until approximately the middle of a subsequent LOW clock signal state. This provides an extended active word cycle, which increases bit line separation. An extended period of the word line signal 304 is denoted as E_t .

[0273] In order to accurately read bits from a cell array, a minimum bit line separation is provided. This bit line separation may be provided by a multi-mode accessing control module or by a timing control module. The minimum separation may be approximately equal to or greater than 100mV. In one embodiment, the extended active word cycle is set to allow for a bit line separation of approximately equal to the minimum separation plus at least 30mV, as denoted by maximum bit line separation BL_{max} . In another embodiment, the extended word cycle is set to allow for bit line separation of approximately 150mV. The extended word cycle is directly related to number of read cycles for a given word of instructions or number of instructions read for the generated word line signal 304. The additional separation increases the likelihood of an accurate read for each read cycle.

[0274] When performing multiple read access cycles, such as in a sequential read mode, control accounts for the amount of leakage that may occur during the read access cycles. The magnitude and polarity of precharging, the number of access cycles, and the timing of the precharging and access cycles are selected and performed to maintain a minimum precharge separation and to assure that a maximum precharge separation is not exceeded.

[0275] A bit line separation range may be stored and used to assure that the bit line separation remains within a maximum and minimum separation. Control may have predetermined precharge information relating to an amount of separation that occurs over one or more read cycles. Control may operate in the sequential read mode or perform multiple access cycles for a single precharge

based on a clock frequency. For example, control may operate in a discrete mode at high frequencies and in a sequential read mode for low frequencies.

[0276] In step 410, with the generation of the word line signal 304, bit line separation begins and thus, voltage potential across bit line pairs increases.

5 The maximum bit line separation BL_{max} occurs approximately with a falling edge 330 of the word line signal 304. The generation of the word line signal causes bit line separation between voltage levels of bit lines.

[0277] In step 412, a column selection signal, such as one of the column selection signals 316, is generated to select one or more columns or pair
10 of bit lines associated with an instruction. The column selection signal is generated based on the column decoded addresses. The column selection signal may be provided to a column multiplexer, such as the column multiplexer 122, for selection of the appropriate bit lines. The selection may occur with and/or during the same time period as the generation of the word line signal. In
15 step 414, with the generation of the column selection signal, voltage potential of the common lines begins to separate.

[0278] In step 415, the SA enable signal 310 is generated. SA pulses 332_{1-N} are generated based on rising edges of the clock signal 300, as denoted by arrows 334_{1-N} . The SA enable signal 310 activates a SA cell. For example,
20 the SA enable signal 310 may activate the fifth transistor S_{T5} , which enables current flow through the SA cell and detection and amplification of SA bit A and/or SA bit B signals 312, 314. The SA bit A and/or SA bit B values are detected and amplified for each of the selected cells. For each cell, a first common line is pulled to voltage potential V_{dd} and a second common line is
25 pulled to ground.

[0279] In step 416, the instruction output signal 318 is generated, which includes data from each of the selected cells for the current instruction. Each instruction portion of the instruction output signal 318 is generated based on the rising edges 370_{1-N} of the SA enable signal 310, as denoted by arrows
30 372_{1-N} . Either a SA bit A or a SA bit B value is provided to a latch for each of the selected cells. The SA bit A or SA bit B signals 312, 314 may be inverted prior

to being received by the latch. A latch signal may be generated to latch the SA bit A or SA bit B values to generate the instruction output signal.

[0280] In step 417, the word line signal 304 is deactivated or transitioned from a HIGH state to a LOW state. The deactivation of the word line signal 304 causes the potential of the bit lines to drift as a result of leakage. Over time and read cycles the potential across the bit lines decreases. In the example shown, a voltage potential of a first bit line decreases by approximately 2mV over a 40ns period and relative to a first original state of the first bit line, as denoted by bit line drift BL_D . The voltage potential of a second bit line increased toward the first bit line. The extended active word cycle assures that there is enough bit line separation during a last read cycle along a word line.

[0281] In step 418, when multiple instructions are being read along a single word line, control proceeds to step 420, otherwise control proceeds to step 419. In step 419, when another read signal is generated, control returns to step 401, otherwise control may end.

[0282] In step 420, the instruction counter is incremented by one (1). In step 421, the column address may be advanced. The column address may be advanced linearly, successively, or in an interleaved fashion. In step 422, control determines whether the instruction counter is greater than a maximum instruction counter value. The maximum instruction counter value may be a predetermined and/or stored value. When the instruction counter is not greater than the maximum instruction counter value then step 424 is performed, otherwise control proceeds to step 419. In step 419, when another read signal is generated, control returns to step 401, otherwise control may end.

[0283] In step 424, upon detection of a rising edge of the next clock cycle, the SA enable signal 310 is transitioned from a HIGH state to a LOW state and a SA precharge signal is generated to precharge the SA common lines. The precharge for each cycle is shown by the rising edges 350_{1-N} of the SA bit B signal 314 of one of the SA common lines. The rising edges 350_{1-N} are based on the rising edges of the clock signal 300, as denoted by arrows 352_{1-N-1}. This illustrates potential between the SA common lines decreasing. Note that the energy used to precharge the SA common lines is less than the energy used to

precharge the bit lines. For example, the energy to precharge the SA common lines may be approximately 10% of the energy for precharging the bit lines. Thus, energy is saved in performing a SA precharge for each read cycle, as opposed to performing a bit line precharge for each read cycle.

5 **[0284]** In step 425, column decoding is performed to determine bit lines associated with a next instruction. In step 426, a next column selection signal is generated, such as one of the column selection signals 316, and voltage potential of the SA common lines begin to separate.

10 **[0285]** In step 428, the SA enable signal 310 is activated. The SA enable signal activates a SA cell. For example, the SA enable signal may activate the fifth transistor S_{T5} , which enables current flow through the SA cell and detection and amplification of SA bit A and SA bit B signals 312, 314 for each of the selected cells.

15 **[0286]** In step 432, the next instruction output signal is generated. Either a SA bit A or a SA bit B value is provided to a latch for each of the selected cells. The SA bit A or SA bit B signals 312, 314 may be inverted prior to being received by the latch. A latch signal may be generated to latch the SA bit A or SA bit B values to generate the instruction output signal.

20 **[0287]** As an alternative, a SA enable signal and a latch signal may be generated to acquire, amplify, and latch bit information associated with the selected instruction for a current read cycle. The sense-amplification signal may be generated to detect bit line separation for the selected cells, which provides bit information. The sense-amplification signal may be generated with the falling edges of the word line signal and the column selection signal. The bit
25 information for each cell may be latched and provided as an output signal, denoted as instructions in the output signal. Upon completion of step 432, the processor may return to step 420 and repeat steps 420-432 for a next instruction.

30 **[0288]** The above-described steps are meant to be illustrative examples; the steps may be performed sequentially, synchronously, simultaneously, or in a different order depending upon the application.

[0289] Referring now to FIG. 10, another method of operating a multi-mode processor is shown. The method may begin at step 439. In step 440, a read signal is generated to read one or more word(s) of instructions from a processor memory, such as the processor memories 59, 69. In step 441, a maximum word count is set equal to the number of words to access. In step 442, a word counter is initialized. The word counter is set equal to the value one (1). In step 444, received addresses for the word(s) of instructions are row and column decoded, such as by the row and column decoders 112, 114. The received addresses may be received during separate time intervals and decoded as received.

[0290] Control may access cells associated with each word, as addresses for that word are received. For example, control may access cells associated with a first word before accessing cells associated with a second word. The cells associated with a word may be associated with one or more word lines. The word lines associated with each word may be accessed in any order. When accessing each word line steps 402-432 of the method of FIG. 8 may be performed.

[0291] In step 446, cells associated with a first or current word line are accessed. During step 446 control may perform steps 402-432. In step 446A, which may correspond with step 407, a first set of bit lines associated with the current word line is precharged. In step 446B, which may correspond with step 408, the current word line is accessed via generation of a first word line signal. After generation of the appropriate instruction output signal(s) associated with the current word line control proceeds to step 448.

[0292] In step 448, the word counter is incremented. In step 450, when the word counter is greater than the maximum word count, control proceeds to step 452, otherwise control proceeds to step 453. In step 453, when another read signal is generated control may return to step 441, otherwise control may end, identified by step 454.

[0293] In step 452, cells associated with a second or next word line are accessed. During step 452 control may perform steps 402-432. In step 452A, which may correspond with step 407, a second or next set of bit lines associated

with the next word line is precharged. The next set of bit lines may be included in the previous set of bit lines. In step 452B, which may correspond with step 408, the next word line is accessed via generation of a second or next word line signal. After generation of the appropriate instruction output signal(s) associate
5 with the next word line control returns to step 448.

[0294] Referring now to FIG. 11, a precharging method is shown. The following steps 600-622 may be performed when a processor is operating in a sequential read mode. The method may begin at step 599.

[0295] In step 600, a read command is received and/or generated to
10 perform a series of read instructions_{1-X}. The instructions_{1-X} may be associated with a single word line 152₁. In step 602, a program counter value P₁ is set equal to 1. In step 604, a precharge is formed on bit lines associated with the word line. In step 606, an output instruction signal is generated based on the precharge of step 604. The output instruction signal may be generated based on
15 a read of one of the instructions_{1-X}.

[0296] By reading the instructions_{1-X}, the processor executes a program. The instructions are received from the processor memory and are generally performed in a sequential order. In processing the instructions_{1-X}, a program counter, such as a program counter that stores the program counter
20 value P₁, may be used to track a current position in the program. The processor determines tasks to perform based on the instructions_{1-X}. The instructions_{1-X} may include branch instructions. When a branch instruction is received, the processor may be directed to read from cells along a different word line than previously asserted, such as the word line 152_Y. Thus, the program counter
25 instead of being incremented to the next sequential instruction may be changed to point to an instruction some where else in the program or another program counter may be used.

[0297] In step 608, when the program counter value P₁ is equal to the number of instructions X, control ends at step 609. When the program counter
30 value P₁ is less than the number of read instructions X, control proceeds to step 610. In step 610, control increments the program counter value P₁.

[0298] The following steps 614-620 may be performed during the same time period and/or in parallel. In step 614, control checks whether a precharge flag is set. The precharge flag may indicate that a previous precharge has been performed, such as the precharge of step 604. When a previous precharge has not been performed control may proceed to step 622, otherwise control may proceed to step 618.

[0299] In step 618, control determines whether timing of a previous precharge is undetermined or improper. When timing of a previous precharge is undetermined or improper, control proceeds to step 622, otherwise control may proceed to step 620.

[0300] In step 620, control determines whether a branch instruction is received to read another set of instructions_{1-w}. When the branch instruction is received, control may proceed to step 624, otherwise control may proceed to step 621.

[0301] When executing the branch instruction, the processor may branch out of a current set of instructions_{1-x} to perform other instructions, such as instructions_{1-w}. Thus, the processor may cease performing a sequential read in association with a current word line 152₁ and initiate another sequential read in association with another word line 152_y. In FIG. 12, a portion of the memory 102 is shown. The set of instructions_{1-w} may be associated with the word line 152_y, whereas the set of instructions_{1-x} may be associated with the word line 152₁. Branch out arrows 700 are shown to indicate that a branch instruction has been generated and/or received and that cells along a different word line are to be read. Performance of the instructions_{1-w} is provided by steps 624-638.

[0302] For example only, when a branch instruction is generated and control is directed to a "do loop", a sequential read may be interrupted and multiple precharge events may be performed. A "do loop" refers to a set of instructions that are repeatedly performed. When performing a branch instruction, the processor may jump to a set of instructions and execute the set of instructions once or repeatedly. The processor after performing the set of instructions may continue on in the program or return to an instruction sequentially following the branch instruction. A return instruction may be

received that directs the processor to return to the instruction following the branch instruction. The multiple precharge events may be performed before the full length of the original sequential read is completed.

5 **[0303]** Due to the reception of the branch instruction another precharge is performed in step 624. As a default when control does not have knowledge of a precharge and/or when a branch instruction has been generated, control may perform a precharge.

10 **[0304]** In step 621, control generates another output instruction signal. The output instruction signal may be based on the precharge of step 604 or another precharge. In step 624, control performs a precharge on the bit lines. The precharge is performed for access to the set of instructions_{1-W}.

[0305] In step 628, control sets a program counter value P_2 equal to 1. In step 630, control generates an output instruction signal associated with the instructions_{1-W}.

15 **[0306]** In step 632, when the program counter value P_2 is equal to the number of instructions W , control ends at step 634 or returns to step 604 when continuing on with the instructions_{1-X}. When the program counter value P_2 is less than the number of read instructions W , control proceeds to step 636. In step 636, control increments the program counter value P_2 .

20 **[0307]** In step 638, control generates another output instruction signal. The output instruction signal may be based on the precharge of step 626 or another precharge. Control may repeat and/or perform steps 614-620 during the reading of instructions_{1-W}.

25 **[0308]** Referring now to FIG. 13, a signal timing diagram illustrating delayed precharging of bit lines of a processor memory is shown. The precharge of bit line signals may occur at various times and conditions. Additional precharging may occur during low processor clock rates. When the clock rate is slow or reduced, power consumption is decreased. However, a period between precharge events increases with a decrease in clock rates.

30 When slowing the clock rate to reduce power, control may operate in a discrete read mode, perform additional precharging and/or repeat assertion of the word line associated with the current word.

[0309] When the clock rate is reduced, precharging may be delayed to reduce leakage. When the bit lines are fully precharged, leakage may be at a maximum rate. After a precharge event, the amount and rate of leakage decreases.

5 **[0310]** The delay in precharging may occur for a predetermined period of time. When the clock rate increases, control may return to normal precharge timing. Also, precharging may be performed in time close to and before the generation of a word line signal. This maximizes the time between precharges and decreases power consumption. In other words, power consumption is
10 reduced by delaying a precharge until just before the generation of a word line signal.

[0311] FIG. 13 provides an example of when the clock rate is reduced. A clock signal 710, a word line signal 712, a precharge signal 714, and bit line signals 716 and 718 are shown. The rate of the clock signal 710 changes from a
15 high rate to a low rate, as shown by the increase in time between rising edges 720₁₋₃ of the clock signal 710. ΔT_1 represents the time period between first and second clock pulses 722₁ and 722₂ of the clock signal 710. ΔT_2 represents the time period between second and third clock pulses 722₂ and 722₃ of the clock signal 710. ΔT_2 is greater than ΔT_1 .

20 **[0312]** During the time period ΔT_2 , the processor may refrain from precharging. This delay in precharging reduces leakage in memory cells of the processor memory. The leakage may refer to the amount of current that leaks through transistors, such as pass-gate and pull-down transistors, in a memory cell between reference potentials, such as Vdd and ground. Reference
25 potentials V_1 and V_2 are shown for bit lines 716 and 718.

[0313] As an example, current may leak through transistors M6 and M3 of FIG. 6 between Vdd and Vss, as indicated by bit line leakage current i_{BL} . The leakage current exists when the transistors M6 and M3 are in an OFF state. As the bit line separation increases, the bit line current i_{BL} decreases.

30 **[0314]** The bit lines 716 and 718 as shown include two precharge events P1 and P2. The first precharge event P1 begins at a first rising edge 730₁ of the precharge signal 714 and ends at time t_1 . The second precharge event P2

occurs at a second rising edge 730₂ of the precharge signal 714 and ends at time t₄. The first precharge event P1 occurs when the clock rate is high and the second precharge events P2 occurs when the clock rate is low.

[0315] After rising edges, such as rising edges 740₁ and 740₂, of the word line signal 712 bit line separation begins. Thus, the bit lines 716, 718 begin to separate at time t₁. ΔQ_1 represents charge used during time period ΔT_4 , which is time between times t₁ and t₂, due to leakage. ΔQ_2 represents charge used to precharge the bit lines during time period ΔT_6 , which is the time between times t₃ and t₄. Charges ΔQ_1 and ΔQ_2 are provided by equation 1, where i_{sc} represents transistor saturation current, such as PMOS saturation current for precharge transistors.

$$\Delta Q_1 = \Delta Q_2 = i_{sc} \cdot \Delta T_4 = i_{sc} \cdot \Delta T_6 \quad (1)$$

[0316] Instead of precharging at time t₂, control refrains from precharging until time t₃. Time t₃ may be determined based on a predetermined amount of time to precharge the bit lines 716 and 718, the current clock rate and timing of clock pulses, and/or a predetermined time of a next rising edge of a word line signal. When a read access cycle and or a rising edge of a word line signal is anticipated, a precharge may be performed beginning at time t₃ as identified by rising edge 730₂. In other words, the precharge is performed close in time and before the anticipated word line pulse. ΔT_5 represents the time period between times t₂ and t₃. During the time period ΔT_5 , charge ΔQ_{SV} is saved. However, due to a switching charge ΔQ_{SW} associated with a switching precharge device, such as a precharging circuit used to precharge the bit lines 716 and 718, the net charge saved ΔQ_N is provided by equation 2.

$$\Delta Q_N = \Delta Q_{SV} - \Delta Q_{SW} \quad (2)$$

[0317] The switching charge ΔQ_{SW} is provided by equation 3, where C is capacitance of the precharging device. The capacitance may also include capacitance of corresponding signal lines.

$$\Delta Q_{SW} = C \cdot V_{dd} \quad (3)$$

[0318] The wireless network devices and systems disclosed herein, may comply with IEEE standards, such as 802.11, 802.11a, 802.11b, 802.11g,

802.11h, 802.11n, 802.16, and 802.20. Also, the embodiments disclosed herein may utilize and/or incorporate Bluetooth devices and techniques.

[0319] Referring now to FIG. 14, a CPU 760 comprises a fetch/decode module 764 that fetches and decodes sequential and branch instructions from memory such as instruction cache 766. Some of the instructions may be pre-fetched and decoded in advance. For example only, the instruction cache 766 includes sequential instructions 768-S1, 768-S2, ..., and 768-S6 (collectively sequential instructions 768-S). For example only, the instruction cache 766 also includes branch instructions 768-B1, 768-B2, and 768-B3 (collectively branch instructions 768-B). As can be appreciated, branch and sequential instructions may be arranged in any sequence.

[0320] The fetch/decode module 765 or another component of the CPU 760 includes a program counter (PC) 765. The program counter 765 keeps track of the location of the next instruction in the instruction memory 766. The CPU 760 further includes a branch prediction module 776 that predicts the outcome of a branch instruction to facilitate the efficiency of pre-fetching and decoding. The branch prediction module 776 may comprise a branch history module 780 that stores branch prediction data for branch instructions.

[0321] The instructions are typically stored in successive addressable locations within the memory such as the instruction cache 766 of the CPU 760. When processed by the CPU 760, the instructions are fetched from consecutive memory locations and executed. Each time an instruction is fetched from memory, the program counter 765 within the CPU 760 is incremented so that it contains the address of the next instruction in the sequence. Fetching of an instruction, incrementing of the program counter 765, and execution of the instruction continues until a branching instruction is encountered.

[0322] The branching instruction, when executed, changes the address in the program counter 765 and causes the flow of control to be altered. For example only, the branch instructions may include conditional or unconditional branches. Example branch instructions include jump, test and jump conditionally (such as if...then...else or similar), call, return, etc. The jump instruction causes the CPU 760 to unconditionally change the contents of the

program counter 765 to a specific value, such as the target address for the instruction where the program is to continue execution.

5 **[0323]** The test and jump conditionally instruction causes the CPU 760 to test the contents of a status register, compare values such as those in cache, or perform another test and either continue sequential execution or jump to a target address based on the outcome. The call instruction causes the CPU to unconditionally jump to a new target address, but also saves the value of the program counter 765 to allow the CPU 760 to return to the program location. The return instruction causes the CPU 760 to retrieve the value of the program
10 counter that was saved by the last call instruction, and return program flow back to the retrieved instruction address.

[0324] Early CPUs were designed to execute only one instruction at a time. For these CPUs, it was not important whether the next instruction was sequential or a branch. More sophisticated CPUs operate on several instructions
15 at the same time, within different blocks or pipeline stages of the CPU. In other words, the CPU may be pipelined and include two or more pipelines stages. As instructions are fetched, they are introduced into one end of the pipeline. The instructions proceed through pipeline stages within the CPU until they complete execution.

20 **[0325]** In pipelined CPUs, it is often not known whether a branch instruction will alter program flow until it reaches a late stage in the pipeline. By this time, the CPU has already fetched other instructions and is executing them in earlier stages of the pipeline. If a branch causes a change in program flow, all of the instructions in the pipeline that followed the branch must be thrown out. In
25 addition, the instruction specified by the target address of the branch instruction must be fetched. Throwing out the intermediate instructions, and fetching the instruction at the target address creates processing delays.

[0326] To alleviate the delay, the branch prediction module 776 predicts the likely outcome of branch instructions, and then fetches subsequent
30 instructions according to the branch prediction. The branch prediction module 776 may include the branch history module 780 that makes predictions about conditional branch instruction outcomes.

[0327] For example only, the branch history module 780 may comprise an array of one or more bits indexed by a branch instruction address or other suitable scheme. Each bit stores one or more prior outcomes of the branch instruction. For example, the bit stores a 1 if the branch was taken the last time
5 it was executed and a 0 if the branch was not taken the last time it was executed. Additional bits may be used to implement more complex criteria such as A out of B or other criteria.

[0328] To make a prediction for a branch instruction, the branch prediction module 776 takes the address of the branch instruction and evaluates
10 the contents of the branch history module 780. For the single bit example, the prediction for a given execution of a branch instruction is the outcome of the previous execution of the branch instruction. After the branch instruction executes or is not executed, the branch history module 780 may be updated with the actual branch instruction outcome.

[0329] According to the present disclosure, power consumption is reduced by reducing precharging events and/or assertion of the same word line when accessing predicted branch instructions associated with the same word line. In other words when the CPU 760 fetches subsequent instructions in a pipeline processor, the CPU 760 may encounter one or more branch
15 instructions. When the branch instructions are encountered, the branch prediction module 776 uses prediction data associated with the branch instruction to predict whether the branch is likely to be taken or not. Based on the predicted outcome, the CPU loads the corresponding branch instruction and continues with other subsequent instructions. The multi-mode accessing control
20 module selectively uses either sequential or discrete read modes as described above.

[0330] Referring now to FIGs. 15A-15F, various exemplary implementations incorporating the teachings of the present disclosure are shown.

[0331] Referring now to FIG. 15A, the teachings of the disclosure can
30 be implemented in a processor 513 to access memory cells in a processor memory 517 of a hard disk drive (HDD) 500. The HDD 500 includes a hard disk

assembly (HDA) 501 and an HDD printed circuit board (PCB) 502. The HDA 501 may include a magnetic medium 503, such as one or more platters that store data, and a read/write device 504. The read/write device 504 may be arranged on an actuator arm 505 and may read and write data on the magnetic medium 503. Additionally, the HDA 501 includes a spindle motor 506 that rotates the magnetic medium 503 and a voice-coil motor (VCM) 507 that actuates the actuator arm 505. A preamplifier device 508 amplifies signals generated by the read/write device 504 during read operations and provides signals to the read/write device 504 during write operations.

[0332] The HDD PCB 502 includes a read/write channel module (hereinafter, "read channel") 509, a hard disk controller (HDC) module 510, a buffer 511, nonvolatile memory 512, the processor 513, and a spindle/VCM driver module 514. The read channel 509 processes data received from and transmitted to the preamplifier device 508. The HDC module 510 controls components of the HDA 501 and communicates with an external device (not shown) via an I/O interface 515. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 515 may include wireline and/or wireless communication links.

[0333] The HDC module 510 may receive data from the HDA 501, the read channel 509, the buffer 511, nonvolatile memory 512, the processor 513, the spindle/VCM driver module 514, and/or the I/O interface 515. The processor 513 may process the data, including encoding, decoding, filtering, and/or formatting. The processed data may be output to the HDA 501, the read channel 509, the buffer 511, nonvolatile memory 512, the processor 513, the spindle/VCM driver module 514, and/or the I/O interface 515.

[0334] The HDC module 510 may use the buffer 511 and/or nonvolatile memory 512 to store data related to the control and operation of the HDD 500. The buffer 511 may include DRAM, SDRAM, etc. The nonvolatile memory 512 may include flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, or multi-state memory, in which each memory cell has more than two states. The spindle/VCM driver module 514 controls the spindle motor 506 and the VCM 507. The HDD PCB

502 includes a power supply 516 that provides power to the components of the HDD 500.

[0335] Referring now to FIG. 15B, the teachings of the disclosure can be implemented in a processor 524 to access memory cells of a processor memory 537 of a DVD drive 518 or of a CD drive (not shown). The DVD drive 518 includes a DVD PCB 519 and a DVD assembly (DVDA) 520. The DVD PCB 519 includes a DVD control module 521, a buffer 522, nonvolatile memory 523, the processor 524, a spindle/FM (feed motor) driver module 525, an analog front-end module 526, a write strategy module 527, and a DSP module 528.

[0336] The DVD control module 521 controls components of the DVDA 520 and communicates with an external device (not shown) via an I/O interface 529. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 529 may include wireline and/or wireless communication links.

[0337] The DVD control module 521 may receive data from the buffer 522, nonvolatile memory 523, the processor 524, the spindle/FM driver module 525, the analog front-end module 526, the write strategy module 527, the DSP module 528, and/or the I/O interface 529. The processor 524 may process the data, including encoding, decoding, filtering, and/or formatting. The DSP module 528 performs signal processing, such as video and/or audio coding/decoding. The processed data may be output to the buffer 522, nonvolatile memory 523, the processor 524, the spindle/FM driver module 525, the analog front-end module 526, the write strategy module 527, the DSP module 528, and/or the I/O interface 529.

[0338] The DVD control module 521 may use the buffer 522 and/or nonvolatile memory 523 to store data related to the control and operation of the DVD drive 518. The buffer 522 may include DRAM, SDRAM, etc. The nonvolatile memory 523 may include flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, or multi-state memory, in which each memory cell has more than two states. The DVD PCB 519 includes a power supply 530 that provides power to the components of the DVD drive 518.

[0339] The DVDA 520 may include a preamplifier device 531, a laser driver 532, and an optical device 533, which may be an optical read/write (ORW) device or an optical read-only (OR) device. A spindle motor 534 rotates an optical storage medium 535, and a feed motor 536 actuates the optical device
5 533 relative to the optical storage medium 535.

[0340] When reading data from the optical storage medium 535, the laser driver provides a read power to the optical device 533. The optical device 533 detects data from the optical storage medium 535, and transmits the data to the preamplifier device 531. The analog front-end module 526 receives data
10 from the preamplifier device 531 and performs such functions as filtering and A/D conversion. To write to the optical storage medium 535, the write strategy module 527 transmits power level and timing data to the laser driver 532. The laser driver 532 controls the optical device 533 to write data to the optical storage medium 535.

[0341] Referring now to FIG. 15C, the teachings of the disclosure can be implemented in a HDTV control module 538 to access memory cells of an internal memory 544 of a high definition television (HDTV) 537. The HDTV 537 includes the HDTV control module 538, a display 539, a power supply 540, memory 541, a storage device 542, a network interface 543, and an external
15 interface 545. If the network interface 543 includes a wireless local area network interface, an antenna (not shown) may be included.
20

[0342] The HDTV 537 can receive input signals from the network interface 543 and/or the external interface 545, which can send and receive data via cable, broadband Internet, and/or satellite. The HDTV control module 538
25 may process the input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may be communicated to one or more of the display 539, memory 541, the storage device 542, the network interface 543, and the external interface 545.

[0343] Memory 541 may include random access memory (RAM)
30 and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 542 may include an optical storage drive, such as a DVD drive,

and/or a hard disk drive (HDD). The HDTV control module 538 communicates externally via the network interface 543 and/or the external interface 545. The power supply 540 provides power to the components of the HDTV 537.

5 **[0344]** Referring now to FIG. 15D, the teachings of the disclosure may be implemented in a vehicle control module 547 to access memory cells of an internal memory 551 of a vehicle 546. The vehicle 546 may include the vehicle control module 547, a power supply 548, memory 549, a storage device 550, and a network interface 552. If the network interface 552 includes a wireless local area network interface, an antenna (not shown) may be included. The
10 vehicle control module 547 may be a powertrain control system, a body control system, an entertainment control system, an anti-lock braking system (ABS), a navigation system, a telematics system, a lane departure system, an adaptive cruise control system, etc.

15 **[0345]** The vehicle control module 547 may communicate with one or more sensors 554 and generate one or more output signals 556. The sensors 554 may include temperature sensors, acceleration sensors, pressure sensors, rotational sensors, airflow sensors, etc. The output signals 556 may control engine operating parameters, transmission operating parameters, suspension parameters, etc.

20 **[0346]** The power supply 548 provides power to the components of the vehicle 546. The vehicle control module 547 may store data in memory 549 and/or the storage device 550. Memory 549 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two
25 states. The storage device 550 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The vehicle control module 547 may communicate externally using the network interface 552.

30 **[0347]** Referring now to FIG. 15E, the teachings of the disclosure can be implemented in a set top control module 580 to access memory cells of an internal memory 586 of a set top box 578. The set top box 578 includes the set top control module 580, a display 581, a power supply 582, memory 583, a storage device 584, and a network interface 585. If the network interface 585

includes a wireless local area network interface, an antenna (not shown) may be included.

[0348] The set top control module 580 may receive input signals from the network interface 585 and an external interface 587, which can send and receive data via cable, broadband Internet, and/or satellite. The set top control module 580 may process signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may include audio and/or video signals in standard and/or high definition formats. The output signals may be communicated to the network interface 585 and/or to the display 581. The display 581 may include a television, a projector, and/or a monitor.

[0349] The power supply 582 provides power to the components of the set top box 578. Memory 583 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 584 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD).

[0350] Referring now to FIG. 15F, the teachings of the disclosure can be implemented in a mobile device control module 590 to access memory cells of an internal memory 595 of a mobile device 589. The mobile device 589 may include the mobile device control module 590, a power supply 591, memory 592, a storage device 593, a network interface 594, and an external interface 599. If the network interface 594 includes a wireless local area network interface, an antenna (not shown) may be included.

[0351] The mobile device control module 590 may receive input signals from the network interface 594 and/or the external interface 599. The external interface 599 may include USB, infrared, and/or Ethernet. The input signals may include compressed audio and/or video, and may be compliant with the MP3 format. Additionally, the mobile device control module 590 may receive input from a user input 596 such as a keypad, touchpad, or individual buttons. The mobile device control module 590 may process input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals.

[0352] The mobile device control module 590 may output audio signals to an audio output 597 and video signals to a display 598. The audio output 597 may include a speaker and/or an output jack. The display 598 may present a graphical user interface, which may include menus, icons, etc. The power supply 591 provides power to the components of the mobile device 589. Memory 592 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 593 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The mobile device may include a personal digital assistant, a media player, a laptop computer, a gaming console, or other mobile computing device.

[0353] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification, and the following claims.

CLAIMS

What is claimed is:

1. A processor comprising:
a cache memory that comprises:

5 an array;
 word lines; and
 bit lines; and

 a control module that accesses cells of said array during access cycles to
access instructions stored in said cache memory,

10 wherein said control module selectively performs one of a first sequential
read and a first discrete read to access instructions in a first set of cells of said
array that are connected to a first word line and that selectively performs one of
a second sequential read and a second discrete read based on a first branch
instruction to access instructions in a second set of cells of said array that are
15 connected to a second word line, and

 wherein said second word line is different than said first word line.

2. The processor of claim 1 wherein said control module, when
performing said first sequential read, enables said first word line of said cache
20 memory to access a first cell in said first word line, disables said first word line,
and maintains said first word line in a disabled state when accessing a second
cell in said first word line.

3. The processor of claim 1 wherein said control module, when
25 performing said first sequential read, generates a first word line pulse associated
with said first word line for a first access cycle of said bit lines and selectively
refrains from generating a second word line pulse for said first word line for a
second access cycle of said bit lines.

30 4. The processor of claim 1 wherein said control module determines
bit line separation based on a number of said access cycles to be performed
along a first word line, and

wherein said control module precharges said bit lines connected to said first word line to provide said bit line separation when accessing said first set of cells.

5 5. The processor of claim 4 wherein said control module precharges a set of said bit lines connected to said first word line to provide said bit line separation when accessing a first set of cells of said array, and

 wherein said control module selectively refrains from precharging at least one of said set of said bit lines when accessing a second set of cells of said
10 array based on connections between said second set of cells and said first word line.

 6. The processor of claim 5 wherein said control module refrains from precharging said at least one of said set of said bit lines when said second set of
15 cells is connected to said first word line.

 7. The processor of claim 5 wherein said control module precharges said at least one of said set of bit lines when said second set of cells is connected to a word line other than said first word line.
20

 8. The processor of claim 1 wherein said control module adjusts precharge timing of said bit lines based on a rate of a clock signal.

 9. The processor of claim 1 wherein said control module delays
25 precharging of said bit lines when a rate of a clock signal is less than a predetermined rate.

 10. The processor of claim 1 wherein said control module selectively operates in a discrete read mode and a sequential read mode.
30

11. The processor of claim 1 wherein said control module generates a sequential read signal to enable a sequential read mode and generates a word line signal based on said sequential read signal.

5 12. The processor of claim 1 wherein said control module generates a sequential read signal to enable a sequential read mode and precharges said bit lines based on said sequential read signal.

10 13. The processor of claim 1 wherein said control module, when in a discrete mode, performs row address decoding, word line enablement, and bit line precharging for each access of each of said cells.

14. The processor of claim 1 wherein said control module, when accessing cells in a first mode, precharges said bit lines and performs row address decoding for each read cycle, and

wherein said control module, when accessing cells in a second mode, precharges said bit lines, performs row address decoding for a first read cycle, does not precharge said bit lines, and does not perform row address decoding for a second read cycle.

20

15. The processor of claim 1 further comprising a column decoder that selects cells of said array via a column select signal, wherein said control module generates a latch signal to latch bit information in said selected cells based on said column select signal.

25

16. The processor of claim 1 further comprising an amplification module that detects and amplifies bit information in said first and second set of cells.

30

17. The processor of claim 1 further comprising a row decoder, wherein said control module generates a word line signal via said row decoder to access said first set of cells.

18. The processor of claim 17 wherein said word line signal defines an extended period to increase said bit line separation.

5 19. The processor of claim 18 wherein said extended period increases bit line separation time and sets said bit line separation at a predetermined voltage.

10 20. The processor of claim 18 wherein said extended period is based on a predetermined number of read cycles.

15 21. The processor of claim 1 further comprising a column decoder, wherein said control module generates bit line signals via said column decoder to access said first set of cells.

20 22. The processor of claim 1 further comprising a sense-amplifier that has a plurality of common lines and that receives a precharge signal to precharge said common lines before latching bit information in said first and second set of cells.

25 23. The processor of claim 1 wherein said control module precharges said bit lines based on a precharge flag that indicates when a precharge has been performed.

30 24. The processor of claim 1 wherein said control module precharges said bit lines based on timing of a previous precharge of said bit lines.

 25. The processor of claim 1 wherein said control module, when performing said second sequential read, enables said second word line of said cache memory to access a cell in said second word line, disables said second word line, and maintains said second word line in a disabled state when accessing another cell in said second word line.

26. The processor of claim 1 wherein said control module performs in a discrete read mode based on said first branch instruction.

5 27. A method comprising:

providing a cache memory that comprises:

an array of cells;

word lines; and

bit lines;

10 accessing cells of said array during access cycles to access instructions stored in said cache memory;

performing one of a first discrete read and a first sequential read to access instructions in a first set of cells of said array that are connected to a first word line; and

15 selectively performing one of a second discrete read and a second sequential read based on a first branch instruction to access instructions in a second set of cells of said array that are connected to a second word line, wherein said second word line is different than said first word line.

20 28. The method of claim 27 further comprising, when performing said first sequential read, enabling said first word line of said cache memory to access a first cell in said first word line, disabling said first word line, and maintaining said first word line in a disabled state when accessing a second cell in said first word line.

25

29 The method of claim 27 further comprising, when performing said first sequential read, generates a first word line pulse associated with said first word line for a first access cycle of said bit lines and selectively refrains from generating a second word line pulse for said first word line for a second access
30 cycle of said bit lines.

30. The method of claim 27 further comprising:

determining bit line separation based on a number of said access cycles to be performed along a first word line; and

precharging said bit lines connected to said first word line to provide said bit line separation when accessing said first set of cells.

5

31. The method of claim 30 further comprising:

precharging a set of said bit lines connected to said first word line to provide said bit line separation when accessing a first set of cells of said array; and

10

selectively refraining from precharging at least one of said set of said bit lines when accessing a second set of cells of said array based on connections between said second set of cells and said first word line.

15

32. The method of claim 31 further comprising refraining from precharging said at least one of said set of said bit lines when said second set of cells is connected to said first word line.

20

33. The method of claim 31 further comprising precharging said at least one of said set of bit lines when said second set of cells is connected to a word line other than said first word line.

25

34. The method of claim 27 further comprising adjusting precharge timing of said bit lines based on a rate of a clock signal.

35. The method of claim 27 further comprising delaying precharging of said bit lines when a rate of a clock signal is less than a predetermined rate.

30

36. The method of claim 27 further comprising selectively operating in a discrete read mode and a sequential read mode.

37. The method of claim 27 further comprising generating a sequential read signal to enable a sequential read mode and generating a word line signal based on said sequential read signal.

5 38. The method of claim 27 further comprising generating a sequential read signal to enable a sequential read mode and precharging said bit lines based on said sequential read signal.

10 39. The method of claim 27 further comprising, when in a discrete mode, performing row address decoding, word line enablement, and bit line precharging for each access of each of said cells.

40. The method of claim 27 further comprising:
when accessing cells in a first mode, precharging said bit lines and
15 performing row address decoding for each read cycle; and
when accessing cells in a second mode, precharging said bit lines, performing row address decoding for a first read cycle, refraining from precharging said bit lines, and refraining from performing row address decoding for a second read cycle.

20

41. The method of claim 27 further comprising:
selecting cells of said array via a column select signal, and
generating a latch signal to latch bit information in said selected cells
based on said column select signal.

25

42. The method of claim 27 further comprising detecting and amplifying bit information in said first and second set of cells.

43. The method of claim 27 further comprising generating a word line
30 signal via said row decoder to access said first set of cells.

44. The method of claim 43 wherein said word line signal defines an extended period to increase said bit line separation.

45. The method of claim 44 wherein said extended period increases bit line separation time and sets said bit line separation at a predetermined voltage.

46. The method of claim 44 wherein said extended period is based on a predetermined number of read cycles.

47. The method of claim 27 further comprising generating bit line signals via said column decoder to access said first set of cells.

48. The method of claim 27 further comprising receiving a precharge signal to precharge common lines of a sense-amplifier before latching bit information in said first and second set of cells.

49. The method of claim 27 further comprising precharging said bit lines based on a precharge flag that indicates when a precharge has been performed.

50. The method of claim 27 further comprising precharging said bit lines based on timing of a previous precharge of said bit lines.

51. The method of claim 27 further comprising, when performing said second sequential read, enabling said second word line of said cache memory to access a cell in said second word line, disabling said second word line, and maintaining said second word line in a disabled state when accessing another cell in said second word line.

52. The method of claim 27 further comprising performing in a discrete read mode based on said first branch instruction.

53. The processor of claim 1 wherein said processor pre-fetches and decodes subsequent instructions in a pipeline and further comprising a branch prediction module that predicts whether one of said subsequent instructions that is a second branch instruction is likely to be taken.

5

54. The processor of claim 53 wherein said branch prediction module selectively performs one of a discrete read and a sequential read on said branch instruction based on said prediction and on whether said branch instruction involves multiple reads along a same word line.

10

55. The processor of claim 54 wherein said branch prediction module includes a branch history module that outputs branch prediction data based on an address of said second branch instruction and wherein said branch prediction module bases said prediction on said branch prediction data.

15

56. The method of claim 27 further comprising:
pre-fetching and decoding subsequent instructions in a pipeline;
predicting whether one of said subsequent instructions that is a second branch instruction is likely to be taken.

20

57. The method of claim 56 further comprising:
selectively performing one of a discrete read and a sequential read on said branch instruction based on said prediction and on whether said branch instruction involves multiple reads along a same word line.

25

58. The method of claim 57 further comprising:
generating branch prediction data based on an address of said second branch instruction; and
basing said prediction on said branch prediction data.

30

AMENDED CLAIMS
received by the International Bureau on 10 February 2009 (10.02.2009)

What is claimed is:

1. A processor comprising:

a cache memory that comprises:

5 an array;
 word lines; and
 bit lines; and

a control module that accesses cells of said array during access cycles to access instructions stored in said cache memory,

10 wherein said control module selectively performs one of a first sequential read and a first discrete read to access instructions in a first set of cells of said array that are connected to a first word line and that selectively performs one of a second sequential read and a second discrete read based on a first branch instruction to access instructions in a second set of cells of said array that are
15 connected to a second word line,

 wherein said second word line is different than said first word line,

 wherein said control module pre-fetches and decodes subsequent instructions in a pipeline and further comprising a branch prediction module that predicts whether one of said subsequent instructions that is a second branch
20 instruction is likely to be taken, and

 wherein said branch prediction module selectively performs one of said second sequential read and said second discrete read on said second branch instruction based on said prediction and based on whether said second branch instruction involves multiple reads along a same word line.

25

2. The processor of claim 1 wherein said control module, when performing said first sequential read, enables said first word line of said cache memory to access a first cell in said first word line, disables said first word line, and maintains said first word line in a disabled state when accessing a second
30 cell in said first word line.

AMENDED SHEET (ARTICLE 19)

3. The processor of claim 1 wherein said control module, when performing said first sequential read, generates a first word line pulse associated with said first word line for a first access cycle of said bit lines and selectively refrains from generating a second word line pulse for said first word line for a
5 second access cycle of said bit lines.

4. The processor of claim 1 wherein said control module determines bit line separation based on a number of said access cycles to be performed along a first word line, and
10 wherein said control module precharges said bit lines connected to said first word line to provide said bit line separation when accessing said first set of cells.

5. The processor of claim 4 wherein said control module precharges a
15 set of said bit lines connected to said first word line to provide said bit line separation when accessing a first set of cells of said array, and
wherein said control module selectively refrains from precharging at least one of said set of said bit lines when accessing a second set of cells of said array based on connections between said second set of cells and said first word
20 line.

6. The processor of claim 5 wherein said control module refrains from precharging said at least one of said set of said bit lines when said second set of cells is connected to said first word line.
25

7. The processor of claim 5 wherein said control module precharges said at least one of said set of bit lines when said second set of cells is connected to a word line other than said first word line.

8. The processor of claim 1 wherein said control module adjusts precharge timing of said bit lines based on a rate of a clock signal.
30

AMENDED SHEET (ARTICLE 19)

9. The processor of claim 1 wherein said control module delays precharging of said bit lines when a rate of a clock signal is less than a predetermined rate.

5 10. The processor of claim 1 wherein said control module selectively operates in a discrete read mode and a sequential read mode.

11. The processor of claim 1 wherein said control module generates a sequential read signal to enable a sequential read mode and generates a word
10 line signal based on said sequential read signal.

12. The processor of claim 1 wherein said control module generates a sequential read signal to enable a sequential read mode and precharges said bit
15 lines based on said sequential read signal.

13. The processor of claim 1 wherein said control module, when in a discrete mode, performs row address decoding, word line enablement, and bit
line precharging for each access of each of said cells.

20 14. The processor of claim 1 wherein said control module, when accessing cells in a first mode, precharges said bit lines and performs row address decoding for each read cycle, and

wherein said control module, when accessing cells in a second mode, precharges said bit lines, performs row address decoding for a first read cycle,
25 does not precharge said bit lines, and does not perform row address decoding for a second read cycle.

15. The processor of claim 1 further comprising a column decoder that selects cells of said array via a column select signal, wherein said control
30 module generates a latch signal to latch bit information in said selected cells based on said column select signal.

AMENDED SHEET (ARTICLE 19)

16. The processor of claim 1 further comprising an amplification module that detects and amplifies bit information in said first and second set of cells.

5 17. The processor of claim 1 further comprising a row decoder, wherein said control module generates a word line signal via said row decoder to access said first set of cells.

10 18. The processor of claim 17 wherein said word line signal defines an extended period to increase said bit line separation.

15 19. The processor of claim 18 wherein said extended period increases bit line separation time and sets said bit line separation at a predetermined voltage.

20 20. The processor of claim 18 wherein said extended period is based on a predetermined number of read cycles.

25 21. The processor of claim 1 further comprising a column decoder, wherein said control module generates bit line signals via said column decoder to access said first set of cells.

30 22. The processor of claim 1 further comprising a sense-amplifier that has a plurality of common lines and that receives a precharge signal to precharge said common lines before latching bit information in said first and second set of cells.

35 23. The processor of claim 1 wherein said control module precharges said bit lines based on a precharge flag that indicates when a precharge has been performed.

AMENDED SHEET (ARTICLE 19)

24. The processor of claim 1 wherein said control module precharges said bit lines based on timing of a previous precharge of said bit lines.

25. The processor of claim 1 wherein said control module, when
5 performing said second sequential read, enables said second word line of said cache memory to access a cell in said second word line, disables said second word line, and maintains said second word line in a disabled state when accessing another cell in said second word line.

10 26. The processor of claim 1 wherein said control module performs in a discrete read mode based on said first branch instruction.

27. A method comprising:

providing a cache memory that comprises:

an array of cells;

15 word lines; and

bit lines;

accessing cells of said array during access cycles to access instructions stored in said cache memory;

performing one of a first discrete read and a first sequential read to
20 access instructions in a first set of cells of said array that are connected to a first word line;

selectively performing one of a second discrete read and a second sequential read based on a first branch instruction to access instructions in a second set of cells of said array that are connected to a second word line;

25 pre-fetching and decoding subsequent instructions in a pipeline;

predicting whether one of said subsequent instructions that is a second branch instruction is likely to be taken; and

selectively performing one of said second sequential read and said second discrete read on said second branch instruction based on said prediction
30 and based on whether said second branch instruction involves multiple reads along a same word line,

wherein said second word line is different than said first word line.

AMENDED SHEET (ARTICLE 19)

28. The method of claim 27 further comprising, when performing said first sequential read, enabling said first word line of said cache memory to access a first cell in said first word line, disabling said first word line, and
5 maintaining said first word line in a disabled state when accessing a second cell in said first word line.

29 The method of claim 27 further comprising, when performing said first sequential read, generates a first word line pulse associated with said first
10 word line for a first access cycle of said bit lines and selectively refrains from generating a second word line pulse for said first word line for a second access cycle of said bit lines.

30. The method of claim 27 further comprising:
15 determining bit line separation based on a number of said access cycles to be performed along a first word line; and
precharging said bit lines connected to said first word line to provide said bit line separation when accessing said first set of cells.

20 31. The method of claim 30 further comprising:
precharging a set of said bit lines connected to said first word line to provide said bit line separation when accessing a first set of cells of said array; and
selectively refraining from precharging at least one of said set of said bit
25 lines when accessing a second set of cells of said array based on connections between said second set of cells and said first word line.

32. The method of claim 31 further comprising refraining from precharging said at least one of said set of said bit lines when said second set of
30 cells is connected to said first word line.

AMENDED SHEET (ARTICLE 19)

33. The method of claim 31 further comprising precharging said at least one of said set of bit lines when said second set of cells is connected to a word line other than said first word line.

5 34. The method of claim 27 further comprising adjusting precharge timing of said bit lines based on a rate of a clock signal.

35. The method of claim 27 further comprising delaying precharging of said bit lines when a rate of a clock signal is less than a predetermined rate.

10

36. The method of claim 27 further comprising selectively operating in a discrete read mode and a sequential read mode.

37. The method of claim 27 further comprising generating a sequential
15 read signal to enable a sequential read mode and generating a word line signal based on said sequential read signal.

38. The method of claim 27 further comprising generating a sequential
read signal to enable a sequential read mode and precharging said bit lines
20 based on said sequential read signal.

39. The method of claim 27 further comprising, when in a discrete mode, performing row address decoding, word line enablement, and bit line precharging for each access of each of said cells.

25

40. The method of claim 27 further comprising:
when accessing cells in a first mode, precharging said bit lines and performing row address decoding for each read cycle; and
when accessing cells in a second mode, precharging said bit lines,
30 performing row address decoding for a first read cycle, refraining from precharging said bit lines, and refraining from performing row address decoding for a second read cycle.

AMENDED SHEET (ARTICLE 19)

41. The method of claim 27 further comprising:
selecting cells of said array via a column select signal, and
generating a latch signal to latch bit information in said selected cells
5 based on said column select signal.

42. The method of claim 27 further comprising detecting and amplifying
bit information in said first and second set of cells.

10 43. The method of claim 27 further comprising generating a word line
signal via said row decoder to access said first set of cells.

44. The method of claim 43 wherein said word line signal defines an
extended period to increase said bit line separation.
15

45. The method of claim 44 wherein said extended period increases bit
line separation time and sets said bit line separation at a predetermined voltage.

46. The method of claim 44 wherein said extended period is based on
20 a predetermined number of read cycles.

47. The method of claim 27 further comprising generating bit line
signals via said column decoder to access said first set of cells.

25 48. The method of claim 27 further comprising receiving a precharge
signal to precharge common lines of a sense-amplifier before latching bit
information in said first and second set of cells.

49. The method of claim 27 further comprising precharging said bit
30 lines based on a precharge flag that indicates when a precharge has been
performed.

AMENDED SHEET (ARTICLE 19)

50. The method of claim 27 further comprising precharging said bit lines based on timing of a previous precharge of said bit lines.

51. The method of claim 27 further comprising, when performing said
5 second sequential read, enabling said second word line of said cache memory to access a cell in said second word line, disabling said second word line, and maintaining said second word line in a disabled state when accessing another cell in said second word line.

10 52. The method of claim 27 further comprising performing in a discrete read mode based on said first branch instruction.

53-54. (Cancelled).

15 55. The processor of claim 54 wherein said branch prediction module includes a branch history module that outputs branch prediction data based on an address of said second branch instruction and wherein said branch prediction module bases said prediction on said branch prediction data.

20 56-57. (Cancelled).

58. The method of claim 57 further comprising:
generating branch prediction data based on an address of said
second branch instruction; and
25 basing said prediction on said branch prediction data.

59. The processor of claim 1 wherein said branch prediction module predicts whether one of said subsequent instructions that is a second branch instruction is likely to be taken based on execution of said first branch instruction.
30

60. The processor of claim 1 wherein said branch prediction module predicts outcome of said second branch instruction based on execution of said first branch instruction, and

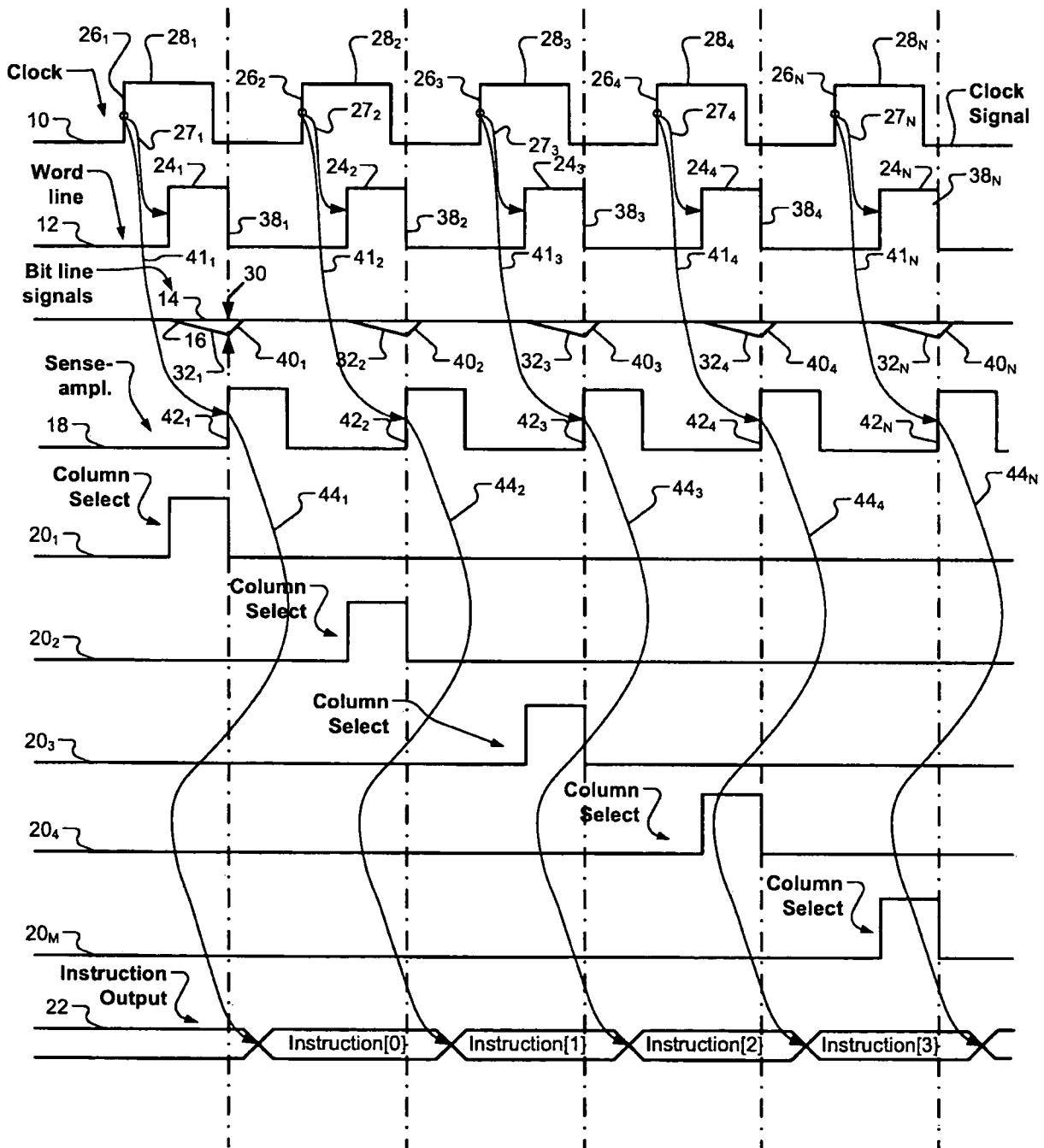
5 wherein said control module fetches instructions subsequent to said second branch instruction based on said predicted outcome of said second branch instruction by performing a sequential read.

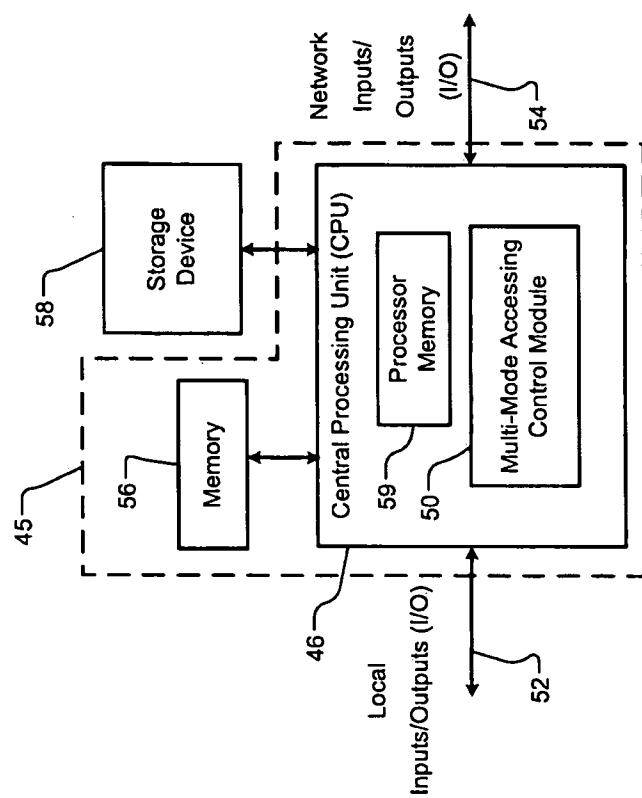
61. The processor of claim 2 wherein said control module performs a second precharge of said bit lines a first period after a first precharge of said bit
10 lines and before enabling said first word line,

wherein said control module performs a third precharge of said bit lines a second period after said second precharge, after disabling said first word line, and before enabling said second word line, and

wherein said second period is greater than said first period.

15

**FIG. 1**

**FIG. 2**

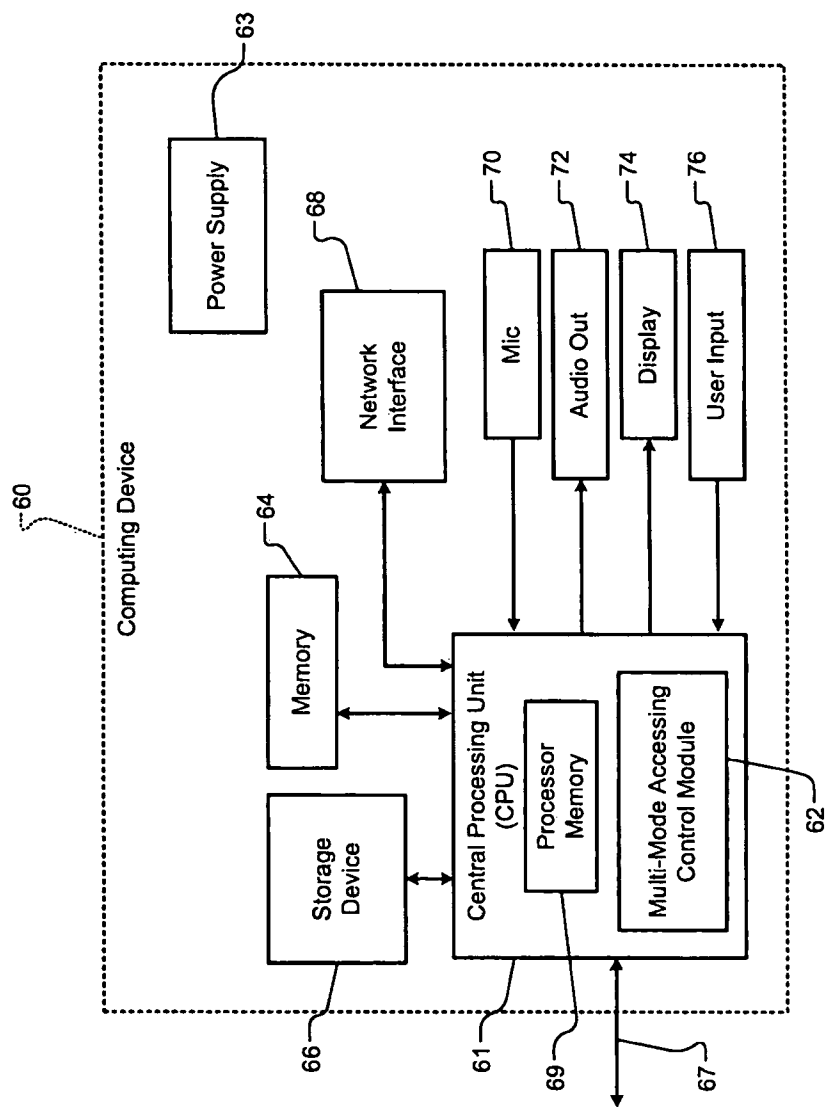


FIG. 3

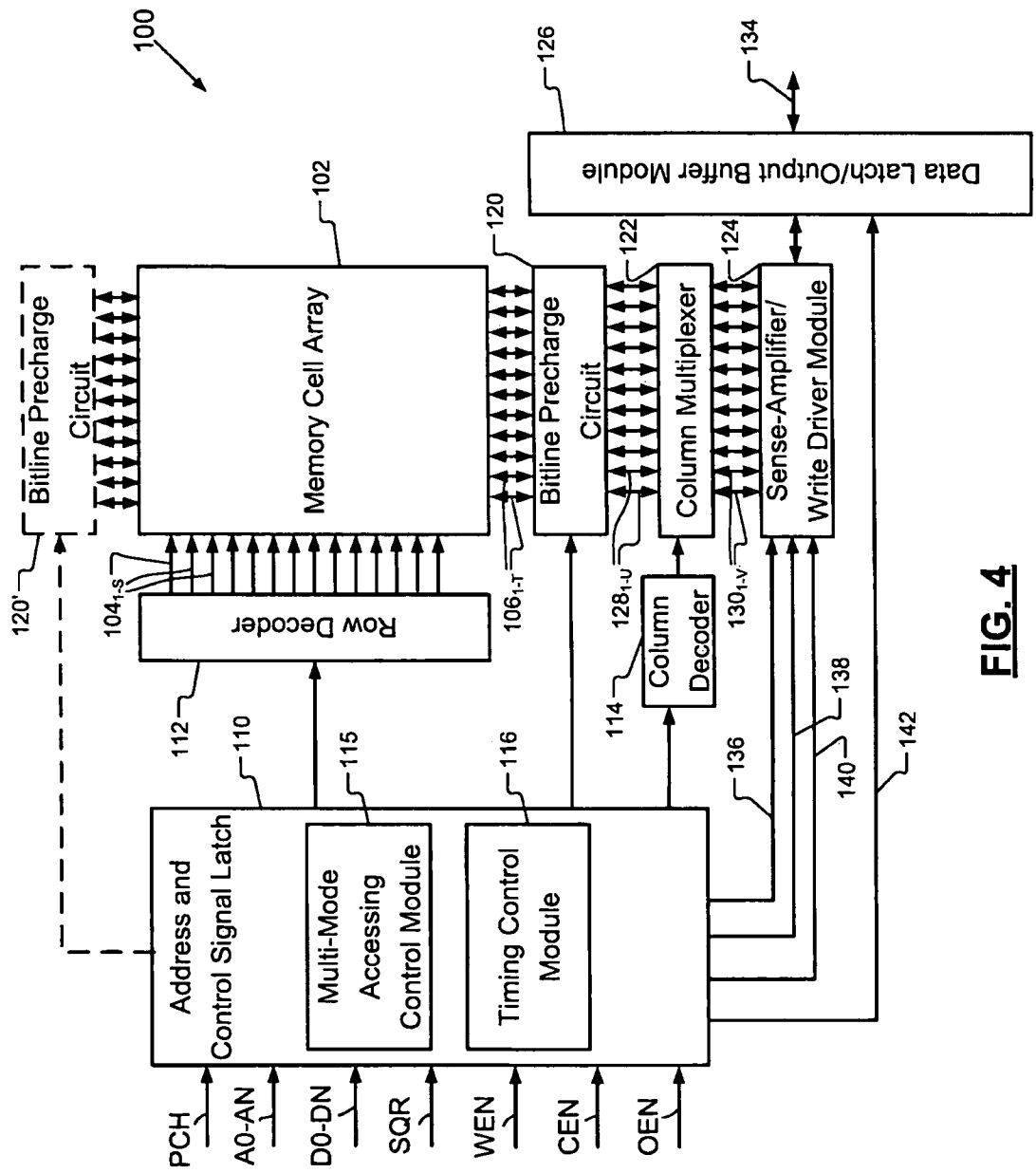
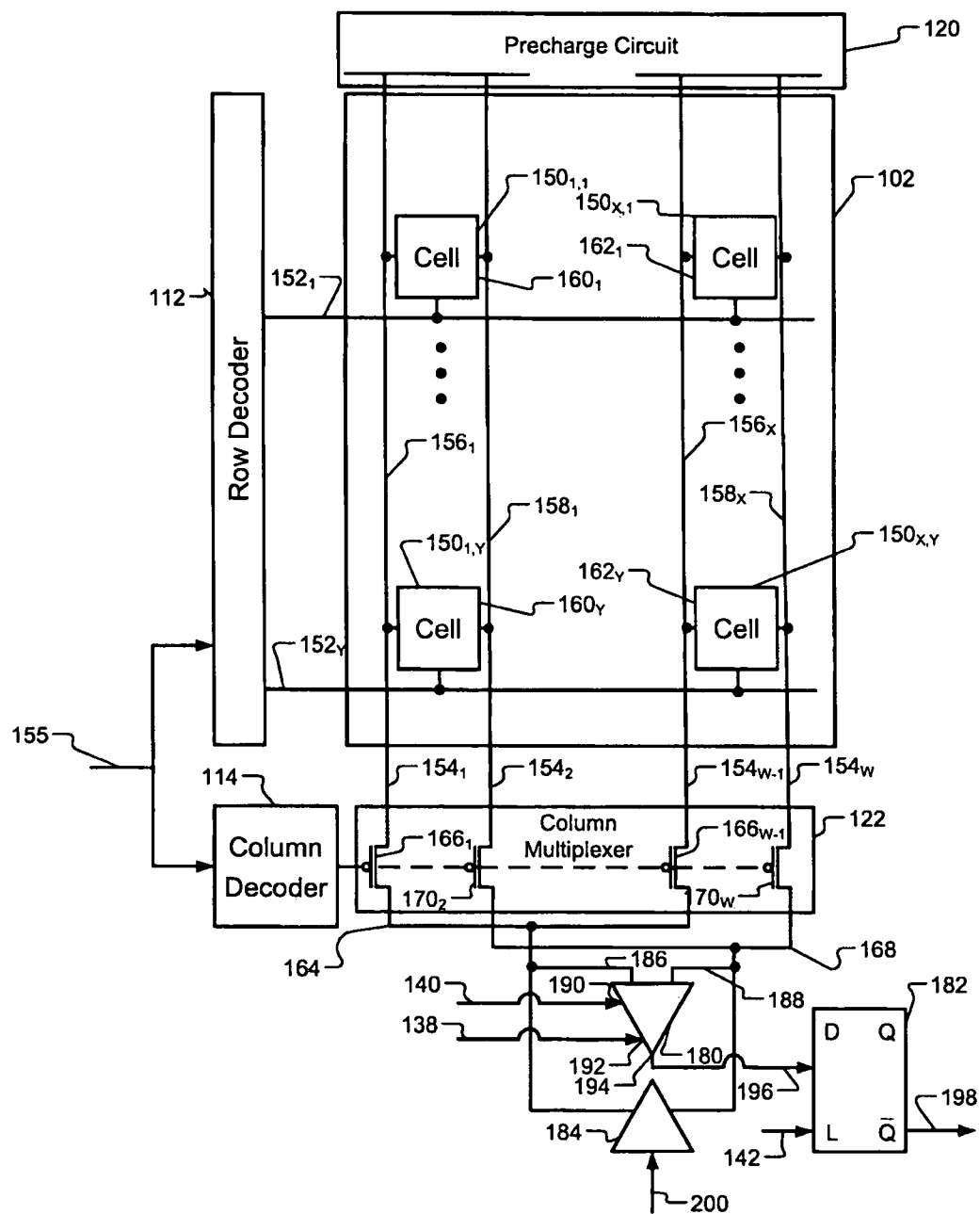
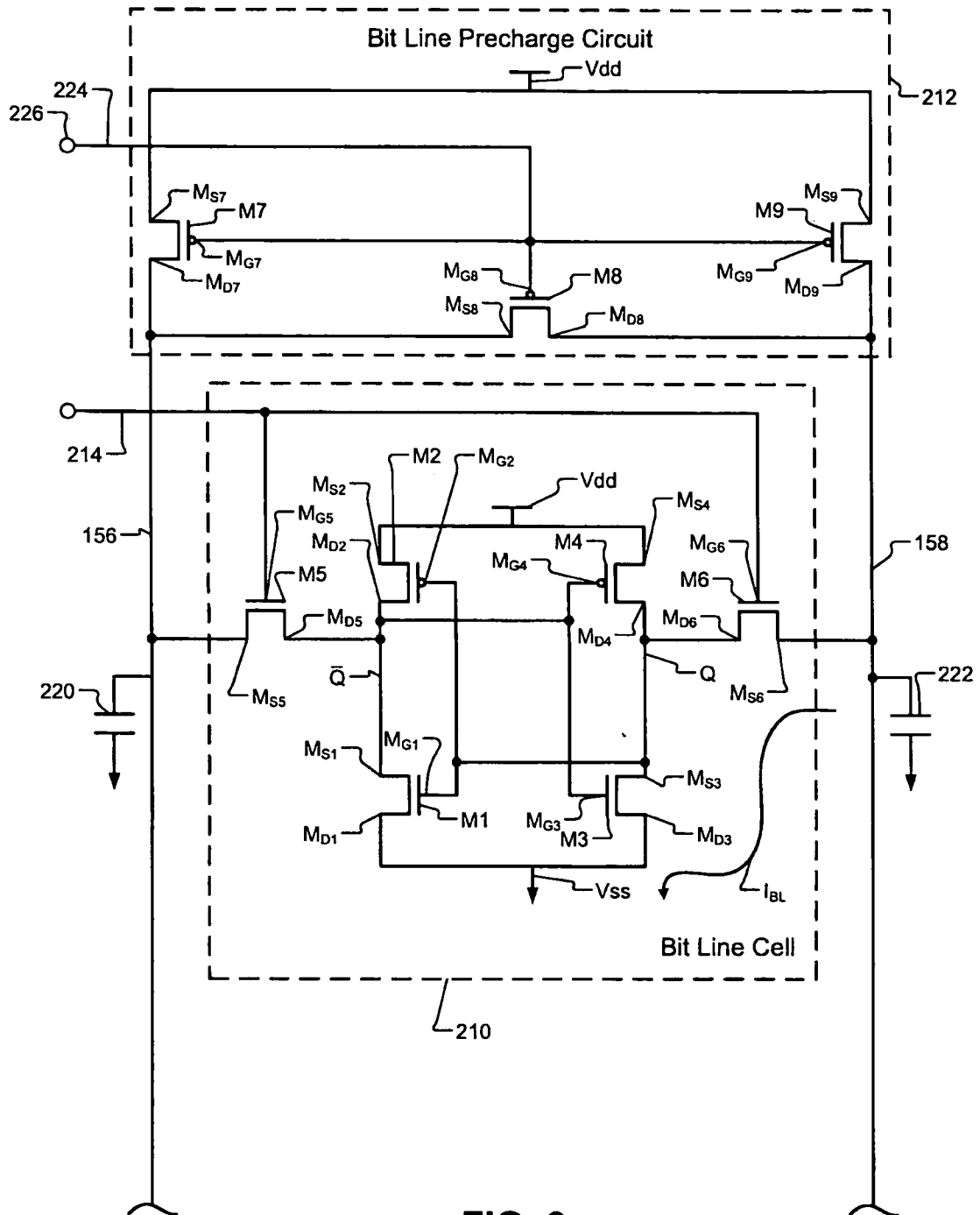


FIG. 4

**FIG. 5**

**FIG. 6**

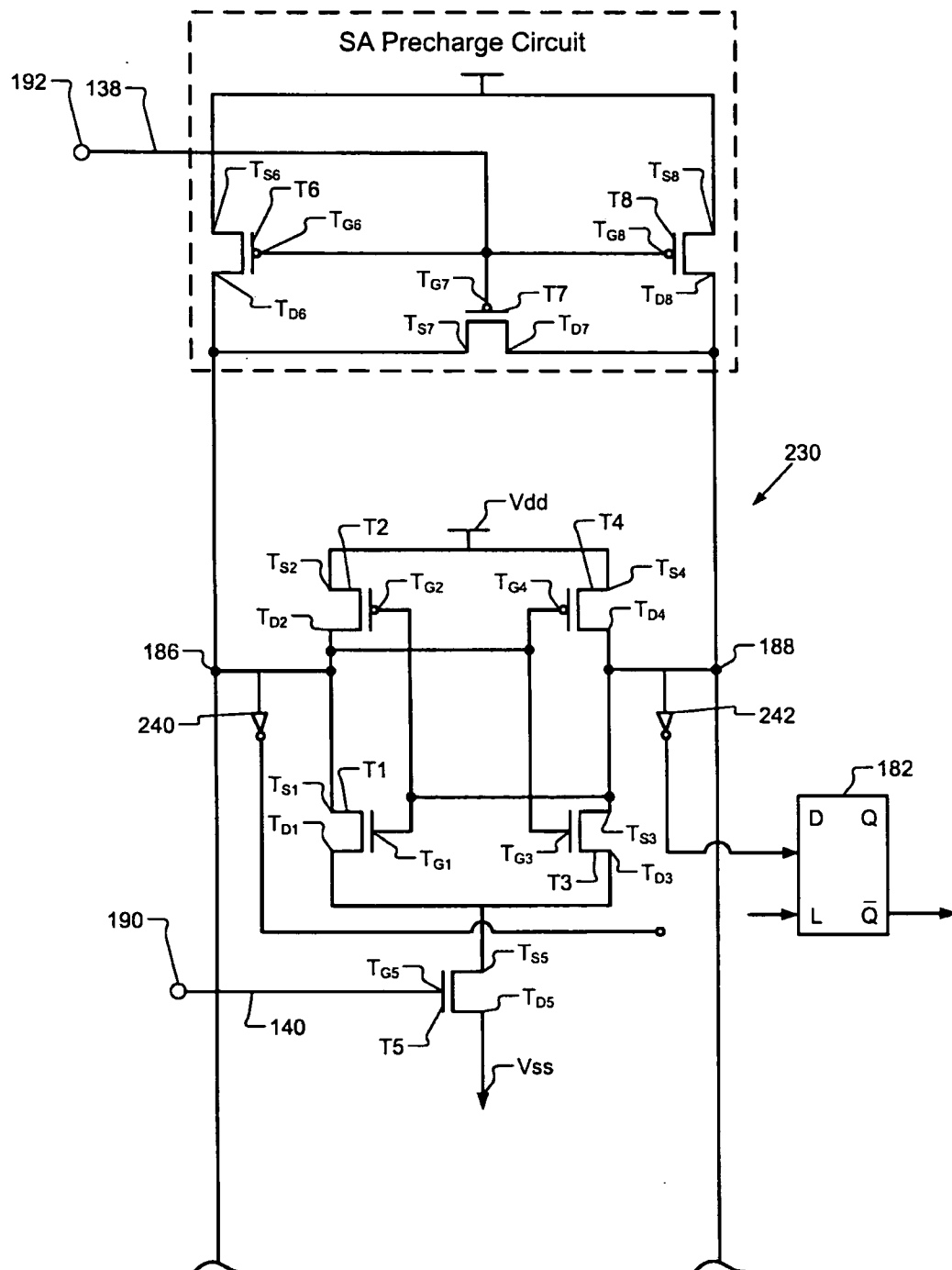
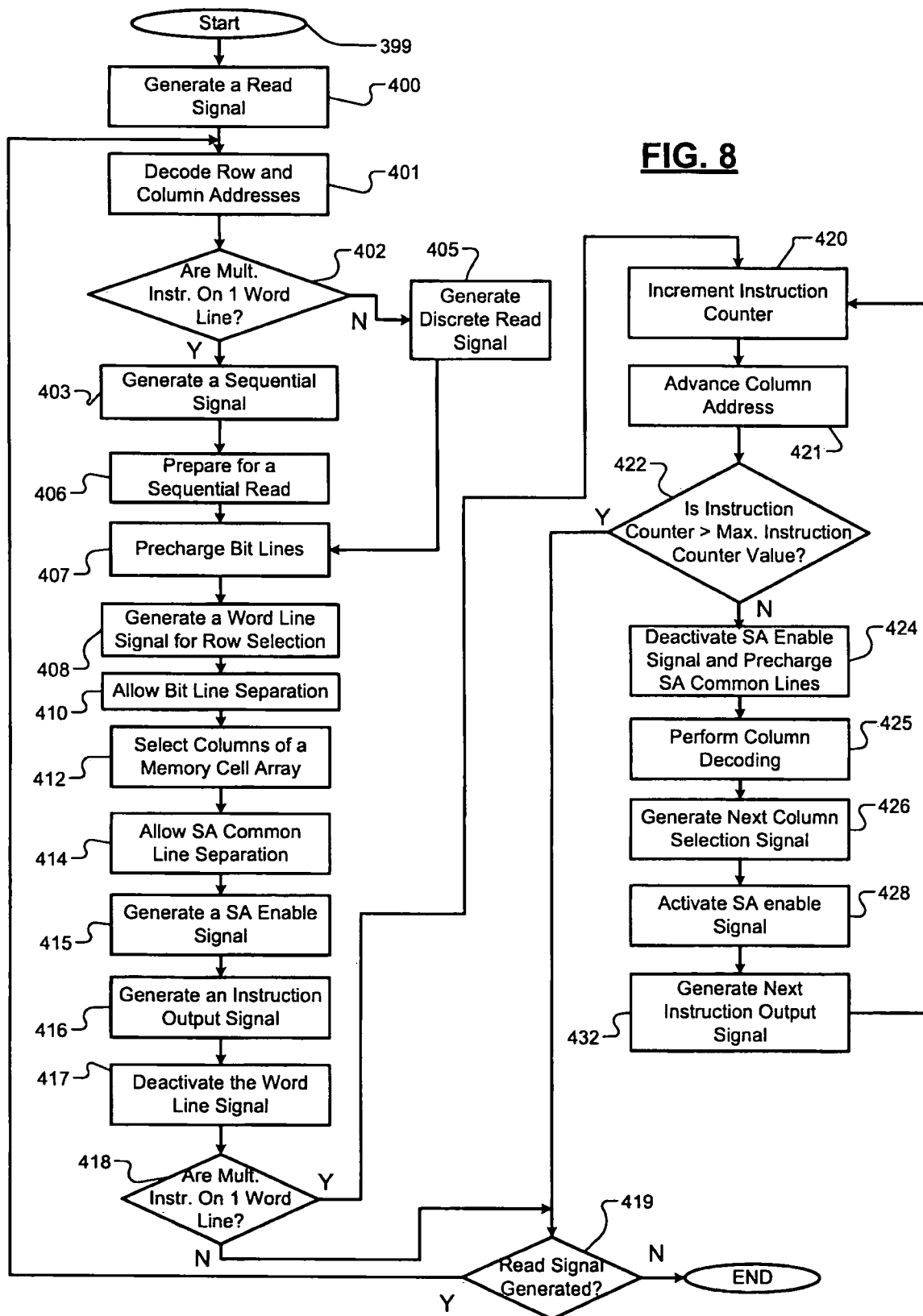
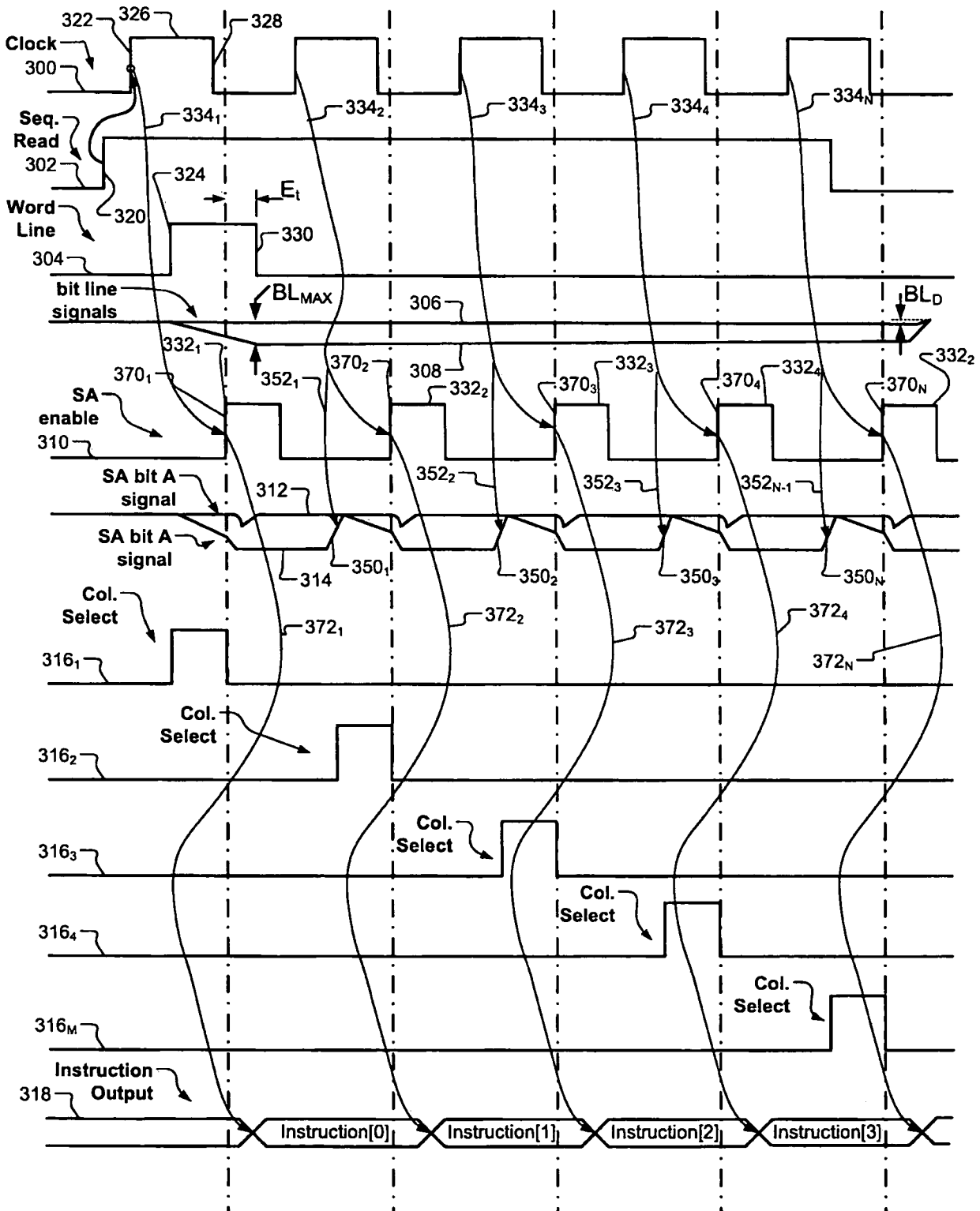
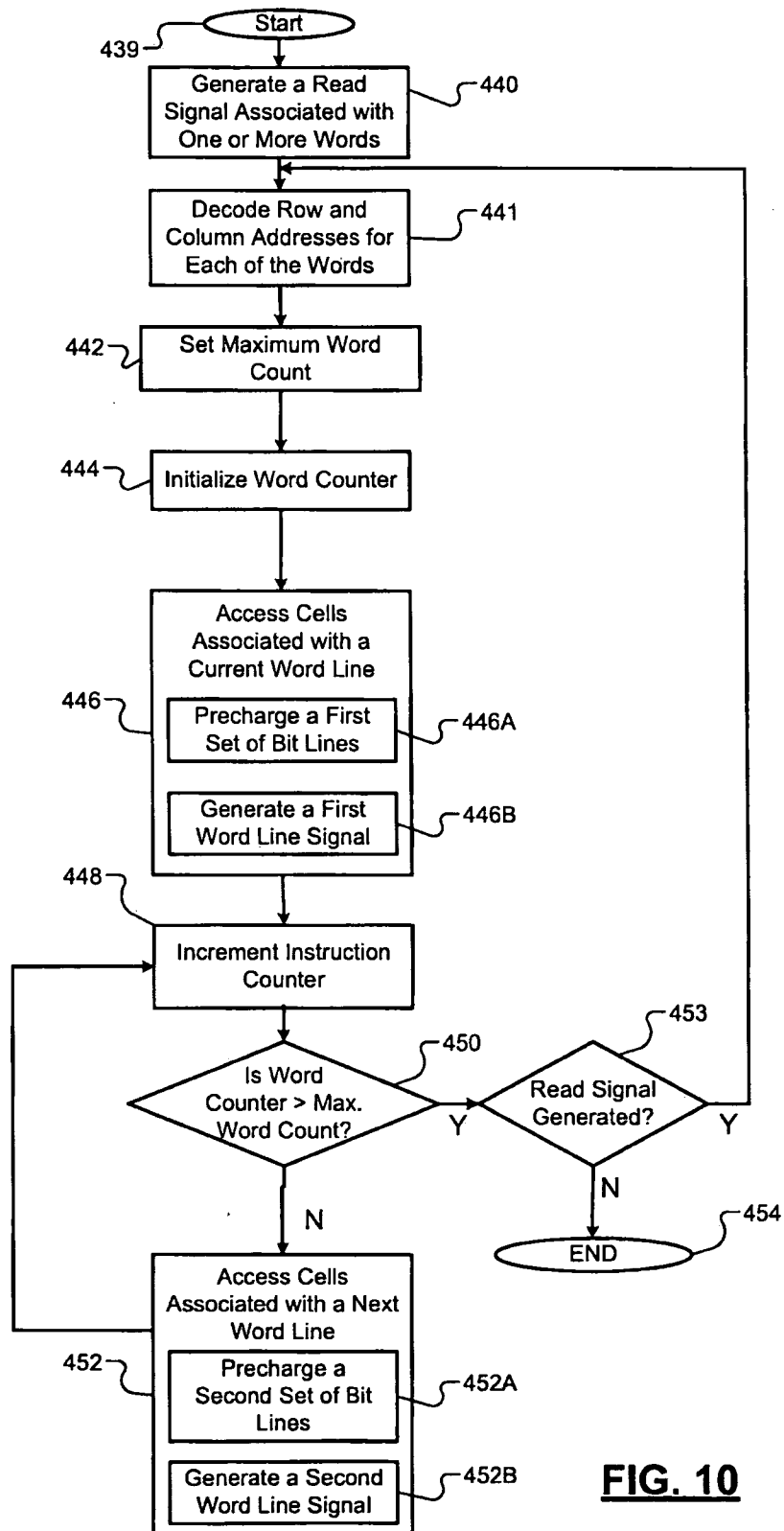
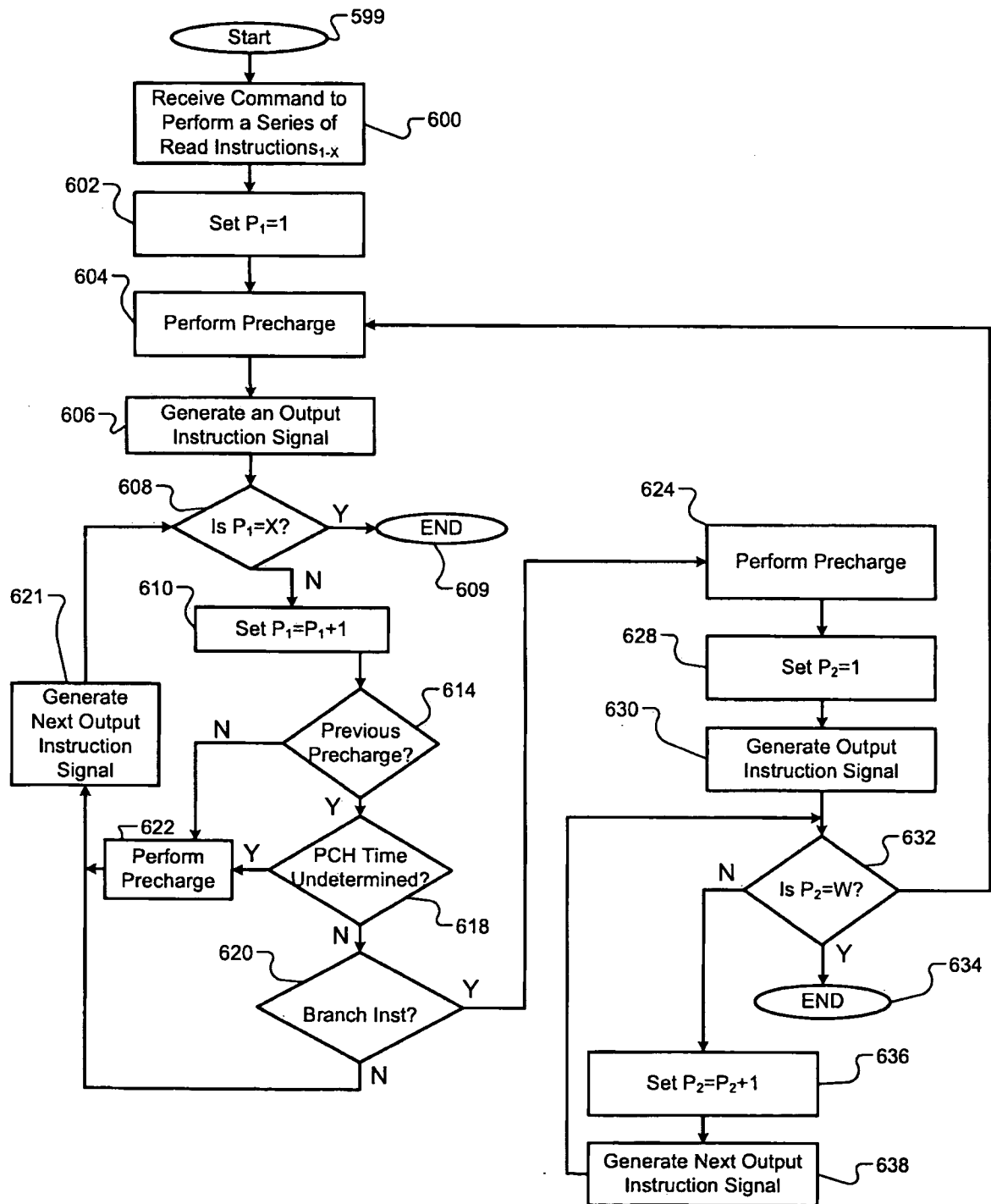


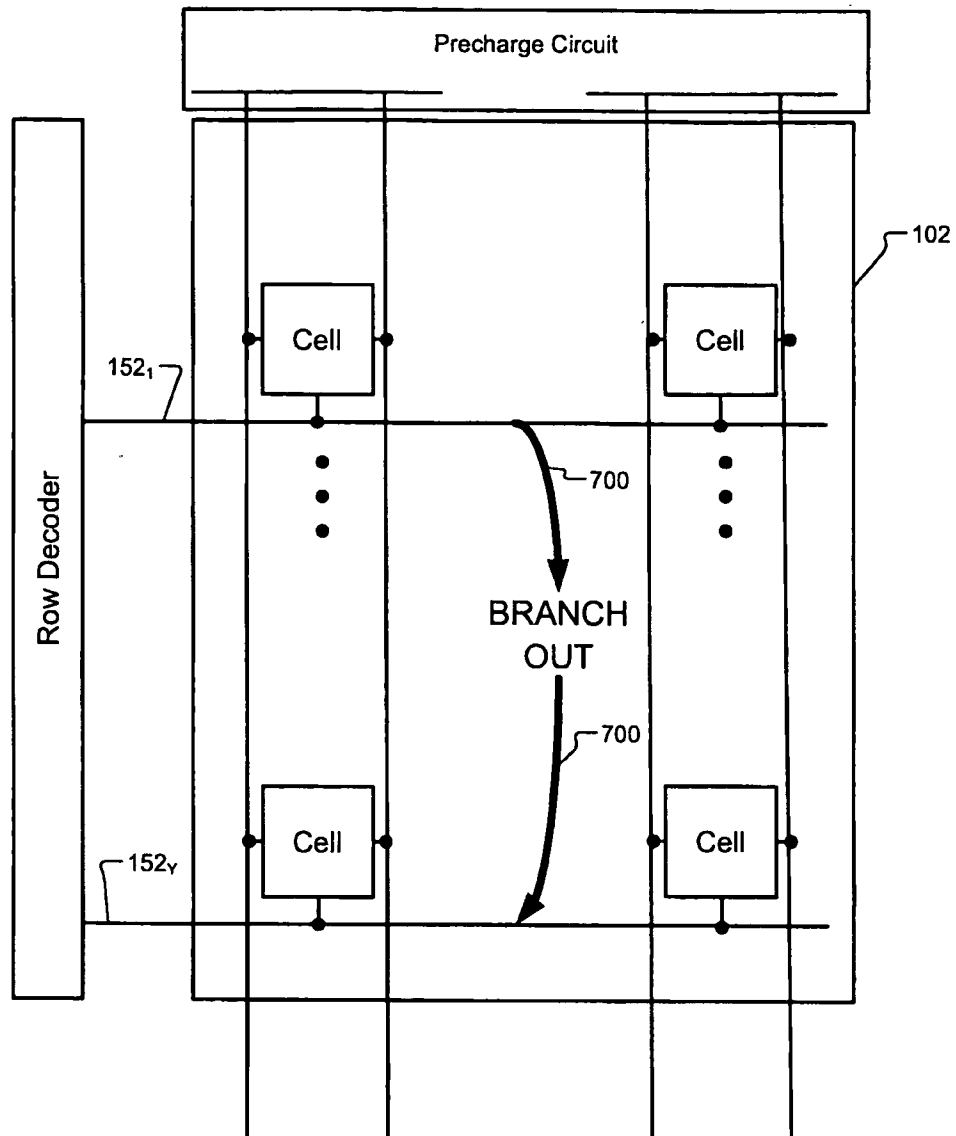
FIG. 7



**FIG. 9**

**FIG. 10**

**FIG. 11**

**FIG. 12**

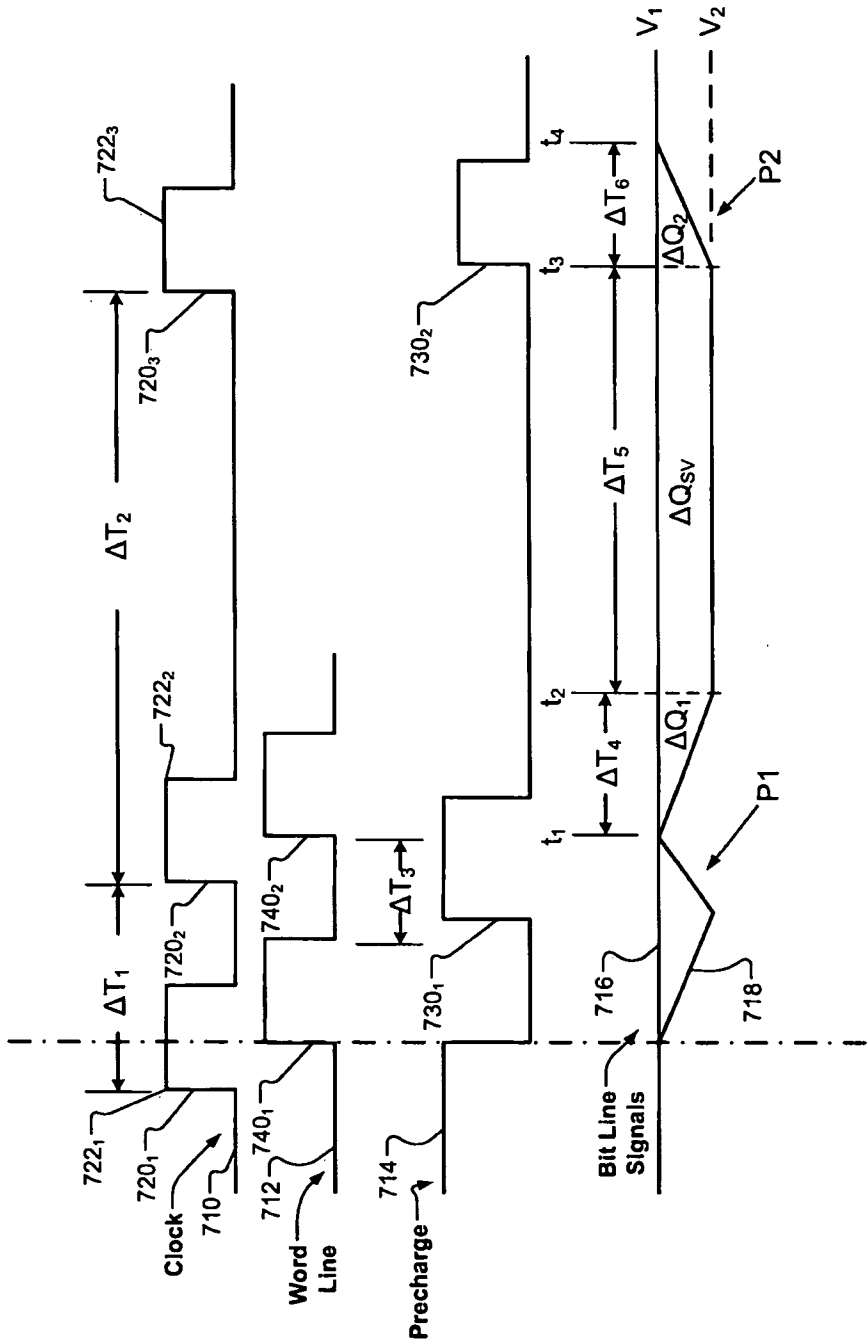


FIG. 13

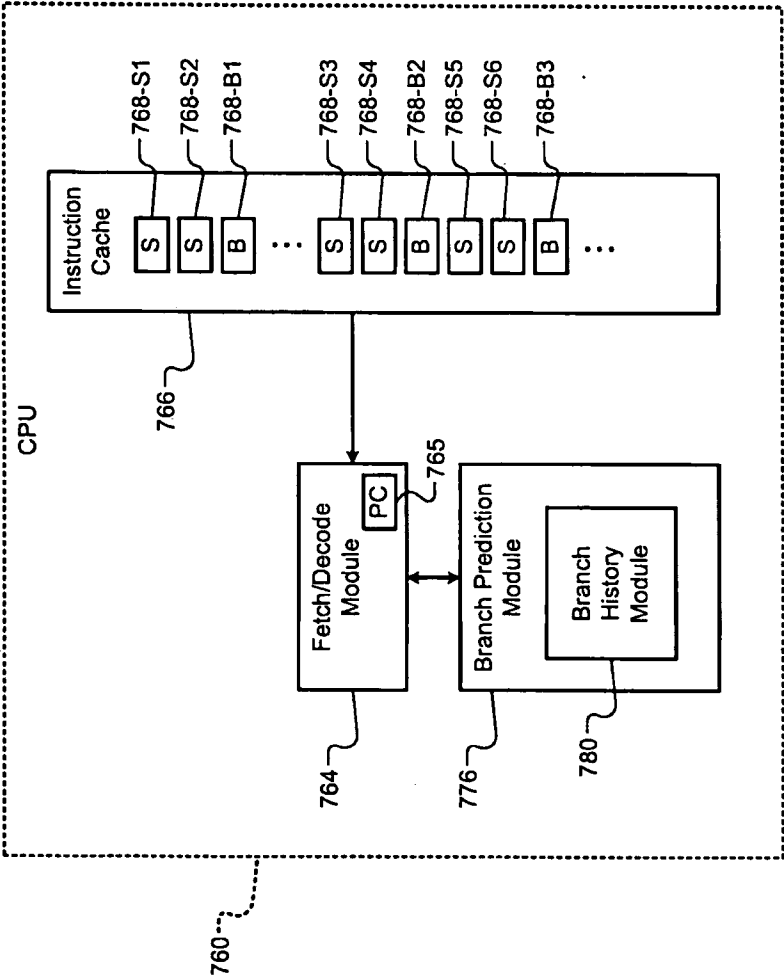


FIG. 14

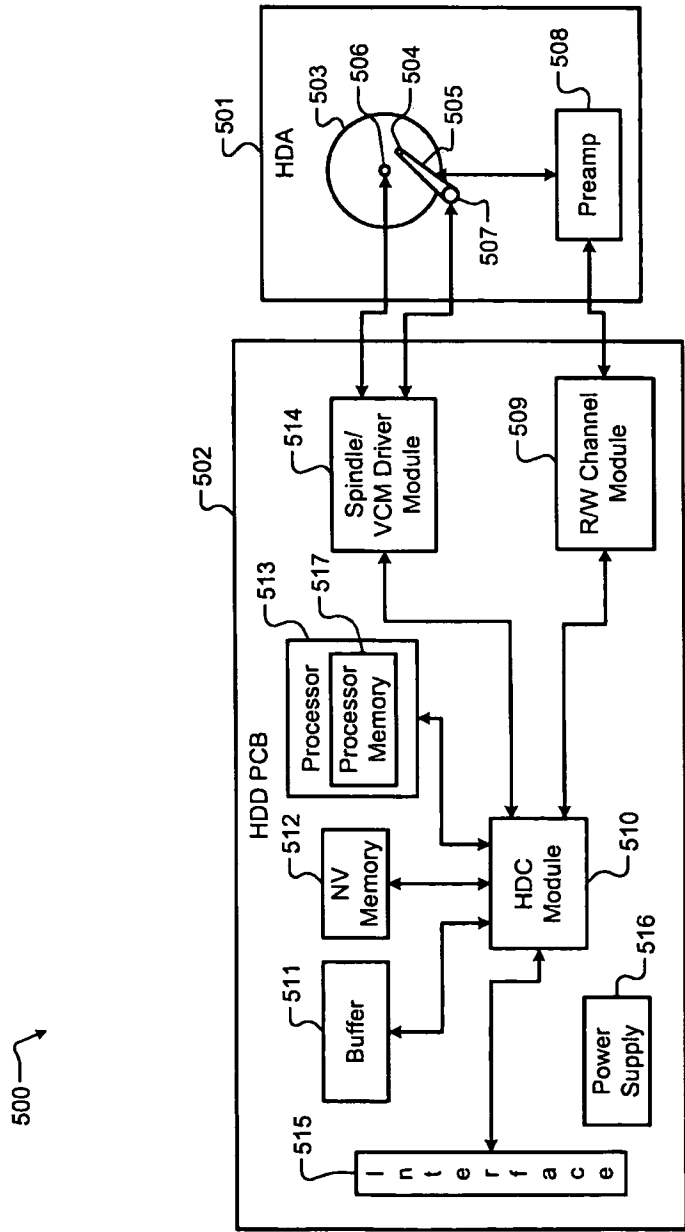


FIG. 15A

518 →

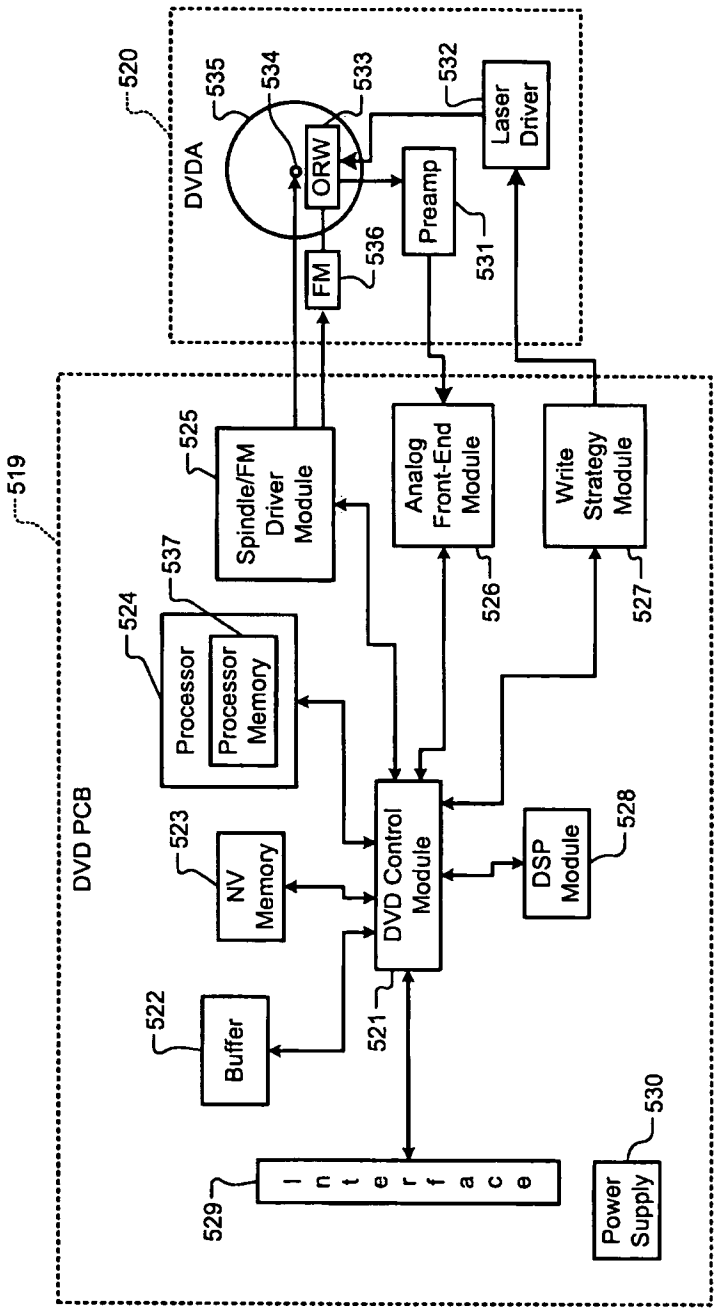


FIG. 15B

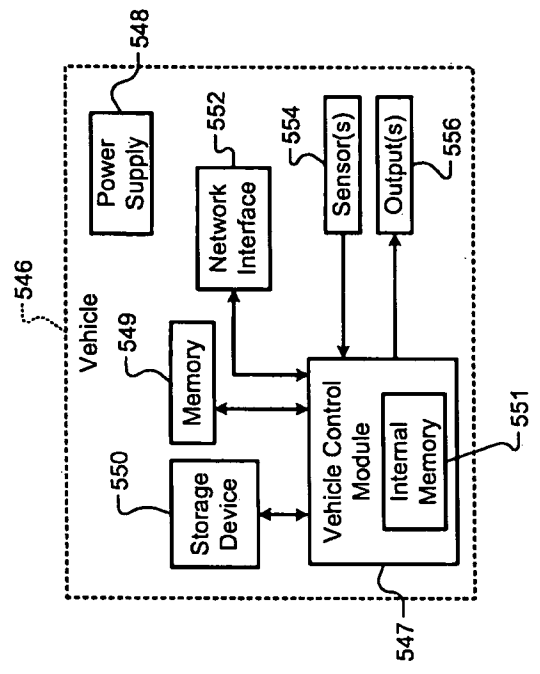


FIG. 15D

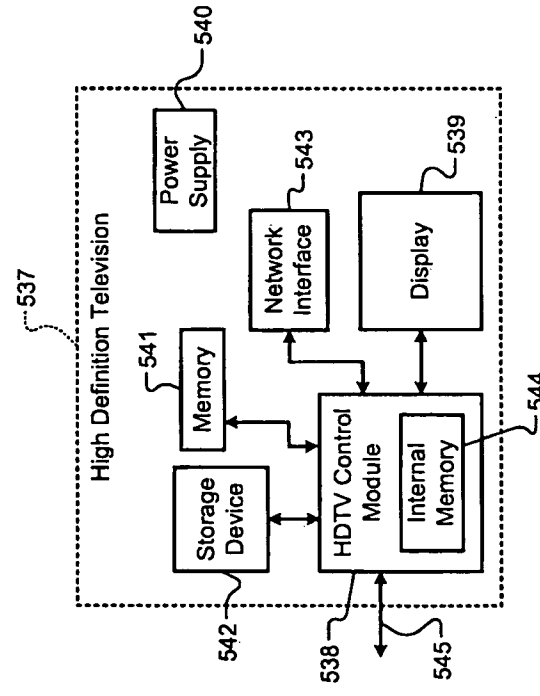


FIG. 15C

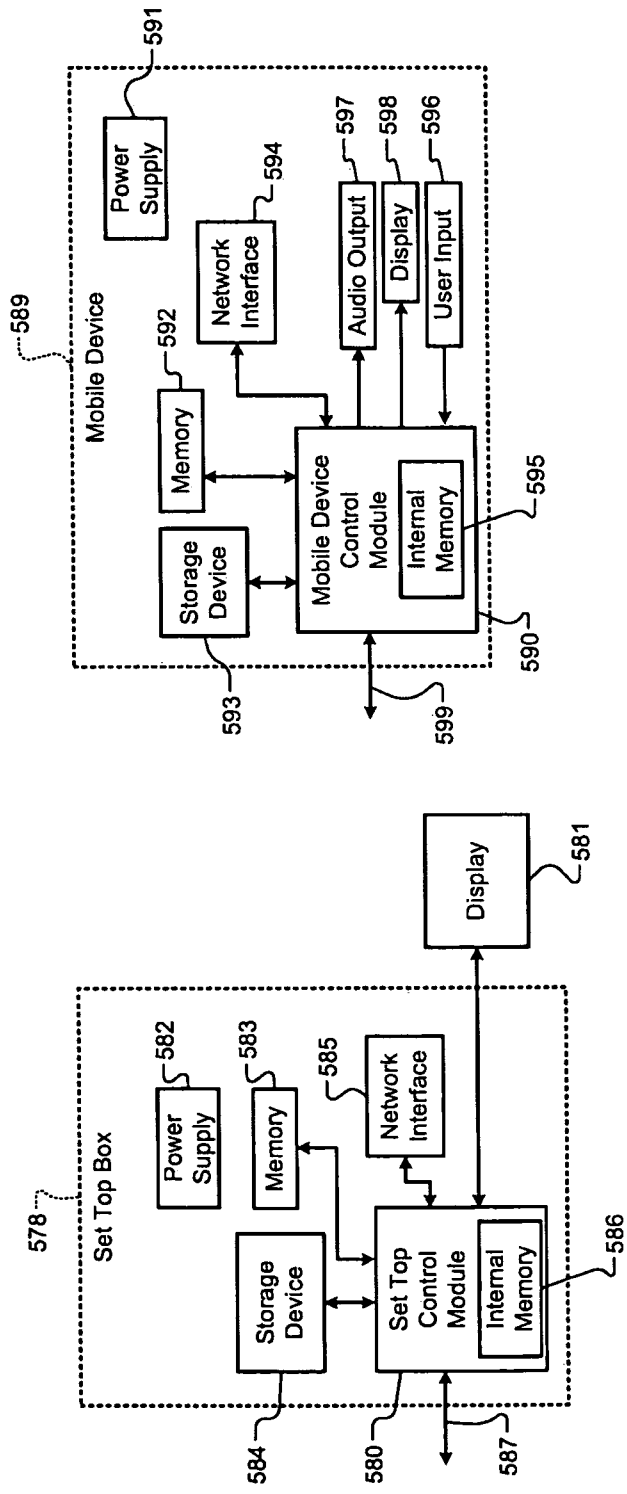


FIG. 15E

FIG. 15F

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/004439

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F12/08 G11C7/10 G11C7/12 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/149708 A1 (GAT TAL [IL] ET AL) 7 July 2005 (2005-07-07)	1,10,13, 26,27, 36,39, 52-58
Y	paragraphs [0001], [0013] - [0030]; figures 1-4	2-9,11, 12, 14-25, 28-35, 37,38, 40-51
X	EP 0 427 425 A (COMPAQ COMPUTER CORP [US]) 15 May 1991 (1991-05-15) column 1, line 16 - column 2, line 17 column 3, lines 11-23 column 4, lines 7-11 column 10, line 32 - column 13, line 12 ----- -/--	1-52

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 98/06100 A (SONY ELECTRONICS INC [US]; SENO KATSUNORI [US]) 12 February 1998 (1998-02-12) abstract; figures 1-5 page 4, line 5 - page 6, line 31 -----	2-9, 11, 12, 14-17, 21-25, 28-35, 37, 38, 40-43, 47-51
Y	US 5 943 284 A (MIZUNO HIROYUKI [JP] ET AL) 24 August 1999 (1999-08-24) figures 1,2(a) column 11, line 16 - column 12, line 20 column 13, lines 20-36 -----	18-20, 44-46
A	EP 1 531 480 A (FUJITSU LTD [JP]) 18 May 2005 (2005-05-18) abstract; figures 2,10 paragraphs [0022] - [0030] -----	1-52
A	US 2006/174090 A1 (SARTORIUS THOMAS A [US] ET AL) 3 August 2006 (2006-08-03) paragraphs [0001], [0016] - [0019]; figures 1-3 -----	53-58

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/004439

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2005149708	A1	07-07-2005	NONE	
EP 0427425	A	15-05-1991	CA 2028085 A1 DE 69032655 D1 DE 69032655 T2 US 5303364 A	04-05-1991 22-10-1998 11-02-1999 12-04-1994
WO 9806100	A	12-02-1998	AU 3973197 A US 5848015 A	25-02-1998 08-12-1998
US 5943284	A	24-08-1999	JP 3560266 B2 JP 9128970 A US 6353569 B1	02-09-2004 16-05-1997 05-03-2002
EP 1531480	A	18-05-2005	NONE	
US 2006174090	A1	03-08-2006	CA 2596865 A1 CN 101147127 A EP 1851621 A2 KR 20070108209 A WO 2006084288 A2	10-08-2006 19-03-2008 07-11-2007 08-11-2007 10-08-2006