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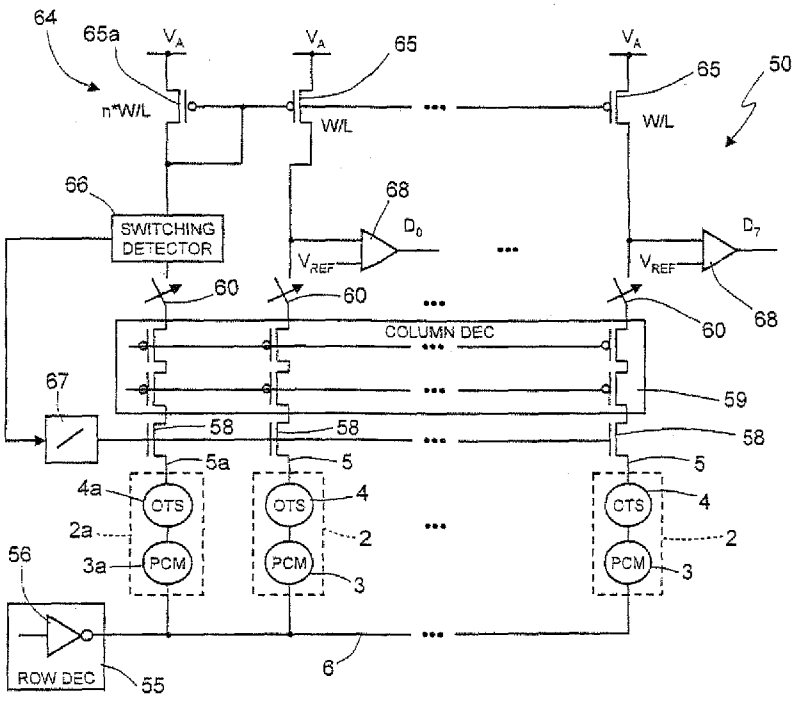
(54) **Title:** PHASE CHANGE MEMORY DEVICE



(57) **Abstract:** A phase change memory device with memory cells (2) formed by a phase change memory element (3) and a selection switch (4). A reference cell (2a) formed by an own phase change memory element (3) and an own selection switch (4) is associated to a group (7) of memory cells to be read. An electrical quantity of the group of memory cells is compared with an analogous electrical quantity of the reference cell, thereby compensating any drift in the properties of the memory cells.

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PHASE CHANGE MEMORY DEVICE

TECHNICAL FIELD

The present invention relates to a phase change memory device, in particular to a phase change memory device having ovonic threshold switch selectors.

BACKGROUND ART

As known, phase change memories use a class of materials that have the property of switching between two phases having distinct electrical characteristics, associated to two different crystallographic structures of the material, and precisely an amorphous, disorderly phase and a crystalline or polycrystalline, orderly phase. The two phases are hence associated to resistivities of considerably different values.

Currently, the alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can be used advantageously in phase change memory cells. The currently most promising chalcogenide is formed from an alloy of Ge, Sb and Te ($Ge_2Sb_2Te_5$), which is now widely used for storing information on overwritable disks and has been also proposed for mass storage.

In the chalcogenides, the resistivity varies by two or more orders of magnitude when the material passes from the amorphous (more resistive) phase to the crystalline (more conductive) phase, and vice versa.

Phase change can be obtained by locally increasing the temperature. Below 150°C, both phases are stable. Starting from an amorphous state, and rising the temperature above 200°C, there is a rapid nucleation of the crystallites and, if the material is kept at the crystallization temperature for a sufficiently long time, it undergoes a phase change and becomes crystalline. To bring the chalcogenide back to the amorphous state it is necessary to raise the temperature above the melting

temperature (approximately 600°C) and then rapidly cool off the chalcogenide.

Memory devices exploiting the properties of chalcogenic materials (also called phase change memory devices) have been already proposed.

In a phase change memory including chalcogenic elements as a storage element, memory cells are arranged in rows and columns to form an array, as shown in Figure 1. The memory array 1 of Figure 1 comprises a plurality of memory cells 2, each including a memory element 3 of the phase change type and a selection element 4. The memory cells 2 are interposed at cross-points between rows 6 (also called word lines) and columns 5 (also called bitlines).

In each memory cell 2, the memory element 3 has a first terminal connected to an own wordline 6 and a second terminal connected to a first terminal of an own selection element 4. The selection element 4 has a second terminal connected a bitline 5. In another solution, the memory element 3 and the selection element 4 of each cell 2 may be exchanged in position.

The composition of chalcogenides suitable for the use in a phase change memory device and a possible structure of a phase change memory cell are disclosed in a number of documents (see, e.g., US-A-5,825,046).

Phase change memory cells comprise a chalcogenic material (forming a proper storage element) and a resistive electrode, also called heater (see, e.g., EP-A-1 326 254, corresponding to US-A-2003/0185047).

From an electrical point of view, the crystallization temperature and the melting temperature are obtained by causing an electric current to flow through the resistive electrode in contact or close proximity with the chalcogenic material and thus heating the chalcogenic material by Joule effect.

In particular, when the chalcogenic material is in the amorphous, high resistivity state (also called the reset state), it is necessary to apply a voltage/current

pulse of a suitable length and amplitude and allow the chalcogenic material to cool slowly. In this condition, the chalcogenic material changes its state and switches from a high resistivity to a low resistivity state (also called the set state).

Vice versa, when the chalcogenic material is in the set state, it is necessary to apply a voltage/current pulse of suitable length and high amplitude so as to cause the chalcogenic material to switch to the amorphous phase.

The selection element is implemented by a switching device, such as a PN diode, a bipolar junction transistor or a MOS transistor.

For example, US-A-5,912,839 describes a universal memory element using chalcogenides and including a diode as a switching element. The diode may comprise a thin film such as polycrystalline silicon or other materials.

GB-A-1 296 712 and US-A-3,573,757 disclose a binary memory formed by an array of cells including a switch element called "ovonic threshold switch" (also referred to as an OTS hereinafter), connected in series with a phase change memory element PCM also called "ovonic memory switch". The OTS and the PCM are formed adjacent to each other on an insulating substrate and are connected to each other through a conducting strip. Figure 2a shows the electrical equivalent of a memory cell 2 having a memory element 3 and an ovonic switch 4.

The PCM is formed by a chalcogenic semiconductor material having two distinct metastable phases (crystalline and amorphous) associated to different resistivities, while the OTS is built with a chalcogenic semiconductor material having one single phase (generally amorphous, but sometimes crystalline) with two distinct regions of operation associated to different resistivities. If the OTS and the PCM have substantially different high resistances, namely with the OTS having a higher resistance than the PCM, when a memory cell is to read, a voltage drop is applied to the cell that is insufficient to trigger the PCM when the latter is in its high

resistance condition (associated with a digital "0" state), but is sufficient to drive the OTS in its low resistance condition when the PCM is already in its low resistance condition (associated with a digital "1" state).

OTS (see, e.g., US-A-3,271,591 and US2006073652, describing its use in connection with memory elements of the phase change type) have the characteristic shown in Figure 2b; Figure 2c shows the characteristic of a reset memory element PCM (with continuous line) and the characteristic of a set PCM (with dashed line).

As shown in Figure 2b, an OTS has a high resistance for voltages below a threshold value $V_{th,OTS}$; when the applied voltage exceeds the threshold value $V_{th,OTS}$, the switch begins to conduct at a substantially constant, low voltage and has a low impedance. In this condition, if the PCM is set, as visible from Figure 2c, the memory cell is on; if the PCM is reset, the memory cell is off.

When the current through the OTS falls below a holding current I_H, the OTS goes back to his high-impedance condition. This behavior is symmetrical and occurs also for negative voltages and currents (not shown).

As shown in Figure 2c, in the amorphous state (reset) a PCM has a plot similar to the plot of an OTS; when crystalline, the PCM has a higher conductance in the lower portion of the characteristic and about the same behaviour of the reset cell in the upper portion.

In OTS, the threshold voltage V_{th} is subject to a drift. The threshold voltage drift is harmful for OTS-selected memory arrays, because it could prevent the storage element of chalcogenic material from being correctly read.

In fact, as immediately recognizable from the comparative observation of Figures 2b and 2c, if the threshold voltage V_{th} of the selector is not known with satisfactory precision, and the chalcogenic storage element is crystalline (and thus stores a logical "1") it could be read as a logical "0" because, at the reading voltage,

the selector has not yet switched to the conductive state. Analogously, a reading error may occur if the chalcogenic storage element is amorphous (and thus stores a logical "0") but at the reading voltage the element is already in the higher portion of the curve of Figure 2c.

In other words, the ideal reading voltage is limited between the threshold voltage of the OTS ($V_{th,OTS}$) and the sum of both threshold voltages ($V_{th,OTS}$ + $V_{th,PCM}$) and the exact knowledge of $V_{th,OTS}$ is thus crucial in order to maximize the reading window.

In general, it may be impossible to determine the value of a stored bit if the threshold of the selector switch is not known.

To solve this problem, peculiar chalcogenide materials are being tested that do not show drift. In the alternative, or as an additional solution, electrode materials are being studied that are able to reduce this problem. However, currently all the materials suitable for the use in phase change memory devices are affected by the threshold drift.

Furthermore, it has been noted that also PCMs undergo a drift of the reset resistance (R_{reset}) with time, which causes a variation in the slope of the curves in Fig. 2c. The drift in the reset resistance poses some problems for multilevel storage based on phase change memories, because intermediate levels of crystallization, corresponding to different levels of resistance, are used to store different bits. Thus, the resistance drift may cause reading errors.

DISCLOSURE OF INVENTION

The object of the invention is thus to provide a solution to the drift problem of the chalcogenide materials.

According to the present invention, there are provided a phase change memory device, a reading and a programming method thereof, as defined in claims

1, 16 and 21, respectively.

In practice, to solve the problem of the drift, each group of memory cells to be read (e.g., all the memory cells arranged on a same row) are associated to one or more reference cells (also called SLC = Single-Level Cell for the single cell and MLC = Multi-Level Cell for multiple reference cells) having the same structure as the associated memory cells. The reference cells may be formed adjacent to the respective memory cells.

Therefore, the reference cells have the same drift in the threshold voltage V_{th} and in the resistance as the memory cells.

During programming, all the memory cells belonging to a same group are programmed together (simultaneously or immediately before or after) with their reference cell(s). If the whole programming operation is performed within a time span of 1-10 μs, it is possible to guarantee the consistency of the electric properties (threshold voltage or resistance) of all the memory cells and their reference cell(s).

During reading, the memory cells are compared with their reference cell(s); thereby it is ensured that any drift affecting an electrical quantity (threshold voltage or resistance) of the memory cells is shared also by the reference cell(s), thereby ensuring a reliable reading of all the memory cells associated to the reference cell(s).

In particular, the problem associated with the drift of the threshold voltage of the OTS selection element may be solved using reference cell(s) having own threshold switches (in the following indicated as threshold reference cell(s)) and the threshold reference cell(s) may be programmed in the set state, so that they switch on when the voltage applied thereto reaches the threshold voltage $V_{th,OTS}$.

Furthermore, by arranging the cells to be read and the threshold reference cell(s) along a same row, the switching of the threshold reference cell(s) may be exploited for all the memory cells to be read, thereby obtaining a simultaneous

reading thereof.

For solving the problem of the resistance drift, it is not necessary to use reference cell(s) having Ovonic Threshold Switches, but the switches may be of any type, for example bipolar or MOS transistors. In this case the reference cells generate the reference values that are compared with the memory cell during reading.

BRIEF DESCRIPTION OF THE DRAWINGS

For the understanding of the present invention, preferred embodiments thereof are now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

- Figure 1 shows the architecture of a memory array;

- Figure 2a shows the electric equivalent of a memory cell having an ovonic switch;

- Figures 2b and 2c plot the current vs. voltage characteristics of an ovonic switch and of a phase change memory element;

- Figures 3 and 4 are cross-section taken along crossing planes of phase change memory cell including an ovonic switch;

- Figure 5 shows the organization of an embodiment of the present phase change memory device;

- Figure 6 shows a circuit diagram of a phase change memory sensing device, according to a first embodiment;

- Figure 7 is a plot showing the distribution of read current for multi-level programming;

- Figure 8 shows a circuit diagram of a phase change memory sensing device, according to a second embodiment; and

- Figure 9 is a system depiction according to one embodiment of the present

invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 3 and 4 show an exemplary structure of a phase change memory cell including an ovonic switch.

In detail, a semiconductor substrate (not shown) is coated with an insulating layer 12. Row lines 13, e.g. of copper, extend on top of the insulating layer 12, insulated from each other by a first dielectric layer 14. A protective region 22 and a first oxide layer 19 encapsulate a heater structure 23 of, e.g., TiSiN, which has a cup-like shape and is internally covered by a sheath layer 24, e.g. of silicon nitride, and filled by a second oxide layer 25.

The memory cells include PCM/OTS (Ovonic Memory Switch/Ovonic Threshold Switch) stacks or dots 31, each comprising a storage region 27 (e.g., $Ge_2Sb_2Te_5$), a first barrier region 28 (e.g., TiAlN), a switching region 29 (e.g., As_2Se_3) and a second barrier region 30 (e.g., TiAlN) extend on and in contact with walls 23a of the heater structures 23. Figure 3 shows two dots 31 which extend substantially aligned along a column 5 of the array 1 (see Figure 1) while Figure 4 shows one and a half dots 31 which extend substantially aligned along a row 6 of the array. The dots 31 are sealed and insulated by a sealing layer 32, e.g., of silicon nitride, and by an intermetal layer 33 of e.g. of silicon dioxide.

Vias openings 35 extend through the intermetal layer 33, the sealing layer 32, the first oxide layer 19 and the protective region 22 down to the row lines 13, while trenches 36a, 36b extend through the intermetal layer 33 down to the top of the dots 31 or vias opening 35. Vias 40, column lines 41a and row line connections 41b are formed in the vias openings 35 and in the trenches 36a, 36b. Column lines 41a correspond to the bitlines 5 while row lines 13 correspond to word lines 6 of Figure 1. Thus each dot 31 is formed at the intersection between a row line 13 and a

column line 41a.

Figure 5 shows an embodiment of a memory array 10 according to the invention. Memory array 10 comprises a plurality of wordlines 6 and a plurality of data bitlines 5. Memory cells 2 are arranged at the cross points of the wordlines 6 and the bitlines 5. Groups 7 of eight memory cells 2 along a same wordline 6 form a word and are associated to an own threshold reference cell 2a. Each threshold reference cell 2a is formed next to the associated group 7 of memory cells 2 and is connected to the same word line 6 of the associated group; the threshold reference cells 2a are coupled to own bitlines, called reference bitlines 5a.

During reading, the data bitlines 5 of all the memory cells 2 belonging to the word to be read receive a biasing voltage, which is a generally increasing voltage, for example a ramp voltage. Simultaneously, also the reference bitline 5a receives the biasing voltage. When the switching of the threshold reference cell 2a is detected, after a small and pre-defined delay, the voltage ramp on the word line 6 may be stopped and the currents of all the memory cells 2 being read may be detected.

Therefore, when the content of the addressed memory cells 2 is read, it is ensured that all the OTS 4 thereof have switched, even if the threshold voltage has drifted, since their reference cell 2a undergoes any such threshold voltage drift.

During programming, the memory element of the threshold reference cell 2a may be set by applying a long and reliable voltage pulse, thus triggering the ovonic switch thereof, and then the memory cells 2 associated to the just set threshold reference cell 2a are programmed (set or reset) by applying voltage/current pulses of suitable amplitude and length. Preferably, the memory cells 2 are programmed as soon as possible after or before programming the threshold reference cell 2a.

Figure 6 shows an implementation of a reading circuit 50 that may be used

with the above described memory architecture.

In Figure 6, word line 6 is shown connected to a final driver 56 of a row decoder 55. Bitlines 5 and 5a are connected to cascode transistors 58 of the NMOS type that regulate the voltage on the bitlines 5, 5a and in particular apply a ramp voltage thereto.

The cascode transistors 58 are connected, through a column decoder 59, shown only partially, and respective switches 60, to respective data loads 65 and reference load 65a, formed by PMOS transistors. In particular, data loads 65 have drain terminals connectable to the data bitlines 5 while the reference load 65a has a drain terminal connectable to the reference bitline 5a. The loads 65, 65a have source terminals connected to a supply voltage V_A and are connected together in a mirror-like configuration; thus, they have gate terminals connected together and the reference load 65a has shorted gate and drain terminals. Preferably, the reference load 65a has an aspect ratio (ratio between the width and the length of the load transistors) n times higher than the data loads 65. Therefore, the current read on the reference branch is mirrored in the data branches divided by n. The actual ratio could be optimized to the specific application. Thus, the loads 65, 65a form a current/voltage converter 64.

A switching detector 66 is coupled between the reference load 65a and the column decoder transistors connected to the reference bitline 5a. However, the switching detector 66 may be located also between the column decoder 59 and the reference bitline 5a or any other suitable position. The switching detector 66 is any suitable circuit able to detect when the current through the reference bitline 5a exceeds a preset reference value, thus detecting switching on of the OTS 4 of the threshold reference cell 2a. For example, the switching detector 66 could be implemented using a comparator having a first input coupled to the reference bitline

5a, a second input coupled to the reference value, and an output that supplies a signal based on a comparison of the two inputs. The switching detector 66 generates a control signal for a voltage generator 67 connected to the gate of the NMOS cascode transistors 58, thus stopping the voltage ramp.

Comparators 68 compare the voltage at the drain terminals of the data loads 65 (outputs of the current/voltage converter 64) with a reference value V_{REF}. The outputs of the comparators 68 represent data bits D_0-D_7.

The switches 60 are closed during reading but are open during programming, thus disconnecting the memory cells 2, 2a from the loads 65, 65a. In this phase, the memory cells 2, 2a are connected to dedicated pumps, of the current-controlled or voltage-controlled type, in a per se known manner.

From the above it is clear that all the memory cells (both data and threshold reference cells) in a string or word have cycle lives which are always synchronized, since they are always programmed together, thus compensating any possible drift of their threshold voltage Vth due to cycling.

Figure 7 shows a plot of the probability density versus current for a four-state PCM cell (additional states may be added by further sub-dividing the current ranges as is well-known in the art). Here, "00" corresponds to an amorphous state associated with reset bits. Level "11" corresponds to a crystalline state associated to set bits. Intermediate levels "01" and "10" correspond to partially crystalline states.

The reset state is typically obtained with a single square pulse (e.g., 50 ns) that drives the chalcogenide material to a melting point of approximately 600°C and then rapidly cools it.

The set state is typically obtained with a single square pulse that drives the chalcogenide material up to crystallization temperature (e.g. 400°C) and maintains it there until long-range order is reconstructed. Alternatively, set can be obtained by

driving the chalcogenide material to the melting point and then cooling it slowly enough for the crystals to reorganize.

The intermediate states ″01″, ″10″ may require additional programming pulses and the creation of a percolation path, as described e.g. in European patent application 05104877.5 filed on 3 June 2005.

ref_{01}, ref_{10}, and ref_{11} are reference currents at intermediate levels generated by reference cells programmed in a same programming operation as the memory cells 2 and used during reading in order to sense the state of the memory cells 2, thus replacing absolute reference values, that are not able to track the drift of the memory cells.

Since the drift of resistance is proportional to the amorphous portion of the storage region 27 (see figure 3), it could be advantageous to place the intermediate levels ("01" and "10" in this case) close to "11", i.e. the fully crystalline state.

During reading, the resistance drift of the reference cells allows to track the window associated with the intermediate levels.

In this case, we don't require the presence of an OTS selector, because the technique could be applied with any kind of selector associated to the PCM.

Such a solution does not require a switching detector on the bitline associated to the reference bits, and it is possible to simply verify the bits stored in the memory cells against the reference bits, using them one at a time.

Figure 8 shows and embodiment of a reading circuit 50' that may be used for tracking resistance drift. In Figure 8, the same reference numbers have been used for elements in common with the reading circuit 50 of Figure 6 and the following description refers only to the differences between the reading circuits 50 and 50'.

In detail, the reading circuit 50' of Figure 8 comprises a plurality of reference bitlines 5a, 5b, and 5c (here three, the same number as the reference levels used to

discriminate the possible states of the memory cells 2). Here, the selection elements 4 are of generic type. Each reference bitline 5a, 5b, 5c is connected to an own reference cell 2a, 2b and 2c, to an own cascode transistor 58, to an own switch 60a, 60b, 60c, and to an own reference load 65a, 65b, 65c. The reference loads 65a, 65b, 65c have a same aspect ratio W/L, equal to the aspect ratio of the data loads 65. No switching detector 66 is provided for.

During programming, the reference cell 2a, 2b and 2c are programmed each to an own threshold voltage, corresponding to a respective reference value ref_{01}, ref_{10}, and ref_{11} of Figure 7.

During reading, the switch 60a are closed in sequence, thus feeding the data bitlines 5 with a current equal to the current flowing in one reference cell 5a, 5b, 5c at time; thus the comparators 68 compare each time the reference value V_{REF} to the output voltages of the current/voltage converter 64 for three different biasing currents (corresponding to the above three reference values). The output of the comparators 68 is used by a hardware or software stage (not shown) configured to extract the complete and correct data, as known in the art of multilevel memories.

Basically, for each memory cell 2 of the group of words 7, the memory cell 2 is connected to a first reference cell 2a through the current/voltage converter 64; a first electrical quantity (current) of the memory cell 2 is read; then the memory cell 2 is connected to a second reference cell 2b through the current/voltage converter 64; a second electrical quantity (current) is read. The process is then repeated for all the intermediate levels provided for. In the embodiment of figure 8, the third reference cell 2c is connected and the output voltage of the converter is compared to the reference value. Then, the state of the memory cell 2 and thus the stored bits is detected based onto the read electrical quantity.

Obviously, a similar approach and a similar reading circuit may be used in

case of a different number of levels stored in the memory cells 2, e.g., in case of only three levels or more than four levels. Obviously, in this case, the number of reference cells 2a-2c depends on the number of levels to be stored, being sufficient a number of reference cells equal to the number of desired levels minus 1.

Other sequences of selection for the reference cells are also possible, based on the reading algorithm chosen among those known in the art of multilevel memories.

Figure 9 shows a portion of a system 500 in accordance with an embodiment of the present invention. System 500 may be used in wireless devices such as, for example, a personal digital assistant (PDA), a laptop or portable computer with wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive information wireless. System 500 may be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network, although the scope of the present invention is not limited in this respect.

System 500 may include a controller 510, an input/output (I/O) device 520 (e.g. a keypad, display), a memory 530, a wireless interface 540, a digital camera 550, and a static random access memory (SRAM) 560 and coupled to each other via a bus 550. A battery 580 may supply power to the system 500 in one embodiment. It should be noted that the scope of the present invention is not limited to embodiments having any or all of these components.

Controller 510 may comprise, for example, one or more microprocessors, digital signal processors, micro-controllers, or the like. Memory 530 may be used to store messages transmitted to or by system 500. Memory 530 may also optionally be used to store instructions that are executed by controller 510 during the

operation of system 500, and may be used to store user data. The instructions may be stored as digital information and the user data, as disclosed herein, may be stored in one section of the memory as digital data and in another section as analog memory. As another example, a given section at one time may be labeled as such and store digital information, and then later may be relabeled and reconfigured to store analog information. Memory 530 may comprise one or more different types of memory. For example, memory 530 may comprise a volatile memory (any type of random access memory), a non-volatile memory such as a flash memory, and memory 1 illustrated in Figure 1 incorporating the architecture described with reference to Figures 5-8.

The I/O device 520 may be used to generate a message. The system 500 may use the wireless interface 540 to transmit and receive messages to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface 540 may include an antenna, or a wireless transceiver, such as a dipole antenna. Also, the I/O device 520 may deliver a voltage reflecting what is stored as either a digital output (if digital information was stored), or it may be analog information (if analog information was stored).

While an example in a wireless application is provided above, embodiments of the present invention may also be used in non-wireless applications as well.

Finally, it is clear that numerous variations and modifications may be made to the phase change memory device and the reading and programming methods described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

CLAIMS

1. A phase change memory device, comprising a memory array (1) formed by a plurality of groups (7) of memory cells (2), the memory cells being arranged in rows and columns and connected at cross-points of word lines (6) and data bitlines (5), each memory cell (2) comprising a phase change memory element (3) and a selection switch (4), characterized by a plurality of reference cells (2a-2c), each reference cell (2a-2c) comprising an own phase change memory element (3a-3c) and an own selection switch (4a-4c) and being associated to at least one group (7) of memory cells.

2. The phase change memory device according to claim 1, wherein each group (7) of memory cells (2) and the associated reference cell (2a-2c) extend along a same word line (6) and the reference cells (2a) are connected to reference bitlines (5a-5c).

3. The phase change memory device according to claim 2, wherein the memory cells (2) and the reference cell (2a-2c) of each group (7) are arranged adjacent to each other.

4. The phase change memory device according to any of claims 1-3, wherein each group of memory cells (2) forms a respective data word.

5. The phase change memory device according to any of claims 1-4, wherein the selection switches (4, 4a) of the memory cells (2) and of the reference cells (2a) are ovonic threshold switches.

6. The phase change memory device according to claim 5, wherein the phase change memory elements (3) of the memory cells (2) are selectively programmable in at least a set state and a reset state and the phase change memory elements (3a) of the reference cells (2a) are programmed in the set state.

7. The phase change memory device according to claim 5 or 6, comprising a

reading stage (50) connected to said memory array (1) and including threshold detecting means (66) selectively coupled to said threshold reference cells (2a) for detecting an electrical quantity of the reference cells reaching a threshold.

8. The phase change memory device according to claim 7, wherein the reading stage (50) comprises a biasing voltage generator (58, 67) for applying a biasing voltage to said data bitlines and a reference bitline (5, 5a); a switching detector (66) selectively coupled to said reference bitline (5a) and detecting a switching of said threshold reference cell (2a), the switching detector generating a deactivation command for said biasing voltage generator (58, 67) when detecting switching of said threshold reference cell (2a).

9. The phase change memory device according to claim 8, wherein said biasing voltage generator comprise a voltage source (67) and a plurality of cascode transistors (58) controllably connected to the voltage source, each cascode transistor being further connected to a respective one of the data and reference bitline (5).

10. The phase change memory device according to claim 8 or 9, wherein said biasing voltage generator (58, 67) generates a generally increasing voltage, preferably a ramp voltage.

11. The phase change memory device according to any of claims 1-4, wherein the phase change memory elements (3) of the memory cells (2) are selectively programmable in a plurality of states including at least a set state, a reset state and an intermediate state, and wherein at least two reference cells (2a-2c) are associated to each group (7) of memory cells, each reference cell (2a-2c) being connected to a respective one of a plurality of reference bitlines (5a-5c).

12. The phase change memory device according to claim 11, comprising a reading stage (50') connected to said memory array (1) and including a

current/voltage converter (64) connectable to said data bitlines (5) and reference bitlines (5a-5c) through respective data bitlines switches (60) and reference bitlines switches (60a-60c); said reference bitlines switches being activated alternately and in sequence.

13. The phase change memory device according to claim 12, wherein the current/voltage converter (64) comprises a plurality of data loads (65) connectable to said data bitlines (5) and at least two reference loads (65a-65c) connectable to said reference bitlines (5), said data and reference loads defining current mirrors.

14. The phase change memory device according to claim 13, wherein said data and reference loads (65, 65a-65c) comprise each a MOS transistor of a plurality of MOS transistors, said MOS transistors having a same aspect ratio.

15. A system comprising:

- a processor (510);
- an input/output device (520) coupled to said processor; and
- a memory (530) coupled to said processor, said memory including the phase change memory device according to any of claims 1-14.

16. A method of reading a phase change memory device comprising a memory array (1) formed by a plurality of groups (7) of memory cells (2), the memory cells being arranged in rows and columns and connected at cross-points of wordlines (6) and data bitlines (5), each memory cell (2) comprising a phase change memory element (3) and a selection switch (4), the memory device further including a plurality of reference cells (5a), each reference cell (5a) comprising an own phase change memory element (3) and an selection switch (4), being associated to at least one group (7) of memory cells and being connected to a reference bitline, characterized by the steps of:

comparing an electrical behavior of said memory cells (2) and of said

reference cells (2a-2c).

17. The method of claim 16, wherein the selection switches of the memory cells and the reference cells are ovonic threshold switches, comprising the steps of:

applying a biasing voltage to said data and reference bitlines;

detecting a switching of the reference cell (2a);

terminating applying a biasing voltage;

reading the state of said memory cells (2).

18. The method of claim 17, wherein the biasing voltage is a generally increasing voltage, preferably a ramp voltage.

19. The method of claim 17 or 18, comprising introducing a delay between detecting a switching of the reference cell and terminating applying a biasing voltage.

20. The method of claim 16, wherein the phase change memory elements (3) of said memory cells (2) are selectively programmable in a plurality of states including at least a set state, a reset state and an intermediate state, and wherein at least a first and a second reference cells (2a-2c) are associated to each group (7) of memory cells, the method including connecting at least one memory cell (2) to the first reference cell (2a) through a current/voltage converter (64), reading a first electrical quantity of said at least one memory cell (2), connecting the at least one memory cell (2) to the second reference cell (2b) through the current/voltage converter, reading a second electrical quantity of the at least one memory cell, detecting a state of the at least one memory cell based onto the reading the first and second quantity.

21. A method of programming a phase change memory device comprising a memory array (10) formed by a plurality of groups (7) of memory cells (2), the memory cells being arranged in rows and columns and connected at cross-points

between word lines (6) and data bitlines (5), each memory cell (2) comprising a phase change memory element (3) and an ovonic threshold switch (4), the memory device further including a plurality of threshold reference cells (5a), each threshold reference cell (5a) comprising an own phase change memory element (3) and an own ovonic threshold switch (4), being associated to a group (7) of memory cells and being connected to a reference bitline, comprising programming a group of memory cells (2) in at least a set state and a reset state, characterized by the steps of:

programming a threshold reference cell (2a) associated to the group of memory cells (2) being programmed into the set state; and

programming the memory cells (2).

22. The method of programming a phase change memory device according to claim 21, wherein programming the threshold reference cell (2a) is performed after programming the group of memory cells (2).

23. The method of programming a phase change memory device according to claim 21, wherein programming the threshold reference cell (2a) is performed before programming the group of memory cells (2).

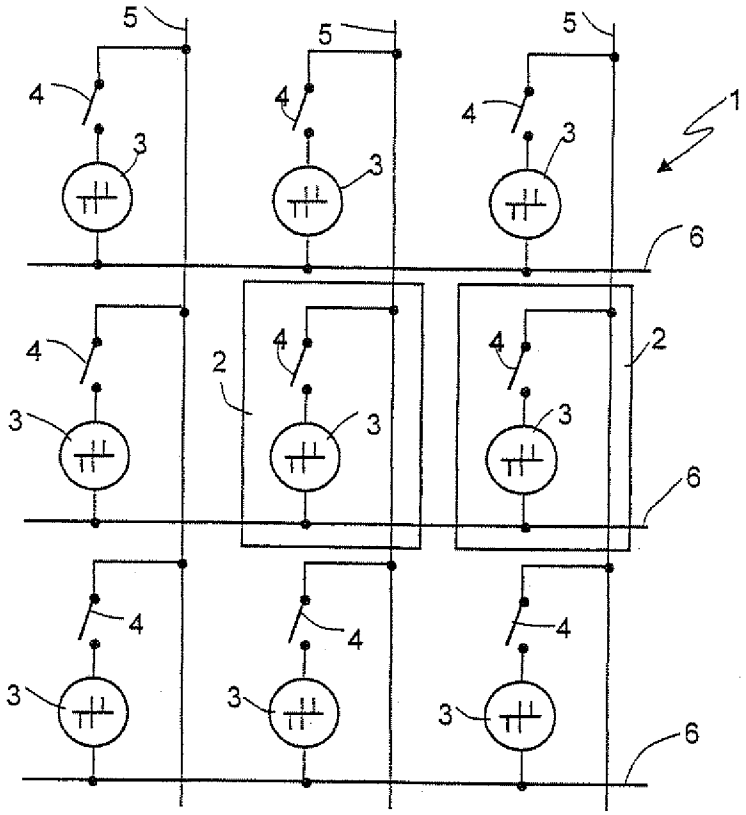
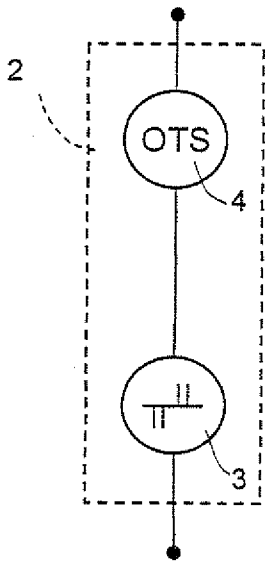


Fig.1

Fig.2a



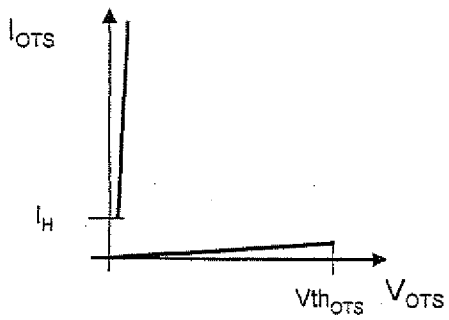


Fig.2b

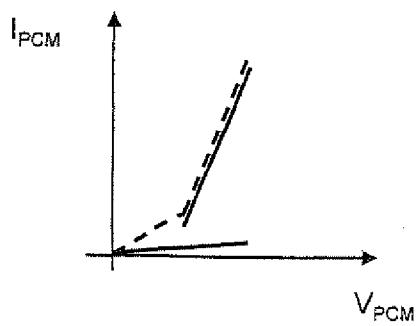
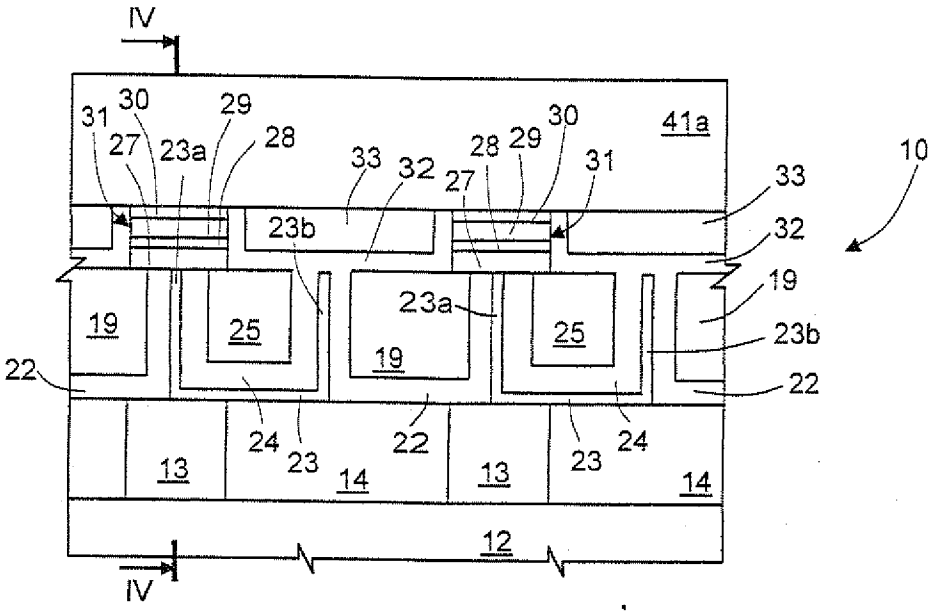


Fig.2c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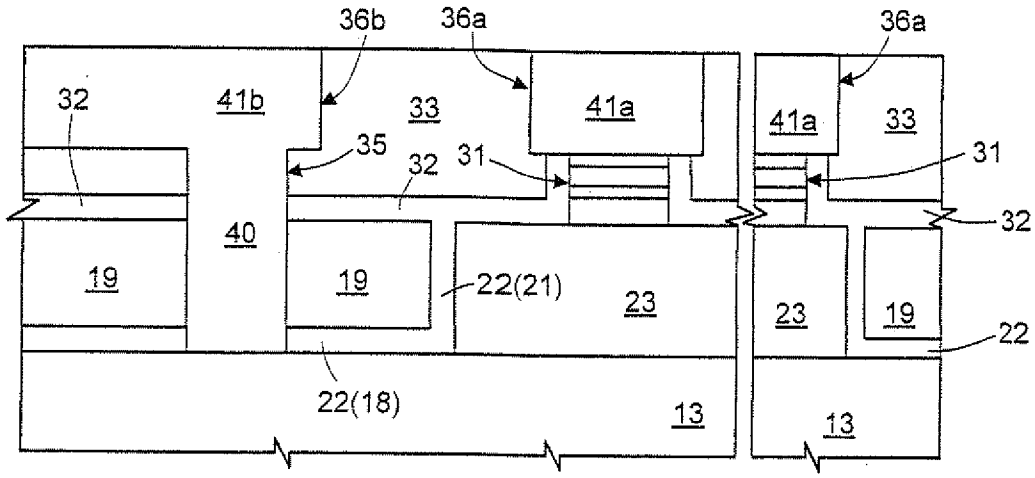
31
29
27
23a
28
33
32
28
29
30
41a
10
31
33
32
23b
19
23a
25
25
23b
19
19
22
22
24
23
22
23
24
13
14
13
14
12
IV

Fig. 3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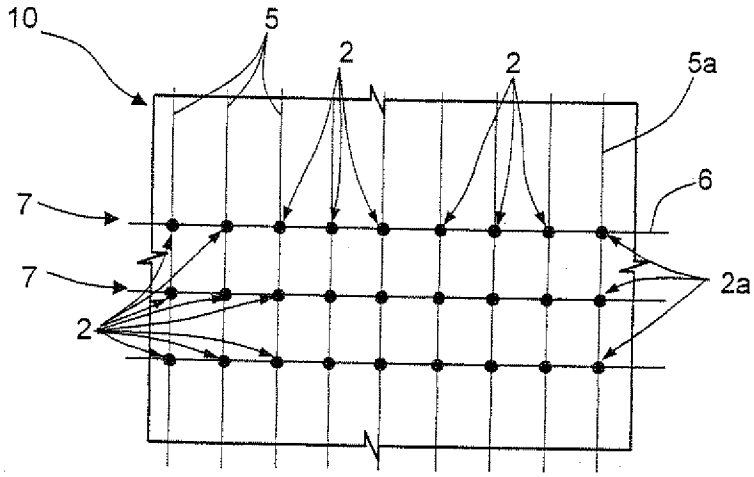
23
19
22
22(18)
13
13

Fig. 4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5
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5a
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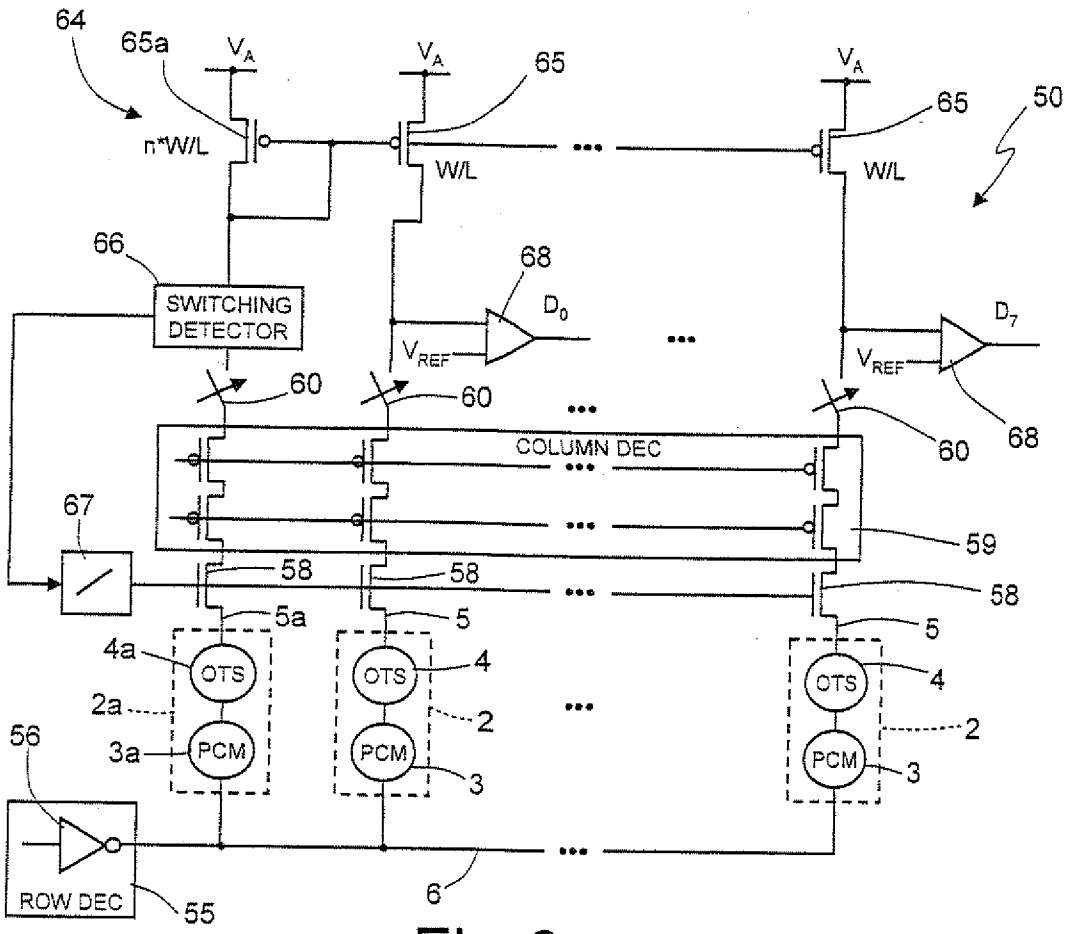
7
2
2a

Fig. 5


64
65a
V_A
V_A
65
V_A
65
50
n*W/L
W/L
W/L
66
68
SWITCHING DETECTOR
D_0
D_7
V_{REF}
V_{REF}
60
60
60
68
COLUMN DEC
67
59
58
58
58
5a
5
5
4a
OTS
OTS
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2a
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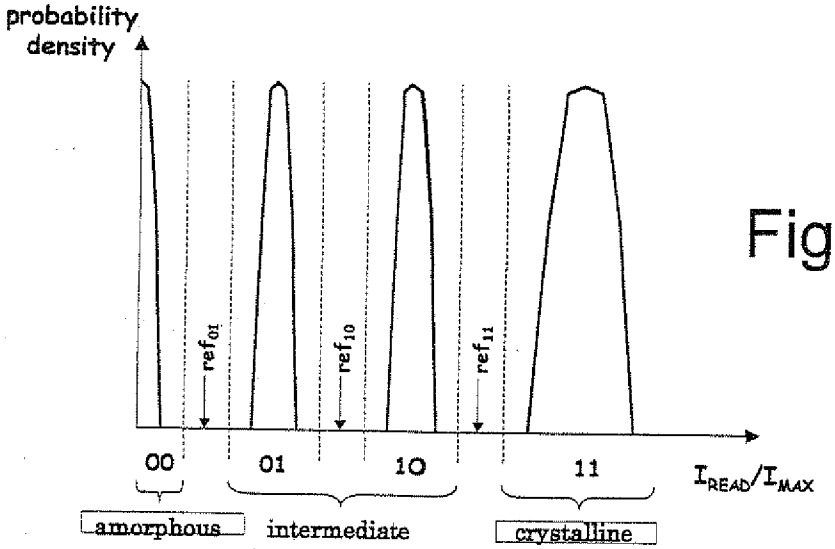
3a
PCM
PCM
3
PCM
3
56
ROW DEC
55
6

Fig.6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ref10
ref11
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01
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11
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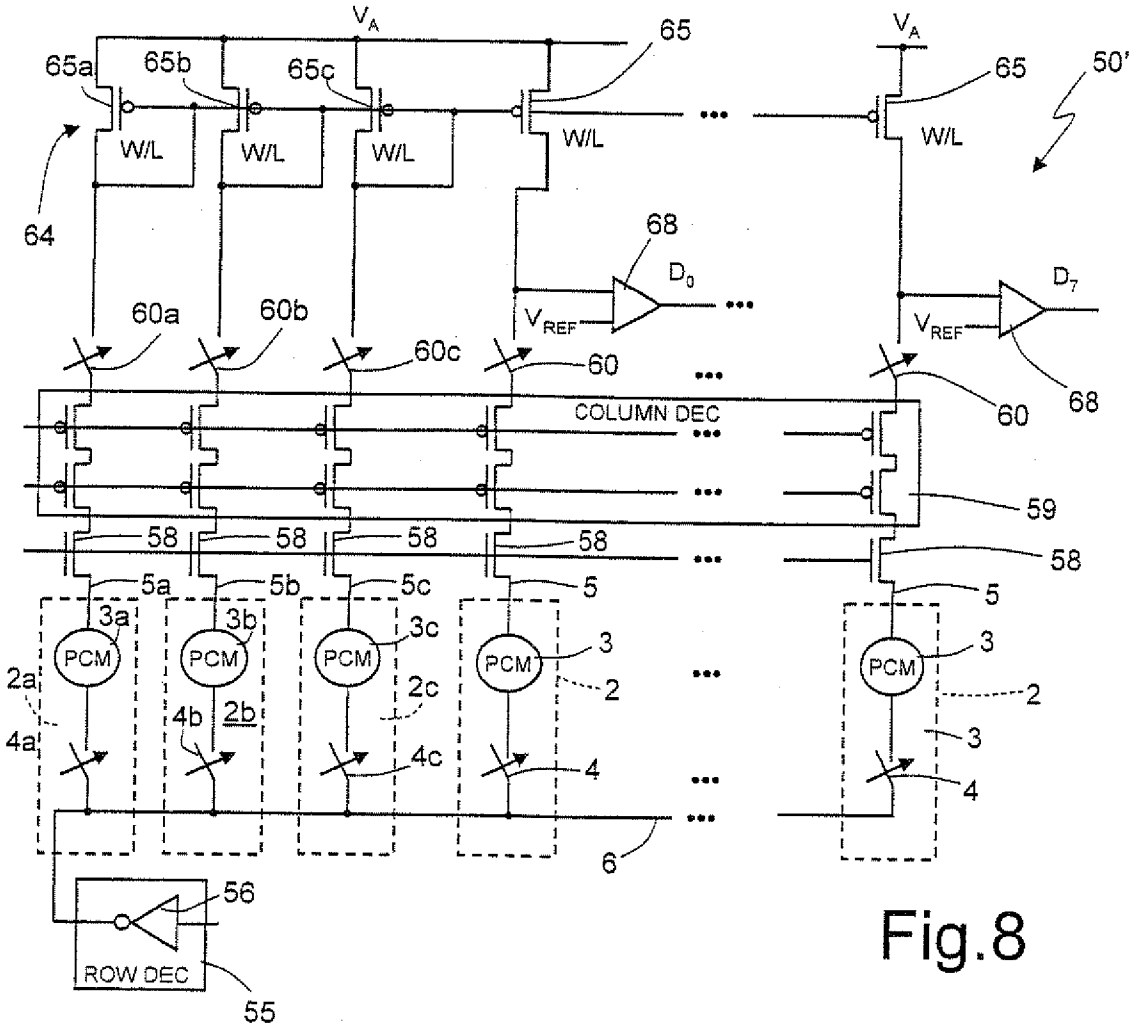
amorphous
intermediate
crystalline

Fig.7


VA
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65b
65c
W/L
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68
D0
D7
VREF
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60b
60c
60
50'
COLUMN DEC
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58
5a
5b
5c
5
3a
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2b
2c
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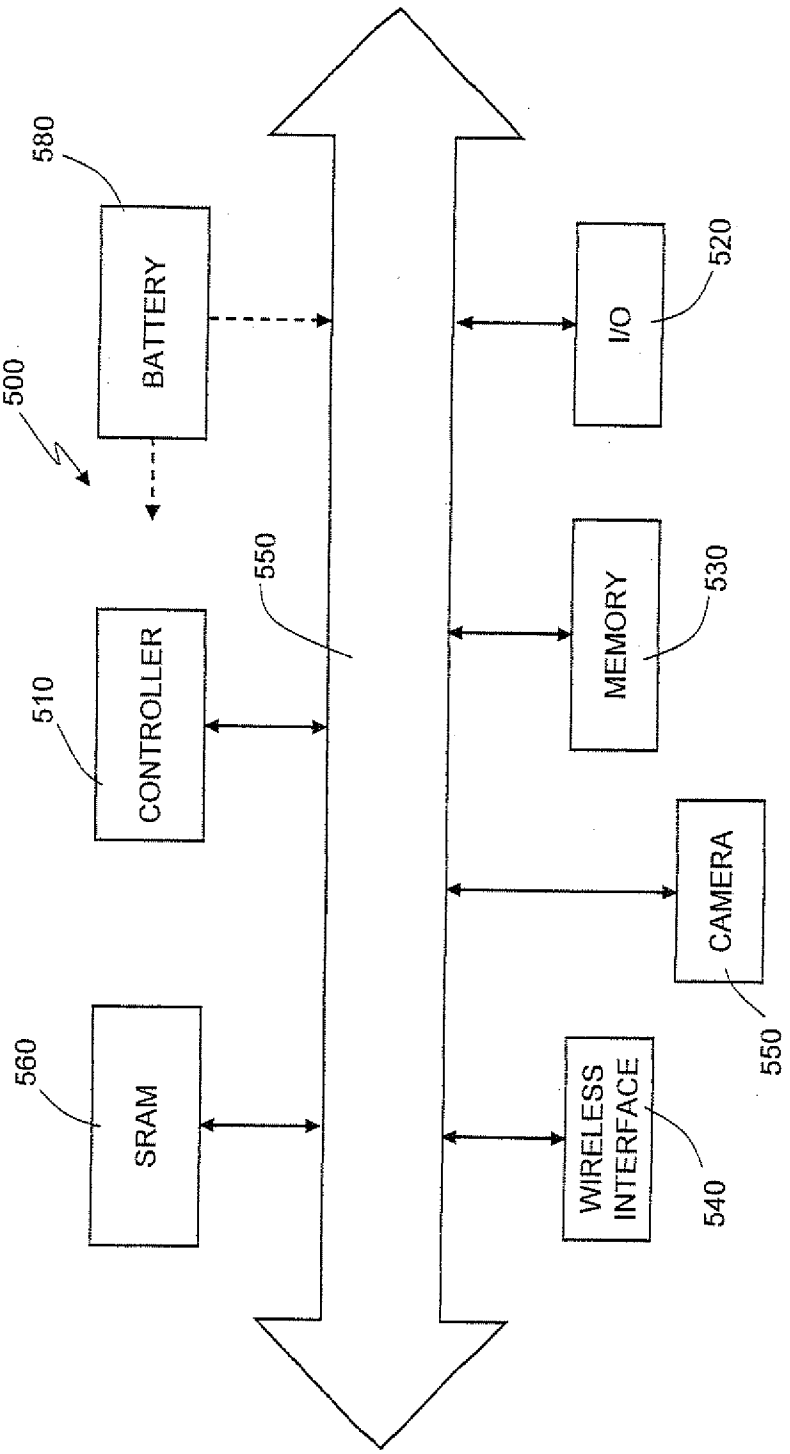
4b
4c
4
6
56
ROW DEC
55
PCM

Fig.8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BATTERY
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510
CONTROLLER
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SRAM
I/O
520
MEMORY
530
CAMERA
550
WIRELESS INTERFACE
540

Fig.9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/057706

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/24 G11C16/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2006/072357 A1 (WICKER GUY C [US]) 6 April 2006 (2006-04-06) the whole document	1-3,5,6, 11,16, 20-23 4,12-15 7-10, 17-19
Y	US 2005/024922 A1 (LI BIN [US] ET AL) 3 February 2005 (2005-02-03) paragraphs [0007], [0015], [0018], [0019]; figures 2,4	12-14
Y	EP 1 511 042 A (ST MICROELECTRONICS SRL [IT]) 2 March 2005 (2005-03-02) paragraphs [0031] - [0044]; figure 2	4,13,14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 October 2007	24/10/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Meul, Hans

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/057706

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 2003/026134 A1 (LOWREY TYLER A [US]) 6 February 2003 (2003-02-06) figure 6	15
Y	US 2005/029505 A1 (LOWREY TYLER A [US]) 10 February 2005 (2005-02-10) figures 1,14	15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2007/057706

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		US 2003198118 A1	23-10-2003
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