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(71) Applicant *(for all designated States except US)*: **INFINEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Str. 53, 81669 München (DE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **COWLEY, Andrew** [GB/US]; 8 Summerlin Court, Wappingers Falls, New York 12590 (US). **FRIESE, Gerald Rudolf** [DE/DE]; St.-Cajetan-Str. 5, 81669 München (DE). **HIERLEMANN, Matthias** [DE/—]; No.3, Li-Hsin-Rd., 2, Science-Based Industrial Park, Hsinchu 30077 (TW). **HOINKIS, Mark** [US/US]; 37 Spruce Ridge Drive, Fishkill, NY 12524 (US). **KALTALIOGLU, Erdem** [DE/US]; 214 Jefferson Blvd., Fishkill, New York 12524 (US). **WARNER, Dennis John** [US/US]; 6070 Pond Grass Road, Mechanicsville, VA 23111 (US).

(74) Agents: **KARL, Frank** et al.; Postfach 1330, 85627 Grasbrunn (DE).

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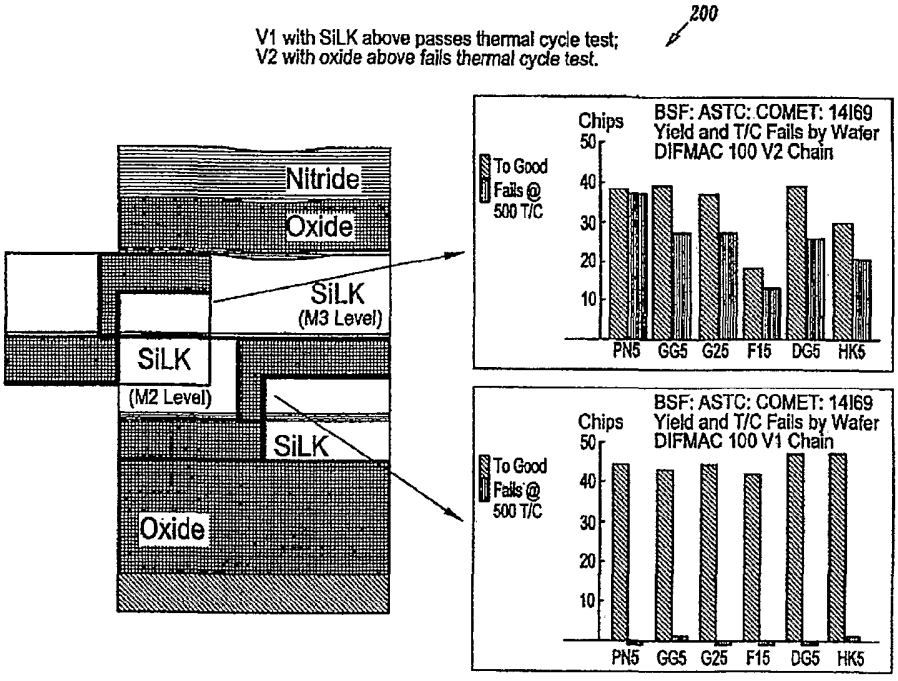
(54) Title: METHOD OF STRESS RELIEF IN SEMICONDUCTOR STRUCTURES



(57) Abstract: A method, apparatus and system are provided for relieving stress in the via structures of semiconductor structures whenever a linewidth below a via is larger than a ground-rule, including providing a via at least as large as the groundrule, providing a landing pad above the via, providing a via bar in place of a via, slotting the metal linewidth below the via, or providing an oversize via with a sidewall spacer.

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METHOD OF STRESS RELIEF IN SEMICONDUCTOR STRUCTURES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the relief of stress in semiconductor structures, and more particularly relates to the relief of stress in the via structures of SiLK™ semiconductor structures.

2. Discussion of the Related Art

SiLK™ is a trademark of Dow Chemical for a polymer thermoset resin exhibiting very low dielectric constant, useful in semiconductor manufacturing, and described in Balance et al., U.S. Patent No. 5,523,163, for LOW DIELECTRIC CONSTANT COATINGS, issued June 4, 1996, and Bremmer et al. U.S. Patent No. 5,906,859, for a METHOD FOR PRODUCING LOW DIELECTRIC COATINGS FROM HYDROGEN SILSEQUIOXANE RESIN, issued May 25, 1999, and Bremmer et al., U.S. Patent No. 6,210,749, THERMALLY STABLE DIELECTRIC COATINGS, issued April 3, 2001, the disclosures of all of which are incorporated by reference herein in their entirety. SiLK™ structures are increasingly being used to replace silicon oxide (SiO_2) as a dielectric because of its superior dielectric qualities, namely a dielectric constant of 2.65 compared with 4.1 for silicon oxide.

SiLK™ also demonstrates comparable toughness and greater resilience than the more brittle silicon oxide. Low dielectric constant in a material permits smaller

structures to be manufactured, which in turn permits closer packing of devices, faster speeds, and reduced crosstalk. The spin-on aromatic polymer has no fluorine in its composition, delivers superior planarization and gapfill, and is stable to 490°C. These properties have made SiLK™ popular for a variety of CMOS technologies demanding "low-K" interlayer dielectrics, such as copper/damascene and aluminum/tungsten technologies.

There are stress problems, however, in vias built with SiLK™ that do not occur with traditional silicon oxide vias. These stresses result in thermal cycle and in-line via-resistance shifts. There are at least three cases in which two-dimensional modeling has predicted high stresses in SiLK™ vias wherein thermal-cycle reliability failures have been directly correlated with the stress, namely (1) vias built in SiLK™ rather than silicon oxide, (2) vias built in SiLK™ wherein the subsequent level is executed in silicon oxide instead of SiLK™, and (3) vias built in SiLK™ wherein the next level is built in oxide compared with vias built in SiLK with a stress-relief layer prior to the subsequent level being built in oxide.

A stress problem with SiLK™ is illustrated in Figure 1a, showing a pair of semiconductor cross-sections depicting a typical prior art oxide embodiment A and a prior art SiLK™ embodiment B of a wafer structure, each comprising a base layer 1 of silicon substrate, atop of which is a silicon oxide base layer 2. Upon these are a first conductive line 3 and a second conductive line 4, usually made of copper metal, that join one another through a first via 5, which penetrates a level-separating nitride layer 6 that separates the first level 10 from a second level 20. In both drawings, third 30 and fourth 40 levels are shown, also separated by level-separating nitride layers 6, the third

level 30 comprising a silicon oxide layer 8 and the fourth level 40 comprising a silicon oxide layer 9 beneath a silicon nitride cap 11. Cross-section A shows a typical via 5 defined by a first level silicon oxide layer 7 and partly by the base silicon oxide layer 2. Cross-section B, however, shows a via 5 defined by a second level SiLK™ layer 7' and a base level SiLK™ structure 2'. The differences between the two structures may be seen in corresponding stress analysis images A', B', wherein darkened areas indicate high stresses. Comparing B' to A', it is apparent that the SiLK™ via structure creates much more stress and distortion than the traditional silicon oxide structure.

Referring to Figure 1b, plots 100 of via resistance shift in Ohms/link are shown for SiLK™ and for oxide, respectively. What is needed is a method suitable for making SiLK™ via structures with reduced stress.

SUMMARY OF THE INVENTION

A method, apparatus and system are provided for relieving stress in the via structures of semiconductor structures whenever a linewidth below a via is larger than a ground-rule, including providing a via at least as large as the groundrule, providing a landing pad above the via, providing a via bar in place of a via, slotting the metal linewidth below the via, or providing an oversize via with a sidewall spacer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure teaches a method, apparatus and system for relieving stress in the via structures of semiconductor structures whenever a linewidth below a

via is larger than a ground-rule, in accordance with the following exemplary figures, in which:

Figure 1a shows a schematic diagram of typical vias built in SiLK™ compared with vias built in oxide;

Figure 1b shows a graphical diagram for via resistance of typical vias built in SiLK™ compared with vias built in oxide;

Figure 2a shows a partial schematic diagram of vias built in SiLK™ in which the subsequent level is built in oxide as compared with the subsequent level being built in SiLK™ according to an embodiment of the present disclosure;

Figure 2b shows a graphical diagram of vias built in SiLK™ in which the subsequent level is built in oxide as compared with the subsequent level being built in SiLK™ according to an embodiment of the present disclosure;

Figure 3 shows a schematic diagram of vias built in SiLK™ in which the next level is built in oxide compared with vias built in SiLK™ with a stress-relief layer prior to the subsequent level being built in oxide according to an embodiment of the present disclosure;

Figure 4 shows a graphical diagram of stress-relief layer experimental results according to an embodiment of the present disclosure;

Figure 5 shows a schematic diagram of vias where a second conductive line varies in width according to an embodiment of the present disclosure;

Figure 6 shows a schematic diagram of vias where stress is substantially reduced by increasing via thickness according to an embodiment of the present disclosure; and

Figure 7 shows a schematic diagram of vias where the width of the first lower conductive line varies according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Some of the "8SF" SiLK™-related reliability issues, including thermal cycle and in-line via-resistance shift problems in particular, have been related to stress in the via as determined by stress modeling. There are at least three cases in which 2D stress modeling has predicted high stress in the via and in which thermal-cycle reliability failures have been correlated with this higher stress: 1) vias built in SiLK™ compared with vias built in oxide (Figure 1); 2) vias built in SiLK™ in which the subsequent level is built in oxide as compared with the subsequent level being built in SiLK™ (Figure 2a); and 3) vias built in SiLK™ in which the next level is built in oxide compared with vias built in SiLK™ with a stress-relief layer prior to the subsequent level being built in oxide (Figure 3).

Referring to Figure 2a, there is shown side-by-side a cross-section of a first embodiment of the invention C and the prior art SiLK™ embodiment B from Figure 1. As can be seen, the structures are identical except that in the inventive embodiment C the third level silicon oxide layer 8 has been replaced with a SiLK™ "stress-relief" layer 8'. Examination of the stress analysis images C' and B' plainly show a reduction of stress in the C structure over the prior art.

Referring to Figure 2b, there are shown histograms 200 that quantitatively demonstrate the superiority of the inventive embodiment C over the prior art SiLK™ embodiment B. Here, the via V1 with SiLK™ above passed thermal cycle tests, while

the via V2 with oxide above failed the same thermal cycle tests.

Referring to Figure 3, there is shown the prior art SiLK™ embodiment B next to five variants of the inventive embodiment C of the invention, wherein the stress-relieving SiLK™ layer 8' is varied in thickness from 1,000 Angstroms to 5,000 Angstroms in increments of 1,000 Angstroms. As can be seen in the stress analysis images C'-a through C'-e, there is no appreciable gain in stress relief above one thousand Angstroms. Hence, a 1,000 Angstrom SiLK™ stress-relief layer is all that is required to obtain substantially all of the benefits of the invention.

More recently, 3D stress modeling has been performed and has shown several interesting geometry-dependent stress phenomena. The first is that as the metal linewidth above a via increases, the stress in the via decreases (Figure 4). The second is that as the via-diameter increases, the stress in the via decreases (Figure 5). And third, as the linewidth below the via increases, the stress in the via also increases (Figure 6). These stress-modeling results suggest that a ground-rule line above a via with a large linewidth beneath the via has the highest possible stress in the via. Experimentally, we observe that our "plate-below" macro fails the easiest in terms of thermal-cycle reliability testing. As our modeling shows, by increasing the linewidth above a via, stress should be reduced. Experimentally we observe few or no failures with "plate-above" macros.

Referring to Figure 4, charts 400 of stress-relief layer experimental results illustrate significantly higher failure rates for SiLK™ with no stress-relief layer versus significantly lower failure rates for SiLK™ with the a stress-relief layer according to an embodiment of the present disclosure.

Referring to Figure 5, three dimensional images 500 show a via 5 joining a lower first 3 and upper second 4 conductive lines. The four images are identical except that the second conductive line varies in width. As can be seen, by increasing the width of the second upper conductive line, stress is substantially reduced.

Referring to Figure 6, three dimensional images 600 show a via joining a lower first 3 and upper second 4 conductive lines. Here, it is the diameter of the via 5 that varies. This demonstrates that stress is substantially reduced by increasing via thickness.

Referring to Figure 7, there is again shown a three dimensional image of a via joining a lower first 3 and upper second 4 conductive lines, but here it is the width of the first lower conductive line 3 that varies. Note that here, an increase in the lower conductive line 3, which is adjacent to the silicon oxide substrate layer 2, results in an increase in stress, not a decrease as may have been expected.

The above results allow formulation of inventive design rules for the manufacture of SiLK™ vias. In doing so, we refer to the "groundrule" width of a via, conductive line, or other structure. By "groundrule", we mean the smallest size available given the current technology at the time of manufacture. Unfortunately, lower conductive lines are generally larger than groundrule and therefore contribute to SiLK™ stress. The inventive design rules are as follows:

Whenever a linewidth below a via is larger than ground-rule:

1. *require a via larger than groundrule;*
2. *require a landing pad above the via (ground-rule or larger);*

3. *use a via bar in place of a via;*
4. *slot the metal linewidth below the via;*
5. *use an oversize via with sidewall spacer.*

Thus, embodiments of the present disclosure impose specific design-rules for copper metallization built in SiLK so that stress in the via is minimized. With such an approach, a reliable copper metallization with SiLK can be realized. Improvements in stress-relief will be realized by implementing any number of the above design rules.

It is to be understood that all physical quantities disclosed herein, unless explicitly indicated otherwise, are not to be construed as exactly equal to the quantity disclosed, but rather as about equal to the quantity disclosed. Further, the mere absence of a qualifier such as "about" or the like, is not to be construed as an explicit indication that any such disclosed physical quantity is an exact quantity, irrespective of whether such qualifiers are used with respect to any other physical quantities disclosed herein.

While preferred embodiments have been shown and described, various modifications and substitutions may be made thereto without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the present invention has been described by way of illustration only, and such illustrations and embodiments as have been disclosed herein are not to be construed as limiting to the claims.

What is claimed is:

1. A method of relieving stress in the via structures of semiconductor structures whenever a linewidth below a via is larger than a ground-rule, the method comprising at least one of:

providing a via at least as large as the groundrule;

providing a landing pad above the via;

providing a via bar in place of a via;

slotting the metal linewidth below the via; and

providing an oversize via with a sidewall spacer.

2. A method as defined in Claim 1 wherein the semiconductor structures are formed from SiLK™.

3. A method as defined in Claim 1 wherein the via is larger than the groundrule.

4. A method as defined in Claim 1 wherein the landing pad above the via is at least as large as the groundrule.

5. A method as defined in Claim 1 wherein the via is formed by chemical vapor deposition.

6. A method as defined in Claim 1 wherein the via is formed by masking a

SiLK™ deposition.

7. A method as defined in Claim 1 wherein the via is formed by etching.

8. A method as defined in Claim 1 wherein the landing pad is formed from a conductive material.

9. A method as defined in Claim 1 wherein the sidewall spacers are non-conductive.

10. A semiconductor structure having a via with reduced stress where a linewidth below the via is larger than a ground-rule, the semiconductor comprising at least one of:

a via at least as large as the groundrule;

a landing pad above the via;

a via bar in place of the via;

a slot in the metal linewidth below the via; and

an oversize via with a sidewall spacer.

11. A semiconductor structure as defined in Claim 10 wherein the semiconductor structure comprises SiLK™.

12. A semiconductor structure as defined in Claim 10 wherein the via is larger than the groundrule.

13. A semiconductor structure as defined in Claim 10 wherein the landing pad above the via is at least as large as the groundrule.

14. A semiconductor structure as defined in Claim 10 wherein the via is formed by chemical vapor deposition.

15. A semiconductor structure as defined in Claim 10 wherein the via is formed by masking a SiLK™ deposition.

16. A semiconductor structure as defined in Claim 10 wherein the via is formed by etching.

17. A semiconductor structure as defined in Claim 10 wherein the landing pad comprises a conductive material.

18. A semiconductor structure as defined in Claim 10 wherein the sidewall spacers are non-conductive.

19. A semiconductor manufacturing system for manufacturing a semiconductor structure having a via with reduced stress where a linewidth below the via is larger than a ground-rule, the semiconductor manufacturing system comprising at least one of:

via means for providing a via at least as large as the groundrule;

pad means for providing a landing pad above the via;

bar means for providing a via bar in place of a via;

slot means for slotting the metal linewidth below the via; and

spacer means for providing an oversize via with a sidewall spacer.

20. A semiconductor manufacturing system as defined in Claim 19 wherein the semiconductor structures are formed from SiLK™.

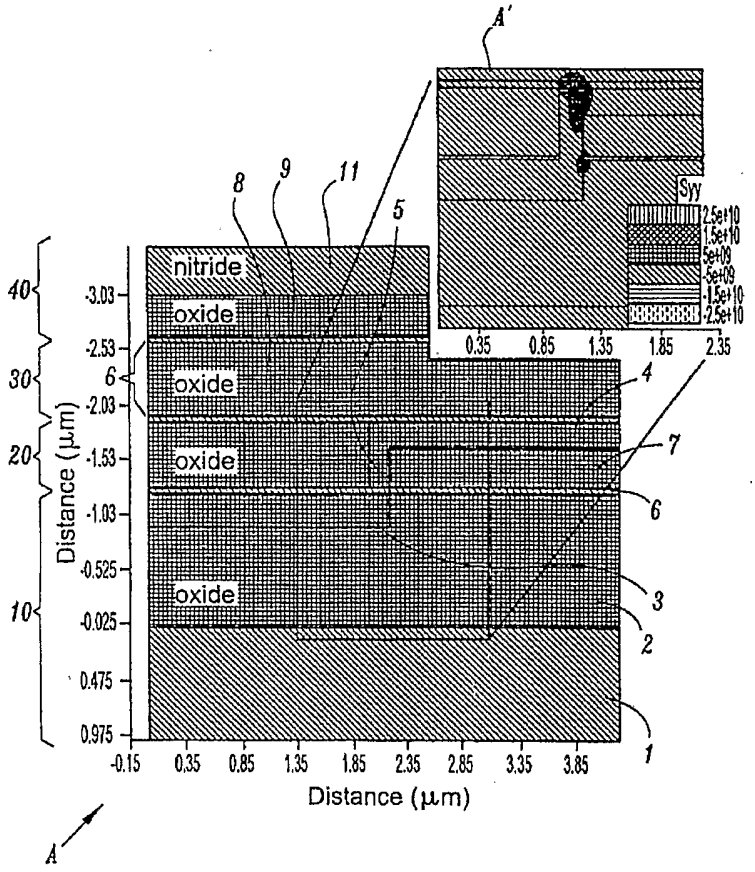
A'
Syy
2.5e+10
1.5e+10
5e+09
-5e+09
-1.5e+10
-2.5e+10
0.35
0.85
1.35
1.85
2.35
8
9
11
5
nitride
oxide
oxide
oxide
oxide
6
4
7
6
3
2
1
40
30
20
10
Distance (µm)
-3.03
-2.53
-2.03
-1.53
-1.03
-0.525
-0.025
0.475
0.975
-0.15
0.35
0.85
1.35
1.85
2.35
2.85
3.35
3.85
Distance (µm)
A

FIG. 1a-1

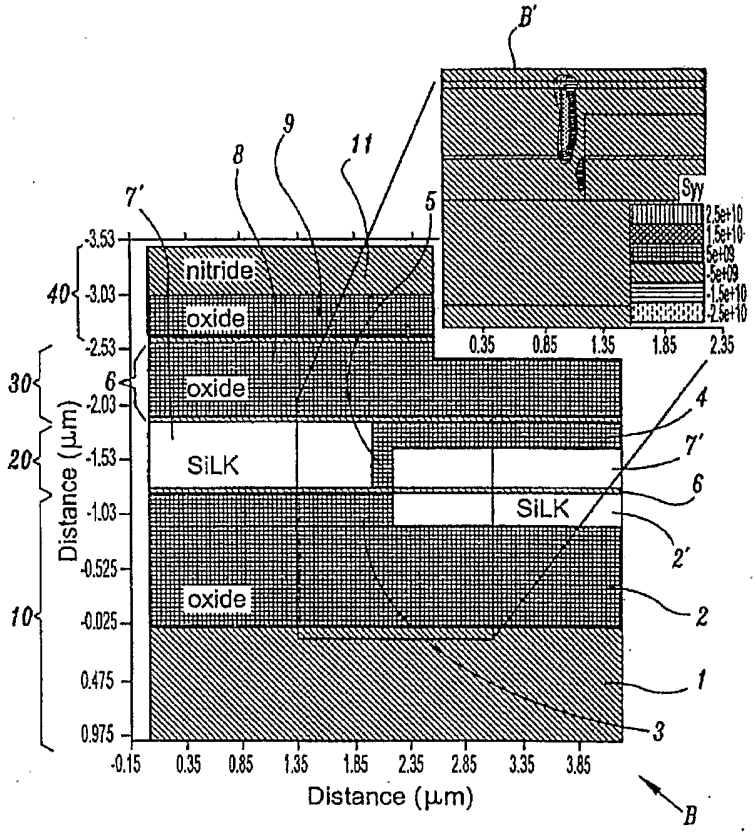
B'
9
8
11
7'
5
Syy
2.5e+10
1.5e+10
5e+09
-5e+09
-1.5e+10
-2.5e+10
0.35
0.85
1.35
1.85
2.35
nitride
oxide
oxide
SiLK
SiLK
oxide
40
30
20
10
6
4
7'
6
2'
2
1
3
B
-3.53
-3.03
-2.53
-2.03
-1.53
-1.03
-0.525
-0.025
0.475
0.975
Distance (µm)
-0.15
0.35
0.85
1.35
1.85
2.35
2.85
3.35
3.85
Distance (µm)

FIG. 1a-2

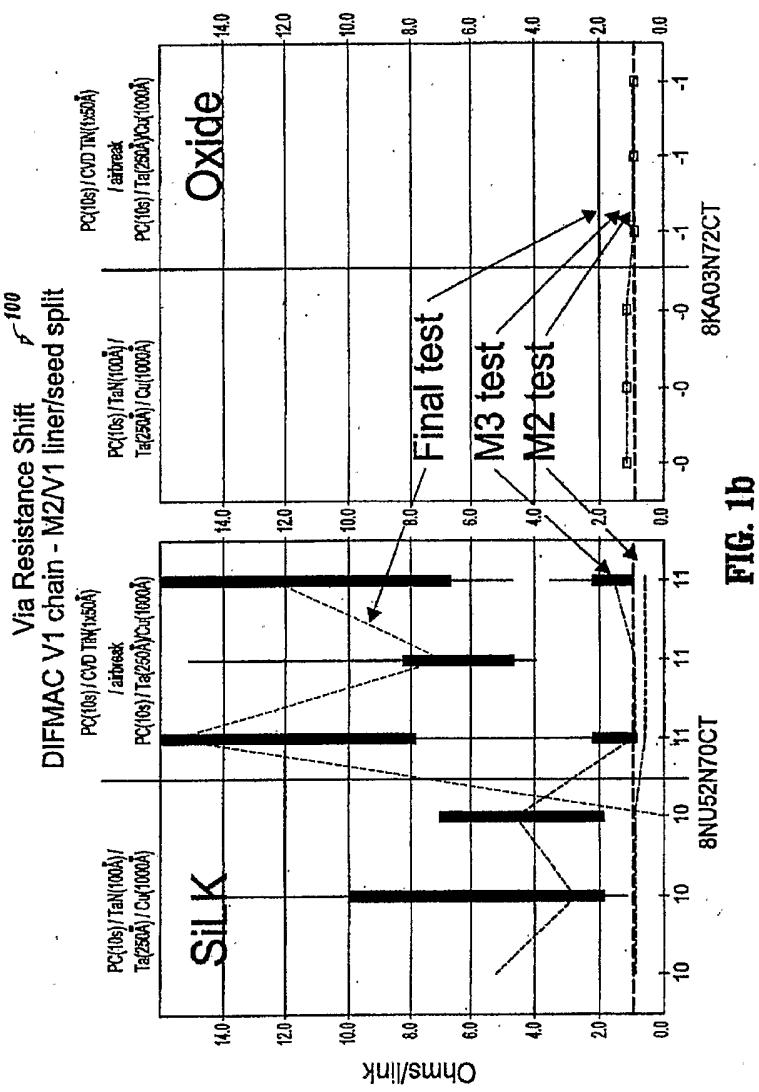
Via Resistance Shift
DIFMAC V1 chain - M2/V1 liner/seed split
100
SiLK
Oxide
Final test
M3 test
M2 test
Ohms/link
8NU52N70CT
8KA03N72CT

FIG. 1b

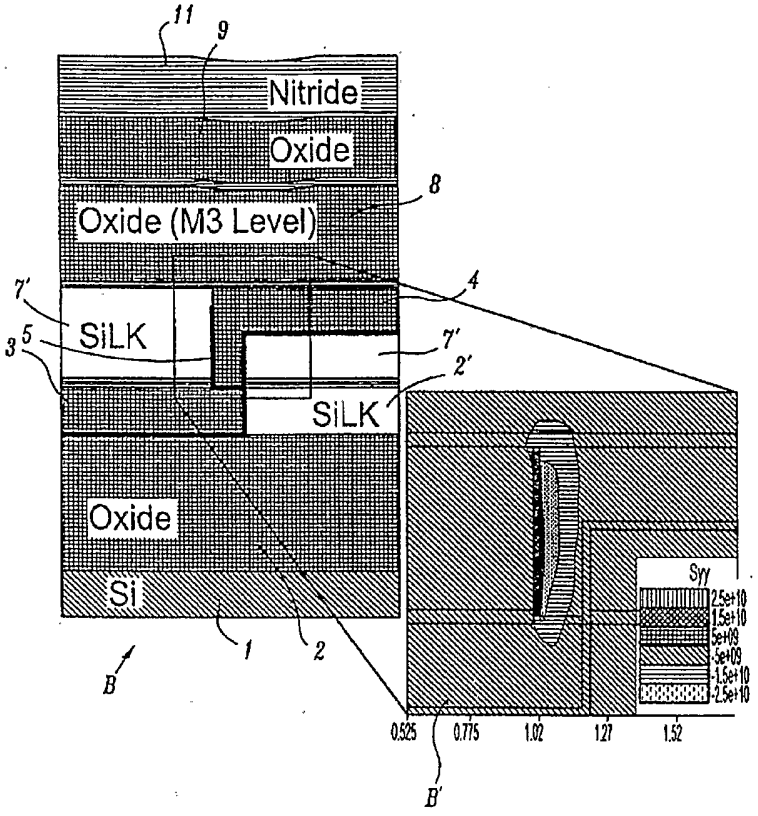
11
9
Nitride
Oxide
8
Oxide (M3 Level)
4
7'
SiLK
3
5
7'
2'
SiLK
Oxide
Si
1
2
B
B'
Syy
2.5e+10
1.5e+10
5e+09
-5e+09
-1.5e+10
-2.5e+10
0.525
0.775
1.02
1.27
1.52

FIG. 2a-1

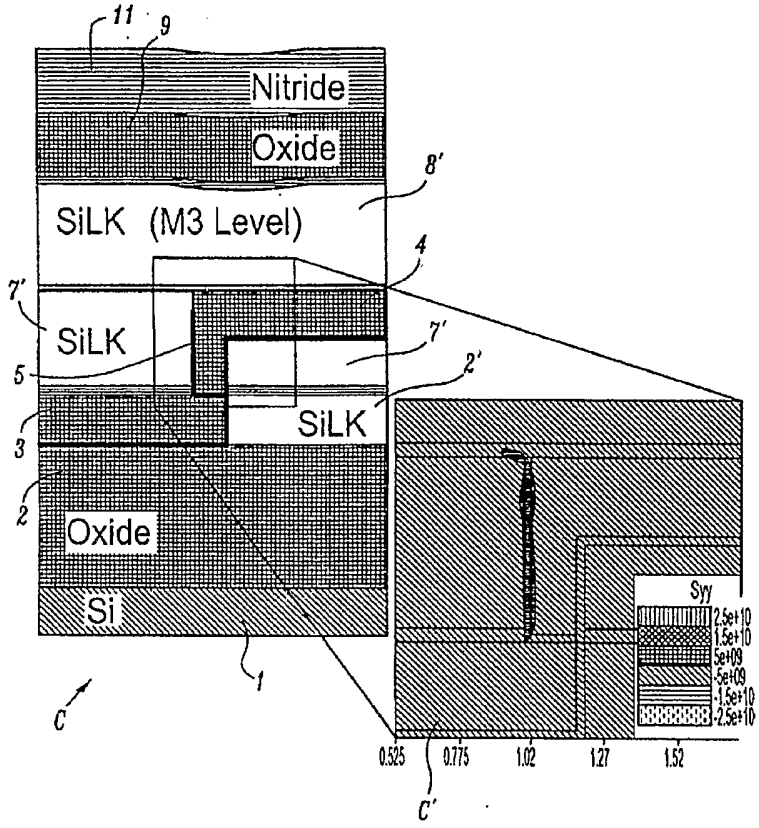
11
9
Nitride
Oxide
8'
SiLK (M3 Level)
4
7'
SiLK
7'
5
2'
SiLK
3
2
Oxide
Si
1
C
C'
Syy
2.5e+10
1.5e+10
5e+09
-5e+09
-1.5e+10
-2.5e+10
0.525
0.775
1.02
1.27
1.52

FIG. 2a-2

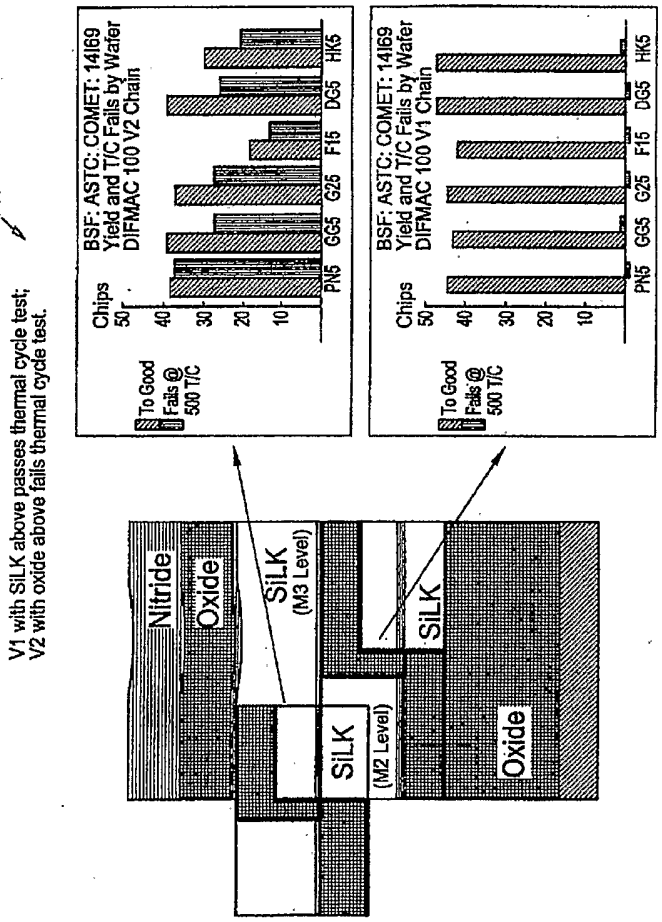
200
V1 with SiLK above passes thermal cycle test;
V2 with oxide above fails thermal cycle test.
BSF: ASTC: COMET: 14169
Yield and T/C Fails by Wafer
DIFMAC 100 V2 Chain
Chips
To Good
Fails @ 500 T/C
PN5 GG5 G25 F15 DG5 HK5
BSF: ASTC: COMET: 14169
Yield and T/C Fails by Wafer
DIFMAC 100 V1 Chain
Nitride
Oxide
SiLK
(M3 Level)
SiLK
(M2 Level)
SiLK
Oxide

FIG. 2b

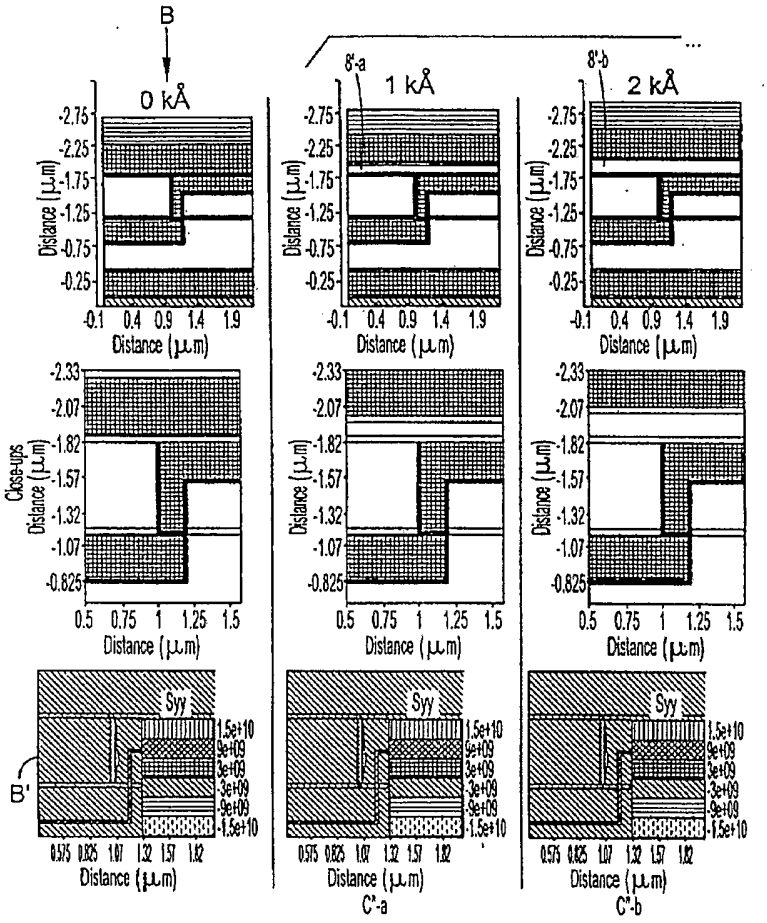

FIG. 3-1

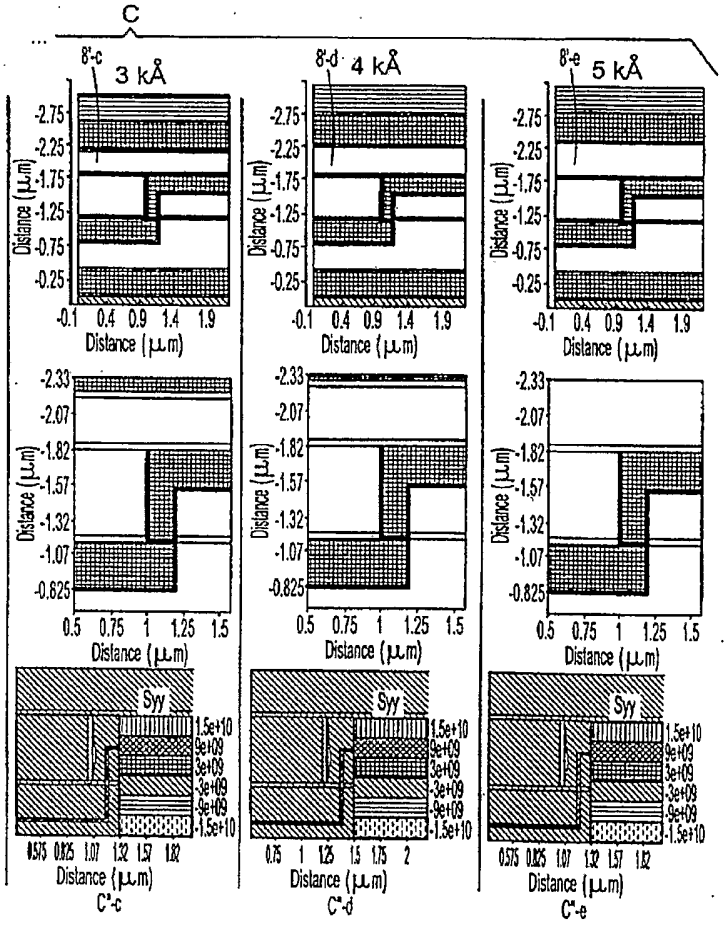

FIG. 3-2

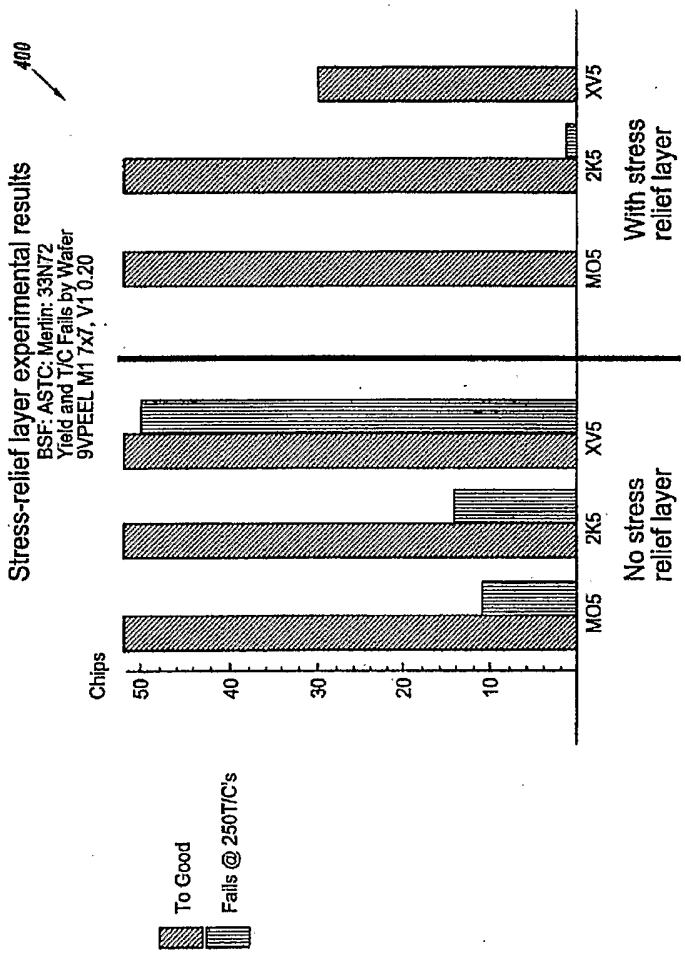
400
Stress-relief layer experimental results
BSF: ASTC: Merlin: 33N72
Yield and T/C Fails by Wafer
9VPEEL M1 7x7, V1 0.20
Chips
50
40
30
20
10
MO5
2K5
XV5
No stress relief layer
MO5
2K5
XV5
With stress relief layer
To Good
Fails @ 250T/C's

FIG. 4

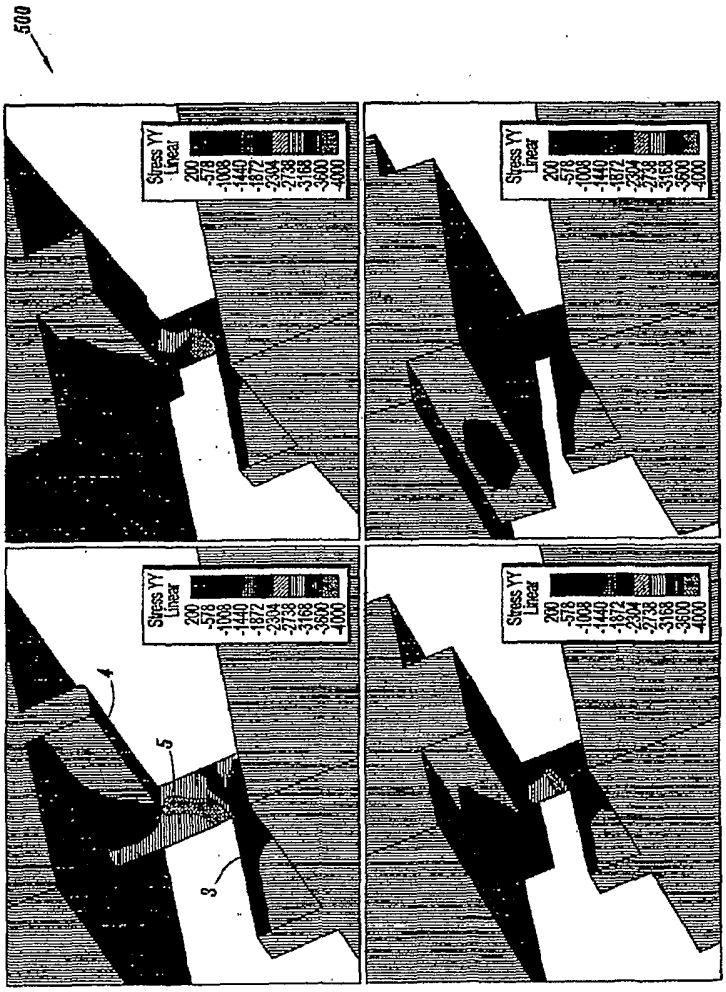
500
Stress YY
Linear
200
-576
-1008
-1440
-1872
-2304
-2736
-3168
-3600
-4000
4
5
3

FIG. 5

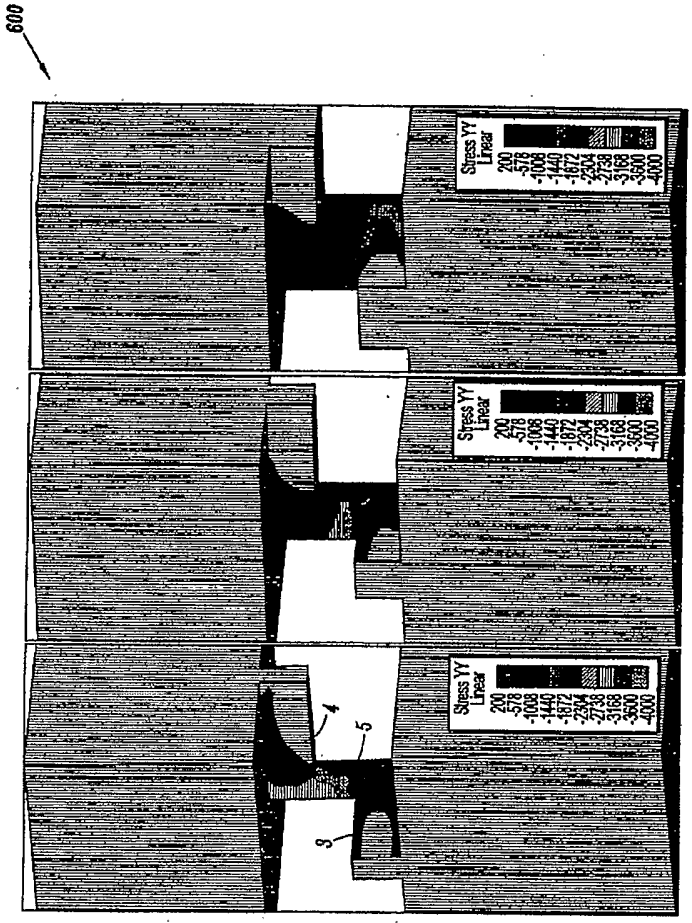
600
Stress YY
Linear
200
-576
-1008
-1440
-1872
-2304
-2736
-3168
-3600
-4000
3
4
5

FIG. 6

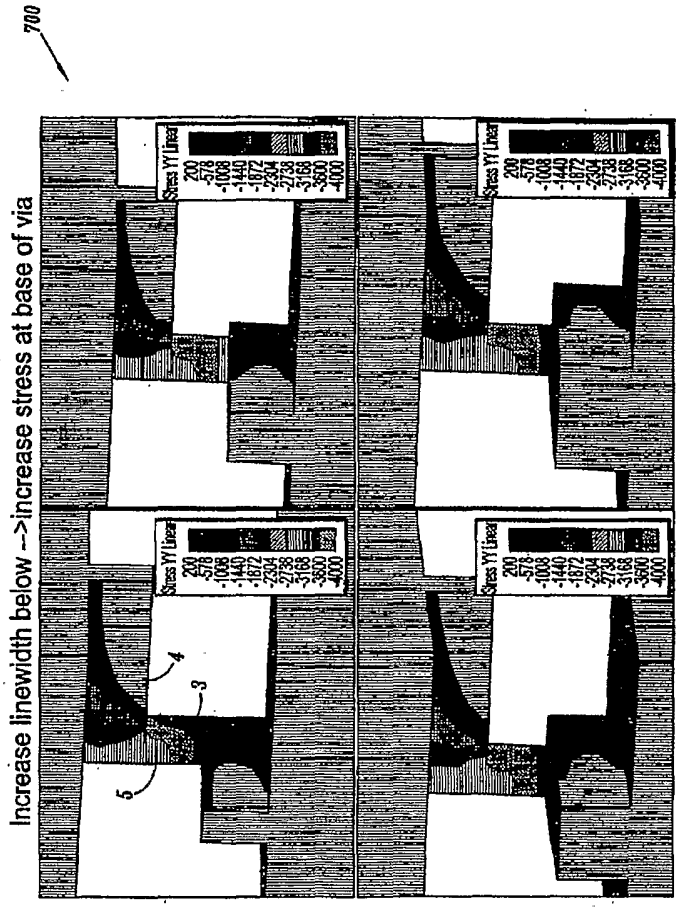
700
Increase linewidth below -->increase stress at base of via
Stress YY Linear
200
-576
-1008
-1440
-1872
-2304
-2736
-3168
-3600
-4000
3
4
5

FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/050778

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L23/522

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/042580 A1 (STETTER MICHAEL ET AL) 6 March 2003 (2003-03-06) the whole document _____	1-5,7,8, 10-14, 16,17

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 September 2004	13/09/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ploner, G

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2004/050778

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 6,9,15,18,19,20
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 6,9,15,18,19,20

1. In claim 1 the method steps

-) providing a via bar in place of a via;
-) slotting the metal linewidth below the via;
-) providing an oversize via with a sidewall spacer;

as well as the corresponding device features in claim 10 are unclear because

a) the difference between a "via bar" and a conventional via is obscure;
b) the step "slotting the linewidth" is incomprehensible;
c) it is unclear what represents an "oversize" via, relative to which other feature the via is "oversized" and to which extent an "oversize" via is different from a via that is larger than the design rule.

As no details regarding the above unclear method steps and/or features are disclosed in the description, an interpretation of the claims in the light of the description is impossible. Consequently, claims 1 and 10 are so unclear (Article 6 PCT) and so insufficiently disclosed (Article 5 PCT) that a meaningful comparison with the state of the art is impossible.

The search relating to claims 1 and 10 has therefore been restricted to the method steps

-) providing a via at least as large as the ground rule (i.e. having an arbitrary width);
-) providing a landing pad above the via;

and to the corresponding device features in claim 10.

2. For the same reasons as above (unclarity combined with no disclosure), the method steps and corresponding device features of dependent claims 6, 9, 15 and 18 cannot be made the subject of a meaningful search and therefore have not been searched at all.

3. The apparatus claims 19, 20 relate to a "manufacturing system" comprising "via means", "pad means", "bar means", "slot means" or "spacer means". It is obscure which components of a "manufacturing system" said "means" relate to. The description contains no information at all which could be used to interpret claims 19 and 20.

Therefore, claims 19 and 20 are so unclear (Article 6 PCT) and so insufficiently disclosed (Article 5 PCT) that a meaningful comparison with the prior art is impossible. No search can therefore be carried out with respect to these claims.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2004/050778

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003042580 A1	06-03-2003	WO 02103790 A1	27-12-2002