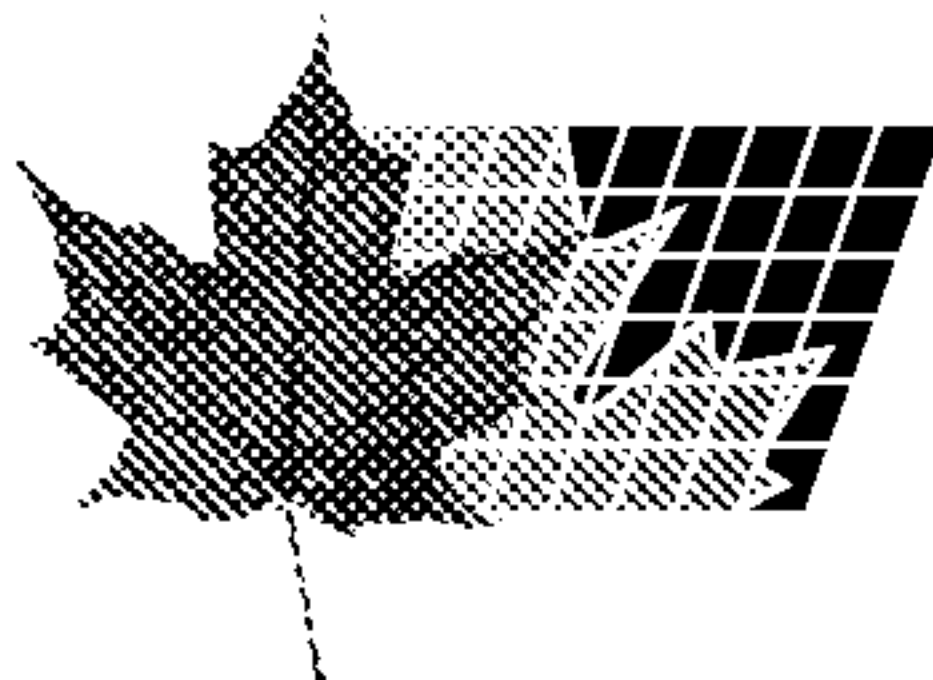




(22) 1998/01/13

(43) 1998/07/14

(45) 2001/05/01

(72) LEE, Kab-Keun, KR

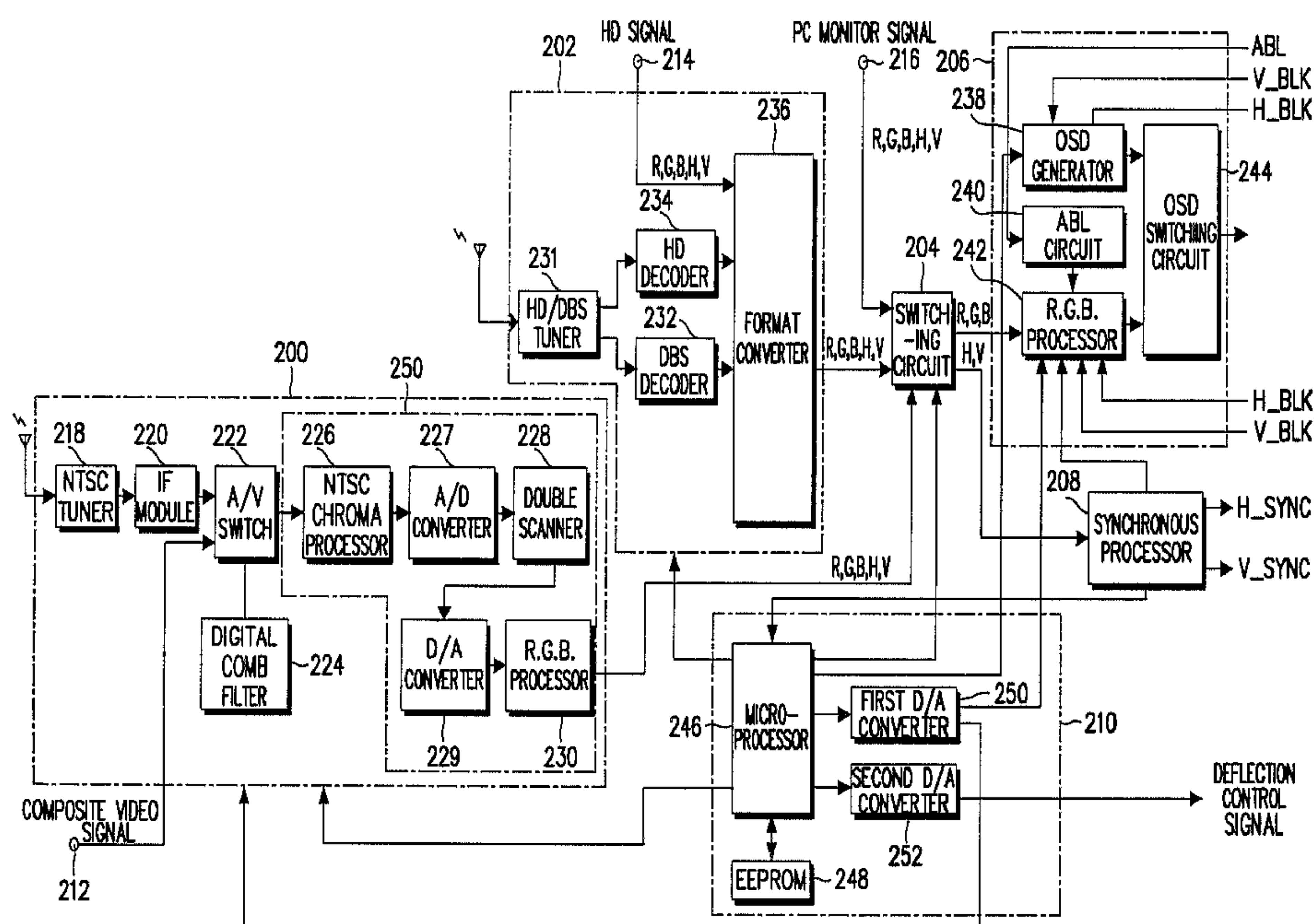
(73) SAMSUNG ELECTRONICS CO., LTD., KR

(51) Int.Cl.⁶ H04N 7/01, H04N 5/44, G06F 3/14

(30) 1997/01/14 (882/1997) KR

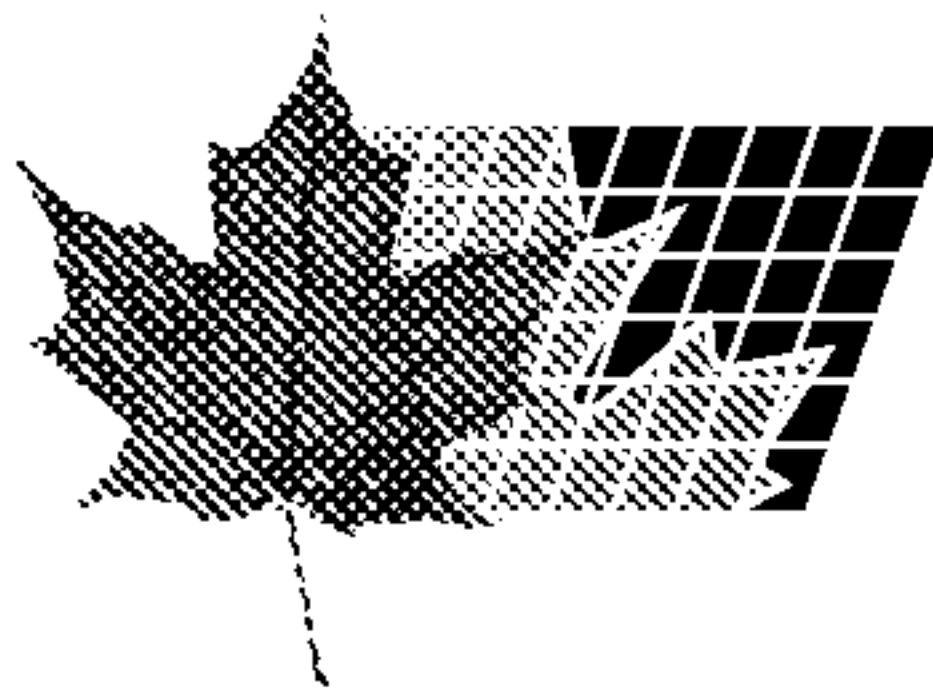
(54) **TELEVISEUR MULTISYSTEME UTILISABLE COMME
MONITEUR D'ORDINATEUR PERSONNEL**

(54) **MULTISYSTEM TELEVISION WHICH IS USABLE AS
MONITOR OF PERSONAL COMPUTER**



(57) L'invention est un téléviseur multisystème utilisable comme moniteur ou comme ordinateur personnel (PC). Ce téléviseur comprend un processeur à signaux NTSC servant à décomposer les signaux de diffusion NTSC en un signal de luminance et un signal de chrominance et à produire des signaux couleur à double balayage; un processeur à signaux de diffusion numériques servant à décoder les signaux de diffusion DBS (Direct Broadcasting Satellite) et les signaux de diffusion haute définition HD et à convertir en mode de visualisation courant pour les afficher les signaux HD et DBS décodés et les signaux HD de sources externes; un circuit de commutation servant à produire sélectivement un signal de moniteur reçu d'un PC, le signal de sortie du processeur à signaux de diffusion numériques et le signal

(57) A multisystem TV which is usable as a monitor of a personal computer (PC). The multisystem television includes an NTSC signal processor for separating an NTSC broadcasting signal into a luminance signal and a chrominance signal and generating double-scanned original color signals; a digital broadcasting signal processor for decoding a DBS (Direct Broadcasting Satellite) broadcasting receiving signal and an HD (High Definition) broadcasting receiving signal and converting a signal corresponding to a current viewing mode out of the decoded HD signal, the decoded DBS signal and an external HD signal into a display type; a switching circuit for selectively generating one of a PC monitor signal received from a PC, an output signal of the digital broadcasting signal processor and an output signal of the



(11) (21) (C) **2,226,792**

(22) 1998/01/13

(43) 1998/07/14

(45) 2001/05/01

de sortie du processeur à signaux NTSC selon le mode de visualisation du moment; un circuit de sortie vidéo permettant de régler la qualité de l'image du signal de sortie du circuit de commutation avant de le transmettre au tube image; un contrôleur servant à contrôler le traitement effectué par le processeur à signaux NTSC, le processeur à signaux de diffusion numériques et le circuit de sortie vidéo, la commutation effectuée par le circuit de commutation et la déviation dans le tube image selon le mode de visualisation du moment; et un processeur synchrone servant à traiter les signaux de synchronisation produits par le circuit de commutation et à transmettre les signaux traités au circuit de sortie vidéo et au contrôleur.

NTSC signal processor according to the current viewing mode; a video output circuit for adjusting picture quality of a signal generated from the switching circuit so as to be supplied to a picture tube; a controller for controlling the signal processing of the NTSC signal processor, digital broadcasting. signal processor and video output circuit, the switching of the switching circuit, and the deflection of the picture tube, according to the current viewing mode; and a synchronous processor for processing a synchronizing signal generated from the switching circuit and supplying the processed signal to the video output circuit and the controller .

ABSTRACT OF THE DISCLOSURE

A multisystem TV which is usable as a monitor of a personal computer (PC). The multisystem television includes an NTSC signal processor for separating an NTSC broadcasting signal into a luminance signal and a chrominance signal and generating double-scanned original color signals; a digital broadcasting signal processor for decoding a DBS (Direct Broadcasting Satellite) broadcasting receiving signal and an HD (High Definition) broadcasting receiving signal and converting a signal corresponding to a current viewing mode out of the decoded HD signal, the decoded DBS signal and an external HD signal into a display type; a switching circuit for selectively generating one of a PC monitor signal received from a PC, an output signal of the digital broadcasting signal processor and an output signal of the NTSC signal processor according to the current viewing mode; a video output circuit for adjusting picture quality of a signal generated from the switching circuit so as to be supplied to a picture tube; a controller for controlling the signal processing of the NTSC signal processor, digital broadcasting signal processor and video output circuit, the switching of the switching circuit, and the deflection of the picture tube, according to the current viewing mode; and a synchronous processor for processing a synchronizing signal generated from the switching circuit and supplying the processed signal to the video output circuit and the

controller.

MULTISYSTEM TELEVISION WHICH IS USABLE AS MONITOR OF
PERSONAL COMPUTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a television (TV), and more particularly, to a TV which is usable as a monitor of a personal computer (PC).

2. Description of the Related Art

To use a TV for watching NTSC (National Television System Committee) broadcasting as a monitor of a PC or to watch DBS (Direct Broadcasting Satellite) broadcasting, there is needed additional equipment.

Referring to FIG. 1, a DBS receiver 102 and a PC/NTSC converter 104 are additionally connected to a general TV 100 coupled to an NTSC receiving antenna 101. Then the TV 100 can perform a general broadcasting receiving function, a DBS receiving function and a PC monitor function. That is, in order to watch the DBS broadcasting, the DBS receiver 102 is installed at the TV 100 to convert a satellite broadcasting signal into a signal suitable for NTSC RF (Radio Frequency) standard. The converted signal is applied to the TV 100

through its antenna input terminal. Alternatively, a base band composite video signal generated from the DBS receiver 102 may be applied to the TV through its external input terminal. In order to perform the PC monitor function, there is needed the PC/NTSC converter 104 for converting a PC monitor signal into an NTSC signal which can be displayed in the TV 100. If the output of the PC/NTSC converter 104 is connected to the external input terminal of the TV 100, the PC monitor signal can be displayed in the TV 100.

However, even if the DBS receiver 102 for watching such DBS broadcasting is installed, a digital DBS signal is converted into an analog NTSC signal and analog signal processing is implemented. During such processes, the characteristic of the DBS signal may be deteriorated. Further, if the TV is used as the PC monitor, the resolution, 800 x 600 for example, of the output of the PC monitor is lowered to the resolution, 640 x 480 for example, of the NTSC system. Therefore, it is difficult to receive future HDTV (high definition TV) broadcasting.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a multisystem TV which can be used as a PC monitor and watch NTSC broadcasting, DBS broadcasting and HDTV broadcasting.

To achieve the above and other objects, there is provided a multisystem TV including an NTSC signal processor for separating an NTSC broadcasting signal into a luminance signal and a chrominance signal and generating double-scanned original color signals; a digital broadcasting signal processor for decoding a DBS (Direct Broadcasting Satellite) broadcasting receiving signal and an HD (High Definition) broadcasting receiving signal and converting a signal corresponding to a current viewing mode out of the decoded HD signal, the decoded DBS signal and an external HD signal into a display type; a switching circuit for selectively generating one of a PC monitor signal received from a PC, an output signal of the digital broadcasting signal processor and an output signal of the NTSC signal processor according to the current viewing mode; a video output circuit for adjusting picture quality of a signal generated from the switching circuit so as to be supplied to a picture tube; a controller for controlling the signal processing of the NTSC signal processor, digital broadcasting signal processor and video output circuit, the switching of the switching circuit, and the deflection of the picture tube, according to the current viewing mode; and a synchronous processor for processing a synchronizing signal generated from the switching circuit and supplying the processed signal to the video output circuit and the controller.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages and features of the present invention will become better understood by reference to the following detailed description of the preferred embodiment when considered in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of a conventional multisystem TV;

FIG. 2 is a block diagram of a multisystem TV in accordance with a preferred embodiment of the present invention; and

FIG. 3 is a flow chart showing a deflection control data output process executed by a microprocessor 246 illustrated in FIG. 2 according to a viewing mode.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, numerous specific details are set forth to provide a more thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known functions or constructions are not described in detail since they would obscure the present invention in unnecessary detail.

Referring to FIG. 2, a multisystem TV according to the present invention includes an NTSC signal processor 200, a digital broadcasting signal processor 202, a switching circuit 204, a video output circuit 206, a synchronous processor 208 and a controller 210. For these constructions, typically used circuits and integrated circuits are employed.

A microprocessor 246 of the controller 210 controls the operation of the NTSC signal processor 200, digital broadcasting signal processor 202, switching circuit 204 and video output circuit 206, according to a current viewing mode among 4 viewing modes of an NTSC broadcasting receiving mode, a DBS broadcasting receiving mode, an HDTV broadcasting receiving mode and a PC monitor mode, and controls the overall operation of a multisystem display unit.

The NTSC signal processor 200 includes an NTSC tuner 218, an intermediate frequency (IF) module 220, an audio/video (A/V) switch 222, a digital comb filter 224 and a double scanning circuit 250. The double scanning circuit 250 has an NTSC chroma processor 226, an analog-to-digital (A/D) converter 227, a double scanner 228, a digital-to-analog (D/A) converter 229, and an R.G.B. processor 230. The NTSC signal processor 200 separates an NTSC RF signal

received through an antenna or a composite video signal received through an external input terminal 212 into a luminance signal and a chrominance signal. Thereafter, the NTSC signal processor 200 converts the separated signals into color difference signals and double-scans the color difference signals.

In more detail, the NTSC tuner 218 selects an NTSC broadcasting receiving signal by the control of the controller 210 and generates an IF signal. The IF module 220 processes the IF signal generated from the NTSC tuner 218 and generates a base band video signal. The A/V switch 222 selects either the base band video signal generated from the IF module or the composite video signal received through the external input terminal 212. The external composite video signal is an NTSC signal. The digital comb filter 224 connected to the A/V switch 222 separates a signal selected by the A/V switch 222 into the luminance signal and the chrominance signal. The separated luminance signal and chrominance signals are applied to the NTSC chroma processor 226. In this case, the composite video signal received through the external input terminal 212 may be a super video signal. Since the luminance signal of the super video signal and the chrominance signal thereof has already been separated, if the A/V switch selects the super video signal of the external composite video signal, the super video

signal is directly supplied to the NTSC chroma processor 226 without passing through the digital comb filter 224. The NTSC chroma processor 226 processes a signal generated from the A/V switch 222 and converts the processed signal into the color difference signals, that is, Y, R-Y and B-Y. The A/D converter 227 converts the color difference signals Y, R-Y and B-Y into digital signals. The double scanner 228 double-scans the color difference signals of the digital form. The D/A converter 229 converts the double-scanned digital color difference signals into double-scanned analog color difference signals. The R.G.B. processor 230 converts the double-scanned analog color difference signals into original color signals R, G and B. The original color signals R, G and B are applied to the switching circuit 204 together with vertical and horizontal synchronizing signals H and V. By the double scanning conversion, horizontal and vertical deflection frequencies of 15.75 KHz-60 KHz are converted into 31.5 KHz-60 KHz.

The digital broadcasting signal processor 202 includes an HD/DBS tuner 231, an HD decoder 234, a DBS decoder 232 and a format converter 236. The digital broadcasting signal processor 202 decodes a DBS broadcasting receiving signal and an HD broadcasting receiving signal, and converts a signal corresponding to a current viewing mode out of an external HD signal received through an external input

terminal 214, the decoded HD signal and the decoded DBS signal into a display type by the control of the controller 210.

The HD/DBS tuner 231 selects a signal corresponding to the current viewing mode out of the HD broadcasting receiving signal and the DBS broadcasting receiving signal. The HD decoder 234 decodes the HD signal selected by the HD/DBS tuner 231 and generates a digital HD signal. The DBS decoder 232 decodes the DBS signal selected by the HD/DBS tuner 231 and generates a digital DBS signal. The format converter 236 converts a signal corresponding to the current viewing mode out of the HD signal received through the external input terminal 214, and the digital HD signal and the digital DBS signal decoded from the HD and DBS decoders 234 and 232 into the display type by the control of the controller 210. The format converter 236 consists of a format converter IC, a memory, a timing generator, and a D/A converter. The external HD signal is supplied to the format converter 236 together with the original color signals R, G and B and the horizontal and vertical synchronizing signals H and V. An example of the display format is that the horizontal frequency is 45 KHz and the vertical frequency is 60 Hz. The converted original color signals R, G and B and horizontal and vertical synchronizing signals H and V are applied to the switching circuit 204.

The switching circuit 204 generates a signal corresponding to the current viewing mode out of a signal generated from the NTSC signal processor 200, a PC monitor signal received from a PC through a PC monitor input terminal 216 and a signal generated from the format converter 236 by the control of the controller 210. The PC monitor input terminal 216 uses an RS-232C interface. The PC monitor signal received through the PC monitor input terminal 216 is supplied to the switching circuit 204 together with the original color signals R, G and B and the horizontal and vertical synchronizing signals H and V.

The video output circuit 206 includes an OSD (On Screen Display) generator 238, an ABL (Automatic Beam Limit) circuit 240, an R.G.B. processor 242 and an OSD switching circuit 244. The video output circuit 206 adjusts picture quality of the signals R, G and B generated from the switching circuit 204 by the control of the controller 210 so as to be supplied to a picture tube (not shown).

The OSD generator 238 generates an OSD signal in synchronization with horizontal and vertical blanking signals H_BLK and V_BLK applied from a deflection circuit of the picture tube by the control of the controller 210. The R.G.B. processor 242 receives the original color signals R, G and B from the switching circuit 204, the horizontal and

vertical blanking signals H_BLK and V_BLK from the deflection circuit of the picture tube and a synchronizing signal from the synchronous processor 208, and adjusts the picture quality such as contrast, brightness and white balance with respect to the original color signals R, G and B by the control of the controller 210. The ABL circuit 240 controls the ABL of a signal generated from the R.G.B. processor 242 according to an ABL signal applied from the reflection circuit of the picture tube. The OSD switching circuit 244 switches signals generated from the OSD generator 238 and the R.G.B. processor 242 and supplies the switched signal to the picture tube.

The synchronous processor 208 processes the horizontal and vertical synchronizing signals H and V generated from the switching circuit 204 so as to be converted into horizontal and vertical synchronizing signals H_SYNC and V_SYNC of a constant form, and supplies a clamp signal to the R.G.B. processor 242. The synchronous processor 208 also supplies the horizontal and vertical synchronizing signals H and V to the microprocessor 246 of the controller 210.

The controller 210 includes the microprocessor 246, an EEPROM (Electrically Erasable and Programmable Read Only Memory) 248, and first and second D/A converters 250 and 252. The controller 210 controls the signal processing of

the NTSC signal processor 200, the digital broadcasting signal processor 202 and the video output circuit 206, the switching of the switching circuit 204, and the deflection of the picture tube by the microprocessor 246 according to the current viewing mode. The EEPROM 248 stores control data, that is, picture quality control data, deflection control data and other data according to each viewing mode of the general broadcasting receiving mode, the DBS broadcasting receiving mode, the HDTV broadcasting receiving mode and the PC monitor mode. The microprocessor 246 controls the operation of each mode by reading the control data from the EEPROM 248. The first and second D/A converters 250 and 252 are connected to the microprocessor 246 through an IIC bus. The first D/A converter 250 converts digital data into an analog signal in order to adjust the picture quality and supplies the analog signal to the NTSC signal processor 200 and the R.G.B. processor 242. The second D/A converter 252 converts the deflection control data generated from the microprocessor 246 into an analog deflection control signal and supplies the analog deflection control signal to the deflection circuit of the picture tube.

The operation of 4 viewing modes of the multisystem TV having the above-described configuration will be described hereinafter in detail.

In the NTSC broadcasting receiving mode, a desired channel is selected from the NTSC tuner 218 by the control of the microprocessor 246. The IF signal is applied to the IF module 220. The base band video signal is supplied to the A/V switch 222. If it is desired to receive the NTSC composite video signal from the exterior, the external composite video signal is applied to the A/V switch 222 through the external input terminal 212. The A/V switch 222 selectively generates the base band signal generated from the IF module 222 or the external composite video signal received through the external input terminal 212. The signal generated from the A/V switch 222 is separated into the luminance signal and the chrominance signal by the digital comb filter 224. The A/D converter 227 converts the color difference signals Y, R-Y and B-Y into the digital signals. The double scanner 228 double-scans the digital color difference signals. The double-scanned digital color difference signals are converted into the double-scanned analog signals by the D/A converter 229. The doubled analog color difference signals are supplied to the R.G.B. processor 230 and then converted into the original color signals R, G and B. The original color signals R, G and B are supplied to the switching circuit 204 together with the horizontal and vertical synchronizing signals H and V. The original color signals R, G and B and the horizontal and vertical synchronizing signals H and V are selected by the

switching of the switching circuit 204. The original color signals R, G and B are applied to the R.G.B. processor 242, and the horizontal and vertical synchronizing signals H and V are supplied to the synchronous processor 208.

The synchronous processor 208 converts the horizontal and vertical synchronizing signals H and V into the horizontal and vertical synchronizing signals H_SYNC and V_SYNC of a constant form, and supplies the clamp signal to the R.G.B. processor 242. The synchronous processor 208 provides the horizontal and vertical synchronizing signals H and V to the microprocessor 246 as a reference signal for judging an input signal when the multisystem TV operates as the PC monitor mode. The R.G.B. processor 242 adjusts the picture quality of the contrast, brightness and white balance according to the signal applied from the first D/A converter 250. The output of the R.G.B. processor 242 is applied to the OSD switching circuit 244. The control of the ABL is performed by the ABL circuit 240. The OSD signal corresponding to the horizontal and vertical frequencies is generated from the OSD generator 238 and supplied to the OSD switching circuit 244. Signals generated from the OSD switching circuit 244 are the original color signals R, G and B including OSD information and applied to a cathode of the picture tube through a final output amplifying terminals. Therefore, the NTSC broadcasting or an image by

external input is displayed on a screen.

In the DBS broadcasting receiving mode, the DBS broadcasting signal is supplied to the HD/DBS tuner 231 and decoded by the DBS decoder 232. The decoded DBS signal is converted into the display format by the format converter 236 according to the control of the microprocessor 246. The original color signals R, G and B and the horizontal and vertical synchronizing signals H and V are applied to the switching circuit 204. Thereafter, the same operation as the NTSC broadcasting receiving mode is performed and the DBS broadcasting is displayed on the screen. Therefore, there is no needed an additional satellite broadcasting receiver. Further, since the digital DBS signal is directly analog-processed without being converted into an analog NTSC signal format, there is no degradation in the characteristic of the DBS signal.

In the HDTV broadcasting receiving mode, the HDTV broadcasting signal is supplied to the HD/NTSC tuner 228 and decoded by the HD decoder 234. The decoded HDTV signal is converted into the display format by the format converter 236 according to the control of the microprocessor 246. The original color signals R, G and B and the horizontal and vertical synchronizing signals H and V are applied to the switching circuit 204. Thereafter, the same operation as the

NTSC broadcasting receiving mode is implemented and the HDTV broadcasting is displayed on the screen.

In the PC monitor mode, the PC monitor signal is supplied to the switching circuit 204 from the PC through the PC monitor input terminal 216. The original color signals R, G and B are applied to the R.G.B. processor 242, and the horizontal and vertical synchronizing signals H and V are applied to the synchronous processor 208. Thereafter, the same operation as the NTSC broadcasting receiving mode is performed and the PC monitor screen is displayed.

Referring to FIG. 3, there is shown a deflection control data output process executed by the microprocessor 246 according to the current viewing mode of the TV.

In the PC monitor mode, the deflection control data corresponding to the horizontal and vertical frequencies of the PC monitor signal is generated. In the NTSC broadcasting or other modes, the deflection control data of a fixed value suitable for corresponding broadcasting is generated.

At step 300, the microprocessor 246 checks whether the current viewing mode is the PC monitor mode. If not, for example, if the current viewing mode is the NTSC broadcasting receiving mode, the microprocessor 246 reads

the deflection control data fixed as a value of the NTSC broadcasting receiving mode from the EEPROM 248 at step 306. If the current viewing mode is the PC monitor mode, the microprocessor 246 counts the horizontal and vertical frequencies of the horizontal and vertical synchronizing signals applied from the synchronous processor 208 at step 302. The microprocessor 246 reads the deflection control data corresponding to the counted frequencies from the EEPROM 248 at step 304. The microprocessor 246 generates the deflection control data through the second D/A converter 252 at step 308.

As described above, the multisystem TV can view the NTSC, DBS and HDTV broadcasting by one apparatus without degrading the picture quality. Moreover, the multisystem TV is usable as the PC monitor. Hence, the multisystem TV according to the present invention is convenient to use and economical. Since the composite video signal is converted into the color difference signal and double-scanned, the frequency band is limited and thus the resolution is improved.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art the various changes in form and details may be made therein without

departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A multisystem television which is usable as a monitor of a personal computer (PC), comprising:

an NTSC (National Television System Committee) signal processor for separating an NTSC broadcasting signal into a luminance signal and a chrominance signal and generating double-scanned original color signals;

a digital broadcasting signal processor for decoding a DBS (Direct Broadcasting Satellite) broadcasting receiving signal and an HD (High Definition) broadcasting receiving signal, and converting a signal corresponding to a current viewing mode out of the decoded HD signal, the decoded DBS signal and an external HD signal into a display type;

a switching circuit for selectively generating one of a PC monitor signal received from said PC, an output signal of said digital broadcasting signal processor and an output signal of said NTSC signal processor according to the current viewing mode;

a video output circuit for adjusting picture quality of a signal generated from said switching circuit so as to be supplied to a picture tube;

a controller for controlling the signal processing of said NTSC signal processor, digital broadcasting signal processor and video output circuit, the switching of said switching circuit, and the deflection of said picture tube,

according to the current viewing mode; and

a synchronous processor for processing a synchronizing signal generated from said switching circuit and supplying the processed signal to said video output circuit and said controller.

2. A multisystem television as set forth in claim 1, wherein, if the current viewing mode is a PC monitor mode, said controller judges horizontal and vertical frequencies of said synchronizing signal and controls the deflection of said picture tube so as to correspond to the horizontal and vertical frequencies.

3. A multisystem television as set forth in claim 2, wherein said NTSC signal processor comprises:

an NTSC tuner for selecting said NTSC broadcasting receiving signal by the control of said controller and generating an intermediate frequency signal;

an intermediate frequency module for processing said intermediate frequency signal generated from said NTSC tuner and generating a base band video signal;

an audio/video switch for selecting either said base band video signal generated from said intermediate frequency module or a composite video signal received from the exterior by the control of said controller;

a digital comb filter for separating a signal selected

by said audio/video switch into said luminance signal and said chrominance signal; and

a double scanning circuit for double-scanning said signal generated from said audio/video switch and generating double-scanned original color signals.

4. A multisystem television as set forth in claim 3, wherein said double scanning circuit comprises:

an NTSC chroma processor for processing said signal selected by said audio/video switch and generating color difference signals;

an analog-to-digital converter for converting said color difference signals into digital color difference signals;

a double scanner for double-scanning said digital color difference signals;

a digital-to-analog converter for converting the double-scanned digital color difference signals into double-scanned analog color difference signals; and

an R.G.B. processor for converting said double-scanned analog color difference signals into original color signals.

5. A multisystem television as set forth in any one of claims 3 and 4, wherein horizontal and vertical deflection frequencies are limited to 31.5-60 KHz by the double scanning conversion.

6. A multisystem television as set forth in claim 3, wherein said digital broadcasting signal processor comprises:

an HD/DBS tuner for selecting a signal corresponding to the current viewing mode out of said HD broadcasting receiving signal and said DBS broadcasting receiving signal;

an HD decoder for decoding said HD broadcasting signal selected by said HD/DBS tuner and generating a digital HD signal;

a DBS decoder for decoding said DBS broadcasting signal selected by said HD/DBS tuner and generating a digital DBS signal; and

a format converter for converting a signal corresponding to the current viewing mode out of said digital HD signal, said digital DBS signal, and a digital HD signal received from the exterior into a signal of a display type, and generating analog original color signals.

7. A multisystem television as set forth in claim 6, wherein said video output circuit comprises:

an on-screen display generator for generating an on-screen display signal by the control of said controller;

an R.G.B. processor for adjusting picture quality with respect to a signal generated from said switching circuit;

an automatic beam limit circuit for controlling an automatic beam limit of a signal processed from said R.G.B.

processor; and

an on-screen display switching circuit for switching signals generated from said on-screen display generator and said R.G.B. processor and supplying the switched signal to said picture tube.

R. WILLIAM WRAY & ASSOCIATES
BOX 2760 - STATION D
OTTAWA, CANADA K1P 5W8
PATENT AGENT FOR THE APPLICANT

1/3

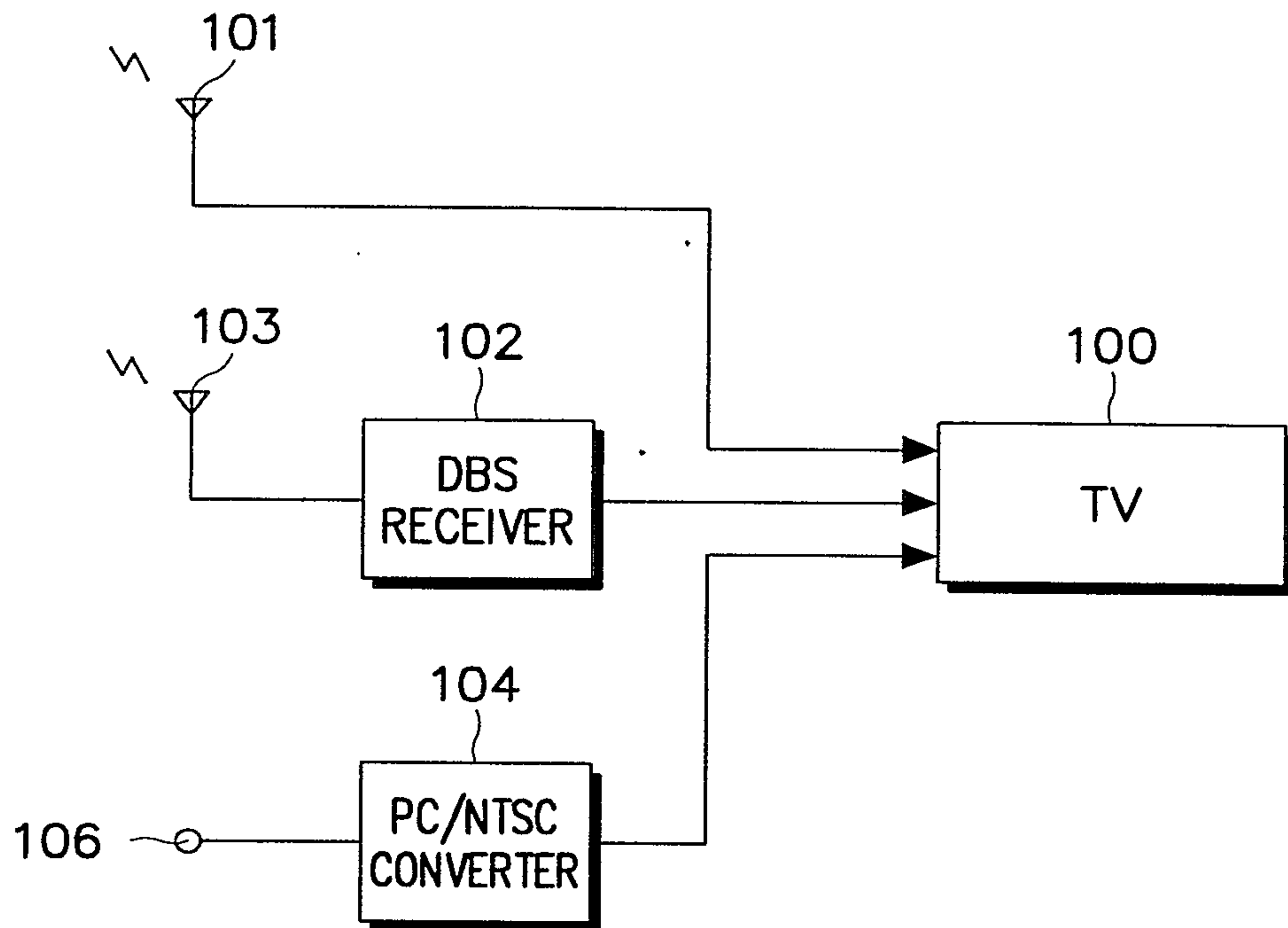
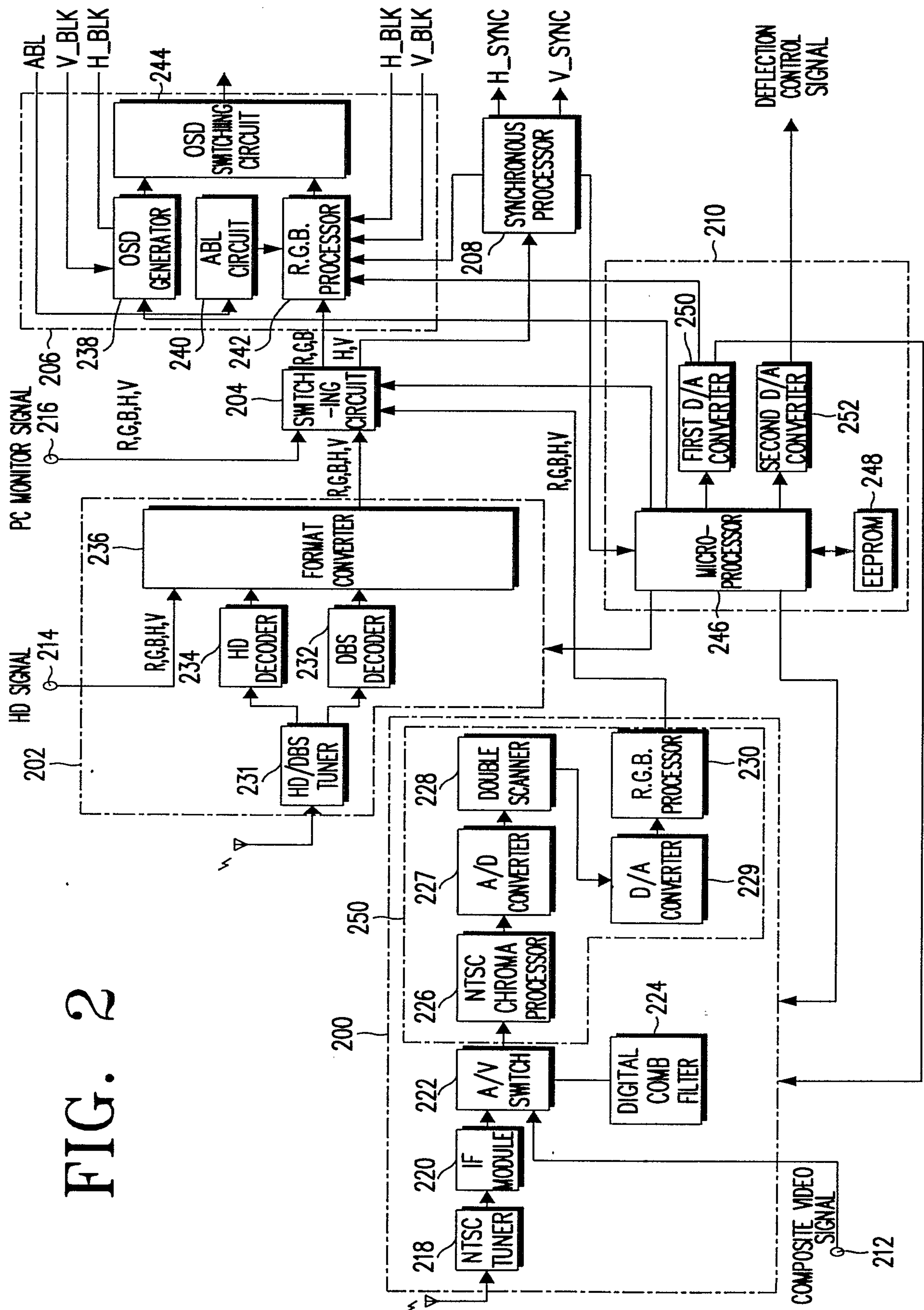


FIG. 1



3/3

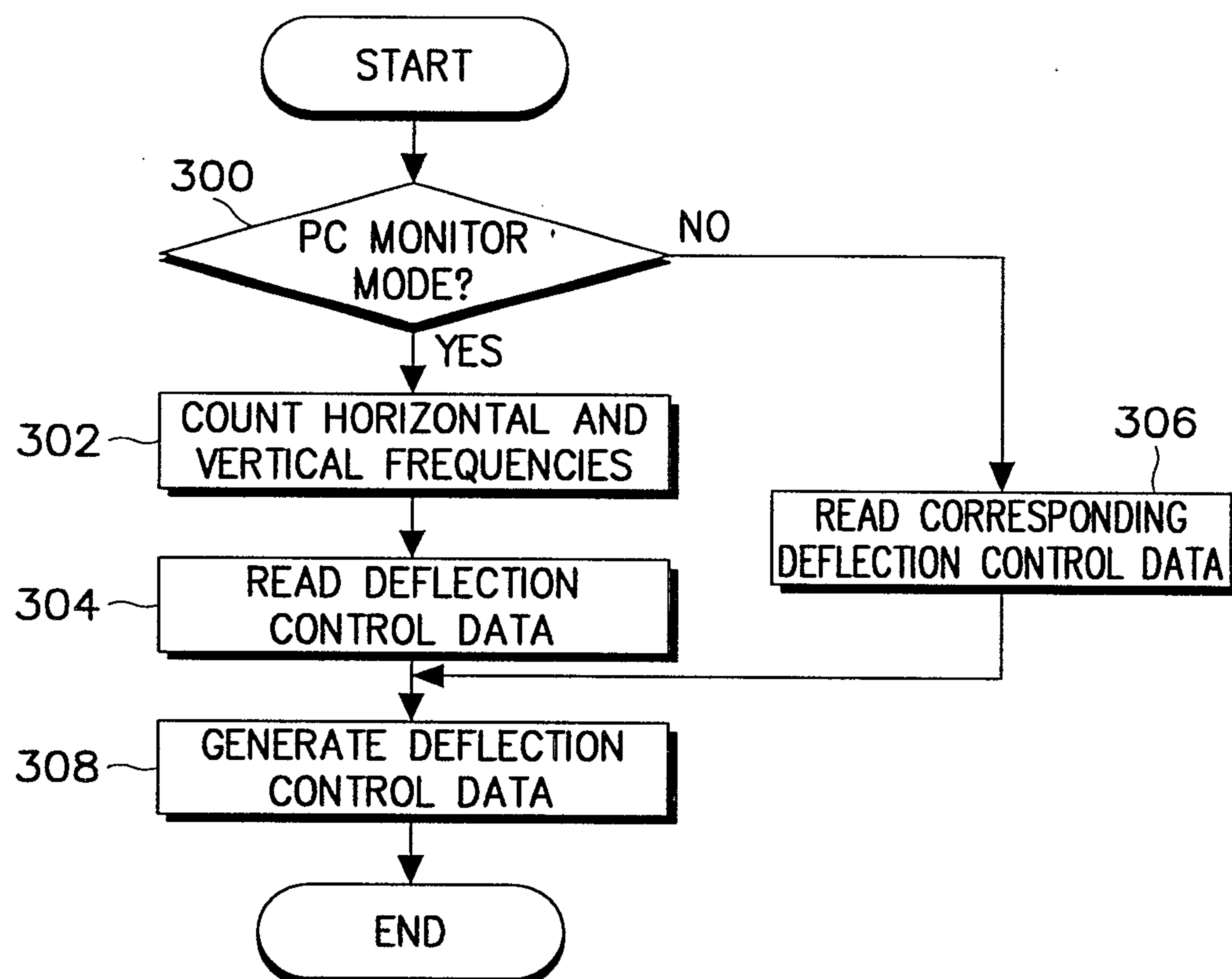


FIG. 3

