

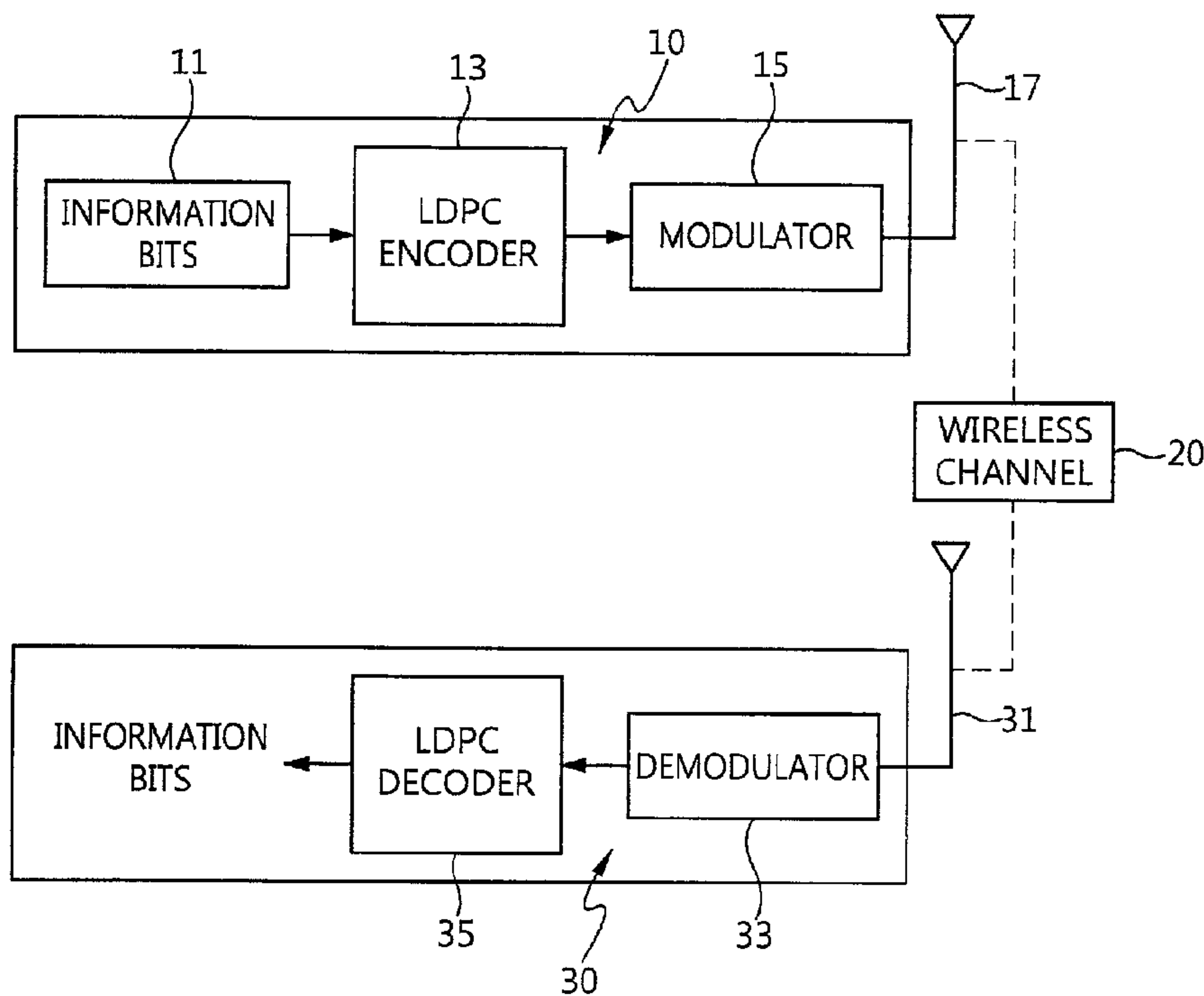


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(54) Titre : CODEUR DE VERIFICATION DE PARITE A FAIBLE DENSITE AYANT UNE LONGUEUR DE 64 800 BITS ET UN TAUX DE CODE DE 7/15 ET PROCEDE D'ENCODAGE DE VERIFICATION DE PARITE A FAIBLE DENSITE UTILISANT CELUI-CI

(54) Title: LOW DENSITY PARITY CHECK ENCODER HAVING LENGTH OF 64800 AND CODE RATE OF 7/15, AND LOW DENSITY PARITY CHECK ENCODING METHOD USING THE SAME



(57) Abrégé/Abstract:

A low density parity check (LDPC) encoder, an LDPC decoder, and an LDPC encoding method are disclosed. The LDPC encoder includes first memory, second memory, and a processor. The first memory stores an LDPC codeword having a length of 64800

(57) **Abrégé(suite)/Abstract(continued):**

and a code rate of 7/15. The second memory is initialized to 0. The processor generates the LDPC codeword corresponding to information bits by performing accumulation with respect to the second memory using a sequence corresponding to a parity check matrix (PCM).

ABSTRACT

A low density parity check (LDPC) encoder, an LDPC decoder, and an LDPC encoding method are disclosed. The LDPC encoder includes first memory, second memory, and a processor. The first memory stores an LDPC codeword having a length of 64800 and a code rate of 7/15. The second memory is initialized to 0. The processor generates the LDPC codeword corresponding to information bits by performing accumulation with respect to the second memory using a sequence corresponding to a parity check matrix (PCM).

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LOW DENSITY PARITY CHECK ENCODER HAVING LENGTH OF 64800 AND
CODE RATE OF 7/15, AND LOW DENSITY PARITY CHECK ENCODING METHOD
USING THE SAME

This application is a divisional of Canadian Patent Application No. 2,864,634 filed on September 25, 2014.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Patent Application Nos. 10-2013-0119514, 10-2013-0120573, 10-2013-0149478 and 10-2014-0120015, filed October 7, 2013, October 10, 2013, December 3, 2013 and September 11, 2014, respectively.

BACKGROUND

1. Technical Field

[0002] The present disclosure relates generally to a low density parity check (LDPC) code that is used to correct errors occurring over a wireless channel, and, more particularly, to an LDPC code that is applicable to a digital broadcasting system.

2. Description of the Related Art

[0003] Current terrestrial television (TV) broadcasting generates co-channel interference across an area within a distance that is three times a service radius, and thus the same frequency cannot be reused in the area within the distance that is three times the service radius. An area in which the same frequency cannot be reused is called a white space. Spectrum efficiency significantly deteriorates due to the occurrence of a white space.

[0004] Accordingly, there arises a need for the development of a transmission technology that facilitates the elimination of a white space and the reuse of a frequency with an emphasis on reception robustness in order to improve spectrum efficiency.

[0005] In response to this, the paper "Cloud Transmission: A New Spectrum-Reuse Friendly Digital Terrestrial Broadcasting Transmission System" published on September of 2012 in IEEE Transactions on Broadcasting, Vol. 58, No. 3 proposes a terrestrial cloud transmission technology that facilitates reuse, does not generate a

white space, and makes the construction and operation of a single frequency network easy.

[0006] Using this terrestrial cloud transmission technology, a broadcasting station can transmit the same nationwide content or locally different content over a single broadcasting channel. However, for this purpose, a receiver should receive one or more terrestrial cloud broadcast signals in an area in which signals transmitted from different transmitters overlap each other, that is, an overlap area, over a single frequency network, and then should distinguish and demodulate the received terrestrial cloud broadcast signals. That is, the receiver should demodulate one or more cloud broadcast signals in a situation in which co-channel interference is present and the timing and frequency synchronization between transmitted signals are not guaranteed.

[0007] Meanwhile, Korean Patent Application Publication No. 2013-0135746 entitled "Low Density Parity Check Code for Terrestrial Cloud Transmission" discloses an LDPC code that is optimized for terrestrial cloud transmission and exhibits excellent performance at low code rate (<0.5).

[0008] However, Korean Patent Application Publication No. 2013-0135746 is directed to a code length completely different from an LDPC code length used in the DVB broadcast standard, etc., and does not teach a specific LDPC encoding method.

SUMMARY

[0009] At least one embodiment of the present invention is directed to the provision of a new LDPC codeword having a length of 64800 and a code rate of $7/15$, which is capable of being used for general purposes.

[0010] At least one embodiment of the present invention is directed to the provision of an LDPC encoding technique that is capable of efficiently performing LDPC encoding using a sequence having a number of rows equal to a value that is obtained by dividing the sum of the length of the systematic part of an LDPC codeword, that is, 30240, and the length of the first parity part of the LDPC codeword, that is, 1080, by 360.

[0011] In accordance with an aspect of the present invention, there is provided an LDPC encoder, including first memory configured to store an LDPC codeword having a length of 64800 and a code rate of $7/15$; second memory configured to be initialized

to 0; and a processor configured to generate the LDPC codeword corresponding to information bits by performing accumulation with respect to the second memory using a sequence corresponding to a parity check matrix (PCM).

[0012] The accumulation may be performed at parity bit addresses that are updated using the sequence corresponding to the PCM.

[0013] The LDPC codeword may include a systematic part corresponding to the information bits and having a length of 30240, a first parity part corresponding to a dual diagonal matrix included in the PCM and having a length of 1080, and a second parity part corresponding to an identity matrix included in the PCM and having a length of 33480.

[0014] The sequence may have a number of rows equal to the sum of a value obtained by dividing a length of the systematic part, that is, 30240, by a circulant permutation matrix (CPM) size corresponding to the PCM, that is, 360, and a value obtained by dividing a length of the first parity part, that is, 1080, by the CPM size.

[0015] The sequence may be represented by the following Sequence Table:

Sequence Table

1st row: 460 792 1007 4580 11452 13130 26882 27020 32439
 2nd row: 35 472 1056 7154 12700 13326 13414 16828 19102
 3rd row: 45 440 772 4854 7863 26945 27684 28651 31875
 4th row: 744 812 892 1509 9018 12925 14140 21357 25106
 5th row: 271 474 761 4268 6706 9609 19701 19707 24870
 6th row: 223 477 662 1987 9247 18376 22148 24948 27694
 7th row: 44 379 786 8823 12322 14666 16377 28688 29924
 8th row: 104 219 562 5832 19665 20615 21043 22759 32180
 9th row: 41 43 870 7963 13718 14136 17216 30470 33428
 10th row: 592 744 887 4513 6192 18116 19482 25032 34095
 11th row: 456 821 1078 7162 7443 8774 15567 17243 33085
 12th row: 151 666 977 6946 10358 11172 18129 19777 32234
 13th row: 236 793 870 2001 6805 9047 13877 30131 34252
 14th row: 297 698 772 3449 4204 11608 22950 26071 27512
 15th row: 202 428 474 3205 3726 6223 7708 20214 25283
 16th row: 139 719 915 1447 2938 11864 15932 21748 28598

17th row: 135 853 902 3239 18590 20579 30578 33374 34045
18th row: 9 13 971 11834 13642 17628 21669 24741 30965
19th row: 344 531 730 1880 16895 17587 21901 28620 31957
20th row: 7 192 380 3168 3729 5518 6827 20372 34168
21st row: 28 521 681 4313 7465 14209 21501 23364 25980
22nd row: 269 393 898 3561 11066 11985 17311 26127 30309
23rd row: 42 82 707 4880 4890 9818 23340 25959 31695
24th row: 189 262 707 6573 14082 22259 24230 24390 24664
25th row: 383 568 573 5498 13449 13990 16904 22629 34203
26th row: 585 596 820 2440 2488 21956 28261 28703 29591
27th row: 755 763 795 5636 16433 21714 23452 31150 34545
28th row: 23 343 669 1159 3507 13096 17978 24241 34321
29th row: 316 384 944 4872 8491 18913 21085 23198 24798
30th row: 64 314 765 3706 7136 8634 14227 17127 23437
31st row: 220 693 899 8791 12417 13487 18335 22126 27428
32nd row: 285 794 1045 8624 8801 9547 19167 21894 32657
33rd row: 386 621 1045 1634 1882 3172 13686 16027 22448
34th row: 95 622 693 2827 7098 11452 14112 18831 31308
35th row: 446 813 928 7976 8935 13146 27117 27766 33111
36th row: 89 138 241 3218 9283 20458 31484 31538 34216
37th row: 277 420 704 9281 12576 12788 14496 15357 20585
38th row: 141 643 758 4894 10264 15144 16357 22478 26461
39th row: 17 108 160 13183 15424 17939 19276 23714 26655
40th row: 109 285 608 1682 20223 21791 24615 29622 31983
41st row: 123 515 622 7037 13946 15292 15606 16262 23742
42nd row: 264 565 923 6460 13622 13934 23181 25475 26134
43rd row: 202 548 789 8003 10993 12478 16051 25114 27579
44th row: 121 450 575 5972 10062 18693 21852 23874 28031
45th row: 507 560 889 12064 13316 19629 21547 25461 28732
46th row: 664 786 1043 9137 9294 10163 23389 31436 34297
47th row: 45 830 907 10730 16541 21232 30354 30605 31847
48th row: 203 507 1060 6971 12216 13321 17861 22671 29825

49th row: 369 881 952 3035 12279 12775 17682 17805 34281
50th row: 683 709 1032 3787 17623 24138 26775 31432 33626
51st row: 524 792 1042 12249 14765 18601 25811 32422 33163
52nd row: 137 639 688 7182 8169 10443 22530 24597 29039
53rd row: 159 643 749 16386 17401 24135 28429 33468 33469
54th row: 107 481 555 7322 13234 19344 23498 26581 31378
55th row: 249 389 523 3421 10150 17616 19085 20545 32069
56th row: 395 738 1045 2415 3005 3820 19541 23543 31068
57th row: 27 293 703 1717 3460 8326 8501 10290 32625
58th row: 126 247 515 6031 9549 10643 22067 29490 34450
59th row: 331 471 1007 3020 3922 7580 23358 28620 30946
60th row: 222 542 1021 3291 3652 13130 16349 33009 34348
61st row: 532 719 1038 5891 7528 23252 25472 31395 31774
62nd row: 145 398 774 7816 13887 14936 23708 31712 33160
63rd row: 88 536 600 1239 1887 12195 13782 16726 27998
64th row: 151 269 585 1445 3178 3970 15568 20358 21051
65th row: 650 819 865 15567 18546 25571 32038 33350 33620
66th row: 93 469 800 6059 10405 12296 17515 21354 22231
67th row: 97 206 951 6161 16376 27022 29192 30190 30665
68th row: 412 549 986 5833 10583 10766 24946 28878 31937
69th row: 72 604 659 5267 12227 21714 32120 33472 33974
70th row: 25 902 912 1137 2975 9642 11598 25919 28278
71st row: 420 976 1055 8473 11512 20198 21662 25443 30119
72nd row: 1 24 932 6426 11899 13217 13935 16548 29737
73rd row: 53 618 988 6280 7267 11676 13575 15532 25787
74th row: 111 739 809 8133 12717 12741 20253 20608 27850
75th row: 120 683 943 14496 15162 15440 18660 27543 32404
76th row: 600 754 1055 7873 9679 17351 27268 33508
77th row: 344 756 1054 7102 7193 22903 24720 27883
78th row: 582 1003 1046 11344 23756 27497 27977 32853
79th row: 28 429 509 11106 11767 12729 13100 31792
80th row: 131 555 907 5113 10259 10300 20580 23029

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81st row: 406 915 977 12244 20259 26616 27899 32228

82nd row: 46 195 224 1229 4116 10263 13608 17830

83rd row: 19 819 953 7965 9998 13959 30580 30754

84th row: 164 1003 1032 12920 15975 16582 22624 27357

85th row: 8433 11894 13531 17675 25889 31384

86th row: 3166 3813 8596 10368 25104 29584

87th row: 2466 8241 12424 13376 24837 32711

[0016] The accumulation may be performed while the rows of the sequence are being repeatedly changed by the CPM size of the PCM.

[0017] In accordance with an aspect of the present invention, there is provided an LDPC encoding method, including initializing first memory configured to store an LDPC codeword having a length of 64800 and a code rate of 7/15 and second memory; and generating the LDPC codeword corresponding to information bits by performing accumulation with respect to the second memory using a sequence corresponding to a PCM.

[0018] The accumulation may be performed at parity bit addresses that are updated using the sequence corresponding to the PCM.

[0019] The LDPC codeword may include a systematic part corresponding to the information bits and having a length of 30240, a first parity part corresponding to a dual diagonal matrix included in the PCM and having a length of 1080, and a second parity part corresponding to an identity matrix included in the PCM and having a length of 33480.

[0020] The sequence may have a number of rows equal to the sum of a value obtained by dividing a length of the systematic part, that is, 30240, by a circulant permutation matrix (CPM) size corresponding to the PCM, that is, 360, and a value obtained by dividing a length of the first parity part, that is, 1080, by the CPM size.

[0021] The sequence may be represented by the above Sequence Table.

[0022] In accordance with still another aspect of the present invention, there is provided an LDPC decoder, including a receiving unit configured to receive an LDPC codeword encoded using a sequence corresponding to a PCM and is represented by the above Sequence Table; and a decoding unit configured to restore information bits from the received LDPC codeword by performing decoding corresponding to the PCM.

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[0022a] According to an embodiment, there is provided a low density parity check (LDPC) decoder, comprising: a receiving unit configured to receive an LDPC codeword having a length of 64800 and a code rate of 7/15, the LDPC codeword encoded using a sequence corresponding to a parity check matrix (PCM); and a decoding unit configured to restore
5 error-corrected bits from the received LDPC codeword by performing decoding corresponding to the parity check matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0024] FIG. 1 is a block diagram illustrating a broadcast signal transmission and reception system according to an embodiment of the present invention;

[0025] FIG. 2 is an operation flowchart illustrating a broadcast signal transmission and reception method according to an embodiment of the present invention;

[0026] FIG. 3 is a diagram illustrating the structure of a PCM corresponding to an LDPC code according to an embodiment of the present invention;

[0027] FIG. 4 is a block diagram illustrating an LDPC encoder according to an embodiment of the present invention;

[0028] FIG. 5 is a block diagram illustrating an LDPC decoder according to an embodiment of the present invention;

[0029] FIG. 6 is an operation flowchart illustrating an LDPC encoding method according to an embodiment of the present invention; and

[0030] FIG. 7 is a graph plotting the performance of a QC-LDPC code having a length of 64800 and a code rate of 7/15 according to an embodiment of the present invention against E_b/N_0 .

DETAILED DESCRIPTION

[0031] Embodiments of the present invention will be described in detail below with reference to the accompanying drawings. Repeated descriptions and descriptions of well-known functions and configurations that have been deemed to make the gist of the present invention unnecessarily obscure will be omitted below. The embodiments of the present invention are intended to fully describe the present invention to persons having ordinary knowledge in the art to which the present invention pertains. Accordingly, the shapes, sizes, etc. of components in the drawings may be exaggerated to make the description obvious.

[0032] Embodiments of the present invention will be described in detail below with reference to the accompanying drawings.

[0033] FIG. 1 is a block diagram illustrating a broadcast signal transmission and reception system according to an embodiment of the present invention.

[0034] Referring to FIG. 1, it can be seen that a transmitter 10 and a receiver 30 communicate with each other over a wireless channel 20.

[0035] The transmitter 10 generates an n-bit codeword by encoding k information bits using an LDPC encoder 13. The codeword is modulated by the modulator 15, and is transmitted via an antenna 17. The signal transmitted via the wireless channel 20 is received via the antenna 31 of the receiver 30, and, in the receiver 30, is subjected to a process reverse to the process in the transmitter 10. That is, the received data is demodulated by a demodulator 33, and is then decoded by an LDPC decoder 35, thereby finally restoring the information bits.

[0036] It will be apparent to those skilled in the art that the above-described transmission and reception processes have been described within a minimum range required for a description of the features of the present invention and various processes required for data transmission may be added.

[0037] In the following, the specific processes of encoding and decoding that are performed using an LDPC code in the LDPC encoder 13 or LDPC decoder 35 and the specific configurations of encoding and decoding devices, such as the LDPC encoder 13 and the LDPC decoder 35, are described. The LDPC encoder 13 illustrated in FIG. 1 may have a structure illustrated in FIG. 4, and the LDPC decoder 35 may have a structure illustrated in FIG. 5.

[0038] FIG. 2 is an operation flowchart illustrating a broadcast signal transmission and reception method according to an embodiment of the present invention.

[0039] Referring to FIG. 2, in the broadcast signal transmission and reception method according to this embodiment of the present invention, input bits (information bits) are subjected to LDPC encoding at step S210.

[0040] That is, at step S210, an n-bit codeword is generated by encoding k information bits using the LDPC encoder.

[0041] In this case, step S210 may be performed as in an LDPC encoding method illustrated in FIG. 6.

[0042] Furthermore, in the broadcast signal transmission and reception method, the encoded data is modulated at step S220.

[0043] That is, at step S220, the encoded n-bit codeword is modulated using the modulator.

[0044] Furthermore, in the broadcast signal transmission and reception method, the modulated data is transmitted at step S230.

[0045] That is, at step S230, the modulated codeword is transmitted over a wireless channel via the antenna.

[0046] Furthermore, in the broadcast signal transmission and reception method, the received data is demodulated at step S240.

[0047] That is, at step S240, the signal transmitted over the wireless channel is received via the antenna of the receiver, and the received data is demodulated using the demodulator.

[0048] Furthermore, in the broadcast signal transmission and reception method, the demodulated data is subjected to LDPC decoding at step S250.

[0049] That is, at step S250, the information bits are finally restored by performing LDPC decoding using the demodulator of the receiver.

[0050] In this case, step S250 corresponds to a process reverse to that of the LDPC encoding method illustrated in FIG. 6, and may correspond to the LDPC decoder of FIG. 5.

[0051] An LDPC code is known as a code very close to the Shannon limit for an additive white Gaussian noise (AWGN) channel, and has the advantages of asymptotically excellent performance and parallelizable decoding compared to a turbo code.

[0052] Generally, an LDPC code is defined by a low-density parity check matrix (PCM) that is randomly generated. However, a randomly generated LDPC code requires a large amount of memory to store a PCM, and requires a lot of time to access memory. In order to overcome these problems, a quasi-cyclic LDPC (QC-LDPC) code has been proposed. A QC-LDPC code that is composed of a zero matrix or a circulant permutation matrix (CPM) is defined by a PCM that is expressed by the following Equation 1:

$$H = \begin{bmatrix} J^{a_{11}} & J^{a_{12}} & \dots & J^{a_{1n}} \\ J^{a_{21}} & J^{a_{22}} & \dots & J^{a_{2n}} \\ \vdots & \vdots & \ddots & \vdots \\ J^{a_{m1}} & J^{a_{m2}} & \dots & J^{a_{mn}} \end{bmatrix}, \text{ for } a_{ij} \in \{0, 1, \dots, L-1, \infty\} \quad (1)$$

[0053] In this equation, J is a CPM having a size of $L \times L$, and is given as the following Equation 2. In the following description, L may be 360.

$$J_{L \times L} = \begin{bmatrix} 0 & 1 & 0 & \dots & 0 \\ 0 & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & 1 \\ 1 & 0 & 0 & \dots & 0 \end{bmatrix} \quad (2)$$

[0054] Furthermore, J^i is obtained by shifting an $L \times L$ identity matrix $I(J^0)$ to the right i ($0 \leq i < L$) times, and J^∞ is an $L \times L$ zero matrix. Accordingly, in the case of a QC-LDPC code, it is sufficient if only index exponent i is stored in order to store J^i , and thus the amount of memory required to store a PCM is considerably reduced.

[0055] FIG. 3 is a diagram illustrating the structure of a PCM corresponding to an LDPC code to according to an embodiment of the present invention.

[0056] Referring to FIG. 3, the sizes of matrices A and C are $g \times K$ and $(N - K - g) \times (K + g)$, respectively, and are composed of an $L \times L$ zero matrix and a CPM, respectively. Furthermore, matrix Z is a zero matrix having a size of $g \times (N - K - g)$, matrix D is an identity matrix having a size of $(N - K - g) \times (N - K - g)$, and matrix B is a dual diagonal matrix having a size of $g \times g$. In this case, the matrix B may be a matrix in which all elements except elements along a diagonal line and neighboring elements below the diagonal line are 0, and may be defined as the following Equation 3:

$$B_{g \times g} = \begin{bmatrix} I_{L \times L} & 0 & 0 & \cdots & 0 & 0 & 0 \\ I_{L \times L} & I_{L \times L} & 0 & \cdots & 0 & 0 & 0 \\ 0 & I_{L \times L} & I_{L \times L} & \vdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & I_{L \times L} & I_{L \times L} & 0 \\ 0 & 0 & 0 & \cdots & 0 & I_{L \times L} & I_{L \times L} \end{bmatrix} \quad (3)$$

where $I_{L \times L}$ is an identity matrix having a size of $L \times L$.

[0057] That is, the matrix B may be a bit-wise dual diagonal matrix, or may be a block-wise dual diagonal matrix having identity matrices as its blocks, as indicated by Equation 3. The bit-wise dual diagonal matrix is disclosed in detail in Korean Patent Application Publication No. 2007-0058438, etc.

[0058] In particular, it will be apparent to those skilled in the art that when the matrix B is a bit-wise dual diagonal matrix, it is possible to perform conversion into a Quasi-cyclic form by applying row or column permutation to a PCM including the matrix B and having a structure illustrated in FIG. 3.

[0059] In this case, N is the length of a codeword, and K is the length of information.

[0060] The present invention proposes a newly designed QC-LDPC code in which the code rate thereof is 7/15 and the length of a codeword is 64800, as illustrated in the following Table 1. That is, the present invention proposes an LDPC code that is designed to receive information having a length of 30240 and generate an LDPC codeword having a length of 64800.

[0061] Table 1 illustrates the sizes of the matrices A, B, C, D and Z of the QC-LDPC code according to the present invention:

Table 1

| Code rate | Length | Sizes | | | | |
|-----------|--------|--------|-------------|---------|---------|--------|
| | | A | B | C | D | Z |
| 7/15 | 64800 | 1080 × | 1080 × 1080 | 33480 × | 33480 × | 1080 × |
| | | 30240 | | 31320 | 33480 | 33480 |

[0062] The newly designed LDPC code may be represented in the form of a sequence (progression), an equivalent relationship is established between the sequence and matrix (parity bit check matrix), and the sequence may be represented, as follows:

Sequence Table

1st row: 460 792 1007 4580 11452 13130 26882 27020 32439
2nd row: 35 472 1056 7154 12700 13326 13414 16828 19102
3rd row: 45 440 772 4854 7863 26945 27684 28651 31875
4th row: 744 812 892 1509 9018 12925 14140 21357 25106
5th row: 271 474 761 4268 6706 9609 19701 19707 24870
6th row: 223 477 662 1987 9247 18376 22148 24948 27694
7th row: 44 379 786 8823 12322 14666 16377 28688 29924
8th row: 104 219 562 5832 19665 20615 21043 22759 32180
9th row: 41 43 870 7963 13718 14136 17216 30470 33428
10th row: 592 744 887 4513 6192 18116 19482 25032 34095
11th row: 456 821 1078 7162 7443 8774 15567 17243 33085
12th row: 151 666 977 6946 10358 11172 18129 19777 32234
13th row: 236 793 870 2001 6805 9047 13877 30131 34252
14th row: 297 698 772 3449 4204 11608 22950 26071 27512
15th row: 202 428 474 3205 3726 6223 7708 20214 25283
16th row: 139 719 915 1447 2938 11864 15932 21748 28598
17th row: 135 853 902 3239 18590 20579 30578 33374 34045
18th row: 9 13 971 11834 13642 17628 21669 24741 30965
19th row: 344 531 730 1880 16895 17587 21901 28620 31957
20th row: 7 192 380 3168 3729 5518 6827 20372 34168
21st row: 28 521 681 4313 7465 14209 21501 23364 25980
22nd row: 269 393 898 3561 11066 11985 17311 26127 30309
23rd row: 42 82 707 4880 4890 9818 23340 25959 31695
24th row: 189 262 707 6573 14082 22259 24230 24390 24664
25th row: 383 568 573 5498 13449 13990 16904 22629 34203
26th row: 585 596 820 2440 2488 21956 28261 28703 29591
27th row: 755 763 795 5636 16433 21714 23452 31150 34545
28th row: 23 343 669 1159 3507 13096 17978 24241 34321
29th row: 316 384 944 4872 8491 18913 21085 23198 24798
30th row: 64 314 765 3706 7136 8634 14227 17127 23437
31st row: 220 693 899 8791 12417 13487 18335 22126 27428
32nd row: 285 794 1045 8624 8801 9547 19167 21894 32657

33rd row: 386 621 1045 1634 1882 3172 13686 16027 22448
34th row: 95 622 693 2827 7098 11452 14112 18831 31308
35th row: 446 813 928 7976 8935 13146 27117 27766 33111
36th row: 89 138 241 3218 9283 20458 31484 31538 34216
37th row: 277 420 704 9281 12576 12788 14496 15357 20585
38th row: 141 643 758 4894 10264 15144 16357 22478 26461
39th row: 17 108 160 13183 15424 17939 19276 23714 26655
40th row: 109 285 608 1682 20223 21791 24615 29622 31983
41st row: 123 515 622 7037 13946 15292 15606 16262 23742
42nd row: 264 565 923 6460 13622 13934 23181 25475 26134
43rd row: 202 548 789 8003 10993 12478 16051 25114 27579
44th row: 121 450 575 5972 10062 18693 21852 23874 28031
45th row: 507 560 889 12064 13316 19629 21547 25461 28732
46th row: 664 786 1043 9137 9294 10163 23389 31436 34297
47th row: 45 830 907 10730 16541 21232 30354 30605 31847
48th row: 203 507 1060 6971 12216 13321 17861 22671 29825
49th row: 369 881 952 3035 12279 12775 17682 17805 34281
50th row: 683 709 1032 3787 17623 24138 26775 31432 33626
51st row: 524 792 1042 12249 14765 18601 25811 32422 33163
52nd row: 137 639 688 7182 8169 10443 22530 24597 29039
53rd row: 159 643 749 16386 17401 24135 28429 33468 33469
54th row: 107 481 555 7322 13234 19344 23498 26581 31378
55th row: 249 389 523 3421 10150 17616 19085 20545 32069
56th row: 395 738 1045 2415 3005 3820 19541 23543 31068
57th row: 27 293 703 1717 3460 8326 8501 10290 32625
58th row: 126 247 515 6031 9549 10643 22067 29490 34450
59th row: 331 471 1007 3020 3922 7580 23358 28620 30946
60th row: 222 542 1021 3291 3652 13130 16349 33009 34348
61st row: 532 719 1038 5891 7528 23252 25472 31395 31774
62nd row: 145 398 774 7816 13887 14936 23708 31712 33160
63rd row: 88 536 600 1239 1887 12195 13782 16726 27998
64th row: 151 269 585 1445 3178 3970 15568 20358 21051

65th row: 650 819 865 15567 18546 25571 32038 33350 33620
 66th row: 93 469 800 6059 10405 12296 17515 21354 22231
 67th row: 97 206 951 6161 16376 27022 29192 30190 30665
 68th row: 412 549 986 5833 10583 10766 24946 28878 31937
 69th row: 72 604 659 5267 12227 21714 32120 33472 33974
 70th row: 25 902 912 1137 2975 9642 11598 25919 28278
 71st row: 420 976 1055 8473 11512 20198 21662 25443 30119
 72nd row: 1 24 932 6426 11899 13217 13935 16548 29737
 73rd row: 53 618 988 6280 7267 11676 13575 15532 25787
 74th row: 111 739 809 8133 12717 12741 20253 20608 27850
 75th row: 120 683 943 14496 15162 15440 18660 27543 32404
 76th row: 600 754 1055 7873 9679 17351 27268 33508
 77th row: 344 756 1054 7102 7193 22903 24720 27883
 78th row: 582 1003 1046 11344 23756 27497 27977 32853
 79th row: 28 429 509 11106 11767 12729 13100 31792
 80th row: 131 555 907 5113 10259 10300 20580 23029
 81st row: 406 915 977 12244 20259 26616 27899 32228
 82nd row: 46 195 224 1229 4116 10263 13608 17830
 83rd row: 19 819 953 7965 9998 13959 30580 30754
 84th row: 164 1003 1032 12920 15975 16582 22624 27357
 85th row: 8433 11894 13531 17675 25889 31384
 86th row: 3166 3813 8596 10368 25104 29584
 87th row: 2466 8241 12424 13376 24837 32711

[0063] An LDPC code that is represented in the form of a sequence is being widely used in the DVB standard.

[0064] According to an embodiment of the present invention, an LDPC code presented in the form of a sequence is encoded, as follows. It is assumed that there is an information block $S = (s_0, s_1, \dots, s_{K-1})$ having an information size K . The LDPC encoder generates a codeword $\Lambda = (\lambda_0, \lambda_1, \lambda_2, \dots, \lambda_{N-1})$ having a size of $N = K + M_1 + M_2$ using the information block S having a size K . In this case, $M_1 = g$, and $M_2 = N - K - g$. Furthermore, M_1 is the size of parity bits

corresponding to the dual diagonal matrix B, and M_2 is the size of parity bits corresponding to the identity matrix D. The encoding process is performed, as follows:

[0065] Initialization:

$$\begin{aligned} \lambda_i &= s_i \text{ for } i = 0, 1, \dots, K-1 \\ p_j &= 0 \text{ for } j = 0, 1, \dots, M_1 + M_2 - 1 \end{aligned} \quad (4)$$

[0066] First information bit λ_0 is accumulated at parity bit addresses specified in the 1st row of the sequence of the Sequence Table. For example, in an LDPC code having a length of 64800 and a code rate of 7/15, an accumulation process is as follows:

$$\begin{aligned} P_{460} &= P_{460} \oplus \lambda_0 & P_{792} &= P_{792} \oplus \lambda_0 & P_{1007} &= P_{1007} \oplus \lambda_0 & P_{4580} &= P_{4580} \oplus \lambda_0 & P_{11452} &= P_{11452} \oplus \lambda_0 \\ P_{13130} &= P_{13130} \oplus \lambda_0 & P_{26882} &= P_{26882} \oplus \lambda_0 & P_{27020} &= P_{27020} \oplus \lambda_0 & P_{32439} &= P_{32439} \oplus \lambda_0 \end{aligned}$$

where the addition \oplus occurs in GF(2).

[0067] The subsequent $L-1$ information bits, that is, λ_m , $m = 1, 2, \dots, L-1$, are accumulated at parity bit addresses that are calculated by the following Equation 5:

$$\begin{aligned} (x + m \times Q_1) \bmod M_1 & \text{ if } x < M_1 \\ M_1 + \{(x - M_1 + m \times Q_2) \bmod M_2\} & \text{ if } x \geq M_1 \end{aligned} \quad (5)$$

where x denotes the addresses of parity bits corresponding to the first information bit λ_0 , that is, the addresses of the parity bits specified in the first row of the sequence of the Sequence Table, $Q_1 = M_1/L$, $Q_2 = M_2/L$, and $L = 360$. Furthermore, Q_1 and Q_2 are defined in the following Table 2. For example, for an LDPC code having a length of 64800 and a code rate of 7/15, $M_1 = 1080$, $Q_1 = 3$, $M_2 = 33480$, $Q_2 = 93$ and $L = 360$, and the following operations are performed on the second bit λ_1 using Equation 5:

$$\begin{aligned} P_{463} &= P_{463} \oplus \lambda_1 & P_{795} &= P_{795} \oplus \lambda_1 & P_{1010} &= P_{1010} \oplus \lambda_1 & P_{4673} &= P_{4673} \oplus \lambda_1 & P_{11545} &= P_{11545} \oplus \lambda_1 \\ P_{13223} &= P_{13223} \oplus \lambda_1 & P_{26975} &= P_{26975} \oplus \lambda_1 & P_{27113} &= P_{27113} \oplus \lambda_1 & P_{32532} &= P_{32532} \oplus \lambda_1 \end{aligned}$$

[0068] Table 2 illustrates the sizes of M_1 , Q_1 , M_2 and Q_2 of the designed QC-LDPC code:

Table 2

| Code rate | Length | Sizes | | | |
|-----------|--------|-------|-------|-------|-------|
| | | M_1 | M_2 | Q_1 | Q_2 |
| | | | | | |

| | | | | | |
|------|-------|------|-------|---|----|
| 7/15 | 64800 | 1080 | 33480 | 3 | 93 |
|------|-------|------|-------|---|----|

[0069] The addresses of parity bit accumulators for new 360 information bits from λ_L to λ_{2L-1} are calculated and accumulated from Equation 5 using the second row of the sequence.

[0070] In a similar manner, for all groups composed of new L information bits, the addresses of parity bit accumulators are calculated and accumulated from Equation 5 using new rows of the sequence.

[0071] After all the information bits from λ_0 to λ_{K-1} have been exhausted, the operations of the following Equation 6 are sequentially performed from $i = 1$:

$$p_i = p_i \oplus p_{i-1} \text{ for } i = 0, 1, \dots, M_1 - 1 \quad (6)$$

[0072] Thereafter, when a parity interleaving operation, such as that of the following Equation 7, is performed, parity bits corresponding to the dual diagonal matrix B are generated:

$$\lambda_{K+L \cdot t+s} = p_{Q_1 \cdot s+t} \text{ for } 0 \leq s < L, \quad 0 \leq t < Q_1 \quad (7)$$

[0073] When the parity bits corresponding to the dual diagonal matrix B have been generated using K information bits $\lambda_0, \lambda_1, \dots, \lambda_{K-1}$, parity bits corresponding to the identity matrix D are generated using the M_1 generated parity bits $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$.

[0074] For all groups composed of L information bits from λ_K to λ_{K+M_1-1} , the addresses of parity bit accumulators are calculated using the new rows (starting with a row immediately subsequent to the last row used when the parity bits corresponding to the dual diagonal matrix B have been generated) of the sequence and Equation 5, and related operations are performed.

[0075] When a parity interleaving operation, such as that of the following Equation 8, is performed after all the information bits from λ_K to λ_{K+M_1-1} have been exhausted, parity bits corresponding to the identity matrix D are generated:

$$\lambda_{K+M_1+L \cdot t+s} = p_{M_1+Q_2 \cdot s+t} \text{ for } 0 \leq s < L, \quad 0 \leq t < Q_2 \quad (8)$$

[0077] FIG. 4 is a block diagram illustrating an LDPC encoder according to an embodiment of the present invention.

[0078] Referring to FIG. 4, the LDPC encoder according to this embodiment of the present invention includes memory 310 and 320 and a processor 330.

[0079] The memory 310 is memory that is used to store an LDPC codeword having a length of 64800 and a code rate of 7/15.

[0080] The memory 320 is memory that is initialized to 0.

[0081] The memory 310 and the memory 320 may correspond to λ_i ($i = 0, 1, \dots, N-1$) and p_j ($j = 0, 1, \dots, M_1 + M_2 - 1$), respectively.

[0082] The memory 310 and the memory 320 may correspond to various types of hardware for storing sets of bits, and may correspond to data structures, such as an array, a list, a stack and a queue.

[0083] The processor 330 generates an LDPC codeword corresponding to information bits by performing accumulation with respect to the memory 320 using a sequence corresponding to a PCM.

[0084] In this case, the accumulation may be performed at parity bit addresses that are updated using the sequence of the above Sequence Table.

[0085] In this case, the LDPC codeword may include a systematic part $\lambda_0, \lambda_1, \dots, \lambda_{K-1}$ corresponding to the information bits and having a length of 30240 ($= K$), a first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ corresponding to a dual diagonal matrix included in the PCM and having a length of 1080 ($= M_1 = g$), and a second parity part $\lambda_{K+M_1}, \lambda_{K+M_1+1}, \dots, \lambda_{K+M_1+M_2-1}$ corresponding to an identity matrix included in the PCM and having a length of 33480 ($= M_2$).

[0086] In this case, the sequence may have a number of rows equal to the sum $(30240/360 + 1080/360 = 87)$ of a value obtained by dividing the length of the systematic part, that is, 30240, by a CPM size L corresponding to the PCM, that is, 360, and a value obtained by dividing the length M_1 of the first parity part, that is, 1080, by 360.

[0087] As described above, the sequence may be represented by the above Sequence Table.

[0088] In this case, the memory 320 may have a size corresponding to the sum $M_1 + M_2$ of the length M_1 of the first parity part and the length M_2 of the second parity part.

[0089] In this case, the parity bit addresses may be updated based on the results of comparing each x of the previous parity bit addresses specified in respective rows of the sequence with the length M_1 of the first parity part.

[0090] That is, the parity bit addresses may be updated using Equation 5. In this case, x may be the previous parity bit addresses, m may be an information bit index that is an integer larger than 0 and smaller than L , L may be the CPM size of the PCM, Q_1 may be M_1/L , M_1 may be the size of the first parity part, Q_2 may be M_2/L , and M_2 may be the size of the second parity part.

[0091] In this case, it may be possible to perform the accumulation while repeatedly changing the rows of the sequence by the CPM size L ($=360$) of the PCM, as described above.

[0092] In this case, the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ may be generated by performing parity interleaving using the memory 310 and the memory 320, as described in conjunction with Equation 7.

[0093] In this case, the second parity part $\lambda_{K+M_1}, \lambda_{K+M_1+1}, \dots, \lambda_{K+M_1+M_2-1}$ may be generated by performing parity interleaving using the memory 310 and the memory 320 after generating the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ and then performing the accumulation using the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ and the sequence, as described in conjunction with Equation 8.

[0094] FIG. 5 is a block diagram illustrating an LDPC decoder according to an embodiment of the present invention.

[0095] Referring to FIG. 5, the LDPC decoder according to this embodiment of the present invention may include a receiving unit 410 and a decoding unit 420.

[0096] The receiving unit 410 receives an LDPC codeword that has been encoded using a sequence that corresponds to a PCM and is represented by the above Sequence Table.

[0097] The decoding unit 420 restores information bits from the received LDPC codeword by performing decoding corresponding to the PCM.

[0098] In this case, the sequence may be used to update the parity bit addresses of the memory, and the parity bit addresses are used for accumulation that is performed to generate parity bits corresponding to the LDPC codeword.

[0099] In this case, the LDPC codeword may include a systematic part $\lambda_0, \lambda_1, \dots, \lambda_{K-1}$ corresponding to the information bits, a first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ corresponding to a dual diagonal matrix included in the PCM, and a second parity part $\lambda_{K+M_1}, \lambda_{K+M_1+1}, \dots, \lambda_{K+M_1+M_2-1}$ corresponding to an identity matrix included in the PCM.

[00100] In this case, the parity bit addresses may be updated based on the results of comparing each x of the previous parity bit addresses specified in respective rows of the sequence with the length M_1 of the first parity part.

[00101] That is, the parity bit addresses may be updated using Equation 5. In this case, x may be the previous parity bit addresses, m may be an information bit index that is an integer larger than 0 and smaller than L , L may be the CPM size of the PCM, Q_1 may be M_1/L , M_1 may be the size of the first parity part, Q_2 may be M_2/L , and M_2 may be the size of the second parity part.

[00102] FIG. 6 is an operation flowchart illustrating an LDPC encoding method according to an embodiment of the present invention.

[00103] Referring to FIG. 6, the LDPC encoding method according to this embodiment of the present invention initializes the first memory that stores an LDPC codeword having a length of 64800 and a code rate of 7/15, and second memory at step S510.

[00104] In this case, step S510 may be performed using Equation 4.

[00105] Furthermore, in the LDPC encoding method according to this embodiment of the present invention, an LDPC codeword corresponding to information bits is generated by performing accumulation with respect to the second memory using a sequence corresponding to a PCM at step S520.

[00106] In this case, the accumulation may be performed at parity bit addresses that are updated using the sequence corresponding to the PCM.

[00107] In this case, the LDPC codeword may include a systematic part $\lambda_0, \lambda_1, \dots, \lambda_{K-1}$ corresponding to the information bits and having a length of 30240 ($= K$), a first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ corresponding to a dual diagonal matrix included in the PCM and having a length of 1080 ($= M_1 = g$), and a second parity part

$\lambda_{K+M_1}, \lambda_{K+M_1+1}, \dots, \lambda_{K+M_1+M_2-1}$ corresponding to an identity matrix included in the PCM and having a length of 33480 ($= M_2$).

[00108] In this case, the sequence may have a number of rows equal to the sum $(30240/360+1080/360=87)$ of a value obtained by dividing the length of the systematic part, that is, 30240, by a CPM size L corresponding to the PCM, that is, 360, and a value obtained by dividing the length M_1 of the first parity part, that is, 1080, by 360.

[00109] As described above, the sequence may be represented by the above Sequence Table.

[00110] In this case, the parity bit addresses may be updated based on the results of comparing each x of the previous parity bit addresses specified in respective rows of the sequence with the length M_1 of the first parity part.

[00111] That is, the parity bit addresses may be updated using Equation 5. In this case, x may be the previous parity bit addresses, m may be an information bit index that is an integer larger than 0 and smaller than L , L may be the CPM size of the PCM, Q_1 may be M_1/L , M_1 may be the size of the first parity part, Q_2 may be M_2/L , and M_2 may be the size of the second parity part.

[00112] In this case, it may be possible to perform the accumulation while repeatedly changing the rows of the sequence by the CPM size $L (=360)$ of the PCM, as described above.

[00113] In this case, the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ may be generated by performing parity interleaving using the memory 310 and the memory 320, as described in conjunction with Equation 7.

[00114] In this case, the second parity part $\lambda_{K+M_1}, \lambda_{K+M_1+1}, \dots, \lambda_{K+M_1+M_2-1}$ may be generated by performing parity interleaving using the memory 310 and the memory 320 after generating the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ and then performing the accumulation using the first parity part $\lambda_K, \lambda_{K+1}, \dots, \lambda_{K+M_1-1}$ and the sequence, as described in conjunction with Equation 8.

[00115] FIG. 7 is a graph plotting the performance of a QC-LDPC code having a length of 64800 and a code rate of 7/15 according to an embodiment of the present invention against E_b/N_0 .

[00116] The graph illustrated in FIG. 7 illustrates results that were obtained on the assumption that a log-likelihood ratio (LLR)-based sum-product algorithm in which binary phase shift keying (BPSK) modulation and 50 rounds of repetitive decoding were performed was used for computational experiments. As illustrated in FIG. 7, it can be seen that the designed code is away from the Shannon limit by about 0.6 dB at $\text{BER}=10^{-6}$.

[00117] At least one embodiment of the present invention has the advantage of providing a new LDPC codeword having a length of 64800 and a code rate of 7/15, which is capable of being used for general purposes.

[00118] At least one embodiment of the present invention has the advantage of providing an LDPC encoding technique that is capable of efficiently performing LDPC encoding using a sequence having a number of rows equal to a value that is obtained by dividing the sum of the length of the systematic part of an LDPC codeword, that is, 30240, and the length of the first parity part of the LDPC codeword, that is, 1080, by 360.

[00119] Although the specific embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

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CLAIMS:

1. A low density parity check (LDPC) decoder, comprising:

a receiving unit configured to receive an LDPC codeword having a length of 64800 and a code rate of 7/15, the LDPC codeword encoded using a sequence corresponding to a parity check matrix (PCM); and

a decoding unit configured to restore error-corrected bits from the received LDPC codeword by performing decoding corresponding to the parity check matrix.

2. The LDPC decoder of claim 1, wherein the sequence is represented by the following Sequence Table:

10

Sequence Table

1st row: 460 792 1007 4580 11452 13130 26882 27020 32439

2nd row: 35 472 1056 7154 12700 13326 13414 16828 19102

3rd row: 45 440 772 4854 7863 26945 27684 28651 31875

4th row: 744 812 892 1509 9018 12925 14140 21357 25106

15 5th row: 271 474 761 4268 6706 9609 19701 19707 24870

6th row: 223 477 662 1987 9247 18376 22148 24948 27694

7th row: 44 379 786 8823 12322 14666 16377 28688 29924

8th row: 104 219 562 5832 19665 20615 21043 22759 32180

9th row: 41 43 870 7963 13718 14136 17216 30470 33428

20 10th row: 592 744 887 4513 6192 18116 19482 25032 34095

11th row: 456 821 1078 7162 7443 8774 15567 17243 33085

12th row: 151 666 977 6946 10358 11172 18129 19777 32234

13th row: 236 793 870 2001 6805 9047 13877 30131 34252

14th row: 297 698 772 3449 4204 11608 22950 26071 27512

25 15th row: 202 428 474 3205 3726 6223 7708 20214 25283

16th row: 139 719 915 1447 2938 11864 15932 21748 28598

17th row: 135 853 902 3239 18590 20579 30578 33374 34045

18th row: 9 13 971 11834 13642 17628 21669 24741 30965

19th row: 344 531 730 1880 16895 17587 21901 28620 31957

30 20th row: 7 192 380 3168 3729 5518 6827 20372 34168

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21st row: 28 521 681 4313 7465 14209 21501 23364 25980
 22nd row: 269 393 898 3561 11066 11985 17311 26127 30309
 23rd row: 42 82 707 4880 4890 9818 23340 25959 31695
 24th row: 189 262 707 6573 14082 22259 24230 24390 24664
 5 25th row: 383 568 573 5498 13449 13990 16904 22629 34203
 26th row: 585 596 820 2440 2488 21956 28261 28703 29591
 27th row: 755 763 795 5636 16433 21714 23452 31150 34545
 28th row: 23 343 669 1159 3507 13096 17978 24241 34321
 29th row: 316 384 944 4872 8491 18913 21085 23198 24798
 10 30th row: 64 314 765 3706 7136 8634 14227 17127 23437
 31st row: 220 693 899 8791 12417 13487 18335 22126 27428
 32nd row: 285 794 1045 8624 8801 9547 19167 21894 32657
 33rd row: 386 621 1045 1634 1882 3172 13686 16027 22448
 34th row: 95 622 693 2827 7098 11452 14112 18831 31308
 15 35th row: 446 813 928 7976 8935 13146 27117 27766 33111
 36th row: 89 138 241 3218 9283 20458 31484 31538 34216
 37th row: 277 420 704 9281 12576 12788 14496 15357 20585
 38th row: 141 643 758 4894 10264 15144 16357 22478 26461
 39th row: 17 108 160 13183 15424 17939 19276 23714 26655
 20 40th row: 109 285 608 1682 20223 21791 24615 29622 31983
 41st row: 123 515 622 7037 13946 15292 15606 16262 23742
 42nd row: 264 565 923 6460 13622 13934 23181 25475 26134
 43rd row: 202 548 789 8003 10993 12478 16051 25114 27579
 44th row: 121 450 575 5972 10062 18693 21852 23874 28031
 25 45th row: 507 560 889 12064 13316 19629 21547 25461 28732
 46th row: 664 786 1043 9137 9294 10163 23389 31436 34297
 47th row: 45 830 907 10730 16541 21232 30354 30605 31847
 48th row: 203 507 1060 6971 12216 13321 17861 22671 29825
 49th row: 369 881 952 3035 12279 12775 17682 17805 34281
 30 50th row: 683 709 1032 3787 17623 24138 26775 31432 33626
 51st row: 524 792 1042 12249 14765 18601 25811 32422 33163

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52nd row: 137 639 688 7182 8169 10443 22530 24597 29039
 53rd row: 159 643 749 16386 17401 24135 28429 33468 33469
 54th row: 107 481 555 7322 13234 19344 23498 26581 31378
 55th row: 249 389 523 3421 10150 17616 19085 20545 32069
 5 56th row: 395 738 1045 2415 3005 3820 19541 23543 31068
 57th row: 27 293 703 1717 3460 8326 8501 10290 32625
 58th row: 126 247 515 6031 9549 10643 22067 29490 34450
 59th row: 331 471 1007 3020 3922 7580 23358 28620 30946
 60th row: 222 542 1021 3291 3652 13130 16349 33009 34348
 10 61st row: 532 719 1038 5891 7528 23252 25472 31395 31774
 62nd row: 145 398 774 7816 13887 14936 23708 31712 33160
 63rd row: 88 536 600 1239 1887 12195 13782 16726 27998
 64th row: 151 269 585 1445 3178 3970 15568 20358 21051
 65th row: 650 819 865 15567 18546 25571 32038 33350 33620
 15 66th row: 93 469 800 6059 10405 12296 17515 21354 22231
 67th row: 97 206 951 6161 16376 27022 29192 30190 30665
 68th row: 412 549 986 5833 10583 10766 24946 28878 31937
 69th row: 72 604 659 5267 12227 21714 32120 33472 33974
 70th row: 25 902 912 1137 2975 9642 11598 25919 28278
 20 71st row: 420 976 1055 8473 11512 20198 21662 25443 30119
 72nd row: 1 24 932 6426 11899 13217 13935 16548 29737
 73rd row: 53 618 988 6280 7267 11676 13575 15532 25787
 74th row: 111 739 809 8133 12717 12741 20253 20608 27850
 75th row: 120 683 943 14496 15162 15440 18660 27543 32404
 25 76th row: 600 754 1055 7873 9679 17351 27268 33508
 77th row: 344 756 1054 7102 7193 22903 24720 27883
 78th row: 582 1003 1046 11344 23756 27497 27977 32853
 79th row: 28 429 509 11106 11767 12729 13100 31792
 80th row: 131 555 907 5113 10259 10300 20580 23029
 30 81st row: 406 915 977 12244 20259 26616 27899 32228
 82nd row: 46 195 224 1229 4116 10263 13608 17830

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83rd row: 19 819 953 7965 9998 13959 30580 30754

84th row: 164 1003 1032 12920 15975 16582 22624 27357

85th row: 8433 11894 13531 17675 25889 31384

86th row: 3166 3813 8596 10368 25104 29584

5 87th row: 2466 8241 12424 13376 24837 32711.

3. The LDPC decoder of claim 2, wherein the LDPC codeword comprises a systematic part corresponding to information bits and having a length of 30240, a first parity part corresponding to a dual diagonal matrix included in the PCM and having a length of 1080, and a second parity part corresponding to an identity matrix included in the PCM and
10 having a length of 33480.

4. The LDPC decoder of claim 3, wherein the sequence has a number of rows equal to a sum of a value obtained by dividing a length of the systematic part, that is, 30240, by a circulant permutation matrix (CPM) size corresponding to the PCM, that is, 360, and a value obtained by dividing a length of the first parity part, that is, 1080, by the CPM size.

15 5. The LDPC decoder of claim 2, wherein the LDPC codeword is generated by performing accumulation with respect to a memory and the accumulation is performed at parity bit addresses that are updated using the sequence.

6. The LDPC decoder of claim 5, wherein the accumulation is performed while the rows of the sequence are being repeatedly changed by the CPM size of the PCM.

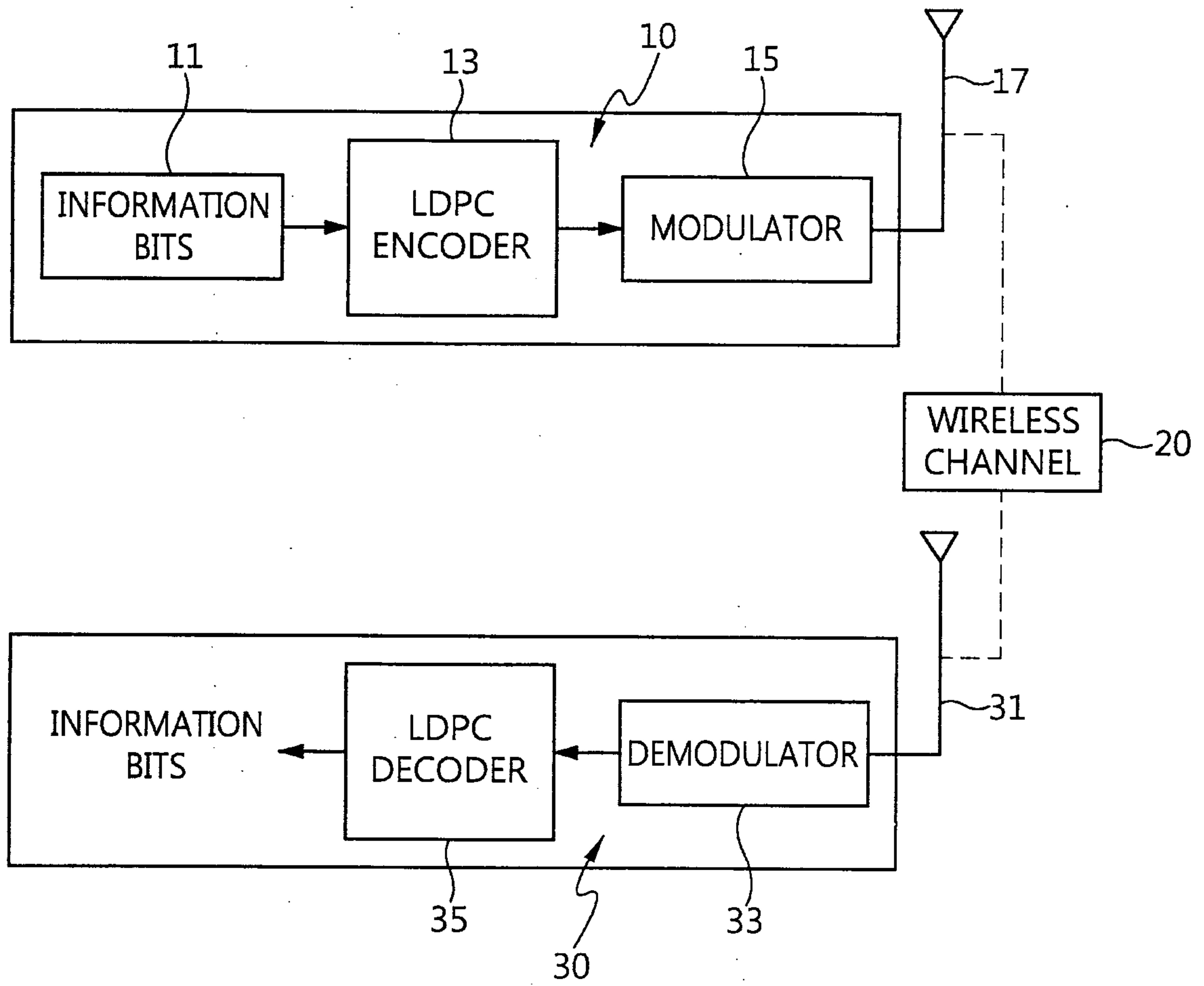


FIG. 1

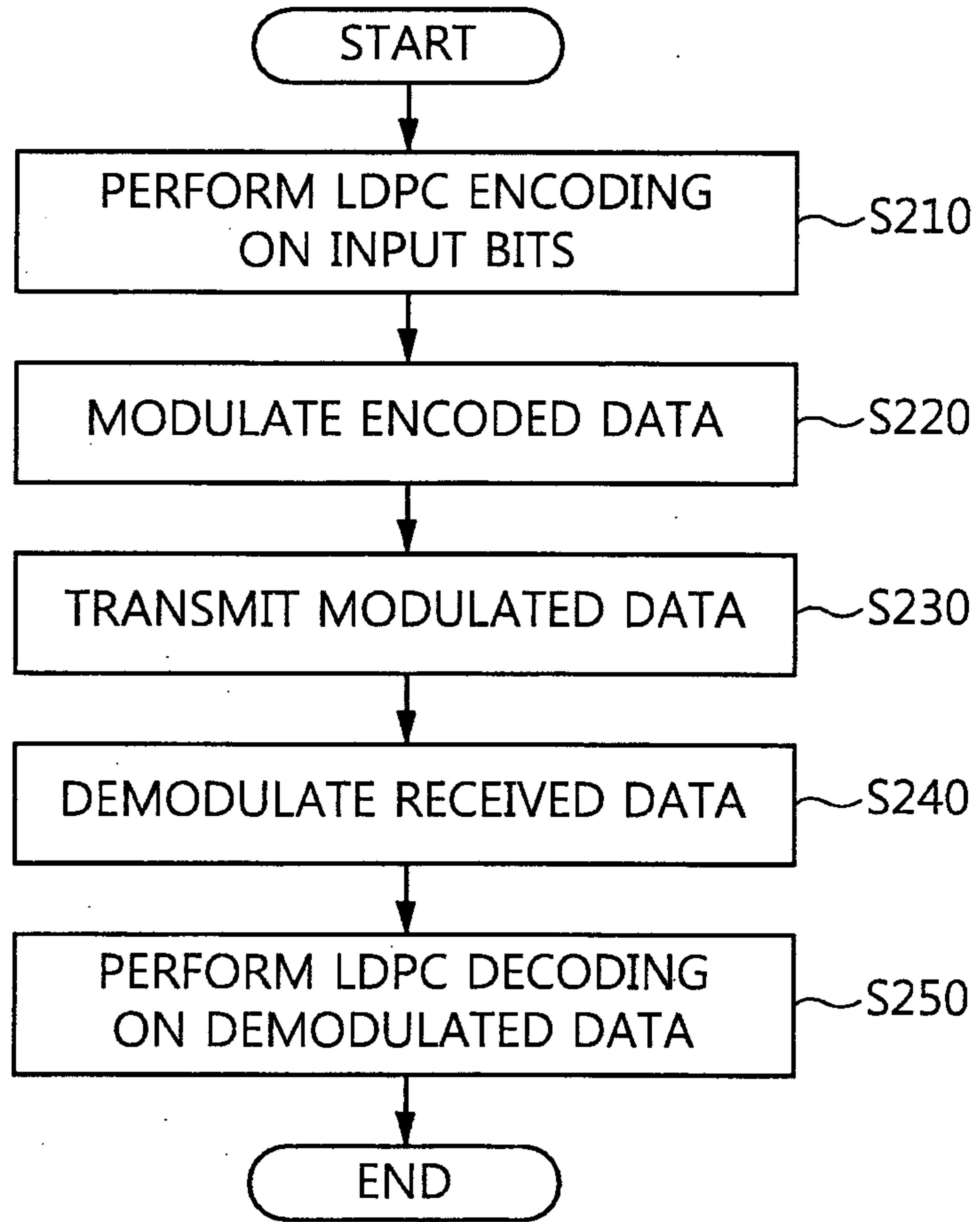


FIG. 2

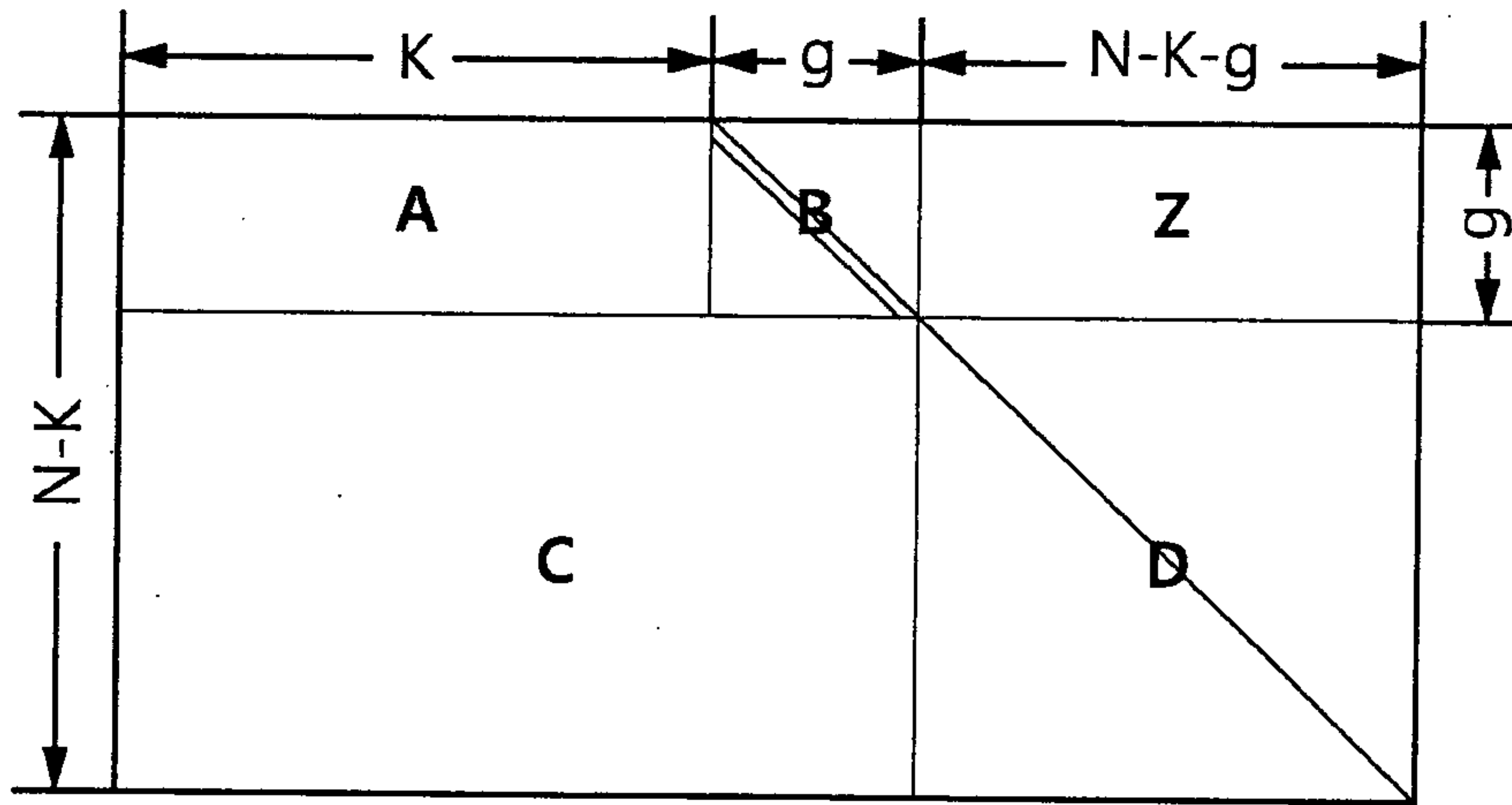


FIG. 3

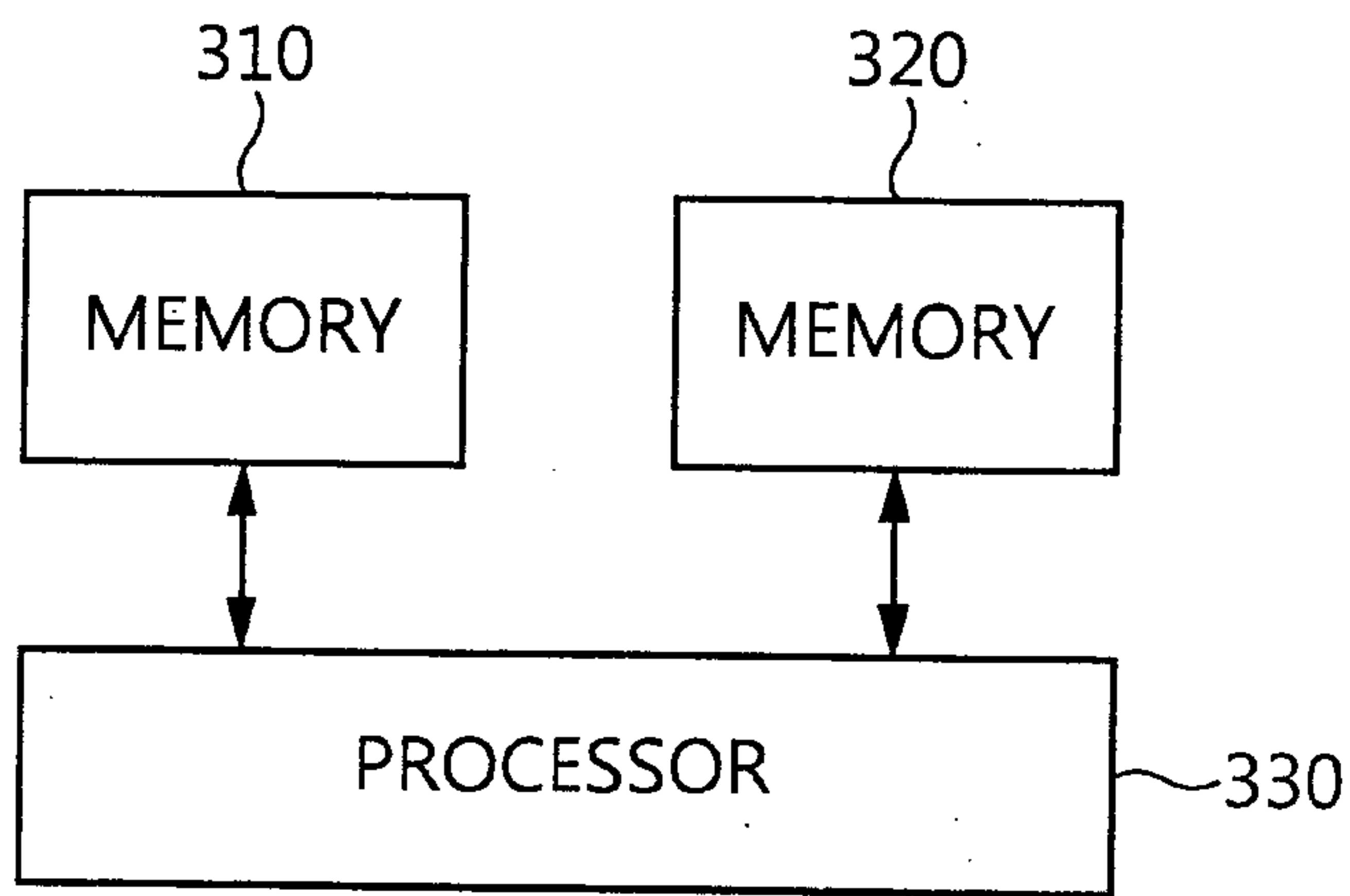


FIG. 4

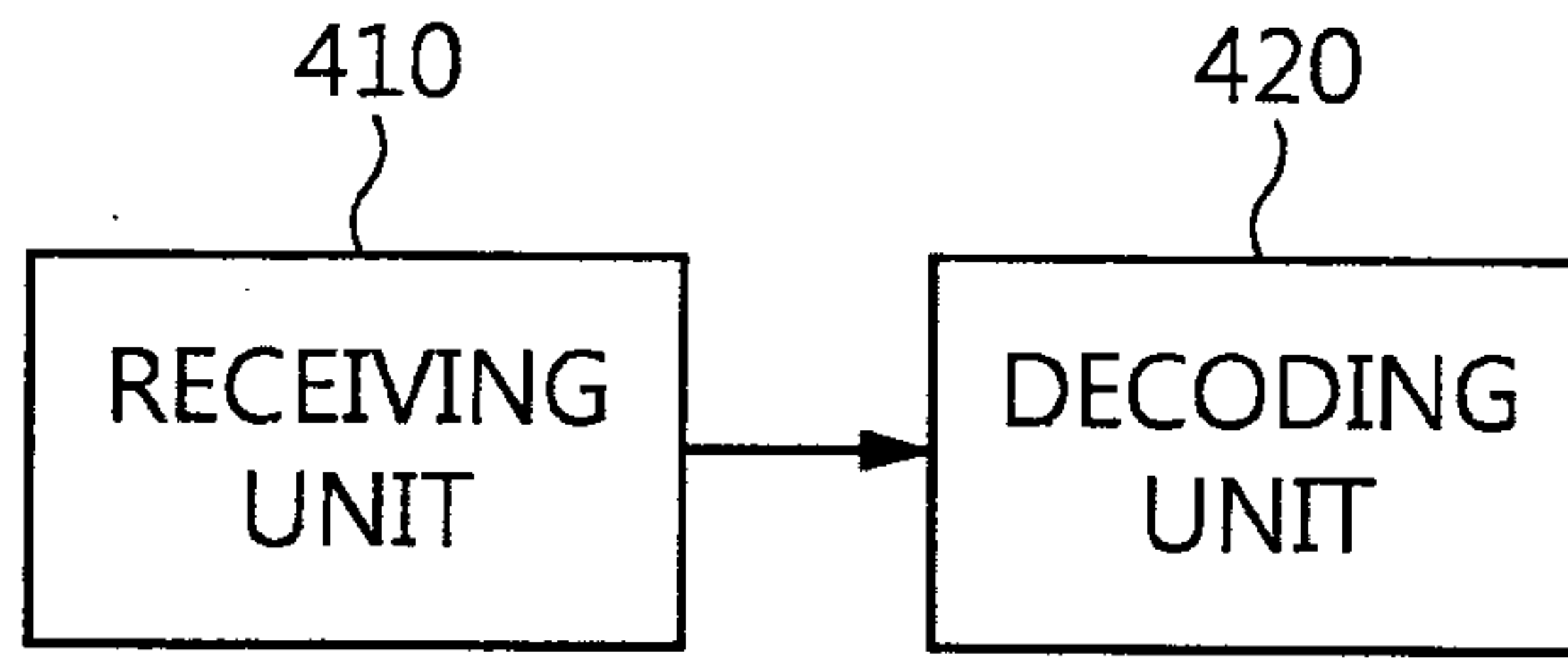


FIG. 5

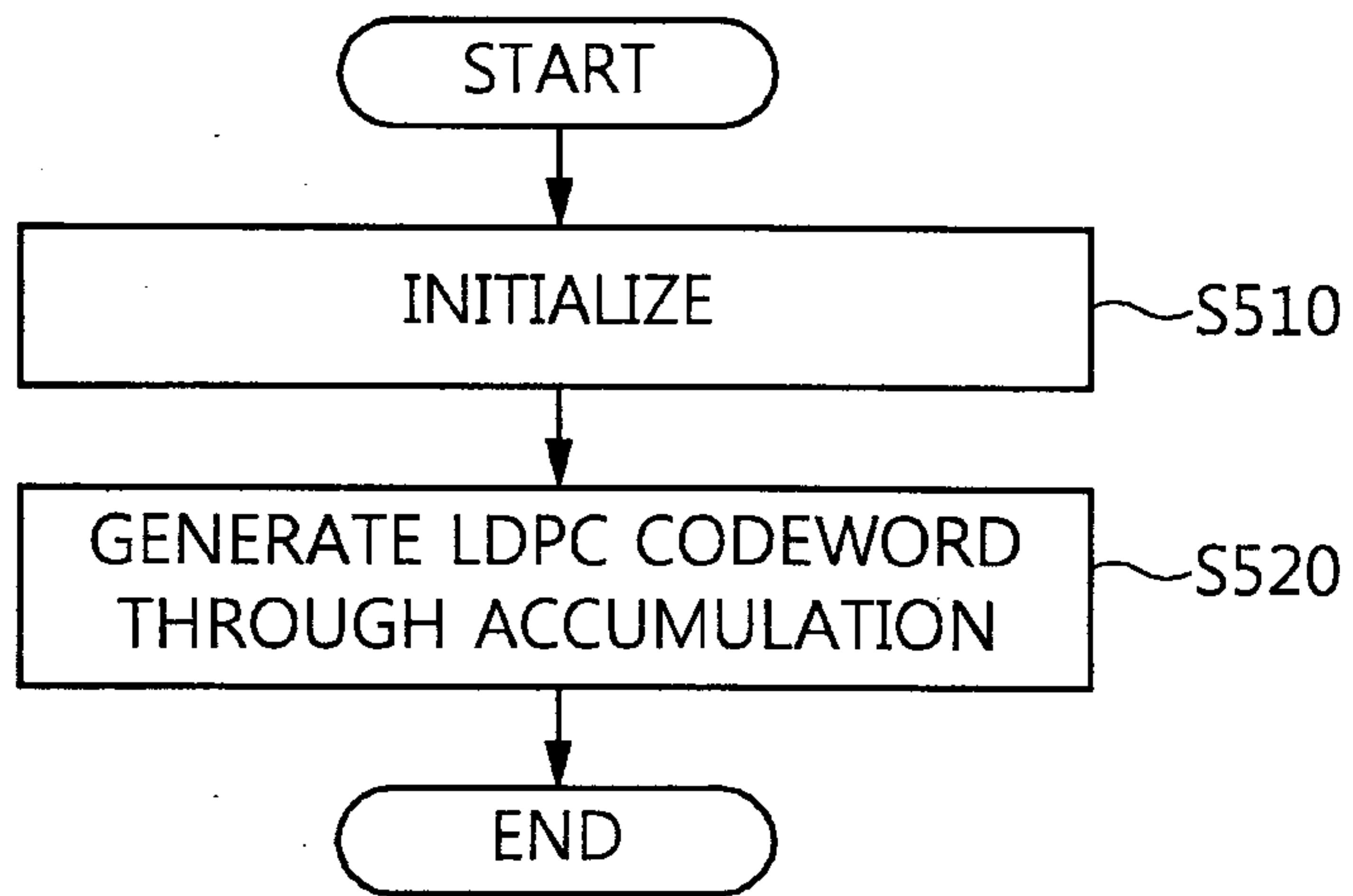


FIG. 6

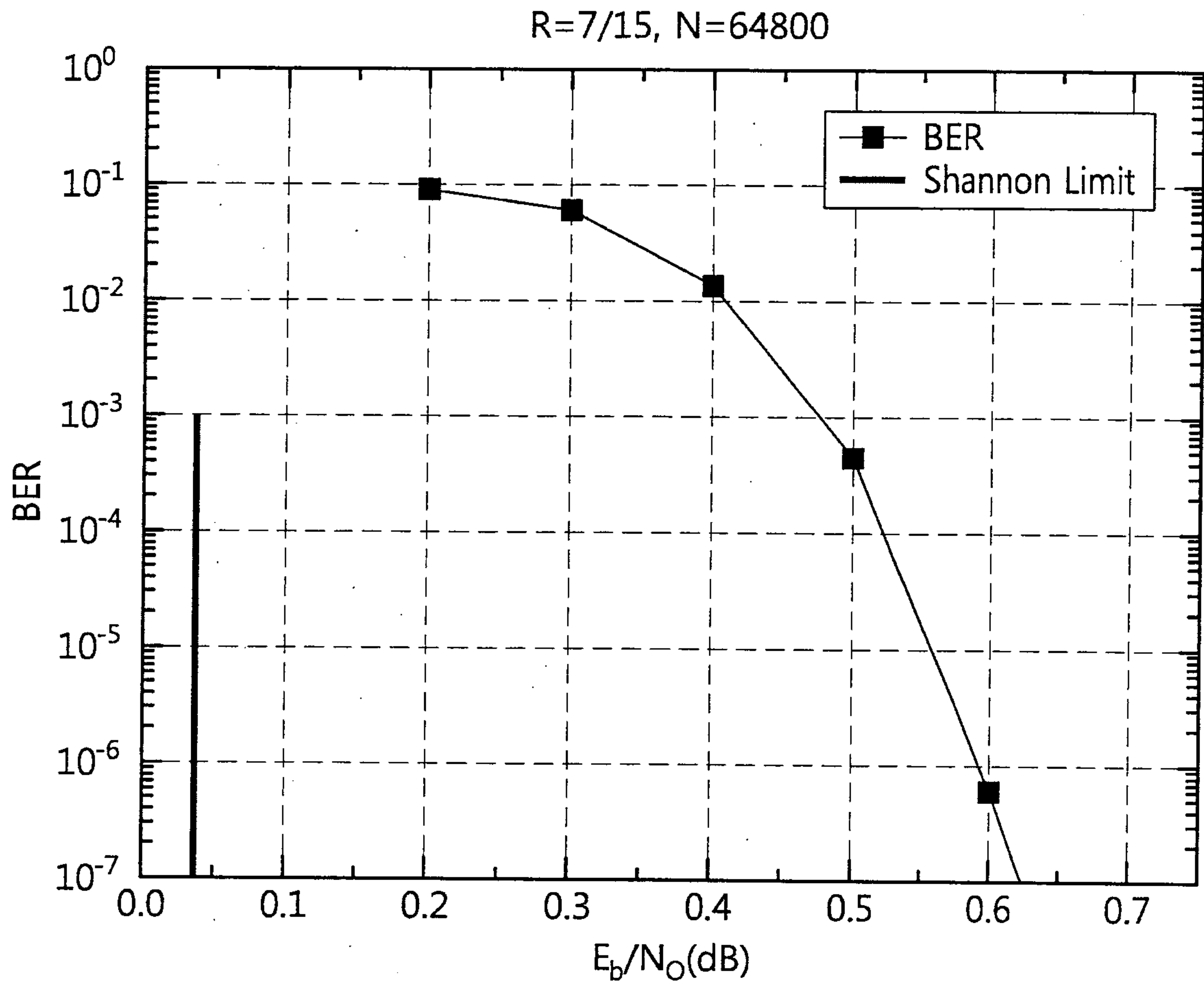


FIG. 7

