A matrix in which each row comprises a charge transfer register, a number of display elements equal to the number of register stages, and modulators responsive to information stored in each register for controlling the amount of excitation received by the display elements for that register.
Fig. 1

Fig. 3

Fig. 4
VERTICAL CLOCK PULSES

VERT SCAN PULSE (LINE 1)

HORIZONTAL CLOCK PULSES

GATED HORIZ. CLOCK LINE 1

POTENTIAL NODE 0₁

POTENTIAL NODE 0₂

POTENTIAL NODE 0₃

POTENTIAL NODE 0₄

POTENTIAL NODE 0₅

POTENTIAL NODE 0₆

SIGNAL ON 1st MODULATOR GATE

ZERO SIGNAL 2nd MODULATOR GATE

SIGNAL ON 3rd MODULATOR GATE

Fig. 6
CHARGE-TRANSFER DISPLAY SYSTEM

There are many types of display systems in which the signal information arrives in serial fashion and is to be displayed in parallel. Television is one example. This application deals with a solid state display of this general type and which is self-scanned.

The invention is illustrated in the drawings of which:

FIG. 1 is a block diagram of one embodiment of the present invention;

FIG. 2 is a block and schematic circuit diagram of an embodiment of the invention;

FIG. 3 is a schematic diagram of a switch which may be used in the circuit of FIG. 2;

FIG. 4 is a schematic diagram of a modified portion of the circuit of FIG. 2;

FIG. 5 is a block and schematic circuit diagram of another form of the invention; and

FIG. 6 is a drawing of waveforms for the operation of the circuit of FIG. 2.

The system shown in FIG. 1 includes a charge transfer register 10 which receives input information from signal source 12. The register 10 may be one of the bucket brigade type or of the charge-coupled device (CCD) type. The shift voltage source 14 connected to the register supplies the shift voltages necessary to transfer the stored information. In the embodiment illustrated in FIG. 2, the shift voltage source is a bipolar horizontal clock voltage source (the voltage swings both positive and negative relative to ground). However, in other embodiments of the invention, the shift voltage source may be a two, three or four or more phase power supply.

The stages of the charge transfer register (FIG. 1) connect to the control elements of a plurality of modulator elements. These are illustrated by the single block 16. Each modulator element is connected to a display element, the group of display elements being shown schematically by the single block 18. Power supply 20 connects through the respective modulator elements to the respective display elements of block 18.

In the operation of the system illustrated in FIG. 1, the video signal source 12 supplies video information to the input stage of the charge transfer register 10. The shift voltage source 14 shifts this video information from stage to stage until the register is fully loaded. Each shift stage connects to the control element of a modulator. Each modulator element, in turn, controls the amount of excitation, provided by the power supply 20, which reaches the display element connected to that modulator element.

The power supply 20 may be maintained effectively in the off condition during the shifting of the charge into the charge transfer register. However, when the register is fully loaded, the power supply 20 effectively turns on and supplies power through each modulator element to the display element connected to that modulator element. The amount of power, as implied above, will depend upon the amount of charge signal stored at the charge transfer stage for the particular display element.

While the circuit of FIG. 1 illustrates only a single charge transfer register and the modulator and display elements associated with that register, it is to be appreciated that the invention is equally applicable to a larger array of such elements. In such an array, there may be a plurality of charge transfer registers and separate modulator elements 16 and display elements 18 associated with each charge transfer register. This plurality of elements 10, 16 and 18 comprises the rows of the array.

A two row-by-three element array of the type discussed above is shown in FIG. 2. The charge transfer registers 10a and 10b are illustrated as bucket brigade register elements of the general type discussed in U.S. Pat. No. 3,683,193, titled "Bucket Brigade Scanning of Sensor Array", issued on Aug. 8, 1972 to the present inventor.

The vertical scan generator 102 corresponds to the like numbered element of FIG. 1 of the same patent. The horizontal clock signal source 112 also corresponds to the like numbered element in the same patent.

In addition to the above, the present system includes a video signal source 30 which connects through the conductive paths of N type transistors such as 30a and 30b to the rows of the array. The modulator elements may be P type insulated gate field effect transistors such as 32a. A gate electrode of a transistor such as 32a connects to a node 34a of the bucket brigade register. The source electrode of transistor 32a may connect to the modulator bias supply and the drain electrode through a display element 36a and switch 38a to power supply 40.

The various waveforms required for the operation of the systems of FIG. 2 are shown in FIG. 6. The video signal provided by source 30 is a time varying signal.

The operation of the system will be discussed by describing the operation of the first charge transfer register 10a. Upon the introduction of vertical synchronization (V-SYNCH) signal into the vertical scan generator and the occurrence of the clock B signal from the vertical clock source, a positive voltage V1 appears at node 40 of the bucket brigade scan generator 102 and a negative signal V2 remains at node 42. The signal V1 remains positive for one line time and then goes negative. When positive, V1 turns on N type transistor 44. The bipolar clock pulses from the horizontal clock supply 112 now are transmitted by the stage 44, 46 and are applied without polarity inversion to alternate transistors in the register. Electrons from the video signal source 30 are drawn into the register 10a through N type transistor 48 during the positive clock cycle. Transistor 30a serves to control the video signal or serves as an alternate video input gate. When the clock signal goes relatively negative, electrons are drawn from capacitor 49 via transistor 50 into capacitor 52. The charges remain in 52 until the positive clock cycle occurs again causing the negative charges to be drawn out of 52 and transmitted via transistor 54 to capacitor 56.

The process above continues until the entire register 10a is filled. When this occurs, the vertical clock A and clock B signals change polarity and cause the positive signal at node 40 to transfer to node 42. The voltage V1 becomes negative turning off transistor 44. The transistor 46 is connected to a negative bias source 45 and when transistor 44 goes off, transistor 46 causes node 47 and the clock bus connected thereto to be drawn negative, thereby turning off transistor 48 at the input to the register 10a. This isolates the charge transfer register 10a from further input of information. The video signal source 30, however, now supplies its information to the second charge transfer register 10b, the horizontal clock signal source 112 causing this information to shift into register 10b.

Returning to charge transfer register 10a, after it is loaded and the two input transistors 44 and 48 turned
off, the switch 38a is closed. This switch may be, for example, a P type transistor such as shown in FIG. 3. The signal \( V_i \) applied to the gate electrode of this transistor (this is the signal from node 40 of the vertical scan generator) switches to a relatively negative value after register 10a is loaded, effectively closing this switch. However, during the time the register 10a is being loaded, \( V_i \) is positive, opening switch 38a, effectively disconnecting the power supply 40 from the display elements.

When this switch 38a closes, the power supply 40 supplies power through the respective display elements such as 36a and through the modulator elements such as 32a to the return bias supply. The power supply 40 may be a direct voltage level, which in the case illustrated, would be a negative level. The amount of current that flows through a display element will depend upon the voltage at the gate electrode of its modulator element. When this gate electrode is relatively more negative, more current will flow through the display element and when it is relatively more positive, less current will flow through the display element.

The display elements which are illustrated in block form in FIG. 2 may take any one of a number of different forms. Examples include liquid crystal elements, electroluminescent elements, light emitting diodes and so on.

An important feature of the present circuit is that the small amount of signal available at the respective stages of a charge transfer register such as 10a can control the substantially larger amount of power provided by supply 40. Another feature of the circuit is that power is supplied to a row of elements continuously except for the time that new information is being transferred into the charge transfer register for that row. Thus, for example, in a 500 line display, power will be supplied to the display elements for 499 of the 500 line times. What this means, in effect, is that the display can be of high brightness because the eye integrates the light output of the elements of the display.

Another feature of the present system is that because the display elements are effectively turned off during the shifting of new information into the display, there is no blurring of the display due to the input of information.

In the example discussed above, it is suggested that the power supply 40 may be a direct voltage power supply. However, in some instances, such as in the case of liquid crystal display elements, it is preferred to employ alternating voltage excitation to extend the lifetime of the liquid crystal. FIG. 4 illustrates one way this may be done. It illustrates only a single display location; however, it is to be understood that the others are identical.

The modulator, rather than comprising a single transistor such as 32a, comprises a dual transmission gate. Such a gate, as is well understood in the art, comprises a N type transistor 770 and a P type transistor 72, the conduction paths of these transistors being connected in parallel. A node such as 34a connects directly to the gate electrodes of P type transistor 70 and through an inverter 74 to the gate electrode of N type transistor 72. One end of the parallel connected conduction paths connects to a point of reference potential, such as the return bias supply (which in this example may be ground), and the other end of conduction paths connect to one terminal of a liquid crystal display element. The other terminal of the liquid crystal display element connects through a switch 76 (corresponding to the switch 38 of FIG. 2), which is common to the entire row, to the alternating current power supply 78. In the case of a liquid crystal display element, this power supply may be at a relatively low frequency such as the ordinary 60 Hz power frequency.

The switch 76 may comprise a dual transmission gate of the same type as already discussed. For the case of register 10a, the dual transmission gate connects to node 40 of the vertical scan generator of FIG. 2 and receives the voltage \( V_i \). During the register 10a line time, the voltage \( V_i \) is relatively positive so that both the P and N type transistors of the switch 76 are off. During the remaining line times, \( V_i \) goes relatively negative and \( V_i \) relatively positive, turning on the dual transmission gate of switch 76. Thus, during these remaining row times, the 60 Hz source 78 supplies power to the liquid crystal through the conduction paths of transistors 70 and 72 in an amount depending upon the charge present at node 34a.

While a bucket brigade embodiment of the invention is illustrated in FIG. 2, it is of course to be understood that this is representative only. Clearly, the same approach is applicable to charged coupled devices and FIG. 1 is intended to be generic to such devices.

Another form of the invention is illustrated in FIG. 5. Here, the display element, which in the embodiment illustrated comprises a liquid crystal display element, serves also as one of the charge storage elements of each bucket brigade stage.

The operation of the circuit of FIG. 5 is the same as that of a conventional bucket brigade circuit. However, after each row is loaded, the respective liquid crystal elements of that row scatter light to an extent proportional to the charge that liquid crystal element is storing. In this circuit, as in the FIG. 2 circuit, after the completion of a row scan time, the vertical scan generator turns the clock gate transistor, such as 79, for that row off and the liquid crystal elements continue to scatter light for the remaining row times (providing the frame time is sufficiently long so that the liquid crystal elements retain charge).

A disadvantage of the circuit of FIG. 5 is that during the refreshing of each row with new information, the image present in a row becomes blurred due to the moving charge pattern across the liquid crystal elements of that row. The blurred component of the image is only 0.2 percent, however, for an array having 500 lines. Another drawback to the system of FIG. 5 is that the capacitance of the liquid crystal element must be carefully chosen to be compatible with that of the conventional capacitors of the bucket brigade register. Also, in the case of liquid crystal, the direct voltage component across the liquid crystal adversely affects the liquid crystal life. In other forms of solid state display elements this disadvantage is not present.

While the circuit in FIG. 5 has been illustrated in terms of liquid crystal elements it is to be understood that other display elements exhibiting capacitance may be employed instead.

What is claimed is:

1. In combination: a multiple-stage, charge-transfer analog signal shift register having an input terminal; means coupled to said terminal for supplying analog signals thereto;
3,866,209

5 a plurality of analog signal display elements equal to
the number of stages in said charge transfer regis-
ter,
a plurality of modulator elements, also equal in num-ber to the number of charge transfer stages, each
modulator element connected to a different charge
transfer stage and each controlled by the charge
stored in that charge transfer stage; and
means for supplying power to each display element
through its modulator element.
2. In the combination as set forth in claim 1, said
charge-transfer register comprising a bucket brigade
register.
3. In the combination as set forth in claim 1, said
charge transfer register comprising a charge-coupled
device register.
4. In the combination as set forth in claim 1, further
including means for preventing the application of
power to said display elements during the shifting
of signals into said register.
5. A display system comprising, in combination:
a shift register comprising a row of charge storage el-
mements, at least two per stage;
means for shifting charge signal from storage element
to storage element of said row; and
one storage element of each stage comprising a dis-
play element.
6. A display system as set forth in claim 5 wherein
said display elements comprise liquid crystal elements.
7. A display system as set forth in claim 5, further in-
cluding in said register one semiconductor device per
storage element, each device having a conduction path
connected between two storage elements, and a control
electrode for controlling the conductance of the con-
duction path, each storage element being connected
between one end of the conduction path of a semicon-
ductor device and the control electrode of that device.
8. In combination:
a multiple-stage analog signal shift register;
a plurality of display elements equal to the number of
stages in said register, each display element for pro-
ducing an analog output proportional to the ampi-
itude of the excitation it receives;
a plurality of modulator elements, also equal in num-er to the number of stages in said register, each
modulator element connected to a different register
stage and each controlled by the analog signal
stored in that register stage; and
means separate from said register for supplying
power to each display element through its modula-	or element.
9. In the combination as set forth in claim 8, further
including a source of video signals coupled to the input
terminal of said shift register for supplying to the regis-
ter the analog signals to be stored.
10. In the combination as set forth in claim 9, each
modulator element comprising semiconductor means
having a transmission path and a control electrode, said
transmission path connected between a display element
and said means for supplying power and said control
element connected to one of said shift register stages.
11. In the combination as set forth in claim 9, said
display element comprising liquid crystal display ele-
ments.