(54) Title: SHORT-PROTECTED BUFFER CIRCUIT

A short-protected buffer circuit comprising a source current output transistor (T1, Fig. 3) and a sink current output transistor (T2) is capable of providing high output current at low output voltage. A current-limiting bypass circuit, comprising two series-connected field effect transistors (T3 and T4) and a voltage reference (T5 and T6), limits the gate voltage on the source current output transistor (T1) and thus limits the output source current. The circuit is compact and can be implemented in integrated circuit form. The output voltage at which protection starts is independent of temperature and of process variations.
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SHORT-PROTECTED BUFFER CIRCUIT

Technical Field

This invention relates generally to a buffer circuit suitable for implementation in an integrated circuit, and, in particular, to a buffer circuit which provides a current limiting protection to the output transistors.

Background of the Invention

In the design of integrated circuits it is known to provide output buffer circuits between signals internal to the integrated circuit and signals off-chip. Since it is generally undesirable to have large current signals within the integrated circuit, as large currents can inhibit the ability of the chip to dissipate heat as well as the operational speed of the circuits internal to the chip, a significant function performed by output buffer circuits is to translate the relatively low current on-chip signals into relatively large current off-chip signals.

Certain applications of integrated circuits require the generation of output signals having relatively low voltage and relatively high current. Prior art output buffers have not been able to provide signals to these specifications without utilizing large on-chip devices.

For example, referring to FIG. 1, there is shown a prior art short-protected output buffer. The circuit comprises a constant current source in the form of depletion mode transistor T7, whose drain is connected to a supply voltage, whose source is connected to its gate, to the drain of inverter transistor T8, and to the gate of source current output transistor T1. The input at lead 5 is connected to the gate of inverter T8 and to the gate of sink current output transistor T2. The output is taken off
lead 10. A large on-chip diffused resistor R is connected between the drain of transistor T1 and the supply voltage.

An input signal at a given logic level (binary 1 or 0) is inverted by transistors T8 and T2. For example, if the input is 1, then T8 and T2 will be conductive. The gate voltage on T1 will be low, rendering it non-conductive, and output lead 10 will be shunted to ground through T2. If the input is 0, then T8 and T2 will be non-conductive. The gate voltage on T1 will be high, so that T1 will be conductive, and thus output lead 10 will be high.

It will be understood by one of ordinary skill in the art that regarding enhancement mode transistors, such as T1, T2, and T8, the transistor is rendered conductive when the gate-to-source voltage is equal to or exceeds the threshold voltage $V_{TH}$. When the gate-to-source voltage is just equal to $V_{TH}$, the transistor is soft conducting, i.e. just beginning to conduct. As the gate-to-source voltage is increased, the drain-to-source current increases until eventually a limit is reached beyond which the transistor is damaged due to current flow beyond its limits.

Regarding the output buffer shown in FIG. 1, let us assume that $V_{TH}$ of T1 is 1.0 volts, and let us assume that the input is a logical 0. Let us further assume that the output voltage on lead 10 is 5.0 volts, and that transistor T7 is supplying a full 5.0 volts on lead 7 to the gate of T1. Under these conditions the gate-to-source voltage across T1 is 0.0 volts, and T1 is non-conductive.

If the output voltage on lead 10 is 4.0 volts, then the gate-to-source voltage across T1 is 1.0 volts, and T1 just begins to turn on.

If the input at lead 5 has just switched from 1 to 0, the voltage on lead 7 has quickly risen to 5.0 volts, while the voltage on lead 10 remains at ground potential. Thus the gate-to-source voltage across T1 is approximately 5.0 volts, so T1 is turned hard on.
Still regarding the prior art circuit shown in FIG. 1, the source current output transistor T1 is protected against excessive drain-to-source current by resistor R. However, this resistor limits the drain-to-source current of T1, so that the output current is also limited. In order to generate high output current, very large output transistors T1 and T2 and a very large resistor R must be provided. But these large devices result in a large, expensive integrated circuit. Also the resultant integrated circuit has high power consumption.

FIG. 2 shows another prior art short-protected buffer circuit. The circuit shown in FIG. 2 is identical to that shown in FIG. 1, except that bypass transistors T3 and T4 are series-connected between the gate of transistor T1 and the output lead 10. T3 and T4 are connected as diodes, with their gates connected to their respective drains. When the drain-to-source voltage drop across both T3 and T4 (i.e. between the gate of T1 and output lead 10) is equal to the sum of their threshold voltages, T3 and T4 are both turned on. That is, the forward voltage is equal to the sum of their threshold voltages, so each diode turns on. As a result, the gate-to-source voltage on T1 cannot exceed a voltage which is equal to the 5.0 volt supply voltage less two times V_{th}. Thus a limit is imposed on the gate-to-source voltage on T1, and as a consequence a limit is imposed on the maximum output current.

A major disadvantage of the prior art circuit shown in FIG. 2 is that the protective action begins while the output voltage is still at too high a value. As mentioned above, certain applications require a relatively high output current at a relatively low output voltage, while still maintaining a limit on the output current. To achieve this result using the circuit shown in FIG. 2, output transistor T1 would have to be greatly enlarged, and the resulting integrated circuit would also be greatly enlarged and therefore more expensive.
The present invention overcomes the disadvantages associated with the above-described prior art output buffer circuits.

Brief Summary of Invention

Accordingly, it is an object of the present invention to provide an improved short-protected buffer circuit.

It is also an object of the present invention to provide a short-protected buffer circuit which can provide relatively high output current levels even at low output voltage levels.

It is a further object of the present invention to provide a short-protected buffer circuit which does not require implementation using large integrated circuit devices.

It is yet another object of the present invention to provide a short-protected buffer circuit whose operation is stable and independent of temperature or process variations.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing a short-protected buffer circuit having an input and an output, the circuit comprising a voltage source, the voltage source being at a certain potential relative to ground; a source current output transistor having a drain coupled to the voltage source, a source coupled to the output, and a gate; a sink current output transistor having a drain coupled to the output, a source coupled to ground, and a gate; and a protection circuit for protecting the output transistors from excessive current, the protection circuit comprising a voltage reference; a third transistor having a drain coupled to the gate of the source current output transistor, a source, and a gate coupled to its drain; and a fourth transistor having a drain coupled to
the source of the third transistor, a source coupled to the output, and a gate coupled to the voltage reference.

Brief Description of the Drawings

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows a prior art short-protected buffer circuit.

FIG. 2 shows another prior art short-protected buffer circuit.

FIG. 3 shows a circuit diagram of a preferred embodiment of the short-protected buffer circuit of the present invention.

FIG. 4 shows an equivalent circuit to that shown in FIG. 3 for ease in understanding the operation of the FIG. 3 circuit.

FIG. 5 shows a graph of output current versus output voltage regarding the preferred embodiment.

FIG. 6 shows a graph of the gate voltage on transistor T1 of the preferred embodiment versus the output voltage.

Detailed Description of the Invention

FIG. 3 shows a circuit diagram of a preferred embodiment of the short-protected buffer circuit of the present invention.

The circuit shown in FIG. 3 differs from that shown in FIG. 2 in at least one significant way. In FIG. 3, transistor T4 is not connected as a diode, as in FIG. 2, but rather is operated as a transistor to whose gate is applied a reference voltage.
The reference voltage is provided by transistor pair T5 and T6. T5 is a depletion mode transistor whose drain is connected to a voltage source, which in the preferred embodiment is 5.0 volts. The source and gate of T5 are connected together and to the gate of T4. Transistor T6 is an enhancement mode transistor whose drain is connected to its gate and to the source of T5, and whose source is coupled to ground.

Operation of Preferred Embodiment

FIG. 4 shows an equivalent circuit to that shown in FIG. 3 for ease in understanding the operation of the FIG. 3 circuit. Regarding FIG. 3, when the input on lead 5 is low, then T8 and T2 are off, so the current source provided by T7 can be shown in equivalent fashion as G1 in FIG. 4, and T8 and T2 can be deleted. In FIG. 3, T3 is operating as a diode, whose equivalent diode D is shown in FIG. 4. Also in FIG. 3, T5 and T6 are operating as a voltage source, represented by voltage source 12 in FIG. 4.

In FIG. 4, diode D has a forward voltage $V_{TE}$, which is defined as the voltage required to just start conduction in the forward direction (i.e. from the gate of T1 to the drain of T4) through D. Voltage source 12 is regulated to $V_{TE}$, where $V_{TE}$ is defined as the threshold voltage of an enhancement mode transistor, such as T4.

Let us assume that when $V_{TE}$ is 1.0 volts, T4 just starts to conduct, and that when $V_{TE}$ reaches 1.4 volts, T4 is fully conductive.

In FIG. 4 let us also connect a variable voltage source 14 to the output lead 10 in order to see how the protection circuit operates as the output voltage changes. T1 will not be conductive unless its gate-to-source voltage is equal or greater than $V_{TE}$. Like T4, transistor T1 will just start to conduct when its gate-to-
source voltage is approximately 1.0 volts, and it will be fully conductive when the gate-to-source voltage reaches 1.4 volts.

Before we begin changing the variable voltage source to explore the operation of the protection circuit, let us look at FIGS. 5 and 6, which will also aid in understanding the operation of the preferred embodiment.

FIG. 5 shows a graph of output current versus output voltage, the output current being plotted on the Y-axis and the output voltage being plotted along the X-axis. The solid line 20 represents the plot for the present invention, while the dashed line 30 represents that for the FIG. 2 prior art circuit. From FIG. 5 it will easily be seen that in the present invention the output current is significantly higher at low output voltages than for the FIG. 2 prior art circuit.

FIG. 6 shows a graph of how the gate voltage on transistor T1 of the preferred embodiment varies with the output voltage. As in FIG. 5, the output voltage is plotted along the X-axis. The gate voltage on T1 is plotted on the Y-axis. Again the solid line 40 represents the curve for the present invention, and the dashed line 50 represents that for the FIG. 2 prior art circuit. It will also be seen from FIG. 6 that the output current limiting action in the present invention doesn't begin to occur until the output voltage drops to approximately 0.4 volts, as shown at point 41 on curve 40, whereas the limiting action in the FIG. 2 prior art circuit begins at approximately 2.6 volts, as shown by point 51 on curve 50.

Referring now to both FIGS. 4 and 5, let us set the variable voltage VS on lead 10 to 5.0 volts. Since the gate voltage on T4 is 1.4 volts, the gate-to-source voltage on T4 is 1.4 volts minus 5.0 volts, or -3.6 volts, so T4 is definitely non-conducting, since, as mentioned above, T4 conduction begins when its gate-to-source voltage is approximately +1.0 volts. Since T4 is non-conducting, the
gate voltage on T1 is 5.0 volts, and the gate-to-source voltage on T1 is 0.0 volts, so T1 is non-conducting. This
is confirmed in FIG. 5, which indicates no output current when the output voltage is 5.0 volts.

If voltage VS is now reduced to 4.0 volts, T4 is still non-conductive. However, T1 just begins to turn on, since
its gate-to-source voltage is approximately 1.0 volts.

As VS is lowered further, T1 turns on increasingly harder, and the output current rises accordingly, as shown
by curve 20 in FIG. 5.

When VS is lowered to 0.4 volts, the gate-to-source voltage across T4 is 1.4 minus 0.4, or approximately 1.0
volts, so T4 is just starting to turn on. The forward voltage across diode D is greater than its threshold
voltage, so it too becomes conductive. As a result, the potential on the gate of T1 is decreased. Thus 0.4 volts
is the value of the output voltage where the current limiting protection starts.

As VS is lowered still further below 0.4 volts, T4 turns on harder and harder, and the gate-to-source voltage
on T1 is reduced still further, thus causing the output current to decrease, as shown by curve 20 in FIG. 5.

When VS is lowered all the way to 0.0 volts, the gate-to-source voltage on T4 is equal to the reference
voltage on the gate of T4, or 1.4 volts. The potential on the drain of T4 is 1.4 volts, and the potential on the
anode of D is also 1.4 volts. So the maximum potential on the gate of T1 is twice VTp, or 2.8 volts, as shown in
FIG 6. The fact that the maximum potential on the gate of T1 is limited to twice VTp limits the output source
current.

It will be apparent to those skilled in the art that the disclosed Short-Protected Buffer Circuit may be
modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and
described above.
For example, the output voltage at which the current limiting protection starts can be changed. This may be done by changing the voltage reference supplied to the gate of T4 by T5/T6 by changing the size (i.e. the gate length and width) of T5. By changing the reference voltage on the gate of T4, the protection starting voltage is changed. For example, if the output current level of the circuit is found to be too high at 0.4 output volts, then the reference voltage can simply be changed from 1.4 volts to 1.5 volts, thereby increasing the protection starting voltage from 0.4 output volts to 0.5 output volts.

It will be noted that the protection starting voltage is determined by the difference between the reference voltage (approximately 1.4 volts) and the T4 threshold voltage (approximately 1.0 volt). Even if the threshold voltages are shifted, as a result of process variations, the reference voltage supplied by T5/T6 will shift in the same direction, so that the difference will remain constant. Thus the protection starting voltage will remain constant despite minor process variations which result in different thresholds on different wafers.

Likewise, the operating characteristics are not affected by variations in temperature, since such variations affect the reference voltage supplied by T5/T6 and the T4 threshold to the same extent, so that the difference again remains constant.

The present invention finds utility, for example, in a telephone control integrated circuit, but it will be understood that it may be implemented in many different forms depending upon the particular application required.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:
Claims

1. In a short-protected buffer circuit having an input and an output; a voltage source, said voltage source being at a certain potential relative to ground; a source current output transistor having a drain coupled to said voltage source, a source coupled to said output, and a gate; a sink current output transistor having a drain coupled to said output, a source coupled to ground, and a gate; the improvement characterized whereby there is further provided
   a protection circuit for protecting said output transistor from excessive current, said protection circuit comprising a voltage reference; a third transistor having a drain coupled to the gate of said source current output transistor, a source, and a gate coupled to its drain; and a fourth transistor having a drain coupled to the source of said third transistor, a source coupled to said output, and a gate coupled to said voltage reference.

2. The short-protected buffer circuit as recited in claim 1, wherein said voltage reference comprises
   a first depletion mode transistor having a drain coupled to said voltage source, a source coupled to the gate of said fourth transistor, and a gate coupled to its source; and
   a fifth transistor having a drain coupled to the source of said first depletion mode transistor, a source coupled to ground, and a gate coupled to its drain.

3. The short-protected buffer circuit as recited in claim 1, wherein said circuit comprises an inverter circuit, said inverter comprising
   a constant current source;
   a fifth transistor having a drain coupled to said constant current source and to the drain of said third
transistor, a source coupled to ground, and a gate coupled to said input.

4. The short-protected buffer circuit as recited in claim 3, wherein said constant current source comprises a second depletion mode transistor having a drain coupled to said voltage source, a source coupled to the gate of said source current output transistor, and a gate coupled to its source.

5. The short-protected buffer circuit as recited in claim 1, wherein said first through fourth transistors are enhancement mode field effect transistors.

6. The short-protected buffer circuit as recited in claim 3, wherein said first through fifth transistors are enhancement mode field effect transistors.
1 (Amended). In a short-protected buffer circuit having an input and an output; a voltage source, said voltage source being at a certain potential relative to ground; a source current output transistor having a drain coupled to said voltage source, a source coupled to said output, and a gate; a sink current output transistor having a drain coupled to said output, a source coupled to ground, and a gate; the improvement characterized whereby there is further provided
a protection circuit for protecting said source current output transistor from excessive current, said protection circuit comprising a voltage reference; a third transistor having a drain coupled to the gate of said source current output transistor, a source, and a gate coupled to its drain; and a fourth transistor having a drain coupled to the source of said third transistor, a source coupled to said output, and a gate coupled to said voltage reference.

2. The short-protected buffer circuit as recited in claim 1, wherein said voltage reference comprises
a first depletion mode transistor having a drain coupled to said voltage source, a source coupled to the gate of said fourth transistor, and a gate coupled to its source; and
a fifth transistor having a drain coupled to the source of said first depletion mode transistor, a source coupled to ground, and a gate coupled to its drain.

3. The short-protected buffer circuit as recited in claim 1, wherein said circuit comprises an inverter circuit, said inverter comprising
a constant current source;
a fifth transistor having a drain coupled to said constant current source and to the drain of said third
transistor, a source coupled to ground, and a gate coupled to said input.

4. The short-protected buffer circuit as recited in claim 3, wherein said constant current source comprises a second depletion mode transistor having a drain coupled to said voltage source, a source coupled to the gate of said source current output transistor, and a gate coupled to its source.

5. The short-protected buffer circuit as recited in claim 1, wherein said first through fourth transistors are enhancement mode field effect transistors.

6. The short-protected buffer circuit as recited in claim 3, wherein said first through fifth transistors are enhancement mode field effect transistors.
FIG. 1

PRIOR ART

FIG. 2

PRIOR ART
FIG. 3

FIG. 4
### INTERNATIONAL SEARCH REPORT

#### I. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both National Classification and IPC

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<th>INT. CL.</th>
<th>H02H 3/08; 3/20; 3/28</th>
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<td>U.S. Cl.</td>
<td>361/98; 307/448; 361/86; 307/450; 475</td>
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#### II. FIELDS SEARCHED

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<tr>
<th>Classification System</th>
<th>Classification Symbols</th>
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched:

23GP

#### III. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category</th>
<th>Citation of Document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to Claim No.</th>
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<td>Y</td>
<td>US, A, 4,347,447, (PROEBSTRING) 31 August 1982</td>
<td>1-17</td>
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<td>Y</td>
<td>US, A, 4,314,167, (GROVES, ET AL) 02 February 1982</td>
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<td>A</td>
<td>US, A, 4,175,620, (YU) 11 December 1979</td>
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<td>A</td>
<td>US, A, 3,749,936, (BELL) 31 July 1973</td>
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<td>A</td>
<td>US, A, 4,110,633, (BLASER, ET AL) 29 August 1978</td>
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<td>A</td>
<td>US, A, 4,096,398, (KHAYTAN) 20 June 1978</td>
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* Special categories of cited documents:
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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "Z" document member of the same patent family

#### IV. CERTIFICATION

<table>
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<th>Date of Mailing of this International Search Report</th>
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<td>16 FEB 1984</td>
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International Searching Authority:

ISA/US

Signature of Authorized Officer:

PATRICK SALCE
**Further Information Continued from the Second Sheet**

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<td>A</td>
<td>US,A, 4,275,313, (BOLL et al) 23 June 1981</td>
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<td>A</td>
<td>US,A, 3,407,339, (BOOHER) 22 October 1968</td>
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**Observations Where Certain Claims Were Found Unsearchable**

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. Claim numbers _______ because they relate to subject matter not required to be searched by this Authority, namely:

2. Claim numbers _______ because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

**Observations Where Unity of Invention Is Lacking**

This International Searching Authority found multiple inventions in this international application as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest
- The additional search fees were accompanied by applicant’s protest.
- No protest accompanied the payment of additional search fees.