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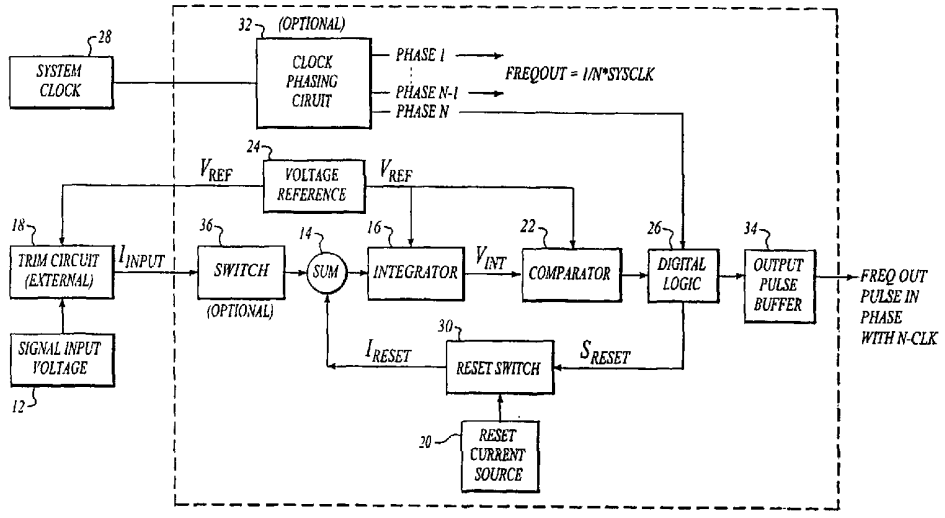

(57) Abstract: A multi-channel synchronous voltage-to-frequency converter (SVFC) realized in an integrated semiconductor circuit. The multi-channel SVFC having an operational amplifier adapted to receive an analog data signal to be converted and a reset signal, the operational amplifier intergrating the sum of the analog signal and the reset signal and generating an output signal as a function of the integrated sum; a comparator coupled to received the integrated sum and a reference level signal, the comparator outputting a logic level signal as a function of the received reference level signal; a digital logic circuit in response to an external clock signal, the digital logic circuit receiving the logic level signal and generating a reset control signal and a frequency output pulse as a function of the logic level signal; and a reset source switch receiving the reset control signal and outputting the reset signal.

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MULTI-CHANNEL PRECISION SYNCHRONOUS VOLTAGE-TO-FREQUENCY CONVERTER

This application claims the benefit of U.S. Provisional Application Serial No. 60/249,938, filed in the name of Douglas C. MacGugan on September 1, 2000, the complete disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to voltage-to-frequency converters, and in particular to a methods and apparatuses for providing multi-channel capability in a synchronous voltage-to-frequency converter realized in an integrated circuit.

BACKGROUND OF THE INVENTION

Several types of precision sensor systems are known that provide an analog signal output. In order to provide useful information to modern digital systems, the analog signal output of these precision sensors must be translated to digital format. Furthermore, many applications require the translation from analog to digital to be accomplished without loss of data during the conversion sequence. Typical applications requiring a "no-loss" conversion include, but are not limited to, Inertial Guidance and Navigation systems, Inertial Pointing Systems, and steering and attitude determination systems. Common successive approximation (SA) analog-to-digital converters (ADC) operate using a "hold" time, which is not compatible with such a no-loss conversion.

Analog to digital conversion without loss of signal during conversion also accommodates digital filtering techniques, such as averaging over multiple samples, wherein quantization errors are reduced much faster, *i.e*, by 1/N rather than $1/\sqrt{N}$, where: N is the number of samples used in averaging.

Voltage-To-Frequency Converters (VFC's) are a form of ADC that provide no-loss conversion. Different VFC's use different approaches to convert the analog signal directly into a frequency proportional to the signal. This frequency is then counted by

electronic counter means, usually in a processing or control system, to complete the digital output.

A synchronous VFC or SVFC is a form of VFC that is available for precision systems. Typically, the SVFC utilizes an external clock to synchronize the frequency output. The SVFC is more precise than the VFC because the counting method of the frequency is synchronized to the input clock of the VFC, which eliminates any errors on the counted digital output due to clock aging or other clock error effects. Any clocking error that does occur is a common mode error between the VFC and the counting electronics. This type of error is normally eliminated in the conversion process. Unfortunately, most available SVFC devices available have limited capability such that they can only handle one channel of analog conversion. Additionally, the available SVFC integrated devices typically consume large amount of power relative to the power consumption desired of a semiconductor circuit.

SUMMARY OF THE INVENTION

The present invention provides a synchronous voltage-to-frequency converter that overcomes the limitations of the prior art by providing a multi-channel capability in a synchronous voltage-to-frequency converter realized in an integrated semiconductor circuit that minimizes power consumption.

According to one aspect of the invention, the multi-channel synchronous voltage-to-frequency converter includes an integrator operational amplifier adapted to receive both an analog data signal to be converted and a reset signal, the integrator operational amplifier being structured to integrate the sum of the analog signal and the reset signal and to generate an output signal as a function of the integrated sum; a comparator coupled to receive the output signal of the integrator and a reference level signal, the comparator being structured to output a logic level signal as a function of the received reference level signal; a digital logic circuit responsive to an external clock signal, the digital logic circuit coupled to receive the logic level signal and being structured to generate a reset control signal and a frequency output pulse as a function of the logic level signal; and a reset source switch coupled to receive the reset control signal and being structured to output the reset signal as a function of the reset control signal.

According to another aspect of the invention, the multi-channel synchronous voltage-to-frequency converter may also include a trimming circuit coupled to an input of the integrator that is adapted to receive both an analog data signal to be converted and a reference voltage for trimming the analog data signal.

According to another aspect of the invention, the multi-channel synchronous voltage-to-frequency converter may also include a clock phasing circuit adapted to receive the external clock signal and to output the clock signal controlling the digital logic circuit, the clock phasing circuit being structured to phase a plurality of frequency output pulses generated by the digital logic circuit as a function of the number of channels of the multi-channel SVFC circuit. The clock phasing circuit may be a digital divider and phase shifter circuit.

According to another aspect of the invention, the multi-channel synchronous voltage-to-frequency converter may also include a self-test circuit coupled to an input to a summing junction of the operational amplifier between the summing junction and analog data signal to be converted. The self-test circuit may be implemented as a MOSFET switch structured to present an essentially zero impedance path for the analog data signal to be converted.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

Figure 1 shows the invention embodied as a multi-channel synchronous voltage-to-frequency converter having phased output pulses and an input self-test feature; and

Figure 2 shows a circuit that embodies the invention in a 4-phase implementation.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

In the Figures, like numerals indicate like elements.

The present invention is a multi-channel synchronous voltage-to-frequency converter having phased output pulses and an input self-test feature.

The present invention also provides a method of converting an analog signal to a digital signal without loss.

Figure 1 is a functional block diagram showing the invention embodied as a multi-channel SVFC (synchronous voltage-to-frequency converter) circuit 10, including optional phased output pulses and an optional input self-test feature. In Figure 1, an input analog data signal 12 to be converted is applied to a summing junction 14 of an integrator operational-amplifier 16, commonly referred to as an "op-amp." The input analog signal 12 is passed through a trimming circuit 18, implemented as a scaling and bias offset resistor array, and applied to the integrator op-amp 16 as a current I_{INPUT}. A reset signal current I_{RESET} from a reset current source 20 is also applied to the summing junction 14. In normal operation, the integrator will integrate the sum of the analog signal current I_{INPUT} and the reset current I_{RESET}.

The output of the integrator op-amp 16 is a voltage V_{INT} that is applied to a fast response comparator 22. The comparator 22 is set to trigger at a level established by a precision voltage reference generator 24 outputting a precision voltage reference V_{REF}. The precision voltage reference V_{REF} establishes the trigger level for the comparator 22 and the non-inverting input reference of the input op-amp 16. The precision voltage reference V_{REF} also provides the scaling and bias voltage of the trimming circuit 18. This method of using the same precision voltage reference V_{REF} for all three circuits: the op-amp 16, the trimming circuit 18, and the comparator 22, makes the frequency output of the device immune to drift or changes in the precision voltage reference device 24.

The output of the comparator 22 is a logic level signal that is applied to a digital logic circuit 26 consisting mainly of flip-flop logic and clocked by an external clock 28. The output of the digital logic circuit 26 determines when the reset current I_{RESET} is switched ON and applied to the summing junction 14 of the integrator op-amp 16. The output of the digital logic circuit 26 also generates the desired frequency output pulses of the multi-channel SVFC 10 circuit.

In normal operation, the input analog signal 12 causes a ramp in the output voltage V_{INT} of the integrator op-amp 16. When this ramped integrator output voltage V_{INT} crosses the reference voltage V_{REF} applied to the comparator 22, the comparator 22 changes state. A reset switch signal S_{RESET} is generated by the digital logic circuit 26 synchronous with a clock pulse from the external clock 28. The reset switch signal S_{RESET} causes a reset switch 30 to apply the reset current I_{RESET} to the integrator op-amp 16, which drives the ramped output voltage V_{INT} of the integrator op-amp 16 in the opposite direction. The comparator 22 flips state again as the ramped integrator output voltage V_{INT} crosses the reference voltage V_{REF}, and the cycle repeats.

By inspection, the input analog signal 12 is never absent from the integrator op-amp 16 during the entire conversion cycle. Therefore, in contrast to the conventional SA ADC devices, no information is lost from the signal.

An optional timing circuit 32 is provided on the input clocking signal from the external clock 28. The timing circuit 32 is a digital divider and phase shifter that phases the multi-channel frequency output pulses generated by the digital logic circuit 26 as a function of the number of channels, whereby the frequency output is equal to 1/n times the clock signal generated by the external system clock 28, where n is the number of channels in the multi-channel SVFC circuit 10.

The frequency output pulse on each channel only occurs out-of-phase with the frequency output pulses on other channels. The frequency output pulses are applied to a frequency output pulse buffer 34, which provides ordered frequency output pulses in phase with the phased clock signal 28. This method reduces switching noise within the integrated circuit embodying the multi-channel SVFC circuit 10 of the invention, reduces spurious power supply spiking due to current surges, and results in lower thermal operations.

An optional "self-test" feature is implemented in the multi-channel SVFC circuit 10 of the invention as a switch 36, such as a MOSFET switch, on the input to the integrator summing junction 14. In normal operation, the MOSFET switch 36 presents an essentially zero impedance path for the analog signal 12 being converted. However, in self-test mode, the MOSFET switch 36 is actuated to block the analog signal and provide a known reference current I_{REF} to the integrator summing junction 14. The MOSFET

switch 36 thereby drives the SVFC frequency to a known frequency. The MOSFET switch 36 is thus useful during system power up and reset, and for fault diagnostics. In an integrated circuit embodying the multi-channel SVFC circuit 10 of the invention, the MOSFET self-test feature is implemented through a digital logic switch input to the integrated circuit.

The combination of the clock phasing circuit 32 with output pulse buffer 34 and the single precision voltage reference generator 24 in combination with the single system clock 28 permit the SVFC circuit 10 of the invention to support multiple channels. This combination of the single precision voltage reference generator 24 with the single system clock 28 ensures that all the channels are matched in performance, which causes the ratio of signals to be highly stable. In other words, the ratio of X versus Y on channel n verses channel m is highly stable.

The common utilization of the system clock 28 and voltage reference generator 24 also significantly reduces errors due to component drift, aging and other changes.

Figure 2 shows one channel of the multi-channel SVFC circuit 10 of the invention embodied as an integrated circuit having at least 4 channels of a charge-reset, mixed-mode circuit. Each circuit includes the essential components of the multi-channel SVFC circuit 10 diagrammed in Figure 1. The invention is not limited to the exemplary 4-channel circuit described in Figure 2, but is applicable to multi-channel SVFC circuits in general, which are considered equivalents of the described circuit 10.

According to one embodiment of the invention, the multiple channels of the multi-channel SVFC circuit 10 are implemented in ASIC (application specific integrated circuit) format, whereby a system level approach to precision analog signal conversion without loss of data is obtained. Various novel aspects of the invention permit the multi-channel SVFC circuit 10 to be implemented in ASIC format, including phasing clocks to reduce integrated circuit noise, using the common voltage reference generator 24 to reduce errors, utilizing a digital approach to enhance performance through long-term stability, and utilizing known circuit design techniques to produce a circuit design conducive to CMOS implementation.

The multi-channel SVFC circuit 10 of the invention is thus implemented as multiple SVFC circuits in a high temperature silicon-on-insulator (SOI) CMOS architecture. The SOI CMOS architecture provides a system level SVFC conversion useful in multiple sensor systems. The SOI CMOS architecture also provides a low power CMOS solution in a high temperature (225°C) compatible semi-conductor. Utilizing a circuit design compatible with CMOS and SOI CMOS implementation results in the lower power consumption, which is aided by actual implementation in ASIC format.

The SOI CMOS architecture results in lower system level costs, and increased system level reliability through reduction of overall parts count. The SOI CMOS architecture also results in lower power requirements and a lower thermal signature. The advantatges of implementing the multiple SVFC circuits of the invention in a high temperature SOI CMOS architecture relate to an enhanced system level performance, versus an implementation using either discrete components or multiple single-channel SVFCs.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property of privilege is claimed are defined as follows:

CLAIMS

1. A multi-channel SVFC (synchronous voltage-to-frequency converter) circuit, each channel of the circuit comprising:

an integrator adapted to receive an analog data signal and a reset signal, the integrator being structured to integrate the sum of the analog signal and the reset signal and generate an output signal as a function of the integrated sum;

a comparator coupled to receive the output signal of the integrator and a reference level signal, the comparator being structured to output a logic level signal as a function of the received reference level signal;

a digital logic circuit responsive to a clock signal, the digital logic circuit coupled to receive the logic level signal and structured to generate a reset control signal and a frequency output pulse as a function of the logic level signal and in phase with the clock signal; and

a reset source switch coupled to receive the reset control signal and structured to output the reset signal as a function of the reset control signal.

2. The circuit of claim 1 wherein the integrator is an operational amplifier having a summing junction adapted to receive the analog data signal and the reset signal.

3. The circuit of claim 1, further comprising a trimming circuit coupled to an input of the integrator that is adapted to receive an analog data signal.

4. The circuit of claim 3, further comprising a voltage reference circuit generating the reference level signal received by each of the comparator, the non-inverting junction of the integrator, and the trimming circuit.

5. The circuit of claim 4 wherein the comparator is a fast response comparator set to trigger at a level established by the voltage reference circuit.

6. The circuit of claim 1 wherein the clock signal is generated by a clock phasing circuit adapted to receive an external clock signal and output the clock signal controlling the digital logic circuit, the clock phasing circuit phasing a plurality of frequency output pulses generated by the digital logic circuit.

7. The multi-channel SVFC circuit of claim 6 wherein the phasing the plurality of frequency output pulses generated by the digital logic circuit is a function of the number of channels of the multi-channel SVFC circuit.

8. The multi-channel SVFC circuit of claim 7 wherein the clock phasing circuit is a digital divider and phase shifter circuit.

9. The multi-channel SVFC circuit of claim 1, further comprising a self-test circuit coupled between the integrator and an input to the circuit adapted to receive an analog data signal.

10. A multi-channel SVFC (synchronous voltage-to-frequency converter) circuit, each circuit comprising:

an integrator operational amplifier having an input for receiving an input to the circuit and for receiving a reset signal, the integrator operational amplifier integrating the sum of an analog signal input of the circuit and the reset signal, and generating an output voltage;

a reference voltage generator generating a reference voltage;

a fast response comparator having an input coupled to the output of the reference voltage generator and to the output of the integrator operational amplifier, the comparator changing state as a function of the reference voltage and outputting a state logic level signal;

a digital logic circuit having a first input coupled to the output of the comparator and a second input for receiving a clock signal from an external clock, the digital logic circuit generating a reset control signal and a plurality of frequency output

pulses as a function of the state logic level signal under the control of an external clock; and

a reset source switch having an input coupled to the output of the digital logic circuit, the reset source switch outputting the reset signal as a function of the reset control signal and in phase with the external clock.

11. The multi-channel SVFC circuit of claim 10, further comprising a clock phasing circuit having an input for receiving a clock signal from an external clock, the clock phasing circuit coupled to the second input of the digital logic circuit for phasing the plurality of frequency output pulses generated by the digital logic circuit.

12. The multi-channel SVFC circuit of claim 11 wherein the phasing the plurality of frequency output pulses generated by the digital logic circuit is a function of the number of channels of the multi-channel SVFC circuit.

13. The multi-channel SVFC circuit of claim 12 wherein the clock phasing circuit is a digital divider and phase shifter circuit.

14. The multi-channel SVFC circuit of claim 10, further comprising a self-test circuit coupled between the input to the integrator operational amplifier and the input to the circuit.

15. The multi-channel SVFC circuit of claim 10 wherein:

the integrator operational amplifier includes a summing junction; and

the input of the integrator operational amplifier for receiving an input to the circuit and for receiving a reset signal is to an input to the summing junction of the integrator operational amplifier.

16. The multi-channel SVFC circuit of claim 10 wherein the integrator operational amplifier is structured to receive an analog data signal input as a current.

17. The multi-channel SVFC circuit of claim 10 wherein the output voltage generated by the integrator operational amplifier is generated as a function of the integrated sum of an analog signal input of the circuit and the reset signal.

18. The multi-channel SVFC circuit of claim 10 wherein the integrator is adapted to receive the input of the circuit as an input current and to receive the reset signal input as an input current.

19. The multi-channel SVFC circuit of claim 10 wherein the comparator is set to trigger at a level established by the reference voltage generator.

20. A multi-channel SVFC (synchronous voltage-to-frequency converter) circuit, comprising:

a plurality of SVFC circuits realized in SOI (silicon-on-insulator) CMOS architecture, each circuit comprising:

an operational amplifier adapted for receiving at a summing junction thereof an analog data signal to be converted by a channel of the circuit and a reset signal, the operational amplifier structured to integrate the sum of an analog signal input of the circuit and the reset signal, and generate an output voltage as a function of the sum of an analog signal and the reset signal;

a reference voltage generator generating a reference voltage;

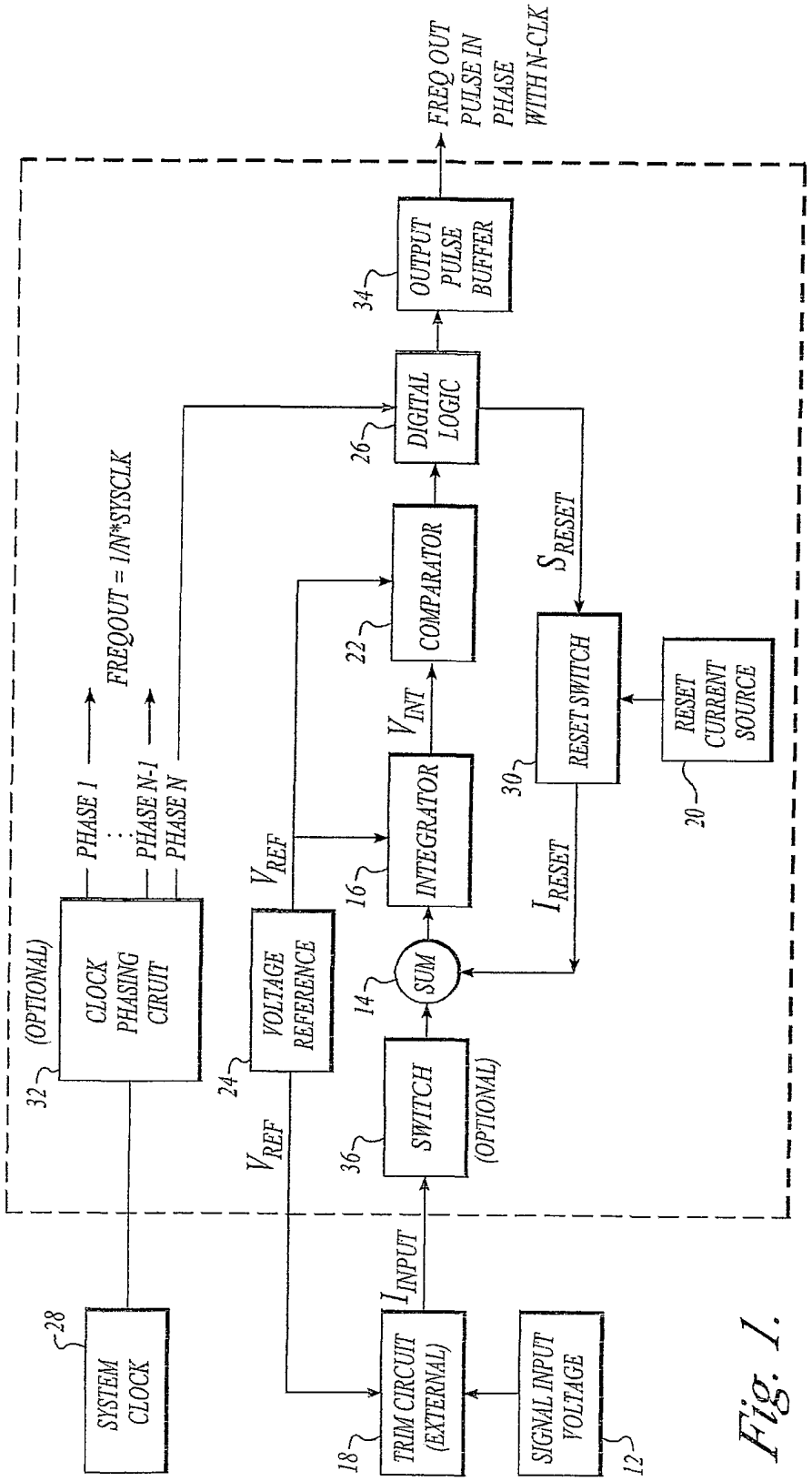
a fast response comparator coupled to receive the output of the reference voltage generator and the output of the operational amplifier, the comparator structured to change state as a function of the reference voltage and output a state logic level signal;

a digital logic circuit coupled to receive the output of the comparator and an external clock signal, the digital logic circuit structured to generate a reset control signal and a plurality of frequency output pulses as a function of the state logic level signal under the control of the external clock; and

a reset source switch coupled to receive the output of the digital logic circuit, the reset source switch structured to output the reset signal in response to the reset control signal.

21. The circuit of claim 20, further comprising a clock phasing circuit coupled to receive an external clock signal and output the clock signal controlling the digital logic circuit, the clock phasing circuit structured to phase a plurality of frequency output pulses generated by the digital logic circuit as a function of the number of channels of the multi-channel SVFC circuit.

22. The multi-channel SVFC circuit of claim 20, further comprising a self-test circuit coupled to an input to the integrator summing junction of the operational amplifier between the summing junction and analog data signal to be converted, the self-test circuit being a MOSFET switch structured to present an essentially zero impedance path for the analog data signal to be converted.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OUTPUT PULSE BUFFER
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COMPARATOR
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RESET SWITCH
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RESET CURRENT SOURCE
20
V_{INT}
INTEGRATOR
16
I_{RESET}
SUM
14
V_{REF}
VOLTAGE REFERENCE
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FREQOUT = 1/N*SYSCLK
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PHASE N-1
PHASE N
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CLOCK PHASING CIRUIT
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SWITCH
(OPTIONAL)
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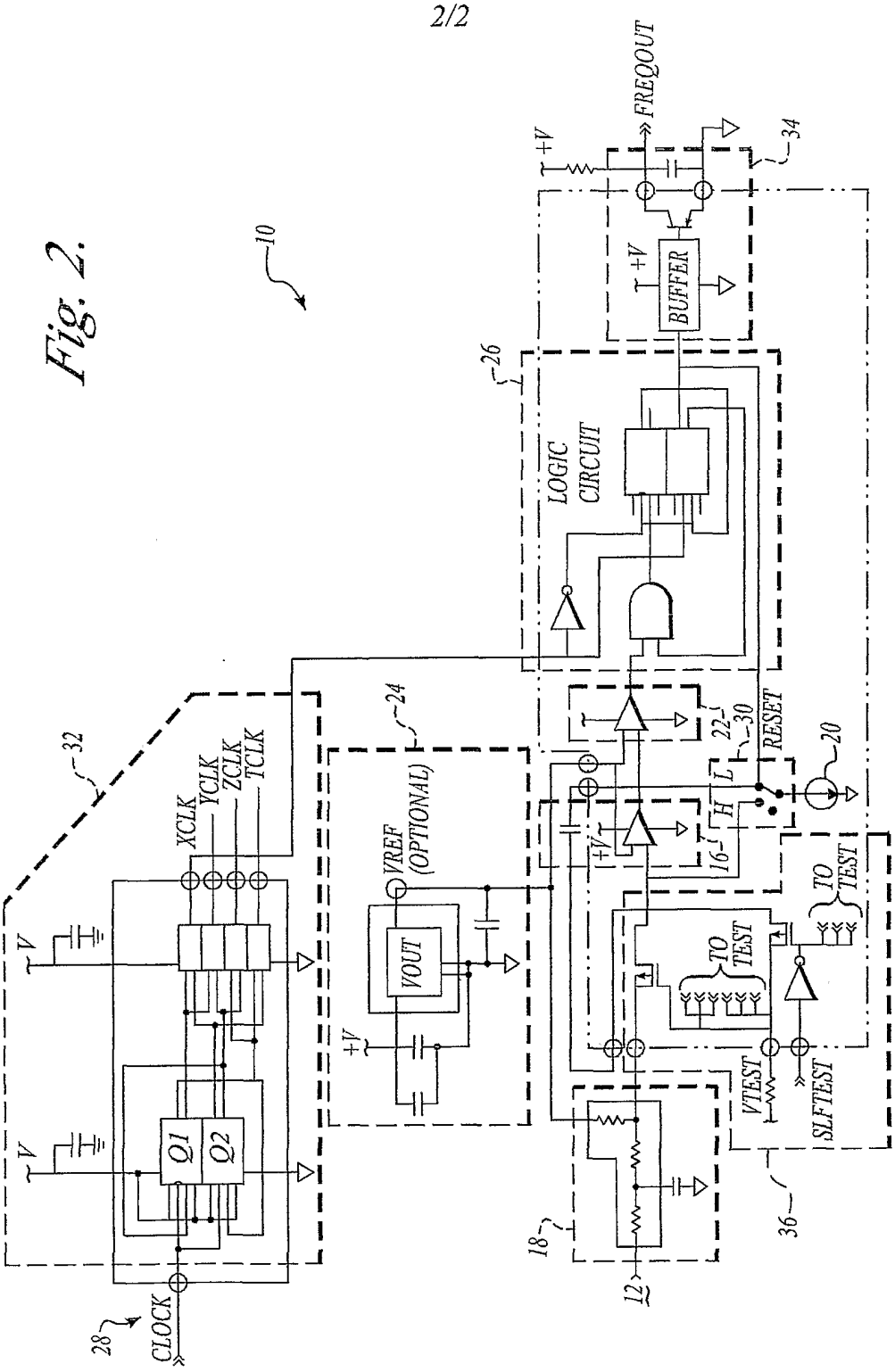
TRIM CIRCUIT (EXTERNAL)
18
SIGNAL INPUT VOLTAGE
12

Fig. 1.

Fig. 2.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YCLK
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Q2
CLOCK
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22
30
RESET
20
16
L
H
TO TEST
VTEST
SLFTEST
18
12
36