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Dietel et al.

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[54] DIGITAL SIGNAL GENERATOR FOR GENERATING A DIGITIZED SINUSOIDAL WAVE

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[52] **U.S. Cl.**.....**235/197**, 235/150.53, 235/152, 328/14

[51] **Int. Cl.**.....**G06f 15/34**

[58] **Field of Search**.....235/150.5, 150.51, 150.52, 235/150.53, 197, 152, 152 IE, 151.11, 151.11 I, 186, 189; 328/14; 318/568, 579, 588, 593; 340/347 DA, 347 DD

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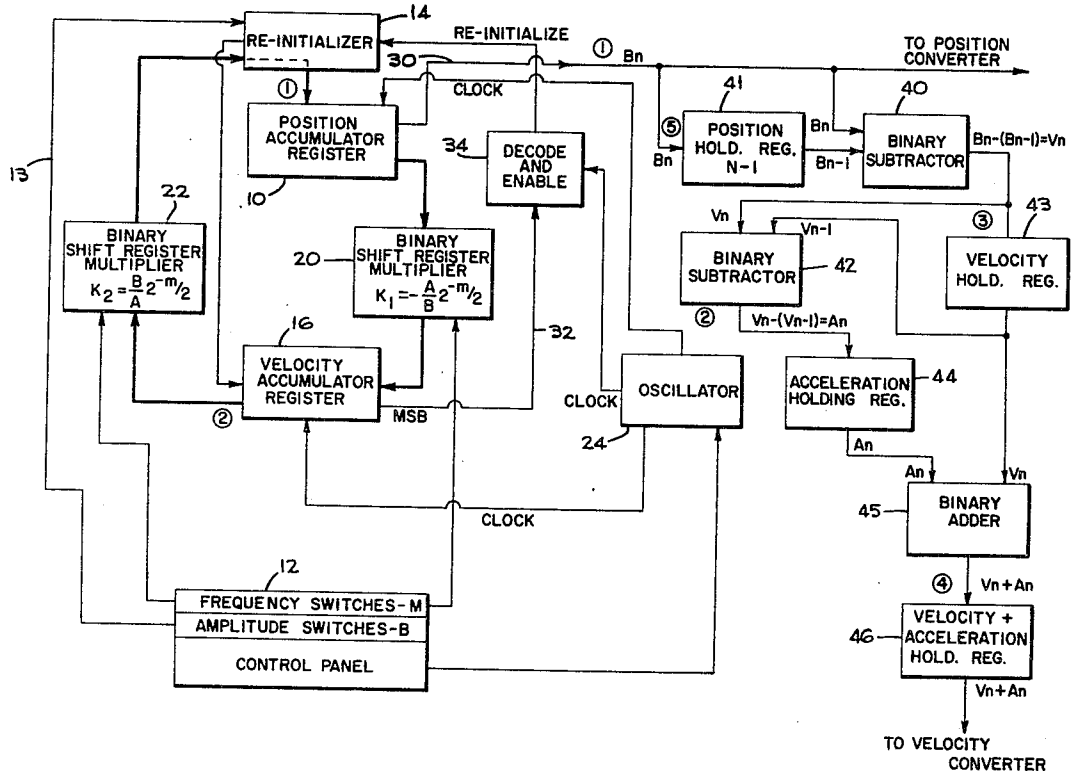
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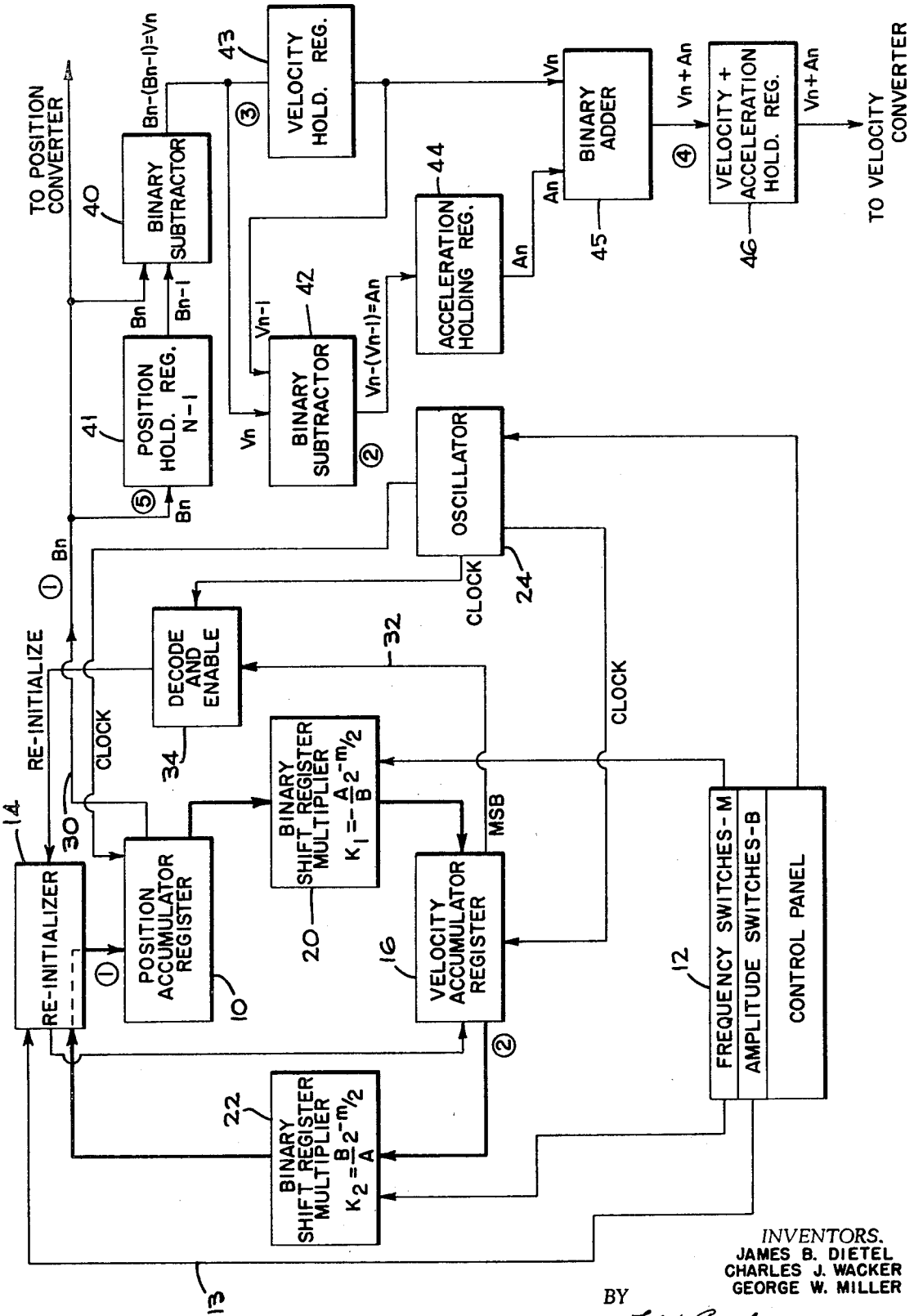
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[57] **ABSTRACT**

Digital signals are generated representative of successive positions on a sinusoidal curve by means of a pair of accumulator registers and a pair of binary shift registers with the registers being alternately positioned and serially connected in a closed-loop system and activated by a split-phase clock so that each accumulator register alternately receives an incremental number from one of the adjacent shift registers representing the number in the other accumulator register multiplied by a predetermined factor. The output of one of the accumulator registers defines a new positional signal at each clock pulse which order can then be processed to provide a corresponding digital velocity signal.

10 Claims, 1 Drawing Figure





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DIGITAL SIGNAL GENERATOR FOR GENERATING A DIGITIZED SINUSOIDAL WAVE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to digital signal generators, and more particularly, it pertains to a special purpose digital signal generator for generating a digitized sinusoidal wave.

2. Description of the Prior Art

For many years the large hydraulic drives used in the elevating and traversing of the barrel of a gun have been controlled by synchros which provide continuous output signals, and the synchros where, in turn, controlled by fire control systems which were analog in nature comprising numerous analog devices such as gear trains and drive motors. It has been proposed that fire control orders be derived in and transmitted from a computer in digital form which information can be processed through a digital-to-resolver converter before it is used to control the synchros at the gun mounts. With the change to digital fire control systems a need has arisen for a means to generate digital order signals for the power drives independent of the fire control system for the purpose of testing and determining the compliance of the gun positioning servomechanisms with known inputs.

In the past, these local order generators, which are commonly known as dummy directors, have comprised electromechanical systems generating continuous synchro signals. These electromechanical signal generators suffered from the typical disadvantages of analog signal generating systems including lack of precision, drift, dependence upon external line voltages for precision, backlash and friction losses in gear trains and associated linkages and inertia problems.

The types of signals which are required of the dummy directors generally comprise static position orders, constant velocity orders and simple harmonic motion orders, i.e., sinusoidally varying positional orders. The latter are obviously the most difficult to generate digitally.

While conventional digital computers have been programmed to generate a digitized sinusoidal wave, such programs are relatively complex and require considerable computer time for their execution. Furthermore, the use of a conventional multipurpose digital computer for the specialized function of generating fire control signals for test purposes is not practical in most instances.

SUMMARY OF THE INVENTION

The apparatus of the present invention comprises a special purpose digital signal generator which utilizes a minimum amount of digital hardware to produce a digitized sinusoidal wave output. A pair of accumulator registers are provided with one register representing the sine of a variable angle and the other register representing the cosine of the same variable angle. By picking an incremental value of the variable angle of a predetermined amount and multiplying such incremental value with the negative of the value of the sine register and adding the resultant product to the cosine register, the sum in the cosine register will represent a new value of the cosine. This new cosine value is then multiplied with the incremental value of the variable angle with the resultant product being added to the sum in the sine register to give a new sine value. The process is continuously repeated in alternate steps between the two registers to generate a series of incremental sine and cosine values representing a sinusoidally varying quantity. The number in the sine register is scaled by a predetermined factor so that the output will be a digitized signal varying sinusoidally and representing a train of positional orders related to said predetermined factor. Such positional orders may be processed through a digital-to-synchro converter and applied to the aforedescribed gun control synchos to simulate the roll of a naval vessel.

The aforedescribed digital generating system is obtained by connecting the output of the sine register to a first digital multiplier the output of which is connected to the input of the cosine register. The output of the cosine register is then connected to a second digital multiplier the output of which is connected to the input of the sine register. The accumulator registers are activated alternately, as by a conventional master clock for example, to generate the new sums therein. At the end of each period of the generated sine wave when the cycle starts anew, the number in one of the accumulator registers can be reset back to its initial value in order to prevent drift in the system.

It is also within the purview of the present invention to use the digital position signals to generate digital velocity signals by differentiating the position signals using holding registers and computing the difference between successive position signals. The accuracy of the digital velocity signal is improved by differentiating the velocity signals in a similar manner to obtain a digital acceleration signal which can be added to the computed velocity signal.

BRIEF DESCRIPTION OF THE DRAWING

The drawing is a block diagram representation of the functional components of the digital signal generator of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the digital signal generator of the present invention there is provided an accumulator register **10** which comprises a conventional binary register of a sufficient number of bits to assure a high degree of accuracy. The accumulator register will include the customary dual ranked flip-flop circuits combined with a binary adder so that binary inputs to the accumulator will be added to the binary sum already appearing therein.

A control panel **12** is provided wherein the desired amplitude and frequency of the sine wave to be generated are selected. The amplitude B is selected and by convenient means is placed in accumulator register **10** prior to the start of the generating cycle; for example, pushbutton switches in the control panel may select the values for each bit in the register which information is transmitted by lines **13** through the reinitializer **14** to the register with the reinitializer serving to clear the register of the information therein prior to the entry of the information from the control panel. The amplitude B represents the maximum amplitude of a sinusoidal wave with its midpoint at zero.

A second accumulator register **16** is provided which is identical to the register **10**. This second register is arranged to store a binary number which will be the derivative of the number in the first register, or, with the number in register **10** representing a position order, the number in register **16** at any given time will represent a velocity order related to the position order in register **10**. In setting the apparatus for operation, the insertion of numerical value B in register **10** is accompanied by clearing register **16** to zero value, i.e., with all of the bits in register **16** being zero.

A pair of binary multipliers **20** and **22** are connected between each of the accumulator registers **10** and **16** for the purpose of multiplying the number in one register by a fractional constant and providing it at the input of the other register. The choice of the multiplying constant determines the particular frequency of the generated sine wave and, therefore, the control panel may be provided with a plurality of frequency switches *m* which are connected with the multipliers through the proper logic circuitry to provide the right multiplying constant for the particular frequency chosen in accordance with the mathematical relationships between the registers to be described in greater detail hereinafter. Because the particular multiplying constants chosen will in each instance be powers of two, the multipliers **20** and **22** may comprise binary shift registers which will shift the input from the adjacent accumulator register a predetermined number of bits to the right or left.

Each accumulator register is driven by a master clock or oscillator **24** which provides clock pulses at a predetermined

frequency in two phases with one phase operating the accumulator register **10** and with the second phase operating the register **16**. Once the amplitude of the sine wave to be generated has been entered in position accumulator register **10** and the velocity register **16** has been cleared to zero, the system is ready to be started. At the first clock pulse of clock phase one the velocity register **16** will be activated to accept and add the product obtained from the shift register **20** which represents the product of the number B in the position register **10** and the negative multiplying constant K_1. At the first clock pulse of clock phase two position register **10** is activated to accept and add the product of the multiplying constant K_2 and the number in the velocity register. At the second clock pulse of clock phase one the velocity register is again activated and the operation is repeated. A binary number will be provided on the output line **30** of accumulator register **10** at each clock pulse and these binary numbers will represent positions on a sine wave with a maximum amplitude of B, a midpoint of zero, and a frequency of m. By using the conventional twos complement representation of negative numbers the accumulator registers can be used to generate negative displacements and negative velocities.

As the system moves incrementally through one complete cycle, the number in the position accumulator register will move from a maximum positive value through zero to a maximum negative value and back through zero to the initial value. However, due to the round off errors generated because of the finite length of the binary registers, the computed value of the maximum amplitude after one cycle may not correspond precisely with the original set value B. In order to prevent the system from drifting because of these round off errors a reinitialize procedure is used. As the velocity accumulator register moves through the zero crossing point at the completion of a sine wave cycle the most significant bit will change state (from a zero to a + assuming that velocity is initially in a negative direction) and this change of state is sensed and transmitted by line **32** to the decode and enable circuitry **34** which puts out a pulse to the reinitializer **14**. The reinitializer serves to clear the position accumulator register and place the number B on the input line **13** from the control panel back in the register. Consequently, the errors generated digitally will be corrected each cycle to prevent their accumulation and the resultant loss of accuracy.

While the accumulator registers have been considered as position and velocity registers it has been pointed out that the values in the registers are derivitives of each other and, since the numerical value in the position register **10** represents the value of the sine of a variable angle, then the numerical value in the velocity register **16** will represent the value of the cosine of that variable angle. The relationship between the sine and cosine of a variable angle θ having an increment h is given by the following trigonometric identities:

$$B\sin(\theta+h/2)=B\sin\theta\cos h/2+B\cos\theta\sin h/2 \quad (1)$$

$$B\sin(\theta-h/2)=B\sin\theta\cos h/2-B\cos\theta\sin h/2 \quad (2)$$

$$A\cos\theta=A\cos[(\theta+h/2)-h/2]$$
$$=A\cos(\theta+h/2)\cos h/2+A\sin(\theta+h/2)\sin h/2 \quad (3)$$

$$A\cos(\theta+h)=A\cos[(\theta+h/2)+h/2]$$
$$=A\cos(\theta+h/2)\cos h/2-A\sin(\theta+h/2)\sin h/2 \quad (4)$$

By subtracting (2) from (1) and transposing and by subtracting (3) from (4) and transposing the following relationships are established:

$$B\sin(\theta+h/2)=B\sin(\theta-h/2)+2B(\sin h/2)\cos\theta \quad (5)$$

$$A\cos(\theta+h)=A\cos\theta-2A(\sin h/2)\sin(\theta+h/2) \quad (6)$$

In terms of the present invention, we can let θ in the above equations (5) and (6) be the argument of the generated sine and cosine functions, h equal an increment in the argument θ in radians, N equal incrementing rate in 1/second (corresponding to the clock pulse rate), T equal the time for one period of the generated sine wave in seconds, and f equal the frequency of the sine wave in cycles/second. Since T is the time required for the argument θ to be incremented by 2π radians; it follows that

$$T=2\pi/hN \quad (7)$$

$$f=1/T=hN/2\pi \quad (8)$$

The common amplitude factor in equations (5) and (6) of 2 sin $h/2$ can be written as a series where $2\sin h/2=2[(h/2)-(h/2)^3/6+\ldots-\ldots]$

$$=h(1-h^2/24+\ldots-\ldots)$$
$$\approx h \quad (9)$$

It will be noted that h can be made to take on values which are powers of 2 and if we let $h=2^{-m/2}$, where m is an integer of 10 or greater, then the maximum error in the approximation of equation (9) will be less than 0.00004 or 0.004 percent. The periods and frequencies of the generated sine wave will then be given by

$$T=2\pi 2^{m/2}/N \quad (10)$$

$$f=N/2\pi 2^{m/2} \quad (11)$$

Equations (5) and (6) can now be rewritten using $2\sin h/2=h$ with $h=2^{-m/2}$ as follows:

$$B\sin(\theta+h/2)=B\sin(\theta-h/2)+(B/A)2^{-m/2}A\cos\theta \quad (13)$$

$$A\cos(\theta+h)=A\cos\theta-(A/B)2^{-m/2}B\sin(\theta+h/2) \quad (14)$$

From equation (13) it will be seen that given the value of the sine term at time $(\theta-h/2)$ and given the value of the cosine term at time θ, the value of the sine term at the subsequent increment of time $(\theta+h/2)$ can be computed. From equation (14) it will be seen that given the value of the cosine term at time θ and given the value of the sine term at time $(\theta+h/2)$, the value of the cosine term at subsequent time $(\theta+h)$ can be computed.

By letting the value in the position register **10** represent the sine term and the value in the velocity register **16** represent the cosine term, and letting the increment h be the clock pulse frequency with the increment between the clock phases being represented by $h/2$, it will be seen that the aforedescribed digital generator can be utilized to generate a series of sine and cosine terms since register **10** functions to add a sine term at time $\theta-h/2$ (the term in the register) to a cosine term at time θ (the term from the multiplier **22** to get a new sine term at time $\theta+h/2$. Also, the register **16** functions, at the subsequent clock pulse incremented by time $h/2$, to add the cosine term at time θ (the term in the register) to the sine term at time $\theta+h/2$ (the term from the multiplier **20**) to get a new cosine term at time $\theta+h$. Clock phase **1** (as indicated in the drawing) is associated with the incrementing of the sine term in register **10**, and clock phase **2** (as indicated in the drawing) is associated with the incrementing of the cosine term in the register **16**.

The constants in equations (13) and (14) are obtained by letting B be the maximum amplitude of the sine (or position) register **10** and A be the maximum amplitude of the cosine (or velocity) register **16**. The multiplier K_2 for the transfer of information from the cosine to the sine register is therefore $(B/A)2^{-m/2}$, and the multiplier K_1 for the transfer of information from the sine to the cosine register is $-(A/B)2^{-m/2}$. With B being selected, A will be chosen as equal to B when m is even, and $A=B/\sqrt{2}$ when m is odd. Consequently, with m even, $K_2=2^{-m/2}$ and $K_1=-2^{-m/2}$; with m odd, $K_2=2^{-(m-1)/2}$ and $K_1=-2^{-(m+1)/2}$. Since these multipliers are all powers of two, it will be seen that conventional binary shift registers can be used to perform the multiplication.

From equations (10) and (11) the values of the periods and frequencies throughout a useful range for fire control orders of simple harmonic motion can be obtained. The following table was derived assuming an N equal to 4,096 pulses/second, a conventional clock pulse rate.

m	T(sec.)	m	f(c.p.s.)
28	25.1	18	1.27
27	17.8	17	1.80
26	12.6	16	2.55
25	8.89	15	3.60
24	6.28	14	5.09
23	4.44	13	7.20
22	3.14	12	10.19
21	2.22	11	14.41
20	1.57	10	20.37

The generated frequencies cover the range which approximates the roll of a naval vessel which range of frequencies will normally be used in test equipment of the type described. However, by changing N, the clock pulse rate, an entirely different range of generated frequencies can be provided.

With a train of digital position orders being generated at the clock pulse rate N, it is also desirable to generate velocity orders at the same rate since positioning servomechanisms of the type in general use are provided with both position and velocity synchros. The generation of a velocity order from a given positional order is obtained with a series of holding registers and a five phase clock. In the drawing, the notation B_n defines the digital position signal at a time N and the notation B_{n-1} defines the position signal at a time one clock pulse earlier. Each phase of the clock from one to five is denoted by an encircled numeral which is placed adjacent to the holding register into which the information is clocked by the corresponding clock phase.

Starting with the clock pulse at phase one, a new position order B_n appears and is directed to the binary subtractor **40** where the previous position order B_{n-1} from the position holding register **41** is subtracted therefrom to give an output of $B_n-(B_n-1)$ which equals the incremental change in position or the velocity V_n. The new velocity order is applied to a second binary subtractor **42** where the previous velocity order V_{n-1} from the velocity holding register **43** is subtracted therefrom to give an output of $V_n-(V_n-1)$ which equals the incremental change in velocity, or the acceleration A_n. At clock phase two, the newly generated acceleration order A_n is clocked into the acceleration holding register **44**. At clock phase three, the new velocity order V_n is clocked into the velocity holding register. A_n and V_n can then be added in a binary adder **45**, the output of which is clocked into the velocity and acceleration register **46** at clock phase four. Finally, at clock phase **5**, the position order is clocked into the position holding register **41** and the circuitry is reset to await the arrival of the subsequent position order B_{n+1} on input line **30**. By the addition of the computed acceleration signal to the computed velocity signal, the velocity signal is made more nearly accurate and changes in velocity are anticipated. With proper scaling, the output of holding register **46** can be applied to subsequent systems in the proper relationship to the position signal on output line **30**.

Although the best mode contemplated for carrying out the present invention has been herein shown and described, it will be apparent that modification and variation may be made without departing from what is regarded to be the subject matter of the invention.

Having completed a detailed description of the invention so that those skilled in the art could practice the same, we claim:

1. A digital signal generator for generating a digitized sinusoidal wave comprising a first means for storing a first number representing a given position, a second means connected to the output of said first means for multiplying said number by a predetermined fractional value, a third means connected to the output of said second means for storing a second number and for adding the product of said multiplication to the second number at a first predetermined time, a fourth means connected to the output of said third means for multiplying the number stored by said third means by a predetermined fractional amount, said first means being connected to the output of said fourth means for adding the product produced thereby to said first number at a second predetermined time subsequent to said first predetermined time so that the sum of said last-mentioned addition is a third number representing a second position displaced by a predetermined incremental amount from said first position along a sinusoidal wave of a predetermined amplitude and frequency, said first and third means comprising accumulator registers for storing a series of digits indicative of said numbers, and pulse producing means for alternately activating said accumulator registers at uniformly spaced time intervals for accepting in digital form the numbers from said second and fourth means and for adding them to the number appearing in the register.

2. A digital signal generator as set forth in claim **1** wherein said second and fourth means comprise shift registers each operable to shift the digital representation of said numbers received from one of said accumulator registers by a predetermined number of digits before transmitting it to the other of said accumulator registers.

3. A digital signal generator as set forth in claim **1** including means for placing in the first accumulator register means prior to the initiation of the signal generating cycle a digital quantity corresponding to the maximum amplitude of the sinusoidal wave to be generated, and output means from said first accumulator register providing a digital output for each pulse thereto from said pulse producing means.

4. A digital signal generator as set forth in claim **3** including means for detecting the time when one complete cycle of said sinusoidal wave has been generated, reinitializing means operatively connected with said detecting means and with said first accumulator register means for replacing the number in said register at said time with said digital quantity corresponding to the maximum amplitude of the sinusoidal wave.

5. A digital signal generator as set forth in claim **1** including velocity signal generating means for comparing successive position signals from said first means and for generating a velocity signal corresponding to the difference between said successive position signals.

6. A digital signal generator as set forth in claim **5** wherein said velocity signal generating means comprises a first holding register connected to the output of said first means, and a digital subtractor having inputs from said first means and from said first holding register.

7. A digital signal generator as set forth in claim **6** wherein said velocity signal generating means further includes a second digital subtractor having one input connected to the output of said first digital subtractor, a second holding register having an input connected to the output of said first digital subtractor and an output connected to the other input of said second digital subtractor, a third holding register connected to the output of said second digital subtractor, a digital adder having inputs connected to the outputs of said second holding register and said third holding register, and a fourth holding register connected to the output of said digital adder for storing a digital quantity corresponding to the derivative of the position signal.

8. A digital signal generator comprising a first accumulator register for storing digital quantities representing a series of successive positions on a sinusoidal wave, a first digital multiplier having an input connected to the output of said first accumulator register, a second accumulator register having an input connected to the output of said digital multiplier for storing digital quantities representing the derivatives of said digital quantities in said first accumulator register, a second digital multiplier having an input connected to the output of said second accumulator register and an output connected to the input of said first accumulator register for successively updating said digital quantities stored in said first accumulator register to define the derivatives of said digital quantities in said second accumulator register, means for initiating the sequential generation of successive position signals from said first accumulator register by placing therein a digital quantity representing the maximum amplitude of said sinusoidal wave, and pulse producing means operative to alternately update each of said accumulator registers at uniformly spaced time intervals.

9. A digital signal generator as set forth in claim **8** wherein said digital multipliers comprise binary shift registers.

10. A digital signal generator as set forth in claim **8** including reinitializing means having an input associated with the most significant bit of one of said accumulator registers in order to detect the condition of said register when one complete cycle of said sinusoidal wave has been generated, said reinitializing means being operative to reintroduce the

digital quantity representing the maximum amplitude of the sinusoidal wave in said first accumulator register upon the detection of said condition.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,636,337 Dated April 24, 1972

Inventor(s) James B. Dietel et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 15, after "A" insert --new--. Column 4, line 74, --19 1.11-- should be inserted.

Signed and sealed this 1st day of August 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents