(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number
WO 2004/010166 A2

(51) International Patent Classification[7]: G02B

(21) International Application Number:
PCT/US2003/014125

(22) International Filing Date: 1 May 2003 (01.05.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/146,278 15 May 2002 (15.05.2002) US

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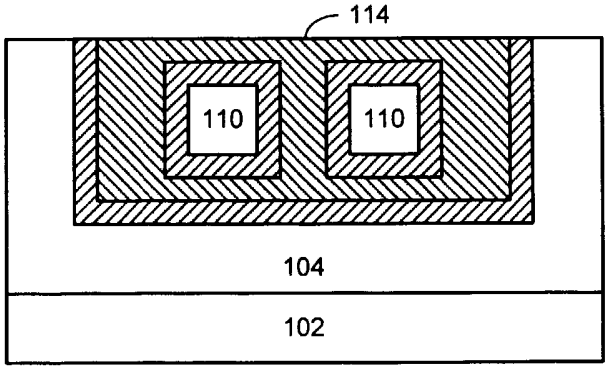
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FABRICATION OF OPTICAL COMPONENTS USING SI, SIGE, SIGEC, AND CHEMICAL ENDPOINT DETECTION



(57) Abstract: One embodiment of the present invention provides a system to facilitate using selective etching to form optical components on a circuit device. The system operates by receiving a substrate composed of a first material including a buffer layer composed of a second material. The system forms a sacrificial layer composed of a third material on the buffer layer. Next, the system forms an optical fiber core composed of a fourth material on the sacrificial layer. After the optical fiber core has been formed, the system performs an etching operation using a selective etchant to remove the sacrificial layer. The system also applies a cladding layer to the optical fiber core.

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FABRICATION OF OPTICAL COMPONENTS USING Si, SiGe, SiGeC, AND CHEMICAL ENDPOINT DETECTION

BACKGROUND

Field of the Invention

[0001] The present invention relates to a process for manufacturing structures on a substrate. More specifically, the present invention relates to creating optical components within an integrated circuit through a process that uses chemically-selective endpoint detection.

Related Art

[0002] The dramatic advances in computer system performance during the past 20 years can largely be attributed to improvements in the processes that are used to fabricate integrated circuits. By making use of the latest fabrication processes, integrated circuit designers can presently integrate computing systems comprised of hundreds of millions of transistors onto a single semiconductor die which is a fraction of the size of a human fingernail.

[0004] Integrated circuit fabrication technology is also being used to fabricate optical devices such as lasers within integrated circuit devices, and which have dimensions measured in fractions of microns.

[0005] A typical fabrication process builds structures through successive cycles of layer deposition and subtractive processing, such as etching. As the dimensions of individual circuit elements continue to decrease, it is becoming necessary to more tightly control the etching operation. For example, in a typical etching process, etching is performed for an amount of time that is estimated by taking into account the time to etch through a layer to reach an underlying layer, and the time to overetch into the underlying layer. However, this process can only be controlled to +/- 100 Angstroms, which can be a problem when fine control of dimensions is required.

[0006] Furthermore, conventional etching processes that indiscriminately etch all exposed surfaces are not well suited to manufacture some structures that require tighter control over subtractive processing operations. As circuit structures become smaller, there is less tolerance available to account for uncertainties in the manufacturing process.

[0007] Additionally, connecting optical devices within an integrated circuit typically requires aligning optical fibers with an optical device such as a laser, or converting the optical signals to electrical signals at the source and converting the electrical signals back to optical signals at the destination. Aligning optical fibers with an optical device is difficult and time consuming because of the small dimensions involved, while converting the form of the signals can lead to signal degradation.

[0008] What is needed is a method of fabricating and connecting optical components that does not have the difficulties listed above.

SUMMARY

[0009] One embodiment of the present invention provides a system to facilitate using selective etching to form optical components on a circuit device. The

system operates by receiving a substrate composed of a first material including a buffer layer composed of a second material. The system forms a sacrificial layer composed of a third material on the buffer layer. Next, the system forms an optical fiber core composed of a fourth material on the sacrificial layer. After the optical fiber core has been formed, the system performs an etching operation using a selective etchant to remove the sacrificial layer. The system also applies a cladding layer to the optical fiber core.

[0010] In one embodiment of the present invention, the system adds a filler to fill the cavity left by removing the sacrificial layer and planarizes the circuit device using chemo-mechanical polishing to create a planarized surface.

[0011] In one embodiment of the present invention, the substrate is Si and the buffer layer is SiGe or SiGeC. Using SiGeC for the buffer layer allows growth of a thicker buffer layer than when using SiGe. In this embodiment, the sacrificial layer is Si, the optical fiber core is SiO_2:GeO_2, the selective etchant used to remove the sacrificial layer is KOH or tetramethylammonium hydroxide (TMAH), and the cladding layer on the optical fiber core is SiO_2. It is appreciated that other materials and etchants may be used.

[0012] In one embodiment of the present invention, the buffer layer is SiGeC, wherein carbon is greater than or equal to one atomic percent.

[0013] In one embodiment of the present invention, the buffer layer is SiGeC, wherein carbon is less than or equal to one atomic percent.

[0014] In one embodiment of the present invention, the filler is SiO_2.

[0015] In one embodiment of the present invention, the buffer layer is an epitaxial layer.

[0016] In one embodiment of the present invention, the sacrificial layer is an epitaxial layer.

[0017] In one embodiment of the present invention, the optical fiber core is an epitaxial layer.

[0018] In one embodiment of the present invention, the system splits the optical fiber core into multiple optical fiber cores to form an optical multiplexer.

[0019] In one embodiment of the present invention, the system combines multiple optical fiber cores into a single optical fiber core to form an optical demultiplexer.

[0020] One embodiment of the present invention provides a system to facilitate integrating active or passive components on a circuit device that includes an optical fiber core that was epitaxially grown. During operation, the system receives this circuit device, and etches a cavity into the circuit device, wherein the cavity passes through the optical fiber core. The system also creates an active device within the cavity that is aligned with the optical fiber core.

[0021] In one embodiment of the present invention, etching the cavity includes etching into a buffer layer below the optical fiber core.

[0022] In one embodiment of the present invention, etching the cavity includes etching into a substrate layer below the optical fiber core.

[0023] In one embodiment of the present invention, the substrate layer includes a doped semiconductor region that can form part of the active device.

[0024] In one embodiment of the present invention, the system applies a metallization layer to the active device to form conduction paths for the active device.

[0025] In one embodiment of the present invention, the metallization layer forms a mirror metallization.

BRIEF DESCRIPTION OF THE FIGURES

[0026] FIG. 1A illustrates preparing a circuit device with a sacrificial layer in accordance with an embodiment of the present invention.

[0027] FIG. 1B illustrates forming optical fiber cores on the sacrificial layer in accordance with an embodiment of the present invention.

[0028] FIG. 1C illustrates removing the sacrificial layer and cladding the optical fiber core in accordance with an embodiment of the present invention.

[0029] FIG. 1D illustrates including a filler in accordance with an embodiment of the present invention.

[0030] FIG. 2A illustrates an optical multiplexer in accordance with an embodiment of the present invention.

[0031] FIG. 2B illustrates an optical demultiplexer in accordance with an embodiment of the present invention.

[0032] FIG. 3 is a flowchart illustrating the process of forming optical fiber cores on a circuit device in accordance with an embodiment of the present invention.

[0033] FIG. 4A illustrates a longitudinal cross-section view of a circuit device in accordance with an embodiment of the present invention.

[0034] FIG. 4B illustrates cavities etched into the circuit device in accordance with an embodiment of the present invention.

[0035] FIG. 4C illustrates active devices formed in the cavities in the circuit device in accordance with an embodiment of the present invention.

[0036] FIG. 4D illustrates metallization applied to the circuit device in accordance with an embodiment of the present invention.

[0037] FIG. 5 is a flowchart illustrating the process of forming active devices in the circuit device in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0038] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Creating a Circuit Device with an Optical Fiber Core

[0039] FIG. 1A illustrates preparing a circuit device with a sacrificial layer in accordance with an embodiment of the present invention. The circuit device includes

substrate 102, which can include the material Si. Note that the materials described herein include only one possible combination. A practitioner with ordinary skill in the art will be able to readily substitute other suitable materials for the ones described.

[0040] Buffer layer 104 is epitaxially grown on substrate 102. Buffer layer 104 can include SiGe or SiGeC. Using SiGeC allows the growth of thicker layers than does using SiGe. Note that using different materials for the various layers allows use of different chemical etchants to selectively etch the various layers.

[0041] Sacrificial layer 106 is epitaxially grown on buffer layer 104. Sacrificial layer 106 can include Si and is used to transfer the crystalline structure of buffer layer 104 to layers that are grown on sacrificial layer 106. Sacrificial layer 106 will be selectively etched away after forming these additional layers. Epitaxial blocking layer 108 has been added to the circuit device to control where additional layers will be grown on sacrificial layer 106. Epitaxial blocking layer 108 can include SiO_2 or SiN.

[0042] FIG. 1B illustrates forming optical fiber cores on the sacrificial layer in accordance with an embodiment of the present invention. Optical fiber cores 110 are epitaxially grown on sacrificial layer 106 and can include SiGe or SiO_2:GeO_2. Optical fiber cores 110 can include beams through the circuit device and can be routed through the circuit device as needed. Note that the material composition may be controlled during growth of optical fiber cores 110 to create a graded index optical fiber core.

[0043] FIG. 1C illustrates removing the sacrificial layer and the addition of cladding to the optical fiber core in accordance with an embodiment of the present invention. After growth of optical fiber cores 110, epitaxial blocking layer 108 is removed and sacrificial layer 106 is selectively etched using an etchant such as KOH or TMAH. Cladding layer 112 can then be added to optical fiber cores 110. A typical material for cladding layer 112 is SiO_2. Note that applying cladding layer 112 by thermal oxidation will tend to round optical fiber cores 110, thereby enhancing the graded index effect. Note also that SiGe and SiGeC can be selectively etched using hydrofluoric/nitric/acetic (HNA) acids.

[0044] FIG. 1D illustrates including filler 114 in accordance with an embodiment of the present invention. Filler 114 can include any suitable material, gas, or liquid such as the same material, SiO_2, used for cladding layer 112. Note that filler 114 is optional and may be wholly or partially omitted.

Optical Multiplexers and Demultiplexers

[0045] FIG. 2A illustrates an optical multiplexer in accordance with an embodiment of the present invention. Optical fiber core 202 is branched into optical fiber cores 204, 206, and 208. Note that optical fiber core 202 may branch into more or less optical fiber cores than shown. The optical multiplexer can be created by controlling the apertures in epitaxial blocking layer 108.

[0046] FIG. 2B illustrates an optical demultiplexer in accordance with an embodiment of the present invention. Optical fiber cores 210, 212, and 214 are combined into optical fiber core 216. Note that optical fiber core 202 may combine more or less optical fiber cores than shown. The optical demultiplexer can be created by controlling the apertures in epitaxial blocking layer 108.

Forming Optical Fiber Cores

[0047] FIG. 3 is a flowchart illustrating the process of forming optical fiber cores on a circuit device in accordance with an embodiment of the present invention. The system starts by receiving substrate 102 including buffer layer 104 (step 302). Next, the system forms epitaxial sacrificial layer 106 on buffer layer 104 (step 304). Note that sacrificial layer 106 is used to transfer the crystalline template from buffer layer 104 to layers grown on sacrificial layer 106 such as optical fiber cores 110.

[0048] Epitaxial blocking layer 108 is then applied to sacrificial layer 106 (step 306). Next, photoresist is applied to epitaxial blocking layer 108 (step 308). After photoresist has been applied, the system exposes and develops the photoresist to create a pattern on the photoresist (step 310). Next, epitaxial blocking layer 108 is etched to transfer the pattern layer 108 (step 312).

[0049] Optical fiber cores 110 are then epitaxially grown on the exposed portions of sacrificial layer 106 (step 314). Next, epitaxial blocking layer 108 is removed (step 316). After epitaxial blocking layer 108 has been removed, sacrificial layer 106 is removed by selective etching (step 318).

[0050] Cladding layer 112 is then added to optical fiber cores 110 (step 320). Finally, filler 114 can be added to the cavity if desired (step 322).

Creating Active Devices

[0051] FIG. 4A illustrates a longitudinal cross-section view of a circuit device in accordance with an embodiment of the present invention. The circuit device includes substrate 402, buffer layer 406, cladding layer 408, filler 410, and optical fiber core 412. The process described above in conjunction with FIGs. 1 through 3 can create these layers.

[0052] Substrate 402 can include regions 404. Regions 404 can be doped semiconductor regions such as N-type or P-type Si, or can be intrinsic Si. As previously noted, the materials described herein are exemplary and are not to be construed as the only possible materials for creating the various layers and structures. Photoresist 414 is applied, exposed, and developed to create windows for etching the structures.

[0053] FIG. 4B illustrates cavities etched into the circuit device in accordance with an embodiment of the present invention. Cavities have been etched into the circuit device using a combination of dry etching and wet etching, wherein wet etching has been used to selectively remove buffer layer 406 while not etching into regions 404 in substrate 402. Note that etching may be used to over-etch into regions 404 if desired. Note also, that etching may be stopped at buffer layer 406 or within buffer layer 406 if desired.

[0054] FIG. 4C illustrates active devices formed in the cavities in the circuit device in accordance with an embodiment of the present invention. Various active layers may be grown within the cavities to form active regions 418 and 419. Note that

circuit layers 420 and 422 are aligned with optical fiber core 412. This allows coupling optical signals through optical fiber core 412 between circuit layers 420 and 422 without the need to couple the signals into an external optical fiber or converting the optical signal to an electrical signal and back to an optical signal. Photoresist 416 has been added for subsequent exposure and developing to create a pattern for metallization.

[0055] FIG. 4D illustrates metallization applied to the circuit device in accordance with an embodiment of the present invention. Metallization 424 has been added to active regions 418 and 419 to allow electrical coupling of signals into and out of active regions 418 and 419. Mirror metallization 426 has been added to the circuit elements of active region 419. Other configurations are equally likely.

Forming Active Devices

[0056] FIG. 5 is a flowchart illustrating the process of forming active devices in the circuit device in accordance with an embodiment of the present invention. The system starts by receiving the circuit device including optical fiber core 412 (step 502). This circuit device with optical fiber core 412 can be constructed as described above in conjunction with FIGs. 1 through 3.

[0057] Next, photoresist 414 is applied to the surface of the circuit device (step 504). Photoresist 414 is then exposed through a mask and developed to form a pattern on the circuit device (step 506).

[0058] Next, the various layers are etched to form cavities within the circuit device (step 508). Note that this etching can include a combination of dry etching and wet etching. The etching can be stopped within buffer layer 406, at regions 404, or can be over-etched into regions 404. Selective chemical etching can be used to automatically terminate etching at regions 404.

[0059] Active devices are then created within the cavities etched into the circuit device (step 510). These active devices can include active devices such as lasers, optical switches, etc., or passive devices such as lenses, mirrors, etc. Note that circuit layers 420 and 422 of the active devices are self-aligned with optical fiber

core 412 eliminating the necessity of connecting an external optical fiber or converting the optical signal to an electrical signal to couple signals between circuit layers 420 and 422.

[0060] After forming the active devices in active regions 418 and 419, photoresist 416 is applied to the surface (step 512). Next a pattern is exposed and developed in photoresist 416 (step 514). Finally, metallization 424 and 426 is applied to the circuit device (step 516).

[0061] The foregoing descriptions of embodiments of the present invention have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. It is appreciated that other active (e.g. moveable mirrors, etc.) and passive devices (e.g. lenses, micro-lenses, gratings, etc.) may be fabricated using the present invention. The scope of the present invention is defined by the appended claims.

What Is Claimed Is:

1. A method for using selective etching to form optical components on a circuit device, comprising:

receiving a substrate composed of a first material including a buffer layer composed of a second material;

forming a sacrificial layer composed of a third material on the buffer layer;

forming an epitaxial blocking layer on the substrate, wherein the epitaxial blocking layer has windows exposing the sacrificial layer;

forming optical components composed of a fourth material on exposed portions of the sacrificial layer; and

performing an etching operation using a selective etchant to remove the sacrificial layer.

2. The method of claim 1,

wherein optical components include an optical fiber core; and

wherein a cladding layer is applied to the optical fiber core.

3. The method of claim 2, wherein receiving the substrate includes receiving the substrate without the buffer layer.

4. The method of claim 2, further comprising adding a filler to fill at least a portion of a cavity left by removing the sacrificial layer.

5. The method of claim 4,

wherein the first material comprises Si;

wherein the second material is SiGe or SiGeC, whereby SiGeC allows growing a thicker buffer layer than using SiGe;

wherein the third material comprises Si;

wherein the fourth material comprises SiO_2:GeO_2;

wherein the selective etchant is KOH or TMAH; and

wherein the cladding layer comprises SiO_2.

6. The method of claim 5, wherein the second material comprises SiGeC, wherein carbon is greater than or equal to one atomic percent.

7. The method of claim 5, wherein the second material comprises SiGeC, wherein carbon is less than or equal to one atomic percent.

8. The method of claim 4, wherein the filler comprises SiO_2.

9. The method of claim 4, wherein the filler is a gas, a liquid, or a solid.

10. The method of claim 2, wherein the buffer layer is an epitaxial layer.

11. The method of claim 2, wherein the sacrificial layer is an epitaxial layer.

12. The method of claim 2, wherein the optical fiber core is an epitaxial layer.

13. The method of claim 2, further comprising splitting the optical fiber core into multiple optical fiber cores, wherein splitting the optical fiber core forms an optical multiplexer.

14. The method of claim 2, further comprising combining multiple optical fiber cores into a single optical fiber core, wherein combining multiple optical fiber cores forms an optical demultiplexer.

15. The method of claim 2, wherein forming the optical fiber core includes:

forming a graded index optical fiber core; and

shaping the optical fiber core prior to applying the cladding layer, wherein shaping the optical fiber core includes rounding the optical fiber core.

16. A method to facilitate integrating active components on a circuit device, wherein the circuit device includes an optical fiber core that was epitaxially grown, comprising;

receiving the circuit device;

etching a cavity into the circuit device, wherein the cavity passes through the optical fiber core; and

creating a device within the cavity, wherein the device is aligned with the optical fiber core and wherein the device is an active device or a passive device.

17. The method of claim 16, wherein etching the cavity includes etching into a buffer layer below the optical fiber core.

18. The method of claim 16, wherein etching the cavity includes etching into a substrate layer below the optical fiber core.

19. The method of claim 18, wherein the substrate layer includes a doped semiconductor region, whereby the doped semiconductor region can form part of the active device.

20. The method of claim 16, further comprising applying a metallization layer to the active device, whereby the metallization layer forms conduction paths for the active device.

21. The method of claim 20, wherein the metallization layer forms a mirror metallization.

22. A method to facilitate self aligned connections, wherein creating a device includes creating a self-aligned device that is self-aligned to an external fiber.

23. An integrated circuit device with an optical fiber core created using a selective etching process, the selective etching process comprising:

receiving a substrate composed of a first material including a buffer layer composed of a second material;

forming a sacrificial layer composed of a third material on the buffer layer;

forming an epitaxial blocking layer on the substrate, wherein the epitaxial blocking layer has windows exposing the sacrificial layer;

forming optical components composed of a fourth material on exposed portions of the sacrificial layer; and

performing an etching operation using a selective etchant to remove the sacrificial layer.

24. The integrated circuit device of claim 23, further comprising applying a cladding layer to the optical fiber core.

25. The integrated circuit device of claim 24, wherein receiving the substrate includes receiving the substrate without the buffer layer.

26. The integrated circuit device of claim 24,

wherein the first material comprises Si;

wherein the second material is SiGe or SiGeC, whereby SiGeC allows growing a thicker buffer layer than using SiGe;

wherein the third material comprises Si;

wherein the fourth material comprises SiO_2:GeO_2;

wherein the selective etchant is KOH or TMAH; and

wherein the cladding layer comprises SiO_2.

27. The integrated circuit device of claim 26, wherein the second material comprises SiGeC, wherein carbon is greater than or equal to one atomic percent.

28. The integrated circuit device of claim 26, wherein the second material comprises SiGeC, wherein carbon is less than or equal to one atomic percent.

29. The integrated circuit device of claim 23, wherein the buffer layer is an epitaxial layer.

30. The integrated circuit device of claim 23, wherein the sacrificial layer is an epitaxial layer.

31. The integrated circuit device of claim 23, wherein the optical fiber core is an epitaxial layer.

32. The integrated circuit device of claim 23, wherein the optical fiber core is split into multiple optical fiber cores to form an optical multiplexer.

33. The integrated circuit device of claim 23, wherein multiple optical fiber cores are combined into a single optical fiber core to form an optical demultiplexer.

34. The integrated circuit device of claim 23, wherein forming the optical fiber core includes:

forming a graded index optical fiber core; and

shaping the optical fiber core prior to applying a cladding layer, wherein the optical fiber core may be rounded.

35. An integrated circuit device including an optical fiber core created using a selective etching process, wherein the integrated circuit device includes integrated active components created by a process comprising:

receiving a circuit device including the optical fiber core;

etching a cavity into the circuit device, wherein the cavity passes through the optical fiber core; and

creating a device within the cavity, wherein the device is aligned with the optical fiber core and wherein the device is an active device or a passive device.

36. The integrated circuit device of claim 35, wherein etching the cavity includes etching into a buffer layer below the optical fiber core.

37. The integrated circuit device of claim 35, wherein etching the cavity includes etching into a substrate layer below the optical fiber core.

38. The integrated circuit device of claim 37, wherein the substrate layer includes a doped semiconductor region, whereby the doped semiconductor region can form part of the active device.

39. The integrated circuit device of claim 35, the process comprising applying a metallization layer to the active device, whereby the metallization layer forms conduction paths for the active device.

40. The integrated circuit device of claim 39, wherein the metallization layer forms a mirror metallization.

41. The integrated circuit device of claim 36, further comprising creating a self-aligned device that is self-aligned to an external fiber.

42. The integrated circuit device of claim 35, further comprising creating a self-aligned device, wherein the self-aligned device is coupled across a gap.

43. The integrated circuit device of claim 42,

wherein the gap is filled with a medium; and

wherein the medium is a gas, a liquid, or a solid.

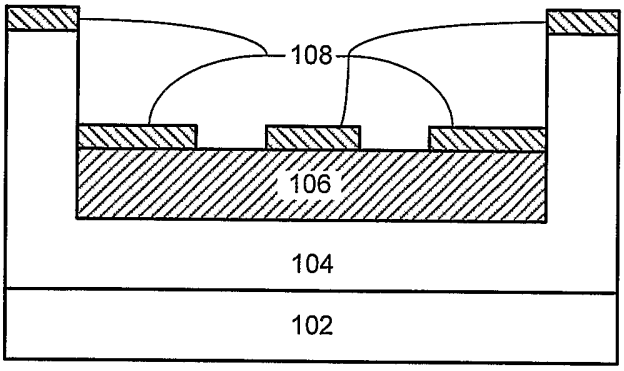

FIG. 1A

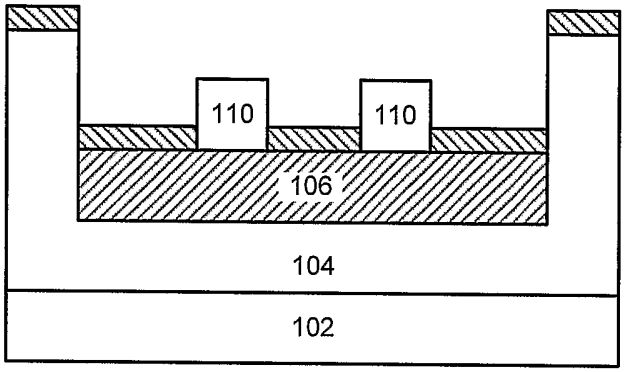

FIG. 1B

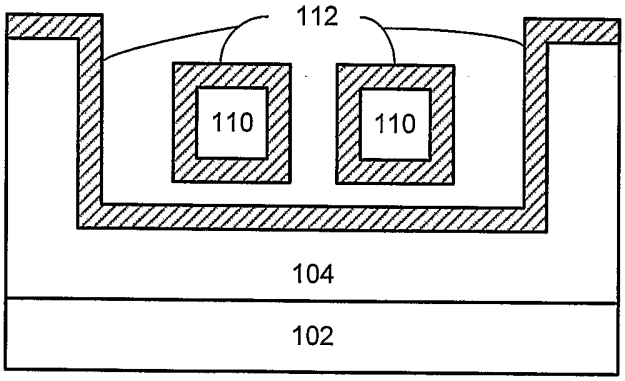

FIG. 1C

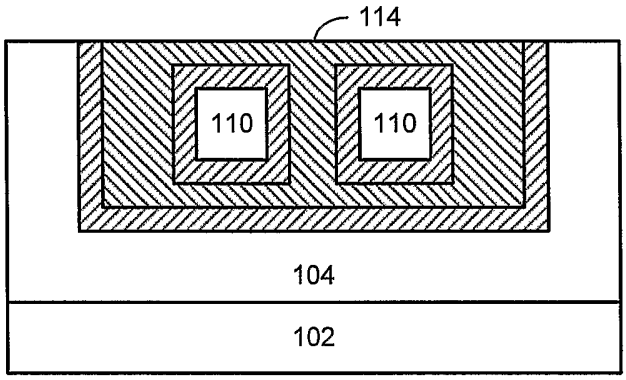

FIG. 1D

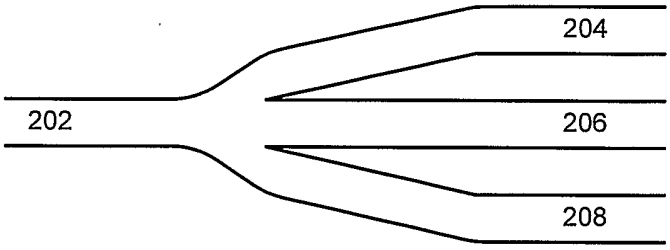

FIG. 2A

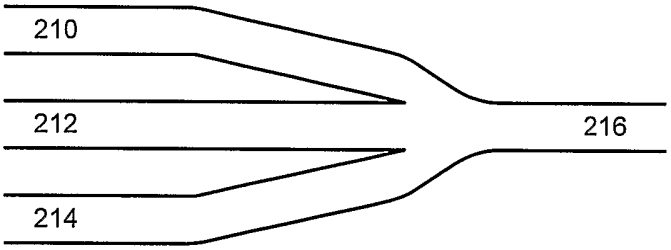

FIG. 2B

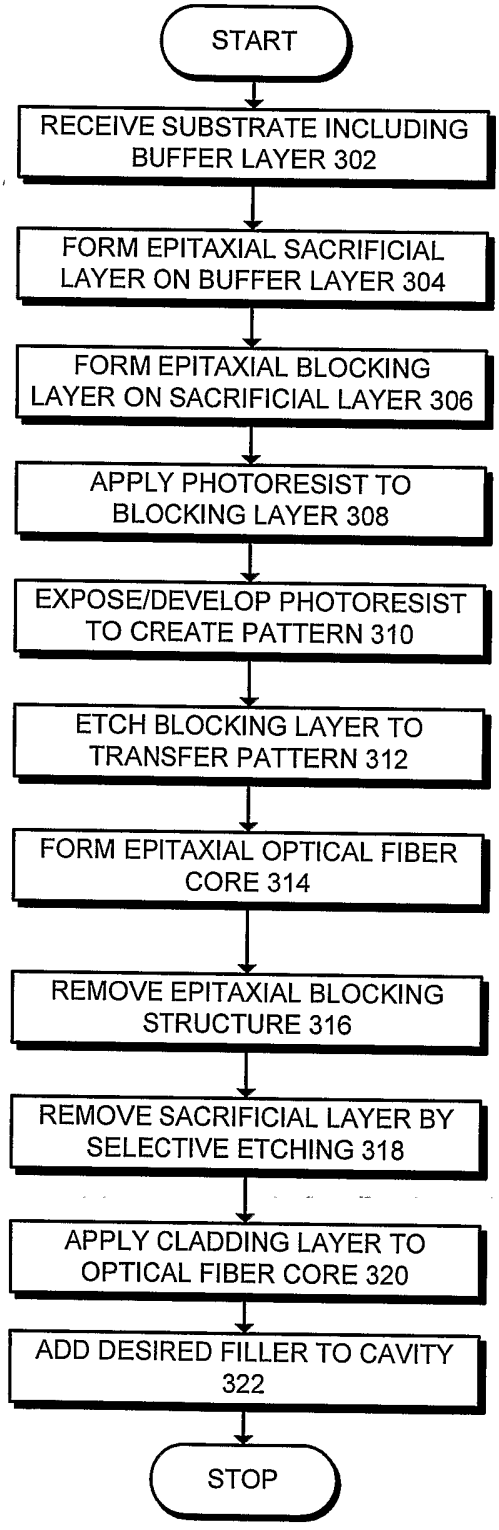
START
RECEIVE SUBSTRATE INCLUDING BUFFER LAYER 302
FORM EPITAXIAL SACRIFICIAL LAYER ON BUFFER LAYER 304
FORM EPITAXIAL BLOCKING LAYER ON SACRIFICIAL LAYER 306
APPLY PHOTORESIST TO BLOCKING LAYER 308
EXPOSE/DEVELOP PHOTORESIST TO CREATE PATTERN 310
ETCH BLOCKING LAYER TO TRANSFER PATTERN 312
FORM EPITAXIAL OPTICAL FIBER CORE 314
REMOVE EPITAXIAL BLOCKING STRUCTURE 316
REMOVE SACRIFICIAL LAYER BY SELECTIVE ETCHING 318
APPLY CLADDING LAYER TO OPTICAL FIBER CORE 320
ADD DESIRED FILLER TO CAVITY 322
STOP

FIG. 3

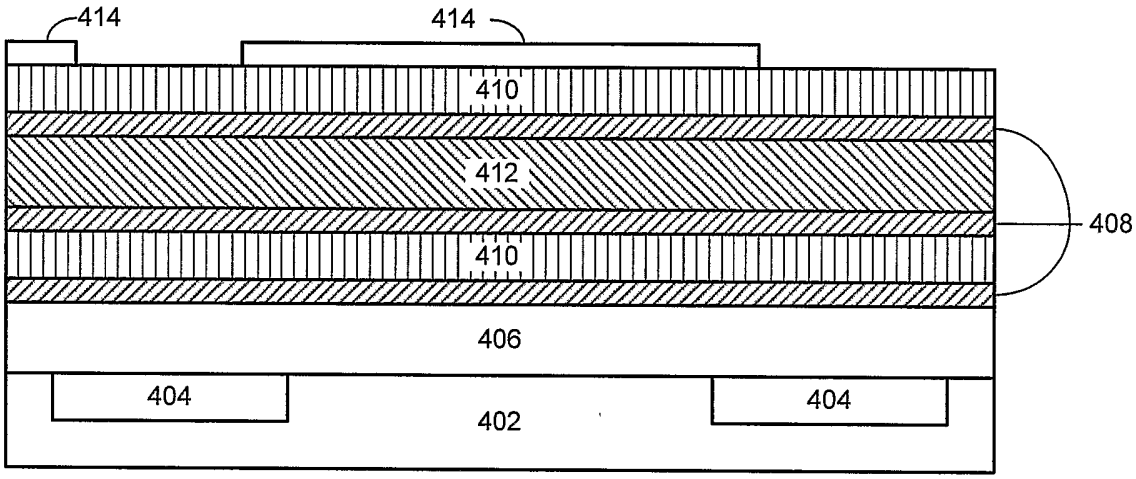
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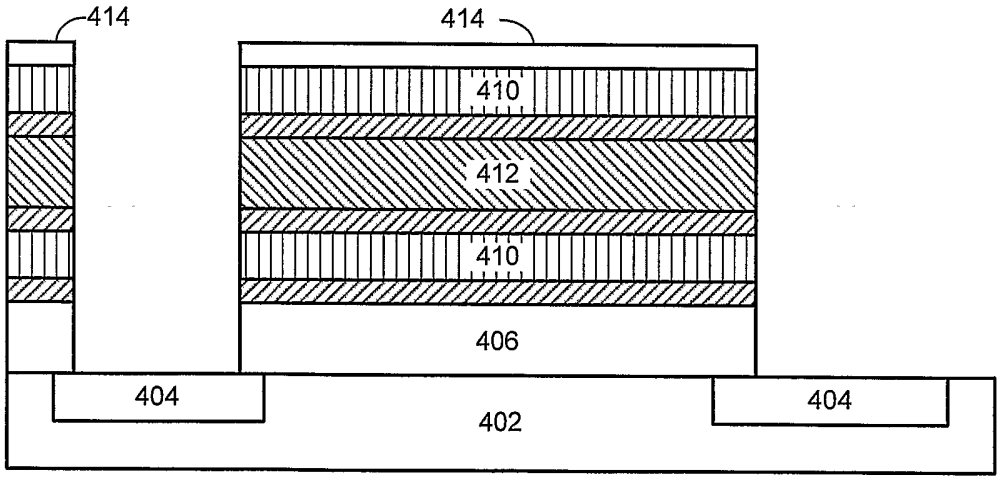
FIG. 4A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402

FIG. 4B

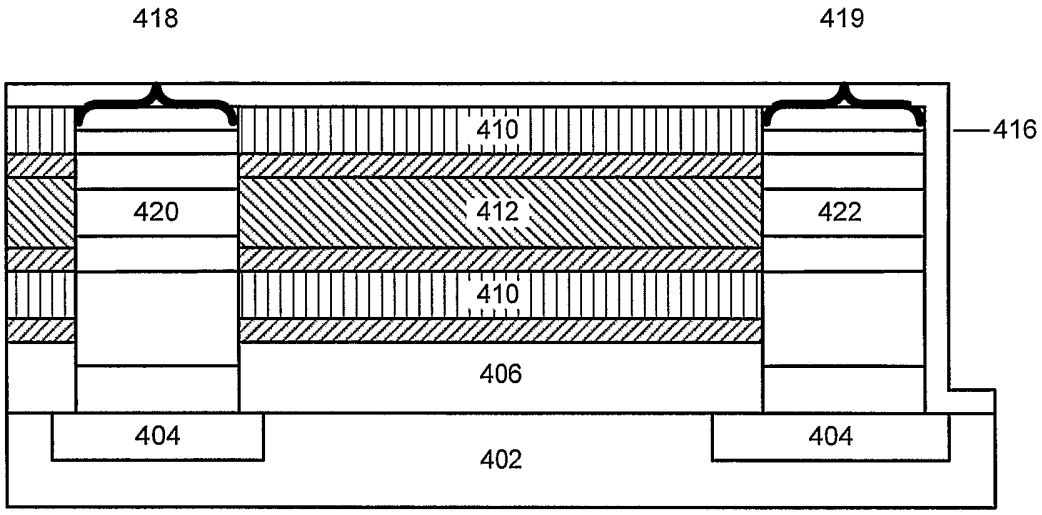
418
419
410
416
420
412
422
410
406
404
404
402

FIG. 4C

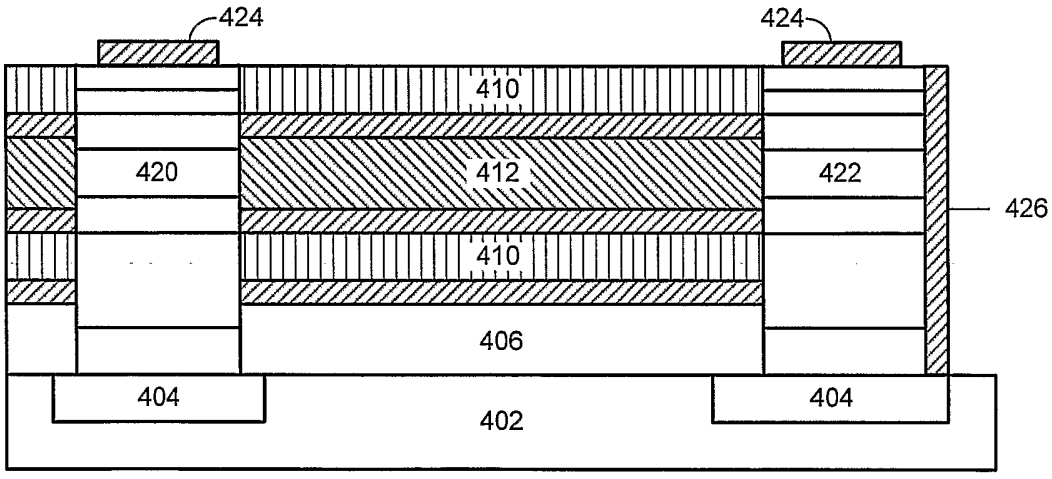
424
424
410
420
412
422
426
410
406
404
404
402

FIG. 4D

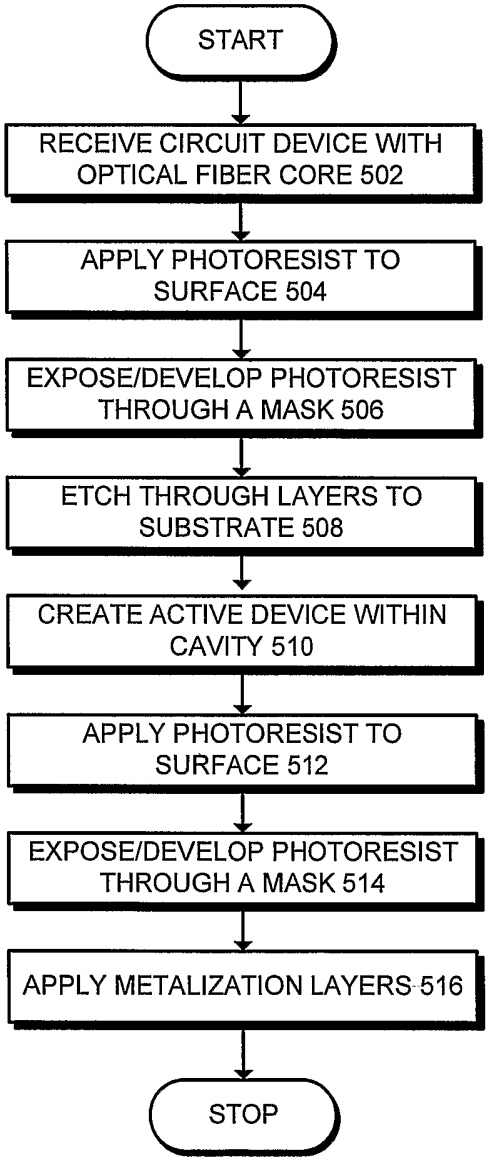
START
RECEIVE CIRCUIT DEVICE WITH OPTICAL FIBER CORE 502
APPLY PHOTORESIST TO SURFACE 504
EXPOSE/DEVELOP PHOTORESIST THROUGH A MASK 506
ETCH THROUGH LAYERS TO SUBSTRATE 508
CREATE ACTIVE DEVICE WITHIN CAVITY 510
APPLY PHOTORESIST TO SURFACE 512
EXPOSE/DEVELOP PHOTORESIST THROUGH A MASK 514
APPLY METALIZATION LAYERS 516
STOP

FIG. 5