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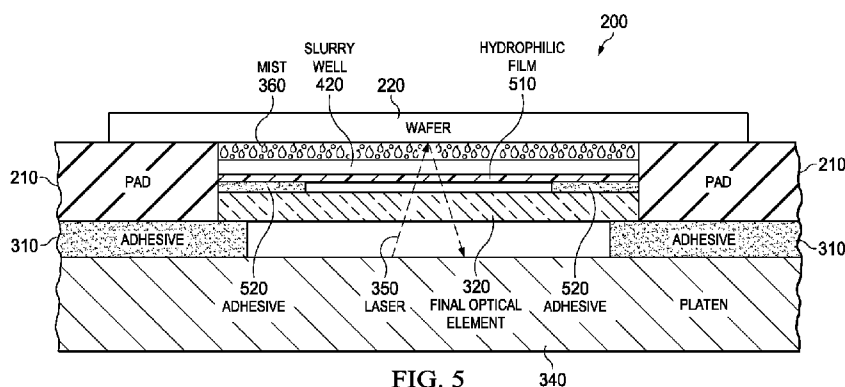
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(54) Title: IMPROVED OPTICAL METROLOGY FOR CHEMICAL MECHANICAL POLISH



(57) Abstract: By way of example, there is disclosed a final optical element for use with a chemical mechanical polish process to measure a reflectivity profile of a wafer being polished, having a transparent final optical element base material; and a transparent hydrophilic surface material. The final optical element base material may be hydrophilic or hydrophobic. There is also disclosed a chemical mechanical polishing apparatus having the final optical element, and a method of manufacturing the final optical element.

IMPROVED OPTICAL METROLOGY FOR CHEMICAL MECHANICAL POLISH

Field of the specification

[0001] This disclosure relates in general to the field of semiconductor devices, and more particularly, though not exclusively to, a system and method for providing improved optical metrology for chemical mechanical polishes.

Background

[0002] Chemical mechanical polishing (CMP), also known as chemical mechanical-mechanical planarization, is a method commonly used in semiconductor manufacturing processes to remove excess material after deposition.

Brief Description of the Drawings

[0003] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not necessarily drawn to scale, and are used for illustration purposes only. Where a scale is shown, explicitly or implicitly, it provides only one illustrative example. In other embodiments, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIGURE 1 is a block diagram of a system on a chip according to one or more examples of the present Specification.

[0005] FIGURE 2 is a top view illustration of a chemical mechanical polishing (CMP) apparatus according to one or more examples of the present Specification.

[0006] FIGURE 3 is a cutaway side view of a CMP apparatus according to one or more examples of the present Specification.

[0007] FIGURE 4 is a cutaway side view of a CMP apparatus according to one or more examples of the present Specification.

[0008] FIGURE 5 is a cutaway side view of a CMP apparatus according to one or more examples of the present Specification.

[0009] FIGURE 6 is a flow chart of a method of manufacturing a wafer with a CMP apparatus of the present Specification according to one or more examples of the present Specification.

Summary

[0010] By way of example, there is disclosed a final optical element for use with a chemical mechanical polish process to measure a reflectivity profile of a wafer being polished, having a transparent final optical element base material; and a transparent hydrophilic surface material. The final optical element base material may be hydrophilic or hydrophobic. There is also disclosed a chemical mechanical polishing apparatus having the final optical element, and a method of manufacturing the final optical element.

Embodiments of the Disclosure

[0011] The following disclosure provides many different embodiments, or examples, for implementing different features of the present disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Further, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Different embodiments may have different advantages, and no particular advantage is necessarily required of any embodiment.

[0012] Chemical-mechanical polishing (CMP) (also called chemical-mechanical planarization) is an intermediate process in the manufacture of integrated circuits (IC), such as microprocessors, systems-on-a-chip, or other similar devices. From a high level, to start with, an IC may start with an appropriate substrate such as a thin wafer cut from a monocrystalline silicon ingot of approximately 12-inches diameter (though this should be understood to be a nonlimiting example). A monocrystalline ingot is one in which the crystal lattice is continuous and unbroken throughout the ingot.

[0013] First, a dielectric substrate, such as silicon dioxide (SiO_2) is deposited on the wafer. The substrate may be doped, and certain features are then chemically etched in the substrate. This process may take place in multiple layers, and what is etched on the substrate may depend on the layer. For example, in the “front end of the line” (FEOL), shallow trench isolation (STI) is used to fabricate semiconductor devices, such as transistors. The shallow trenches may then be planarized using a process such as a combination of resist etching-back and CMP.

[0014] The process may be serialized as follows: First, isolation trenches are transferred to the silicon wafer. Second, oxide is deposited on the wafer in the shape of trenches. A nitride photo mask is patterned on the top of this oxide. A second layer is then added to the wafer to create a planar surface. Next, the silicon is thermally oxidized. The oxidizing agents are unable to diffuse through the nitride mask, so the nitride prevents the oxidation. Chemical etching then leaves a small amount of oxide in the active areas. Finally, CMP may be used to polish and planarize the wafer.

[0015] In CMP, the wafer is placed face-down on a polishing pad, which is attached to a platen. Commonly, the platen and pad are two to three times larger in diameter than the wafer, so as the wafer and platen both spin on different axes (i.e., they are not concentric—the axis of the wafer is about halfway between the axis of the platen and the outer edge) and the wafer is polished down. Note that the platen is generally considered to be durable equipment, while the pad is disposable and replaceable.

[0016] The “chemical” part of CMP is a chemical slurry (often a colloid), which may be both abrasive and corrosive. The polishing pad and wafer may be pressed together by a polishing head, and the wafer may be held in place by a retaining ring. As the wafer and pad rotate, excess material is removed, and irregular topological features are smoothed out. Thus, the wafer becomes much more planar.

[0017] CMP may help to prepare for the formation of additional circuit elements. For example, CMP can bring the surface of the wafer to within the depth of field of a photolithography system, or selectively remove material based on position.

[0018] In an embodiment, CMP *in situ* optical metrology is used to determine how long to polish a wafer. For optical metrology, an aperture is placed in the pad, disposed so that it will periodically pass under the wafer. This aperture has a “final optical element” (FOE) disposed somewhat below the plane of the pad, ensuring that the FOE itself does not abrade the wafer. As the aperture passes beneath the wafer, a laser beam is directed up at the wafer and reflected back down to an optical receiver. For convenience, throughout this application, this process may be referred to as a “ping.” The reflected light of the ping is measured and compared to a profile to determine whether the polishing process is complete. The profile may be, for example, determining whether the reflected light has passed a threshold, such as 50% (e.g., for polishing down a metal, has the reflectivity decreased to 50% or less, so that the underlying nonmetal has been uncovered, or for polishing down a nonmetal, has the reflectivity increased to 50% or more so that the underlying metal has been uncovered).

[0019] The accuracy of this measurement may be characterized by a signal-to-noise ratio (SNR)—how much of the reflected light profile is attributable to the properties of the wafer itself, versus “disturbance” factors. A high signal noise (i.e., low SNR) may cause wafers to be polished less than needed (under-polished) or more than needed (over-polished). Either result may be undesirable.

[0020] A “slurry gap” is defined as the medium between the FOE and the wafer. If a single medium with well-defined optical properties is present in the slurry gap, then a high SNR is experienced. This is true whether the medium is air or slurry, as long as it is consistently and primarily one or the other. But if multiple phases (slurry and air) exist within the “slurry gap” together, optical refraction causes signal noise.

[0021] As noted above, placing the FOE at the plane of the polishing pad essentially eliminates the slurry gap, but there is danger that the FOE will abrade the wafer in an uncontrolled and undesirable way. This may result, for example, in scratches. Thus, it is superior to have a slurry gap having almost exclusively either air or slurry.

[0022] During the CMP process, the wafer is, by necessity (and even by definition) wet. Thus, some existing solutions provide a hydrophobic FOE. As slurry

inevitably falls into the slurry gap, it is mostly ejected by the combination of the hydrophobic FOE and the rotational force of the process.

[0023] If this process were ideal—a “spherical cow,” so to speak—then all slurry would be ejected from the gap, and the slurry gap would include a well of optically-efficient air. But the hydrophobic FOE is not a theoretically-ideal hydrophobe. Much or even most of the slurry is ejected, but a small amount remains in the gap as the aperture passes under the wafer. As the aperture passes under the wafer, the slurry gap is sealed so that the remaining slurry cannot escape. Rather, it becomes a watery mist that causes unwanted refraction. This diffuses the return ping of the laser, making it appear that the reflectivity of the wafer is lower than it actually is. Depending on the nature of the process, this can cause either over-polishing or under-polishing.

[0024] In contrast, the present Specification teaches a hydrophilic FOE. In this case, rather than ejecting most, or “almost all” of the slurry from the slurry gap, the hydrophilic FOE retains most of the slurry in the gap, forming a slurry well that fills most of the slurry gap. Again, this process may not be theoretically ideal: a small amount of slurry may be ejected from the well by the rotational force of the process. This means that there may still be a small, misty layer when the aperture passes under the wafer and seals the slurry gap. But in this case, the layer of “mixed” slurry and air is much shallower than in the previous example, so refraction is reduced significantly.

[0025] The described system and method reduces the signal noise without pressing the FOE against the wafer, thus substantially reducing signal noise without introducing defects on the wafer.

[0026] Embodiments of a hydrophilic FOE may be provided in various ways. In each case, a base layer and top layer are described, though it should be understood that the term “layer” is used herein for convenience in describing the disclosed embodiments. It should be understood that “base layer” and “top layer” are used throughout this Specification and the appended claims to usefully refer to different portions of the FOE, regardless of whether they are of different materials or discretely separate from one another. The base layer may be any appropriate material, such as a glass or a softer polymer. Softer polymer compounds may be more desirable for certain applications, because they will not

shatter and cause possibly catastrophic failure. The softness of the polymer also helps to ensure that if contact is made with the wafer, damage to the wafer is minimized.

[0027] In one example, an existing hydrophobic FOE (base layer) is prepared with an adhesive material (placed around the radius, for example), and a hydrophilic film (top layer) is applied to the adhesive. The hydrophilic top layer may be, for example, 3M "Surfactant Free Fluid Transport Film," product No. 9984, the publicly-available datasheet for which is incorporated herein by reference. 3M No. 9984 is a 3.9 mil transparent polyester with a hydrophilic coating. In another example, a hydrophobic FOE base layer may be conformally coated with a top layer of hydrophilic material. In yet another example, the FOE may be made completely of a hydrophilic material, in which case there may not be an identifiable boundary between the "base layer" and "top layer." In yet another embodiment, the FOE base layer is made of a first material, and the top layer is derived from the first material, such as chemically or mechanically. In a chemical derivation, the top layer of the first material may be oxidized to give it hydrophilic properties. Oxidation may be accomplished for example by heating in a chamber with one surface exposed, or by plasma oxidation. In another embodiment, the top layer may be given hydrophilic properties by diffusion or absorption of a second material. In another embodiment, the top layer may be mechanically prepared, such as with abrasion, to give it a more hydrophilic character. The grit and application of abrasion may be selected according to the design requirements of a particular implementation, balancing the increased hydrophilic properties with the diffraction that the abrasion itself may introduce.

[0028] Note that in some embodiments, advantages are realized by having a hybrid FOE. A hydrophobic base layer may help the FOE to better bond to the polishing pad, while the hydrophilic top layer realizes the advantages disclosed herein. However, this should not be construed to imply that a fully hydrophilic FOE is not within the scope of the appended claims.

[0029] In the appended illustrations, FIGURE 1 is a block diagram of a system-on-a-chip (SoC) 100, which is provided as a nonlimiting example of an integrated circuit that may be manufactured according to the teachings of this Specification. Other nonlimiting examples of circuits that may be similarly

manufactured according to the teachings herein include microprocessors, microcontroller, memories, digital signal processors, radio frequency (RF) amplifiers, RF filters, power conditioners, regulators, and supplies, multiplexers, analog-to-digital converters, and digital-to-analog converters.

[0030] FIGURE 2 is a top view illustration of a CMP apparatus, illustrating in context the placement of a wafer on the CMP pad, and the placement of an aperture for measuring reflectivity.

[0031] FIGURE 3 is a cutaway side view illustration, showing specifically a CMP pad with hydrophilic FOE. In this embodiment, the wafer tends to be wet, while the FOE tends to be dry. When the FOE passes under the wafer, a mix of air and a relatively small amount of slurry still exists within the slurry gap. This can create a mist in the slurry gap, causing optical diffraction of the *in situ* metrology system (in this case a laser).

[0032] FIGURE 4 is a cutaway side view illustrating certain advantages realized by providing an FOE with at least a hydrophilic top layer. In this embodiment, the FOE is coated with a hydrophilic film. This causes more slurry and less air to be present in the "slurry gap," forming effectively a "slurry well" that occupies most of the slurry gap. This reduces the optical diffraction of the laser signal.

[0033] FIGURE 5 is a side view illustrating certain advantages realized by providing an FOE with at least a hydrophilic top layer. In this example, an existing hydrophobic FOE may be prepared with a hydrophilic film mechanically coupled to the base layer with an appropriate adhesive.

[0034] FIGURE 6 is a flow chart of a method of performing CMP on an integrated circuit using the FOE of the present disclosure.

[0035] A system and method for providing improved optical metrology for chemical mechanical polishes will now be described with more particular reference to the attached FIGURES. It should be noted that throughout the FIGURES, certain reference numerals may be repeated to indicate that a particular device or block is wholly or substantially consistent across the FIGURES. This is not, however, intended to imply any particular relationship between the various embodiments disclosed. In certain examples, a genus of elements may be referred to by a particular reference numeral ("widget 10"), while individual species or examples

of the genus may be referred to by a hyphenated numeral ("first specific widget 10-1" and "second specific widget 10-2").

[0036] FIGURE 1 is a block diagram of system-on-a chip (SoC) 100 according to one or more examples of the present Specification. SoC 100 is disclosed as a nonlimiting example, but in a more general sense, the teachings of this Specification are applicable to providing any suitable computing device. In various embodiments, a "computing device" may be or comprise, by way of non-limiting example, a computer, workstation, server, mainframe, virtual machine (whether emulated or on a "bare-metal" hypervisor), embedded computer, embedded controller, embedded sensor, personal digital assistant, laptop computer, cellular telephone, IP telephone, smart phone, tablet computer, convertible tablet computer, computing appliance, network appliance, receiver, wearable computer, handheld calculator, or any other electronic, microelectronic, or microelectromechanical device for processing and communicating data.

[0037] In an example, SoC 100 may be manufactured according to the methods disclosed herein, including the use of CMP. More particularly, SoC 100 may include a number of computing elements, each of which is tightly integrated in a single chip. This may require complex, microscopic circuits and highly complex routing, which may require multiple layers of routing, including vias and tracelines. Furthermore, in embodiments where a computer is used that is not an SoC (such as a traditional desktop computer), certain computing elements of that desktop computer, such as the CPU, may be manufactured according to the present Specification. All of this may require precision planarization to ensure high-quality and high-yield processes with minimal errors.

[0038] In this example, SoC 100 includes a number of computing elements, which include any active or passive elements of SoC 100 that contribute to SoC 100 to perform its intended function. In this example, processor 110 connected is to a memory 120, having stored therein executable instructions for providing appropriate software, such as an operating system and operational software. Other components of SoC 100 include an input/output (I/O) block 140 and a power manager 130. This architecture is provided by way of example only, and is intended to be non-exclusive and non-limiting. In a specific example, each of the listed components may be a physically separate intellectual property (IP) block,

designed in advance for use on SoC 100, and each may occupy a separate space on a silicon wafer. The separate IP blocks may communicate with each other via an on-chip interconnect fabric.

[0039] In other examples, the various disclosed blocks may be logical divisions only, and need not necessarily represent physically separate hardware and/or software components. Certain computing devices provide main memory and storage, for example, in a single physical memory device, and others provide them in separate devices. In the case of virtual machines or hypervisors, all or part of a function may be provided in the form of software or firmware running over a virtualization layer to provide the disclosed logical function. In other examples, a device such as a network interface may provide only the minimum hardware interfaces necessary to perform its logical operation, and may rely on a software driver to provide additional necessary logic. Thus, as appropriate to the embodiment, each logical block disclosed herein may broadly include one or more logic elements configured and operable for providing the disclosed logical operation of that block. As used throughout this Specification, a "logic element" may include hardware, external hardware (digital, analog, or mixed-signal), software, reciprocating software, services, drivers, interfaces, components, modules, algorithms, sensors, components, firmware, microcode, programmable logic, or objects that can coordinate to achieve a logical operation.

[0040] In an example, processor 110 may be communicatively coupled to memory 120 via any suitable memory bus, which may be for example a direct memory access (DMA) or any other suitable bus. Processor 110 may be communicatively coupled to other devices via a system bus or fabric. As used throughout this Specification, a "fabric" includes any wired or wireless interconnection line, network, connection, bundle, single bus, multiple buses, crossbar network, single-stage network, multistage network or other conduction medium operable to carry data, signals, or power between parts of a computing device, or between computing devices. It should be noted that these uses are disclosed by way of non-limiting example only, and that some embodiments may omit one or more of the foregoing buses, while others may employ additional or different buses.

[0041] In various examples, a “processor” may include any combination of logic elements operable to execute instructions, whether loaded from memory, or implemented directly in hardware, including by way of non-limiting example a microprocessor, digital signal processor, field-programmable gate array, graphics processing unit, programmable logic array, application-specific integrated circuit, or virtual machine processor. In certain architectures, a multi-core processor may be provided, in which case processor 110 may be treated as only one core of a multi-core processor, or may be treated as the entire multi-core processor, as appropriate. In some embodiments, one or more co-processors may also be provided for specialized or support functions.

[0042] To simplify this disclosure, memory 120 is disclosed as a single logical block, but in a physical embodiment may include one or more blocks of any suitable volatile or non-volatile memory technology or technologies, including for example DDR RAM, SRAM, DRAM, cache, L1 or L2 memory, on-chip memory, registers, flash, ROM, optical media, virtual memory regions, magnetic or tape memory, or similar. In certain embodiments, memory 120 may comprise both a relatively low-latency volatile main memory, and a relatively higher-latency non-volatile memory. However, the two species of memory need not be physically separate devices, and in some examples may represent simply a logical separation of function (for example, in some devices, all memory is volatile, or all memory is nonvolatile). It should also be noted that although DMA is disclosed by way of non-limiting example, DMA is not the only protocol consistent with this Specification, and that other memory architectures are available.

[0043] Memory 120 may include one or more non-transitory computer-readable mediums, including by way of non-limiting example, a hard drive, solid-state drive, external storage, redundant array of independent disks (RAID), network-attached storage, optical storage, tape drive, backup system, cloud storage, or any combination of the foregoing. Memory 120 may be, or may include therein, a database or databases or data stored in other configurations, and may include a stored copy of operational software such as an operating system and operational software. Many other configurations are also possible, and are intended to be encompassed within the broad scope of this Specification.

[0044] I/O block 140 may be provided to communicatively couple SoC 100 to a wired or wireless network. A "network," as used throughout this Specification, may include any communicative platform operable to exchange data or information within or between computing devices, including by way of non-limiting example, serial or parallel communication ports, an ad-hoc local network, an internet architecture providing computing devices with the ability to electronically interact, an asynchronous transfer mode (ATM) network, a plain old telephone system (POTS), which computing devices could use to perform transactions in which they may be assisted by human operators or in which they may manually key data into a telephone or other suitable electronic equipment, any packet data network (PDN) offering a communications interface or exchange between any two nodes in a system, or any local area network (LAN), metropolitan area network (MAN), wide area network (WAN), wireless local area network (WLAN), virtual private network (VPN), intranet, or any other appropriate architecture or system that facilitates communications in a network or telephonic environment.

[0045] Power manager 130 may be or include a power supply, as well as logic to regulate power to SoC 100. For example, power manager 130 may include logic to detect different operating modes, and to intelligently provide a regulated voltage to on-chip components as the demands of those operating modes dictate.

[0046] For example, temperature sensors within power manager 130 may detect when the temperature of processor 110 rises above a threshold, which may indicate that processor 110 is in danger of being damaged. To prevent damage, power manager 130 may reduce the voltage supplied to processor 110, thus reducing the operating power, and reducing the temperature.

[0047] Power manager 130 may also supply different input voltages to different computing elements of SoC 100 according to the power demands of those processing elements. In various embodiments, power manager 130 may also include current limiters, voltage references, meters, sensors, transducers, drivers, switches, and any other elements that assist power manager 130 in performing its work.

[0048] FIGURE 2 is a top view of a CMP apparatus 200 according to one or more examples of the present Specification.

[0049] CMP apparatus 200 may include a rotating and extremely flat platen 340 (FIGURE 3), covered by pad 210. (Platen 340 is not visible in this top view because it is covered by pad 210.) Note that platen 340 may be durable equipment, while pad 210 may be a consumable.

[0050] In this example, wafer 220 is being polished at an appropriate stage of the manufacturing process, which may be any stage at which CMP may be used to planarize wafer 220. Wafer 220 may be any suitable integrated circuit, such as those discussed in paragraph [0027] above.

[0051] Wafer 220 is mounted upside-down in a carrier or spindle. A retaining ring may keep the wafer correctly horizontally oriented during the CMP process. For simplicity of the drawing, the carrier/spindle, backing film, and retaining ring are not shown in this illustration.

[0052] In an embodiment, while wafer 220 is being loaded onto or unloaded from CMP apparatus 200, wafer 220 is in the carrier by a vacuum. This may help prevent unwanted particles from building up on the wafer surface.

[0053] When the polishing operation is to begin, a slurry is introduced onto the surface of pad 210. This slurry may be a colloid, including an aqueous solution of a chemical reactive to the compound being polished from the surface of wafer 220. For example, if tungsten is deposited on the surface of wafer 220 and needs to be polished down to the substrate (leaving only traced interconnects), the slurry may include a chemical reactive with tungsten. For additional polishing, mechanical beads may be introduced into the colloid to abrade the top surface of wafer 220.

[0054] As polishing commences, both platen 340 (thus, pad 210) and wafer 220 are rotated. They may be rotated in the same direction. A slight downward pressure may also be applied to wafer 220, thus pressing it against pad 210. The magnitude of the force may depend on the size of the contact area.

[0055] Pad 210 may be rigid and may have a roughness of approximately 50 μm . The rigidity of pad 210 helps to maintain a uniform polishing. The rigid pad should maintain alignment with wafer 220. To facilitate this, pad 210 may in fact be an alternating stack of rigid and soft materials, which helps to maintain conformity with wafer 220. Pad 210 may be made of a porous polymeric material,

with a pore size of approximately 30 – 50 μm . In some cases, pad 210 may be consumable after a single polishing of a wafer 210.

[0056] Additional applications are viewable in the following FIGURES.

[0057] FIGURE 3 is a cutaway side view of a CMP apparatus 200 according to one or more examples of the present Specification. The embodiment of FIGURE 3 illustrates challenges that may be encountered in connection with a hydrophobic top layer. It should be noted that the illustrations of FIGURES 3 – 5 are not to either horizontal or vertical scale. Rather, the figures have been optimized to illustrate several discrete features of the embodiments disclosed. The actual dimensions of these features relative to one another may be substantially different from the apparent ratios in these FIGURES.

[0058] Visible in this embodiment are pad 210 and wafer 220, as seen in FIGURE 2. Also visible in this figure is platen 340. Pad 210 may be mechanically coupled to platen 340 via adhesive 310. As discussed above, platen 340 may be durable equipment, while pad 210 and adhesive 310 may be consumables. In some embodiments, pad 210 and adhesive 310 may be replaced after some number of polishings.

[0059] In this example, pad 210 has an aperture 230, and disposed therein is final optical element (FOE) 320. A laser 350 (or other suitable optical metrology source) may be shined through FOE 320. In an example, laser 350 may be a red laser with a wavelength of 670 nm, though any suitable source of focused electromagnetic energy may be used.

[0060] With each pass of wafer 220 over aperture 230, laser 350 may ping wafer 220 through FOE 320, and receive a return signal. An optical characteristic of the return signal may be used to determine whether polishing is complete. For example, a layer of tungsten may have been deposited over a silicon dioxide layer on a silicon substrate. In that case, a slurry appropriate for polishing tungsten may be used. As the polishing begins, laser 350 pings wafer 220 to establish a baseline reflectivity. Once the silicon dioxide layer is reached, the reflectivity will fall substantially. Thus, in an example, when the return ping falls to 50% or less of the baseline, polishing is complete.

[0061] However, as discussed above, the presence of mist 360 within aperture 230 can create difficulties. When wafer 220 passes over aperture 230,

much of the slurry will be ejected, but some may remain within aperture 230. This may form mist 360, which can diffract laser 350, thus introducing noise into the return signal. This can result in the return ping appearing more or less intense than it actually is, meaning that wafer 220 could be either over-polished or under-polished. Thus, it is desirable to have a medium with more predictable optical properties—either closer to pure air, or pure slurry—within aperture 230.

[0062] FIGURE 4 is a cutaway side view of an embodiment where a more uniform medium may be achieved within aperture 230. In one example, a hydrophobic FOE 320 may be conformally coated with a top layer 410 of hydrophilic material. In yet another example, FOE 320 may be made completely of a hydrophilic material, in which case there may not be an identifiable boundary between base layer 320 and top layer 410. In yet another embodiment, FOE 320 is made of a first material, and top layer 410 is derived from the first material, such as chemically or mechanically. In a chemical derivation, the top layer of the first material may be oxidized to give it hydrophilic properties. Oxidation may be caused, for example, by heating and or exposure to an oxygen plasma. In another embodiment, the top layer may be given hydrophilic properties by diffusion or absorption of a second material. In another embodiment, the top layer may be mechanically prepared, such as with abrasion, to give it a more hydrophilic character. Note that in some embodiments, advantages are realized by having a hybrid FOE. A hydrophobic base layer may help the FOE 320 to better bond to polishing pad 210, while hydrophilic top layer 410 realizes the advantages disclosed herein. However, this should not be construed to imply that a fully hydrophilic FOE is not within the scope of the appended claims.

[0063] In this embodiment, as wafer 220 passes over aperture 230, hydrophilic top layer 410 helps to retain more slurry within aperture 230. This forms a slurry well 420, which substantially fills aperture 230. Slurry well 420 has more predictable optical properties, and will cause minimum refraction of laser 350. A relatively shallow layer of mist 360 may still form, and may cause a small amount of refraction, but the noise in the return ping of laser 350 is substantially less in comparison to the return signal of the configuration shown in FIGURE 3.

[0064] FIGURE 5 illustrates that an existing FOE 320 may be modified to realize the advantages disclosed herein. In this example, platen 340, pad 210,

wafer 220 and FOE 320 are disclosed as in FIGURE 3. Again, pad 210 has an aperture 230, and disposed therein is FOE 320. From a commercial perspective, this may be an "off-the-shelf" pad 210 that has not been manufactured or modified for the disclosure of the present specification.

[0065] An adhesive 520 may be mechanically coupled to FOE 320, for example, around the perimeter or radius of FOE 320. A hydrophilic film 510 may then be mechanically coupled to adhesive 510, thus providing a hydrophilic top layer to the base layer of FOE 320.

[0066] Note that although this process is disclosed as an example of modifying an "off-the-shelf" FOE 320 for use with the present disclosure, the process disclosed could just as easily be used to manufacture an FOE with a hydrophilic top layer 510 *ab initia*.

[0067] Again, with this embodiment, a slurry well 420 is formed within aperture 230, substantially filling aperture 230. Slurry well 420 has relatively predictable optical performance, while the thickness of mist 360, with less predictable optical performance, is minimized.

[0068] FIGURE 6 is a flow chart of a method 600 of manufacturing an integrated circuit according to one or more examples of the present Specification. Method 600 may be used to manufacture SoC 100 of FIGURE 1, any of the circuits disclosed in paragraph [0027], or any other suitable integrated circuit or other planarized wafer-based article of manufacture.

[0069] Starting in block 602, at block 604, deposition takes place. The deposition operation may include preparing an appropriate wafer, such as a wafer cut from a monocrystalline silicon ingot, and depositing a material (such as a metal, for example) on the substrate. Because of the nature of the deposition, this may result in an over-deposit of the material. By way of example, tungsten may be deposited on a silicon substrate, and some of it may need to be polished away.

[0070] In block 606, polishing begins. This may include preparing wafer 220 according to the illustrations of FIGURES 2 – 5, introducing an appropriate slurry (such as a slurry appropriate for polishing tungsten), and rotating both wafer 220 and platen 340.

[0071] On the first pass of wafer 220 over aperture 230, laser 350 may ping wafer 220 and measure the intensity of the light returned, thus establishing a

baseline. Note that decreasing magnitude of a red 670 nm-wavelength laser is disclosed herein by way of example, but numerous other examples are possible. The laser could be of any suitable color and wavelength to the application, and may vary according to specific embodiments. Furthermore, if a dielectric is being polished down to a metal, an increase in reflectivity could be the trigger condition. In another embodiment, a monochromatic laser is not used, but rather a multi-chromatic white light may be used. In that case, in one example, the intensity of the reflected signal may not be used, but rather the color spectrum of the return signal. In block 608, the changing character of the reflected light may indicate the changing composition of the top surface material on the wafer (e.g., tungsten will reflect a different spectrum from silicon, similar to mass spectrometry).

[0072] In decision block 610, it is determined whether the condition has been met. In this example, the condition is whether the reflectivity has fallen below 50% of the baseline, but any suitable threshold may be used, including any of those disclosed in the examples above.

[0073] If the threshold has not been reached, then in block 606, polishing continues, and on each pass of wafer 220 over aperture 230, a new measurement is taken.

[0074] When the threshold has been reached, control passes to block 612, where the wafer is finalized. Finalizing the wafer has been collapsed into a single block in this chart for purposes of simplicity, but it should be understood that, like all of the blocks disclosed in method 600, this may represent many discrete operations. Finalizing may include, for example, depositing additional layers of materials, performing additional CMPs (with or without the teachings of the present Specification), adding multiple layers of routing and vias, and performing "back end of the line" (BEOL) operations (which may also include CMPs, with or without the teachings of the present Specification).

[0075] In block 699, the method is done.

[0076] The foregoing outlines features of several embodiments so that those skilled in the art may better understand various aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the

embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

[0077] All or part of any hardware element disclosed herein may readily be provided in a system-on-a-chip (SoC), including central processing unit (CPU) package. An SoC represents an integrated circuit (IC) that integrates components of a computer or other electronic system into a single chip. The SoC may contain digital, analog, mixed-signal, and radio frequency functions, all of which may be provided on a single chip substrate. Other embodiments may include a multi-chip-module (MCM), with a plurality of chips located within a single electronic package and configured to interact closely with each other through the electronic package. In various other embodiments, the computing functionalities disclosed herein may be implemented in one or more silicon cores in Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), and other semiconductor chips.

[0078] Note also that in certain embodiment, some of the components may be omitted or consolidated. In a general sense, the arrangements depicted in the figures may be more logical in their representations, whereas a physical architecture may include various permutations, combinations, and/or hybrids of these elements. It is imperative to note that countless possible design configurations can be used to achieve the operational objectives outlined herein. Accordingly, the associated infrastructure has a myriad of substitute arrangements, design choices, device possibilities, hardware configurations, software implementations, and equipment options.

[0079] In a general sense, any suitably-configured processor can execute any type of instructions associated with the data to achieve the operations detailed herein. Any processor disclosed herein could transform an element or an article (for example, data) from one state or thing to another state or thing. In another example, some activities outlined herein may be implemented with fixed logic or programmable logic (for example, software and/or computer instructions executed by a processor) and the elements identified herein could be some type of a

programmable processor, programmable digital logic (for example, a field programmable gate array (FPGA), an erasable programmable read only memory (EPROM), an electrically erasable programmable read only memory (EEPROM)), an ASIC that includes digital logic, software, code, electronic instructions, flash memory, optical disks, CD-ROMs, DVD ROMs, magnetic or optical cards, other types of machine-readable mediums suitable for storing electronic instructions, or any suitable combination thereof.

[0080] In operation, a storage may store information in any suitable type of tangible, non-transitory storage medium (for example, random access memory (RAM), read only memory (ROM), field programmable gate array (FPGA), erasable programmable read only memory (EPROM), electrically erasable programmable ROM (EEPROM), etc.), software, hardware (for example, processor instructions or microcode), or in any other suitable component, device, element, or object where appropriate and based on particular needs. Furthermore, the information being tracked, sent, received, or stored in a processor could be provided in any database, register, table, cache, queue, control list, or storage structure, based on particular needs and implementations, all of which could be referenced in any suitable timeframe. Any of the memory or storage elements disclosed herein, such as memory and storage, should be construed as being encompassed within the broad terms 'memory' and 'storage,' as appropriate. A non-transitory storage medium herein is expressly intended to include any non-transitory special-purpose or programmable hardware configured to provide the disclosed operations, or to cause a processor to perform the disclosed operations.

[0081] Computer program logic implementing all or part of the functionality described herein is embodied in various forms, including, but in no way limited to, a source code form, a computer executable form, machine instructions or microcode, programmable hardware, and various intermediate forms (for example, forms generated by an assembler, compiler, linker, or locator). In an example, source code includes a series of computer program instructions implemented in various programming languages, such as an object code, an assembly language, or a high-level language such as OpenCL, FORTRAN, C, C++, JAVA, or HTML for use with various operating systems or operating environments, or in hardware description languages such as Spice, Verilog, and VHDL. The source

code may define and use various data structures and communication messages. The source code may be in a computer executable form (e.g., via an interpreter), or the source code may be converted (e.g., via a translator, assembler, or compiler) into a computer executable form, or converted to an intermediate form such as byte code. Where appropriate, any of the foregoing may be used to build or describe appropriate discrete or integrated circuits, whether sequential, combinatorial, state machines, or otherwise.

[0082] In one example embodiment, any number of electrical circuits of the FIGURES may be implemented on a board of an associated electronic device. The board can be a general circuit board that can hold various components of the internal electronic system of the electronic device and, further, provide connectors for other peripherals. More specifically, the board can provide the electrical connections by which the other components of the system can communicate electrically. Any suitable processor and memory can be suitably coupled to the board based on particular configuration needs, processing demands, and computing designs. Other components such as external storage, additional sensors, controllers for audio/video display, and peripheral devices may be attached to the board as plug-in cards, via cables, or integrated into the board itself. In another example, the electrical circuits of the FIGURES may be implemented as stand-alone modules (e.g., a device with associated components and circuitry configured to perform a specific application or function) or implemented as plug-in modules into application specific hardware of electronic devices.

[0083] Note that with the numerous examples provided herein, interaction may be described in terms of two, three, four, or more electrical components. However, this has been done for purposes of clarity and example only. It should be appreciated that the system can be consolidated or reconfigured in any suitable manner. Along similar design alternatives, any of the illustrated components, modules, and elements of the FIGURES may be combined in various possible configurations, all of which are within the broad scope of this Specification. In certain cases, it may be easier to describe one or more of the functionalities of a given set of flows by only referencing a limited number of electrical elements. It should be appreciated that the electrical circuits of the FIGURES and its teachings

are readily scalable and can accommodate a large number of components, as well as more complicated/sophisticated arrangements and configurations. Accordingly, the examples provided should not limit the scope or inhibit the broad teachings of the electrical circuits as potentially applied to a myriad of other architectures.

[0084] Numerous other changes, substitutions, variations, alterations, and modifications may be ascertained to one skilled in the art and it is intended that the present disclosure encompass all such changes, substitutions, variations, alterations, and modifications as falling within the scope of the appended claims. In order to assist the United States Patent and Trademark Office (USPTO) and, additionally, any readers of any patent issued on this application in interpreting the claims appended hereto, Applicant wishes to note that the Applicant: (a) does not intend any of the appended claims to invoke paragraph six (6) of 35 U.S.C. section 112 (pre-AIA) or paragraph (f) of the same section (post-AIA), as it exists on the date of the filing hereof unless the words "means for" or "steps for" are specifically used in the particular claims; and (b) does not intend, by any statement in the specification, to limit this disclosure in any way that is not otherwise expressly reflected in the appended claims.

Example Implementations

[0085] There is disclosed in one example, a final optical element for use with a chemical mechanical polish process to measure a reflectivity profile of a wafer being polished, comprising: a transparent final optical element base material; and a transparent hydrophilic surface material.

[0086] There is further disclosed an example, wherein the base material is hydrophobic.

[0087] There is further disclosed an example, wherein the base material is hydrophilic.

[0088] There is further disclosed an example, wherein the surface material is coupled to the base material via an adhesive.

[0089] There is further disclosed an example, wherein the transparent hydrophilic surface is a derivative of the base material.

[0090] There is further disclosed an example, wherein the transparent hydrophilic surface is a chemical derivative of the base material.

[0091] There is further disclosed an example, wherein the transparent hydrophilic surface is a mechanical derivative of the base material.

[0092] There is further disclosed an example, wherein the surface material conformally coats the base material.

[0093] A chemical mechanical polishing pad comprising an aperture and the final optical element of any of the preceding examples.

[0094] An apparatus to perform chemical mechanical polish of a semiconductor wafer, comprising: a platen; an adhesive mechanically coupled to the platen; a pad mechanically coupled to the adhesive and having an aperture therein; and a final optical element disposed within the aperture, comprising: a transparent final optical element base material; and a transparent hydrophilic surface material.

[0095] There is further disclosed an example, wherein the base material is hydrophobic.

[0096] There is further disclosed an example, wherein the base material is hydrophilic.

[0097] There is further disclosed an example, wherein the surface material is coupled to the base material via an adhesive.

[0098] There is further disclosed an example, wherein the transparent hydrophilic surface is a derivative of the base material.

[0099] There is further disclosed an example, wherein the transparent hydrophilic surface is a chemical derivative of the base material.

[0100] There is further disclosed an example, wherein the transparent hydrophilic surface is a mechanical derivative of the base material.

[0101] There is further disclosed an example, wherein the surface material conformally coats the base material.

[0102] There is further disclosed in an example, a method of manufacturing a final optical element for a semiconductor chemical mechanical polishing process, comprising: forming a final optical element base layer; and forming a hydrophilic surface material as a surface of the final optical element base layer.

[0103] There is further disclosed an example, wherein adding the surface material comprises chemically altering a top surface of the base layer.

[0104] There is further disclosed an example, wherein adding the surface material comprises mechanically altering a top surface of the base layer.

[0105] There is further disclosed an example, wherein adding the surface material comprises conformally depositing a second material above the base layer.

[0106] There is further disclosed an example, wherein adding the surface material comprises adding an adhesive and adhering the surface material to the base layer.

[0107] There is further disclosed an example, wherein the final optical element base layer is hydrophilic, and wherein adding a hydrophilic surface material comprises exposing a top surface of the base layer.

[0108] There is further disclosed an example, wherein the final optical element base layer is hydrophobic.

[0109] There is further disclosed an example, wherein the final optical element base layer is hydrophilic.

[0110] There is further disclosed in an example, a method of manufacturing an integrated circuit comprising performing a chemical mechanical polish using the apparatus, or an apparatus formed by the method, of any preceding example.

[0111] There is further disclosed an example of an apparatus comprising means for performing the method.

Claims

1. A final optical element for use with a chemical mechanical polish process to measure a reflectivity profile of a wafer being polished, comprising:
 - a transparent final optical element base material; and
 - a transparent hydrophilic surface material.
2. The final optical element of claim 1, wherein the base material is hydrophobic.
3. The final optical element of claim 1, wherein the base material is hydrophilic.
4. The final optical element of claim 1, wherein the surface material is coupled to the base material via an adhesive.
5. The final optical element of claim 1, wherein the transparent hydrophilic surface is a derivative of the base material.
6. The final optical element of claim 5, wherein the transparent hydrophilic surface is a chemical derivative of the base material.
7. The final optical element of claim 5, wherein the transparent hydrophilic surface is a mechanical derivative of the base material.
8. The final optical element of claim 1, wherein the surface material conformally coats the base material.
9. A chemical mechanical polishing pad comprising an aperture and the final optical element of any of claims 1 – 8.
10. An apparatus to perform chemical mechanical polish of a semiconductor wafer, comprising:
 - a platen;
 - an adhesive mechanically coupled to the platen;

a pad mechanically coupled to the adhesive and having an aperture therein; and

a final optical element disposed within the aperture, comprising:

a transparent final optical element base material; and

a transparent hydrophilic surface material.

11. The apparatus of claim 10, wherein the base material is hydrophobic.
12. The apparatus of claim 10, wherein the base material is hydrophilic.
13. The apparatus of claim 10, wherein the surface material is coupled to the base material via an adhesive.
14. The apparatus of claim 10, wherein the transparent hydrophilic surface is a derivative of the base material.
15. The apparatus of claim 14, wherein the transparent hydrophilic surface is a chemical derivative of the base material.
16. The apparatus of claim 14, wherein the transparent hydrophilic surface is a mechanical derivative of the base material.
17. The apparatus of claim 16, wherein the surface material conformally coats the base material.
18. A method of manufacturing a final optical element for a semiconductor chemical mechanical polishing process, comprising:
 - forming a final optical element base layer; and
 - forming a hydrophilic surface material as a surface of the final optical element base layer.
19. The method of claim 18, wherein adding the surface material comprises chemically altering a top surface of the base layer.

20. The method of claim 18, wherein adding the surface material comprises mechanically altering a top surface of the base layer.
21. The method of claim 18, wherein adding the surface material comprises conformally depositing a second material above the base layer.
22. The method of claim 18, wherein adding the surface material comprises adding an adhesive and adhering the surface material to the base layer.
23. The method of claim 18, wherein the final optical element base layer is hydrophilic, and wherein adding a hydrophilic surface material comprises exposing a top surface of the base layer.
24. The method of claim 18, wherein the final optical element base layer is hydrophobic.
25. The method of claim 18, wherein the final optical element base layer is hydrophilic.

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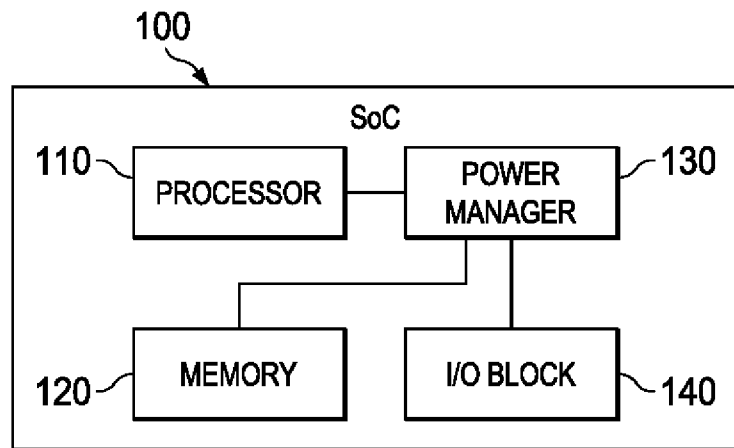


FIG. 1

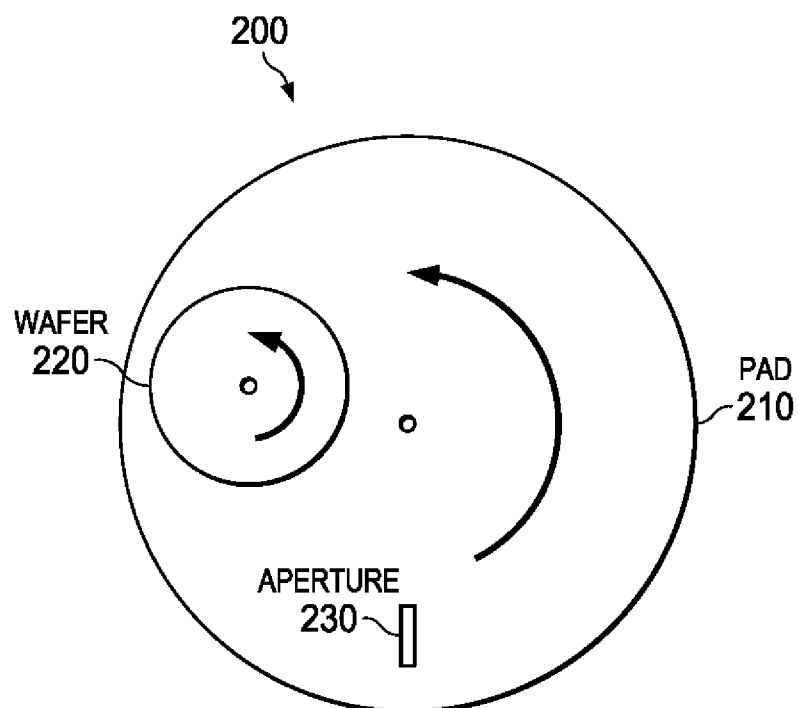
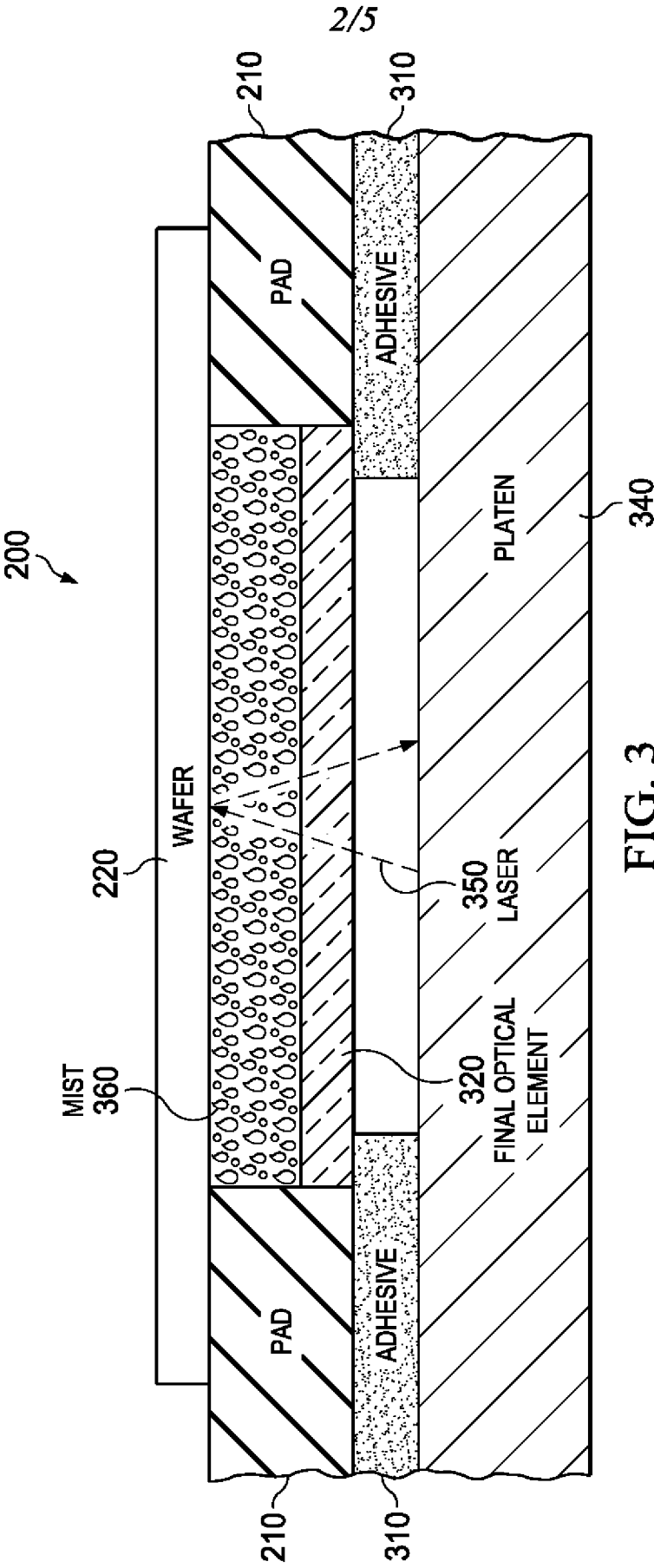


FIG. 2



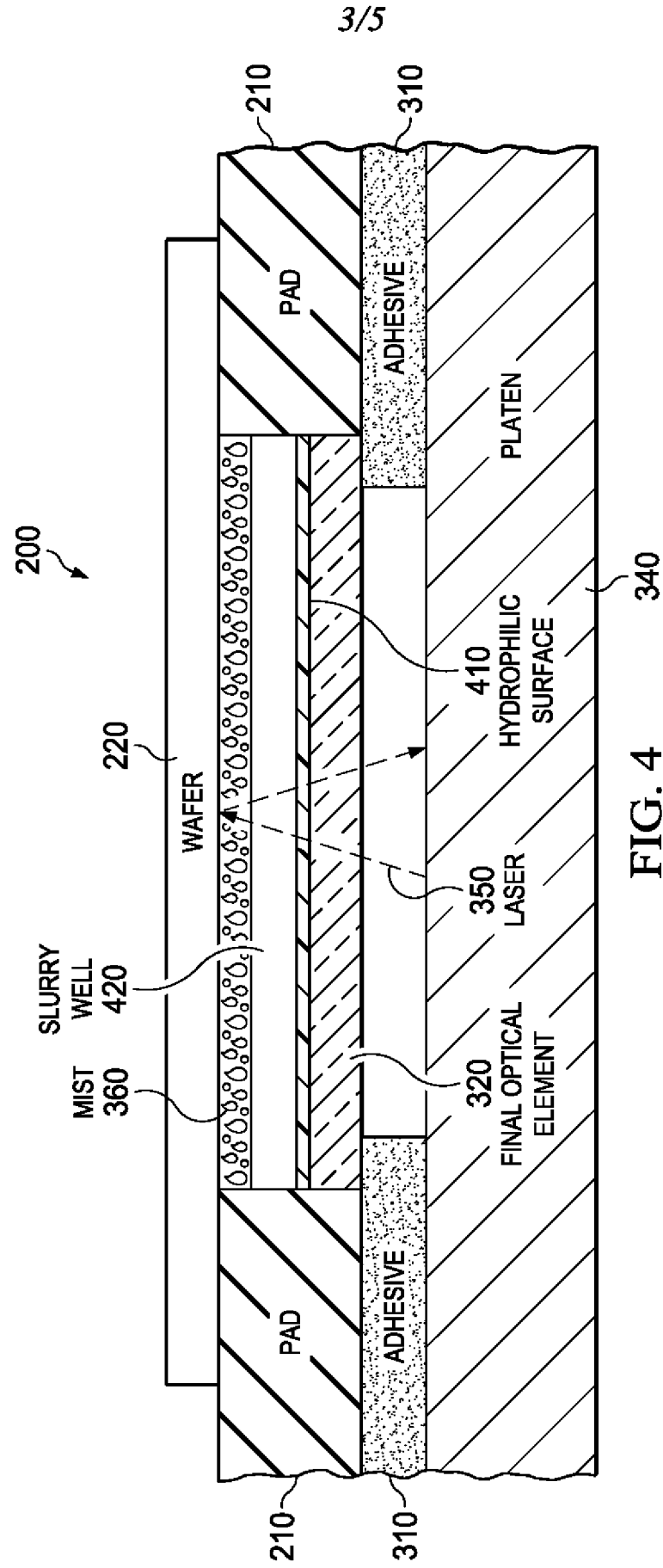


FIG. 4

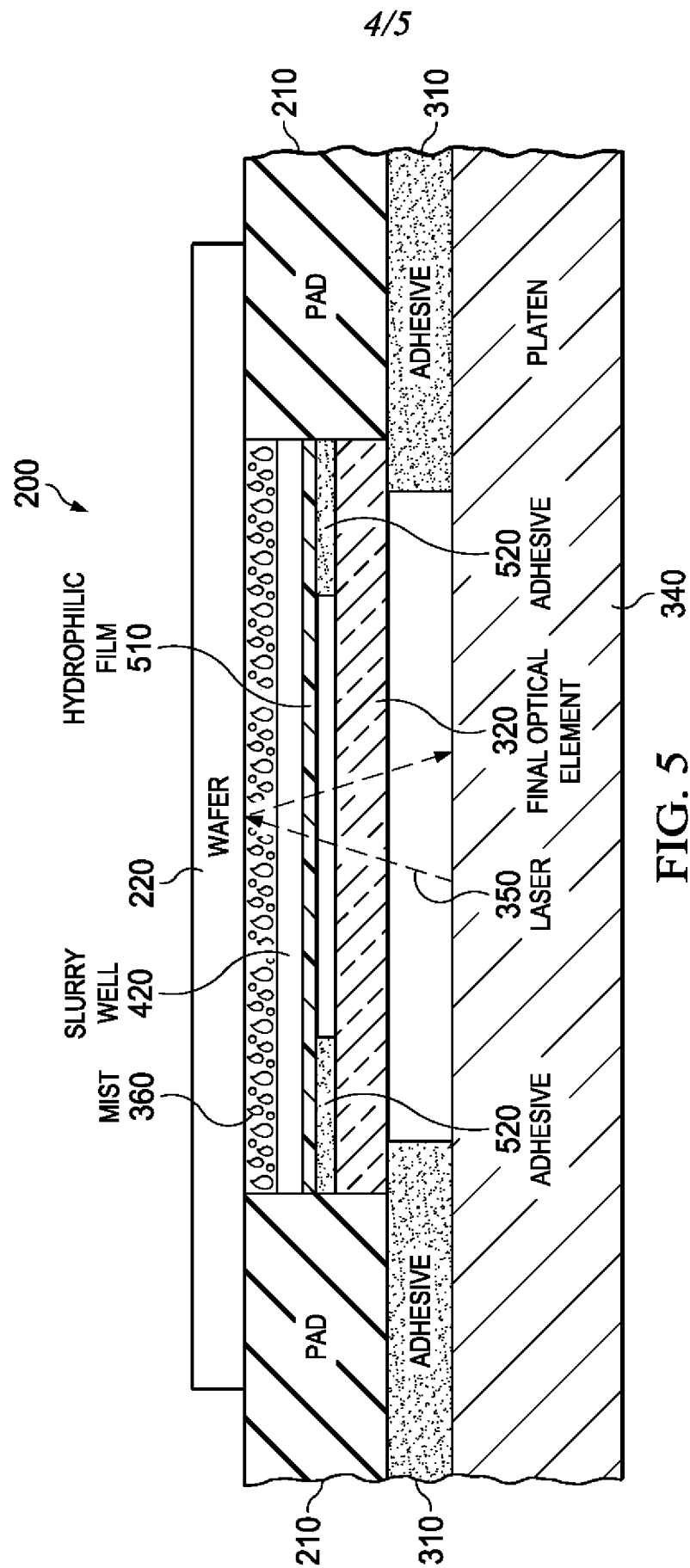


FIG. 5

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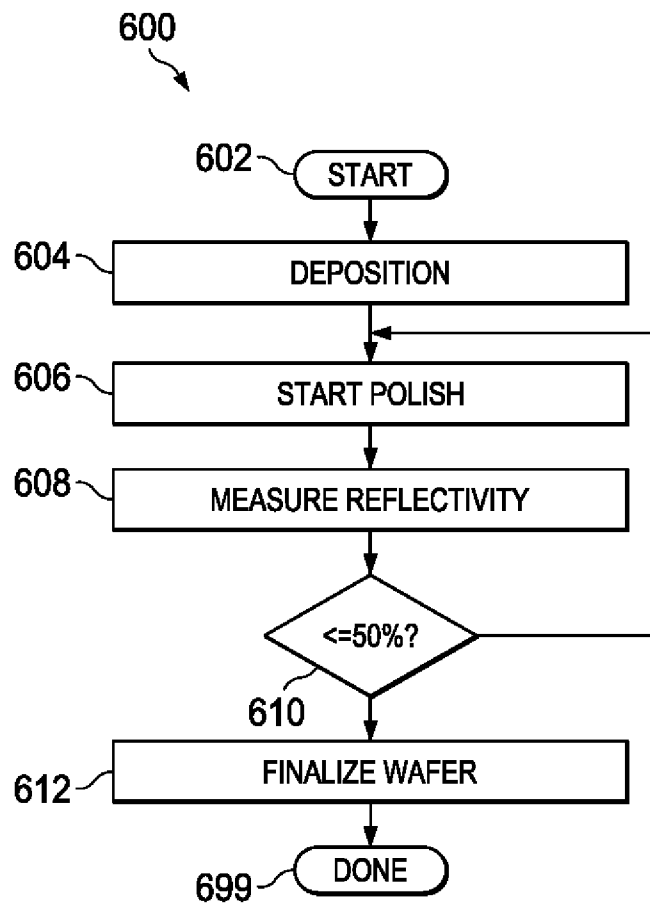


FIG. 6

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/304(2006.01)i, H01L 21/66(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/304; B24D 17/00; H01L 21/306; B24B 37/00; B24B 49/12; H01L 21/3205; H01L 21/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: CMP, pad, sense, hydrophilic, hydrophobic, optical element

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004-0082287 A1 (JASON R. WRIGHT et al.) 29 April 2004 See abstract, paragraphs [0029]-[0044], claims 4, 26 and figures 1-3.	1-25
A	US 2005-0211376 A1 (ABANESHWAR PRASAD) 29 September 2005 See abstract, paragraphs [0015], [0016], claims 1-8 and figures 1, 2.	1-25
A	US 2010-0279585 A1 (JIMIN ZHANG et al.) 04 November 2010 See abstract, paragraphs [0018]-[0025], claims 1-11 and figure 1.	1-25
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A	JP 2010-021353 A (TOSHIBA CORP.) 28 January 2010 See paragraphs [0017], [0018], claim 1 and figure 3.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 December 2016 (12.12.2016)

Date of mailing of the international search report

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Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/023501

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