

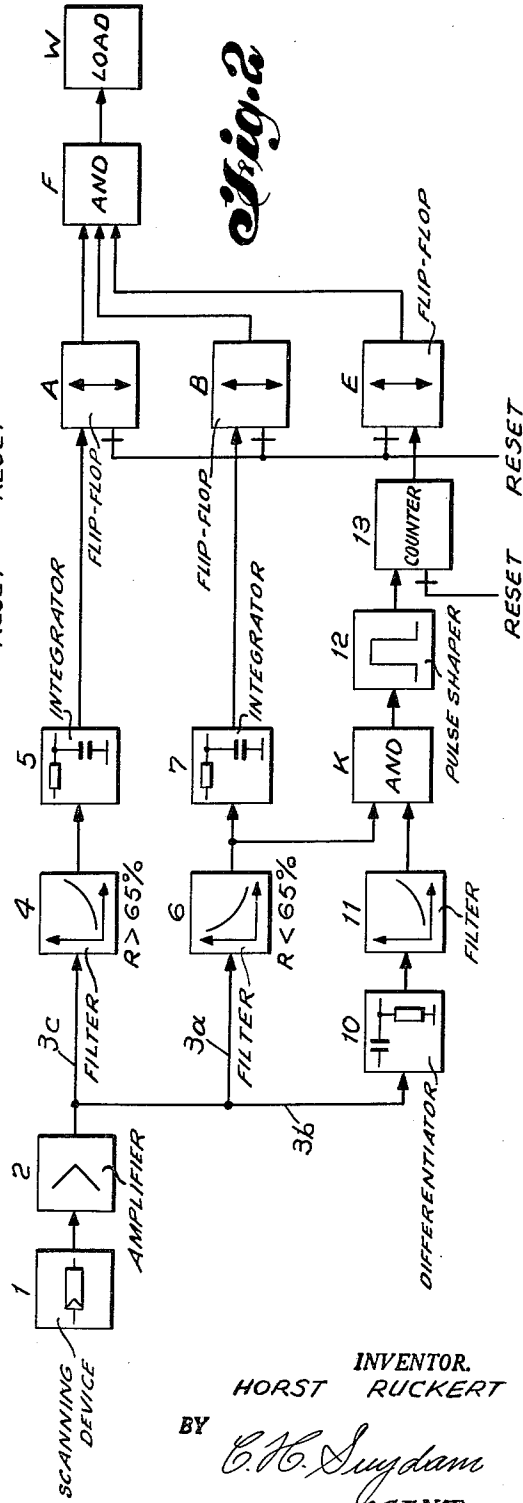
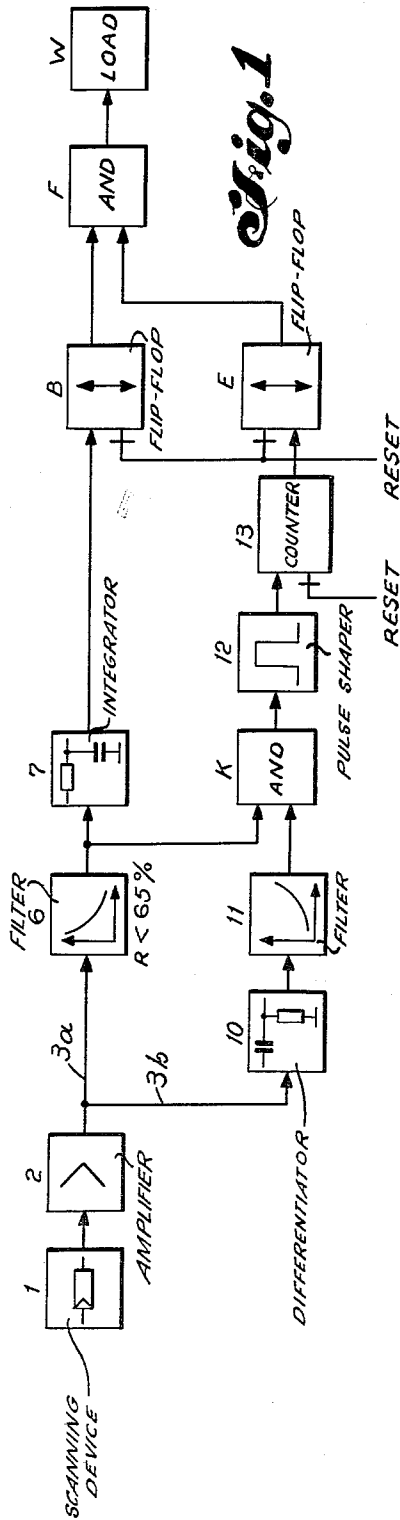
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DETECTION OF STAMPS ON DOCUMENTS

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DETECTION OF STAMPS ON DOCUMENTS

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This invention relates in general to a circuit arrangement for detecting the presence of an identification mark on a document, such as, for example, a stamp on an envelope.

In particular, the invention relates to an arrangement of the above type in which a normally stamped envelope is conveyed passed a photoelectric scanning device to produce a signal which is characteristic of the envelope's stamped condition. The signal is then applied to the inputs of two branched circuits so designed that, if an output signal is simultaneously obtained from each circuit, the signals cause a coincident gate to open and pass a control signal which may be used to influence the further conveyance of the envelope in any desired manner or to indicate the presence of a stamp.

A modification of the invention consists in adding to the circuit arrangement, described in the preceding paragraph, a third circuit whose output signal must also be applied to the coincidence gate in order to obtain the control signal. The control signal in this case may be used to influence the further motion of the envelope in a modified manner, or to indicate a stamp, usually in a more restricted sense.

There presently exists a known circuit arrangement for detecting the presence or absence of a stamp or other identification mark on a document or piece of mail. U.S. Patent 2,966,594, issued December 27, 1960, discloses the known arrangement which was jointly invented by Werner Hinz and the present applicant. The patent is assigned to the assignee of the present patent application. The disclosure of the patent is incorporated by reference in the present application.

To specifically point out the present invention is believed desirable first to describe briefly the field in which the invention is to be used and then to locate the invention in the field.

It is well known that an envelope with its stamp, in moving relative to a beam of light in a photoelectric scanning device, will modulate the output of a photocell due to the variation of the light reflected from its surface toward the photocell.

It is also known that the signal may be applied to each of a number of branch circuits connected in parallel and consisting of various combinations of amplitude responsive threshold gates, integrating circuits, storage units, AND gates, counters, etc., and, depending on the combined output signals from each circuit, a determination can be made regarding the stamped condition of the envelope. Examples of various types of known circuits are illustrated and their method of operation described in U.S. Patent 2,966,594, above referenced.

This present invention discloses a particular manner of interconnecting the known circuits which results in the attainment of the following objects of the invention.

(1) To simplify the known circuit arrangements for determining the stamped condition of an envelope, e.g., whether or not the envelope has been stamped.

(2) To increase the reliability of stamp detection circuit arrangements whereby a more positive determination can be made of whether or not an envelope has been stamped.

(3) To provide a simple circuit arrangement for determining the stamped condition of an envelope regardless

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of the relative background brightness of the envelope as compared with the average brightness of the stamp.

These and other objects of the invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawing, in which:

FIG. 1 is a block diagram illustrating a preferred embodiment of my invention.

FIG. 2 is a block diagram illustrating a modification of my invention by which a more limited selection of the stamped condition of an envelope can be obtained as compared with the embodiment of FIG. 1.

Referring to FIG. 1, block 1 symbolizes a photoelectric scanning device in which a light beam is directed onto a succession of stamped envelopes, or the like, as they pass the device. The device includes a photoelectric cell which receives light reflected from the stamped envelopes and generates a signal voltage proportional to the intensity of the reflected light. The amplifier 2 raises the level of the signal voltage to the desired value for application to the branch circuits 3a and 3b simultaneously.

The circuit 3a comprises an amplitude responsive gate 6 which passes a signal voltage to an integrating device 7 only when the amplitude of the signal from amplifier 2 is lower than that corresponding to a predetermined optimum reflectance value defined as follows: The percentage of the incident light reflected by diffusion from the envelope or the stamp in the direction of the photocell forming part of the photoelectric device is called the reflectance value. In general the reflectance value of postage stamps is usually below 65% as compared to 100% for a standard white reflecting surface. In this application the reflectance value that is usually not exceeded is called the optimum reflectance value, as distinct from the various actual reflectance values that any particular stamp may have. It will be clear that, even though the mean stamp reflectance value will be below the optimum value, there will be occasions during the scanning period when the stamp reflectance value may rise above the optimum value. Hereinafter the optimum value will be referred to as 65%.

The integrating device 7 may comprise the conventional series resistor-shunt capacitor network. When the capacitor accumulates a predetermined charge, a voltage pulse is applied to the store B, which may comprise a conventional bistable multivibrator or flip-flop circuit. The resulting change in the condition of the flip-flop places a marking voltage on one of the inputs of AND gate F. The amount of the charge depends on the choice of several parameters, for example, the time constant of the RC network, the speed with which the envelope passes the photoelectric cell of the scanning device, and the amplitude of the voltage applied to the capacitor at the beginning of the charging period.

The invention has been found to operate satisfactorily when the parameters are such that the predetermined charge necessary to produce the required voltage is accumulated during the time interval required for a width somewhat less than the width of the stamp to pass the light beam.

The circuit 3b comprises a direct-current suppressor circuit 10, amplitude responsive gate 11, AND gate K, pulse shaper 12, pulse counter 13 and store E. The purpose of the circuit 3b is to provide a second marker voltage for AND gate F in response to information stored in E. The need of this second marker voltage arises from the fact that a dark envelope having a reflectance value less than 65% will cause a marker voltage to be applied to AND gate F whether the envelope is stamped or not. It is clear that this condition of operation would be undesirable and hence the necessity of having a second criterion, essentially independent of reflectance values, to indicate that the envelope is stamped (or unstamped).

The second criterion is based on the counting of a predetermined number of pulses before a second store or flip-flop circuit is "flipped" to the condition that indicates that the desired count has been completed and that that "information" has been stored. On the completion of the store, a second marking voltage is applied to the second input of AND gate F. As previously stated the simultaneous application of both marking voltages causes the gate F to open and pass a signal indicating that the envelope is stamped.

The counting operation is performed as follows:

The input signal voltage applied to circuits 3a and 3b consists of an A.-C. voltage superimposed on a D.-C. voltage. The A.-C. component results from changes in the reflectance value due to the printing on the stamp. At the output of the amplitude responsive gate 6 a voltage appears for that part of the input signal representing a reflectance of less than 65%. Such a condition exists when (1) a light or bright envelope is stamped, (2) a dark envelope is stamped, and (3) a dark envelope is not stamped. No output signal appears when a light envelope is not stamped. The pulse is applied as a first marker pulse to one input of AND gate K.

The second marker pulse for AND gate K is obtained from the input pulse after the D.-C. component has been removed by suppressor circuit 10 and after the amplitude responsive gate 11 has passed only those pulses having an amplitude greater than a predetermined value. The amplitude responsive gate thus eliminates pulses which may be produced from stray A.-C. signals and cause a dark unstamped envelope to go through as a stamped envelope. The suppressor circuit 10 may be a conventional peaker or differentiating circuit. The pulses passed by AND gate K are shaped in shaper 12 and counted in counter 13. The counter is so designed that following a predetermined number of counts a voltage is applied to a store E as "information" as above described.

It will be clear that when a dark envelope having no stamp is scanned there will be no marker pulse applied to storage device E since, with no stamp, there will be no A.-C. pulses applied to AND gate K and no count made by counter 13. As a result, AND gate F cannot pass a signal indicative of a stamped envelope. It will also be clear that when a bright envelope with no stamp is scanned there can be no information stored in either store B or store E and AND gate F will not indicate a stamped envelope.

Referring now to FIG. 2, illustrating a modification of the invention, a branch circuit 3c is also connected in parallel with branch circuits 3a and 3b. Branch circuit 3c comprises substantially the same combination of circuit elements as does branch circuit 3a. The amplitude responsive gate 4 delivers an output signal only when the amplitude of the input signal is greater than the optimum reflectance value, rather than less than that value as was the case for gate 6. Integrating device 5 may have the same design as that described for device 7 except for the value of the time constant of the RC network. Branch circuit 3c operates well with branch circuit 3a when the RC time constant of the integrating device 5 is such that the predetermined charge necessary to produce the required voltage is accumulated during a time period at least somewhat greater than the sum of the periods for which the reflectance value of the stamp is greater than 65%. This insures that, in order to recognize a stamp when employing the three branch circuits, a certain portion of the total scanning length must have a reflectance value greater than the optimum reflectance value.

Branch circuit 3c also contains a store or flip-flop circuit A. When "information" is stored in A an output voltage is also applied to the input of AND gate F. A signal is passed to the output circuit of F only when input or marker voltages are applied simultaneously to each of the three inputs.

A feature of the invention illustrated in FIG. 2 is that

a selection can be made between light and dark envelopes when both are stamped. It is clear that only the light envelope would give an output voltage from AND gate F.

The blocks W in FIGS. 1 and 2 represent work or load circuits which may be controlled in response to the output or control signal from AND gate F.

The leads, labeled RESET, to the stores A, B, and E and to the counter 13 are to indicate that these circuits must be restored or reset to their original condition prior to the scanning of each envelope. Such resetting circuits are well-known to those skilled in the art and are not illustrated in detail since they form no part of the present invention.

While I have described above the principles of my invention in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of my invention as set forth in the objects thereof and in the accompanying claims.

I claim:

1. A circuit arrangement to determine the stamped condition of an envelope or document regardless of the background reflectance of the envelope as compared with the reflectance of a stamp having a certain number of reflectance variations below an optimum reflectance value comprising:

means to generate a signal voltage proportional to the successive reflectance values of a portion of said envelope on which a stamp may be normally placed;

means to apply said voltage simultaneously to the inputs of a first circuit having a first storage device and a second circuit having a second storage device including a bistable device;

means in said first circuit to store information in said first storage device only when said signal contains reflectance values lower than said optimum reflectance value for a predetermined time period;

a second means in said second circuit to store information in said second storage device only when said signal contains said certain number of variations in reflectance values exceeding a given range in a time period substantially equal to said first mentioned predetermined time period;

means connecting the output of each of said storage devices to an AND gate whereby the simultaneous occurrence of information in said devices produces a signal in the output of said AND gate to indicate the stamped condition of said envelope.

2. A circuit arrangement according to claim 1 wherein said first means to store information comprises:

a first amplitude responsive gate which passes said signal voltage only when the amplitude thereof is lower than the voltage corresponding to said optimum reflectance value;

an integrating circuit connected between said first amplitude responsive gate and said first storage device; and wherein said second means to store information comprises:

a second amplitude responsive gate which passes said signal voltage only when the amplitude thereof exceeds a predetermined value;

a second AND gate to which the output signals of said first and second amplitude responsive gates are simultaneously applied; and

means for counting the output signals from said second AND gate until a predetermined number of counts is obtained and the information stored in said second storage device.

3. A circuit arrangement according to claim 2 further comprising a direct current suppressor circuit connected between said second amplitude responsive device and said signal voltage generating means.

4. A circuit arrangement according to claim 2 further

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comprising a pulse shaper connected between said second AND gate and said counting means.

5. A circuit arrangement according to claim 1 further comprising:

a third circuit connected to said generator means and containing a third storage device; and means in said third circuit to store information in said third storage device only when said signal contains a reflectance value greater than said optimum reflectance value for a predetermined time period.

6. A circuit arrangement according to claim 5 wherein said third means to store information comprises:

a third amplitude responsive gate which passes said signal voltage only when the amplitude of said voltage is greater than that corresponding to the optimum reflectance value of said stamp; and

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an integrating circuit connected between said third amplitude responsive gate and said third storage device.

7. A circuit arrangement according to claim 6 wherein said integrating circuit has a time constant which is greater than the sum of the time periods for which the reflectance value of the stamp is greater than the optimum reflectance value.

References Cited in the file of this patent

UNITED STATES PATENTS

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2,966,594	Hinz et al.	Dec. 27, 1960
2,991,369	Grewe	July 4, 1961