SYSTEM AND METHOD FOR INCREASING BREAKDOWN VOLTAGE OF LOCOS ISOLATED DEVICES

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ABSTRACT

An efficient method is disclosed for increasing the breakdown voltage of an integrated circuit device that is isolated by a local oxidation of silicon (LOCOS) process. The method comprises forming a portion of a field oxide in an integrated circuit so that the field oxide has a gradual profile. The gradual profile of the field oxide reduces impact ionization in the field oxide by creating a reduced value of electric field for a given value of applied voltage. The reduction in impact ionization increases the breakdown voltage of the integrated circuit. The gradual profile is formed by using an increased thickness of pad oxide and a reduced thickness of silicon nitride during a field oxide oxidation process.
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CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application is related to U.S. patent application Ser. No. (Attorney Docket Number P06588) entitled “System and Method for Creating Different Field Oxide Profiles in a LOCOS Process” that is being filed concurrently with this patent application. This patent application and U.S. patent application Ser. No. (Attorney Docket Number P06588) are both owned by the same assignee.

TECHNICAL FIELD OF THE INVENTION

[0002] The present invention is generally directed to semiconductor technology and, in particular, to a method for increasing the breakdown voltage of integrated circuit devices that are isolated by a local oxidation of silicon (LOCOS) process.

BACKGROUND OF THE INVENTION

[0003] In recent years, there have been great advancements in the speed, power, and complexity of integrated circuits. Large scale integrated circuits comprise thousands of devices placed on a single integrated circuit chip. A standard process for electrically isolating the devices on an integrated circuit chip is the local oxidation of silicon process (LOCOS process).

[0004] The creation of a prior art LOCOS isolation structure is illustrated in FIG. 1 and in FIG. 2. The structure 100 shown in FIG. 1 comprises a silicon substrate 100. A layer of pad oxide 120 made up of silicon dioxide (SiO₂) is placed on the silicon substrate 100. Then a layer 130 of silicon nitride (Si₃N₄) is placed on the layer pad oxide 120. A mask and etch procedure is used to etch an aperture 140 through the silicon nitride layer 130 and through the pad oxide layer 120 down to the silicon substrate 100. The application of the mask and etch procedure creates the structure 100 shown in FIG. 1.

[0005] Then the portions of the silicon substrate 100 that are exposed through aperture 140 are exposed to steam (H₂, O₂) at a relatively high temperature (e.g., one thousand degrees Celsius (1000°C)). The oxygen in the steam oxidizes the silicon substrate 100 to form silicon dioxide (SiO₂). The oxidation process causes the oxidized portion of the silicon substrate to increase in size.

[0006] The resulting structure 200 is shown in FIG. 2. The oxidized portion of the silicon substrate 100 is designated with reference numeral 210. As shown in FIG. 2, the oxidized portion 210 of the silicon substrate 100 is sometimes referred to as a field oxide. The field oxide 210 forms an isolation structure or isolation barrier that electrically separates and isolates portions of the integrated circuit chip.

[0007] At the edges of the field oxide 210 (near the edges of the silicon nitride portions 130) the thickness of the field oxide tapers off. The maximum thickness of the field oxide 210 (shown by double arrows in FIG. 2) gradually decreases near edges of the field oxide 210 and tapers down to the thickness of the pad oxide 120.

[0008] The tapering profile of the edges of the field oxide 210 forms a portion of the field oxide 210 that is known as a "bird's beak." The bird's beak portion of the field oxide 210 in FIG. 2 is designated with reference numeral 220.

[0009] If the bird's peak portion of the field oxide has a relatively graded slow tapering profile the resulting bird's beak profile will have the bird's peak profile 300 shown in FIG. 3. For convenience in description the bird's beak profile 300 will be referred to as a "graded" bird's beak.

[0010] If the bird's peak portion of the field oxide has a relatively short quick tapering profile the resulting bird's beak profile will have the bird's peak profile 400 shown in FIG. 4. For convenience in description the bird's peak profile 400 will be referred to as an "abrupt" bird's beak.

[0011] In prior art manufacturing processes a thick pad oxide and/or a thin silicon nitride layer will create a graded bird's beak 300. Similarly, in prior art manufacturing processes a thin pad oxide and/or a thick silicon nitride layer will create an abrupt bird's beak 400.

[0012] A significant advantage of the abrupt bird's beak is that the abrupt bird's beak takes up less lateral space than a graded bird's beak. This means that there is less space required to form the field oxide isolation structure. Therefore there is more space remaining in the integrated circuit chip for the integrated circuit devices (e.g., transistors). This concept is usually expressed by stating that the abrupt bird's beak provides a better packing density for the integrated circuit devices. A major drawback of the abrupt bird's beak is that the abrupt bird's beak has a lower breakdown voltage.

[0013] Conversely, a major advantage of the graded bird's beak is that it provides a higher breakdown voltage. But the graded bird's beak takes up more lateral space than an abrupt bird's beak. This means that the graded bird's beak has a correspondingly worse packing density in the integrated circuit chip for the integrated circuit devices (e.g., transistors).

[0014] In an integrated circuit device that is isolated by a LOCOS process it is well known that the bird's beak is one of the areas that has a high value of impact ionization. It is also well known that the presence of increased impact ionization reduces the breakdown voltage of the integrated circuit device. Therefore, in order to increase the breakdown voltage of a LOCOS isolated device, it would be desirable to decrease the amount of impact ionization in the LOCOS isolated device.

[0015] There is a need in the art for an efficient method for manufacturing an integrated circuit that has an increased breakdown voltage. In particular, there is a need in the art for a method that is capable of increasing a breakdown voltage in a LOCOS isolated device by reducing the amount of impact ionization that is present in a bird's beak of the device.

[0016] The present invention provides an efficient method for increasing the breakdown voltage in a LOCOS isolation integrated circuit device. The method comprises forming a portion of a field oxide in the integrated circuit so that the field oxide has a gradual profile. The gradual profile of the field oxide reduces the value of impact ionization in the field oxide by creating a reduced value of electric field for a given value of applied voltage. The reduction in the value of impact ionization increases the breakdown voltage of the integrated circuit.

[0017] As will be described more fully below, an advantageous embodiment of the method of the invention forms the gradual profile of the portion of the field oxide by using an increased thickness of pad oxide and a reduced thickness of silicon nitride during the field oxide oxidation process that creates the field oxide.
It is an object of the present invention to provide a method for efficiently manufacturing an integrated circuit that has an increased breakdown voltage.

It is an object of the present invention to provide a manufacturing method for an integrated circuit that increases a breakdown voltage in a LOCOS isolated device by reducing the amount of impact ionization that is present in a bird’s beak of the LOCOS isolated device.

It is another object of the present invention to provide a manufacturing method for an integrated circuit that creates a gradual profile in a bird’s beak field oxide in an area where it is important to have a high breakdown voltage.

The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those persons who are skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Persons who are skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Persons who are skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Before undertaking the Detailed Description of the Invention below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms “include” and “comprise,” as well as derivatives thereof, mean inclusion without limitation; the term “or,” is inclusive, meaning and/or; the phrases “associated with” and “associated therewith,” as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like.

Definitions for certain words and phrases are provided throughout this patent document, those persons of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior uses, as well as future uses, of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numerals represent like parts:

FIG. 1 illustrates an exemplary prior art structure for illustrating a local oxidation of silicon (LOCOS) process;

FIG. 2 illustrates an exemplary prior art structure that results from applying a LOCOS process to the structure shown in FIG. 1;

FIG. 3 illustrates an exemplary profile of a prior art graded bird’s beak;

FIG. 4 illustrates an exemplary profile of a prior art abrupt bird’s beak;

FIG. 5 illustrates an initial stage of a method for manufacturing a prior art integrated circuit device; and

FIGS. 6 through 10 illustrate successive stages of a manufacturing method of the present invention for manufacturing an integrated circuit device of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 5 through 10, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Persons who are skilled in the art will understand that the principles of the present invention may be implemented in any type of suitably arranged semiconductor device.

FIG. 5 illustrates a first stage of a manufacturing method for a prior art integrated circuit device. The structure shown in FIG. 5 comprises a layer of silicon substrate 510. A layer of pad oxide 520 made up of silicon dioxide (SiO_2) is placed on the silicon substrate 510. In a typical prior art integrated circuit device the thickness of the pad oxide 520 is approximately two hundred fifty Angstroms (250 Å). An Angstrom is 10^-10 meter.

Then a layer 530 of silicon nitride (Si_3N_4) is placed on the pad oxide 520. In a typical prior art integrated circuit device the thickness of the layer of silicon nitride 530 is approximately one thousand three hundred fifty Angstroms (1350 Å).

The method of the present invention uses different values of thickness for the pad oxide layer and the silicon nitride layer. In particular, the method of the present invention uses an increased thickness for the pad oxide and a decreased thickness for the silicon nitride. As will be discussed more fully below, the method of the present invention creates a bird’s beak that minimizes impact ionization. A decrease in the impact ionization increases the breakdown voltage of the integrated circuit device for a given value of applied voltage.

FIG. 6 illustrates a first stage of a manufacturing method of the present invention for manufacturing an integrated circuit device of the present invention. The structure shown in FIG. 6 comprises a layer of silicon substrate 510. A layer of pad oxide 610 made up of silicon dioxide (SiO_2) is placed on the silicon substrate 510. In one advantageous embodiment of the method of the present invention the thickness of the pad oxide 610 is approximately one thousand six hundred Angstroms (1600 Å). The 1600 Å thickness of the pad oxide 610 represents an increase of approximately one thousand three hundred fifty Angstroms (1350 Å) over the typical prior art thickness of two hundred fifty Angstroms (250 Å).

Then a layer 620 of silicon nitride (Si_3N_4) is placed on the layer of pad oxide 610. In one advantageous embodiment of the method of the present invention the thickness of the layer of silicon nitride 620 is approximately eight hundred fifty Angstroms (850 Å). The 850 Å thickness of the silicon nitride 620 represents a decrease of approximately five hundred Angstroms (500 Å) from the typical prior art thickness of one thousand three hundred fifty Angstroms (1350 Å).

A mask and etch procedure is used to etch the layer of silicon nitride 620 away from the areas of the integrated circuit chip that will require a high breakdown voltage. The portions of the layer of silicon nitride 620 over the areas of the integrated circuit chip that will require a high packing density are left in place. The resulting structure 700 is shown in FIG. 7.
In the next step of the method of the present invention a field oxide is grown on the structure 700 by subjecting the structure 700 to steam (H₂, O₂) at a relatively high temperature (e.g., one thousand degrees Celsius (1000°C)). The oxygen in the steam oxidizes the portions of the silicon substrate 510 that underlie the exposed portions of pad oxide layer 610 to form silicon dioxide (SiO₂).

The oxidation process causes the oxidized portions of the silicon substrate 510 increase in size. The resulting structure 800 is shown in FIG. 8. The field oxide portions are designated with reference numeral 810.

During the oxidation process in the area with the relatively thick pad oxide 610 and the silicon nitride layer 620 the bird’s beak profile of the field oxide 810 will have a graded and gradual profile.

In the next step of the method of the present invention the silicon nitride layer 620 is removed. Specifically, the remaining portion of the silicon nitride layer 620 is removed from the portion of the integrated circuit that will require a high breakdown voltage. The resulting structure 900 is shown in FIG. 9.

In the last step of the method of the present invention the pad oxide layer 610 is removed. Specifically, the relatively thick pad oxide layer 610 is stripped away. The resulting structure 1000 is shown in FIG. 10.

As shown in FIG. 10, the edge portions of the field oxide 810 in the portions of the integrated circuit that will require a high breakdown voltage comprise a first graded bird’s beak 1010 and a second graded bird’s beak 1020.

The first graded bird’s beak 1010 and the second graded bird’s beak 1020 each have a graded and gradual profile. The presence of a graded and gradual profile in a bird’s beak minimizes the impact ionization for a given value of applied voltage. By providing a graded and gradual profile for the bird’s beak structure the method of the present invention minimizes the impact ionization for a given value of applied voltage and correspondingly increases the breakdown voltage (for the given value of applied voltage).

One prior art method increases the breakdown voltage in an integrated circuit device by increasing the lateral distance between junctions. This type of prior art method incurs a penalty in that the device size must be correspondingly increased. Furthermore, this type of prior art method also incurs a penalty in that it increases the “on resistance” (“Rson”) of the device. The “on resistance” is the resistance between the source and the drain when the device is in an “on” condition.

The method of the present invention provides a novel and efficient method for increasing the breakdown voltage in an integrated circuit device that is LOCOS isolated. The method of the present invention gives an integrated circuit designer the flexibility to create an appropriate field oxide profile where an increased breakdown voltage is desired. Specifically, the designer can create a graded bird’s beak profile in those areas where it is more important to have a higher breakdown voltage than a high packing density.

The method of the present invention creates integrated circuit chips that comprise field oxide portions that facilitate the creation of integrated circuit devices that have a high is breakdown voltage.

Although the present invention has been described with an exemplary embodiment, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

1. A method for increasing a breakdown voltage in an integrated circuit, said method comprising the steps of:
   forming a portion of a field oxide in said integrated circuit so that said portion of said field oxide has a gradual profile; and
   using said gradual profile of said portion of said field oxide to reduce impact ionization in said portion of field oxide to increase said breakdown voltage of said integrated circuit

2-20. (canceled)