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(71) Applicant: **THE REGENTS OF THE UNIVERSITY OF CALIFORNIA** [US/US]; 1111 Franklin Street, Twelfth Floor, Oakland, California 94607-5200 (US).

(72) Inventors: **COHEN-ELIAS, Doron**; c/o ECE Department, University of California, Santa Barbara, California 93106 (US). **RODWELL, Mark**; c/o ECE Department, University of California, Santa Barbara, California 93106 (US).

(74) Agents: **GUNTHER, John E.** et al.; SoCal IP Law Group LLP, 310 N. Westlake Blvd., Suite 120, Westlake Village, California 91362 (US).

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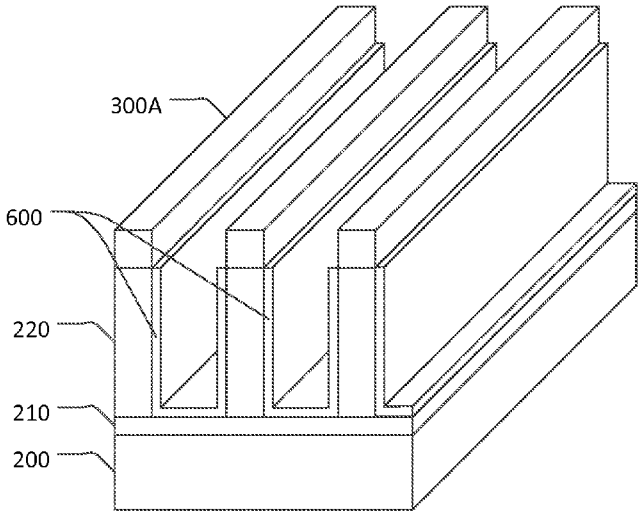
(54) Title: ADDITIVE-FIN FIELD EFFECT TRANSISTOR



(57) Abstract: Additive-fin field effect transistors and fabrication processes are disclosed. An elongate trench having opposed side walls may be formed in a sacrificial support layer on a substrate. A semiconductor layer may be deposited on at least one side wall of the trench. The support layer may be removed leaving the semiconductor layer as a fin extending from the substrate. A field effect transistor may be created in the semiconductor layer.

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ADDITIVE-FIN FIELD EFFECT TRANSISTOR

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RELATED APPLICATION INFORMATION

[0002] This patent claims priority from Provisional Patent Application No. 61/832,444, filed June 7, 2013, titled ADDITIVE-FIN FIELD EFFECT TRANSISTOR which is included by reference in its entirety.

GOVERNMENT INTERESTS

[0003] This invention was made with Government support under grant no. ECCS-1125017 awarded by the National Science Foundation. The Government has certain rights in the invention.

BACKGROUND

[0004] Field

[0005] This disclosure relates to fabrication of semiconductor devices and, in particular, to the fabrication of field effect transistors in semiconductor fins created using an additive process such as atomic layer epitaxy.

[0006] Description of the Related Art

[0007] Electrical scaling of metal oxide semiconductor field effect transistor (MOSFET) circuits aims to maintain or improve individual device performance while increasing device packing density at the same or less total circuit power dissipation level. Improving MOSFET device performance requires a reduction in critical device dimensions (*e.g.*, gate length, oxide thickness, body thickness, etc.). Increasing packing density occurs naturally with proper individual device scaling. As each device becomes smaller, it is easier to pack more in the same space. Maintaining or decreasing total circuit power dissipation while increasing circuit density requires, to the first order, each device to consume less power. This reduction also occurs naturally with device parasitic scaling for improved on-state frequency performance.

[0008] Maintaining low off-state power dissipation requires high on-state/off-state current ratio, requiring excellent gate-to-channel electrostatic control. Recent industrial efforts to improve gate control are silicon-on-insulator (SOI) and finFET. Both of these technologies limit the effective electrical body thickness of device to can improve the on/off current ratio.

[0009] In SOI, transistor devices are formed in a thin semiconductor film that is isolated from a substrate by a buried insulating layer. The body thickness of an SOI transistor is limited to the thickness of the semiconductor film on top of the buried insulation.

[0010] A "finFET" is a field effect transistor formed in a semiconductor fin that stands orthogonal to the surface of a semiconductor wafer or chip. The fin may be formed using a subtractive process (*i.e.* by etching away most of a semiconductor layer, leaving the fins standing). In finFETs, the device body thickness is equal to the thickness of the fins. Additionally, finFETs may include gate electrodes on both sides of the fins, thus "surrounding" the channel of each FET with more gate metal, improving gate control.

[0011] III-V materials (*i.e.* chemical compounds with at least one group III element and at least one group V element) are seen as a replacement for silicon in CMOS VLSI. III-V FETs can outperform silicon FETs at the same scaling generation due to the high carrier mobility of III-IV materials. Maintaining the electrostatic gate control seen in SOI and finFET requires a similar process and device structure in III-V materials. It may be possible to construct an analog of SOI devices in II-IV materials and/or fabricate finFETs in III-V materials using an analog of the processes used for Silicon. However, given the inherent chemical heterogeneity of III-V materials, processes are available to selectively remove materials without affecting others in close proximity. Further, given the atomic precision inherent in their epitaxial growth, III-V materials can be selectively removed and grown with high precision.

DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a flow chart of a process for fabricating an additive-fin field effect transistor

[0013] FIG. 2 is a perspective view of a portion of a substrate.

[0014] FIG. 3 is a perspective view of the portion of the substrate after deposition of a first hard mask.

[0015] FIG. 4 is a perspective view of the portion of the substrate after patterning the first hard mask.

[0016] FIG. 5 is a perspective view of the portion of the substrate after etching a support layer.

[0017] FIG. 6 is a perspective view of the portion of the substrate after growth of a semiconductor fin layer.

[0018] FIG. 7 is a top view and a cross-sectional view of the portion of the substrate after deposition and patterning of a second hard mask.

[0019] FIG. 8 is a top view and a cross-sectional view of the portion of the substrate after deposition of a source/drain contact material.

[0020] FIG. 9 is a top view and cross-sectional views of the portion of the substrate after removal of the first and second hard masks and the support layer.

[0021] FIG. 10 is a top view and cross-sectional views of the portion of the substrate after deposition of a gate dielectric layer and a gate contact layer.

[0022] FIG. 11 is a top view and cross-sectional views of the portion of the substrate after patterning the gate dielectric layer and the gate contact layer.

[0023] FIG. 12 shows a top view and cross-sectional views A-A and B-B of an additive-fin FET.

[0024] Throughout this description, elements appearing in figures are assigned three-digit or four-digit reference designators, where the two least significant digits are specific to the element, and the one or two most significant digit are the figure number where the element is introduced. All elements are described in the discussion of the figure where the element is introduced. An element that is not described in conjunction with a figure may be presumed to have the same characteristics and function as a previously-described element having the same reference designator.

DETAILED DESCRIPTION

[0025] With the previously mentioned MOSFET circuit scaling goals in mind, we disclose a new finFET structure which will be referred to herein as an "additive-fin FET". The additive-fin FET may be fabricated in a III-IV semiconductor material, but is not limited to III-V materials. The manufacturing of the additive-fin FET includes growth of the fin material on a sidewall of a sacrificial support layer using an additive process such as atomic layer epitaxy. The use of an additive process allows the thickness of the fins to be controlled with nanometer or sub-nanometer precision.

[0026] In addition, the additive-fin FET fabrication process involves no dry etching processes which may damage the high quality surface of the grown fins. The surface quality has a direct impact on the finFET performance. After growing the fins, a wet etch is used to etch selectively the support layer and to release the fins. This wet etch maintain the high quality surface of the grown fins.

[0027] Description of Processes

[0028] FIG. 1 is a flow chart of a process 100 to fabricate an additive-fin FET. The process 100 starts at 105 and ends at 195. The flow chart includes major steps in the process 500. Numerous intermediate steps (*i.e.*, depositing, developing, and stripping photoresist layers; cleaning; thermal processing; etc.) performed using conventional semiconductor processes are not shown in FIG. 1.

[0029] The first action in the process 100 is to prepare, at 110, a substrate on which an optional etch-stop layer and a support layer have been deposited. FIG. 2 shows a perspective view of a portion of 1 substrate 200 with the optional etch-stop layer 210 and support layer 220. The portion of the substrate 200 depicted in FIG. 1 and subsequent figures is sufficient to form a single additive-fin FET device. Thus a tiny fraction of a complete semiconductor wafer is shown in each figure. In all figures, the thicknesses of the layers are not drawn to scale. In particular, the actual thickness of the substrate 200 may be much greater than the thickness of the support layer 220 and etch-stop layer 210. For example, the thickness of the substrate 200 may be 500 micrometers to 1 mm, the thickness of the etch-stop layer 210 may be 5 to 100 nanometers, and the thickness of the support layer may be 10 to 500 nanometers. The optional etch-stop layer 210 between the substrate 200 and the support layer 220 may be useful to control the depth of slots that will be subsequently etched into the support layer 220. Alternatively, the etch-stop layer 210 may be omitted, and the depth of the slots etched in the support layer 220 may be controlled by the time of etching.

[0030] In this patent, variants of the term "deposit" (*e.g.* "deposited" and "depositing") refer to any process that adds material to a surface. Additive processes include, for example, sputtering, evaporation, chemical vapor deposition, epitaxial growth processes, and other processes. The etch-stop layer 210 and the support layer 220 may be deposited, for example, by an epitaxial growth process.

[0031] The substrate 200 may be, for example, InP. The etch-stop layer 210 may be InGaAs deposited on the substrate 200, and the support layer 220 may also be InP deposited on the etch-stop layer 210. In this patent, "InGaAs" refers to a semiconductor material having a chemical formula $Ga_xIn_{1-x}As$, where x has a value between 0 and 1. To match the lattice constant of InP and thus minimize strain, $Ga_{0.47}In_{0.53}As$ is typically deposited on InP.

[0032] InGaAs may be chosen as the etch-stop layer 210 since highly selective wet etch chemistries are available that etch InP but not InGaAs. The substrate 200, etch-stop layer 210, and support layer 220 are not limited to InP/InGaAs/InP, but may be any semiconductor materials that allow high quality films to be grown over the underlying materials, and for which a highly selective wet or dry etch process is available. For further example, the substrate 200 and support layer 220 may be Si, and the etch-stop layer 210 may be Si-Ge or a buried dielectric layer (as in an SOI wafer).

[0033] Referring back to FIG. 1, a first hard mask may be deposited on top of the support layer at 115. As shown in FIG. 3, the first hard mask 300 may be a uniform layer covering the surface of the support layer 220. The first hard mask 300 may be a dielectric material, such as SiO_x or SiN, deposited by, for example, sputtering, evaporation, or CVD (chemical vapor deposition). The first hard mask 300 may be a resist material such as HSQ (Hydrogen silsesquioxane) deposited by, for example, spinning.

[0034] Referring back to FIG. 1, the first hard mask may be patterned at 120. In the case of a sputtered or CVD deposited dielectric material, the first hard mask may be patterned by

conventionally depositing and exposing a photoresist and then etching the hard mask material. In the case of HSQ, the HSQ material may be directly patterned by e-beam or extreme UV exposure and developed.

[0035] FIG. 4 illustrates the result of patterning the first hard mask. For ease of illustration, the patterned first hard mask is shown as three parallel strips 300A, 300B, 300C on top of the support layer 220.

[0036] Referring back to FIG. 1, the support layer may be etched at 125. FIG. 5 illustrates the result of etching the support layer 220 through the patterned first hard mask 300A, 300B, 300C. Preferably, the etching may be performed at 125 using a wet etchant that is both material-selective and orientation-selective. In particular, the etching may be performed using a wet etchant that does not etch the etch-stop layer, and etches the support layer preferentially along a particular crystal plane orthogonal to the surface of the support layer 220. Other high-aspect-ratio dry or wet etching methods may be used that result in acceptable quality of the exposed surfaces of the support layer, which is to say the etching method results in surfaces upon which a crystalline epitaxial layer may be grown. The result of etching the support layer 220 is the creation of a series of elongated trenches 522A, 522B having smooth side walls (for example side wall 525) in the support layer 220.

[0037] Referring back to FIG. 1, at 130, a fin layer may be deposited onto the exposed side walls (such as the side wall 525 in FIG. 5) of the elongated trenches (522A, 522B in FIG. 5) formed in the support layer at 125. FIG. 6 illustrates the result of depositing the fin layer 600

onto the exposed surfaces of the support layer and, optionally, on to the exposed surfaces of the etch-stop layer 210. Preferably, the fin layer 600 may be deposited using a slow-growth process, such as atomic layer epitaxy, to provide conformal growth of the fin layer 600 and precise control of the thickness of the fin layer 600. Another additive process may be used to deposit the fin layer 600. The thickness of the deposited fin layer may be, for example, 1 to 50 nanometers.

[0038] The fin layer 600 may be a semiconductor material that is suitable for fabricating FETs and compatible with the underlying support layer 220. In particular, the fin layer 600 may be a material that is not etched by the process used to etch the support layer 220. The fin layer 600 may be, for example, the same material (InGaAs in the previous example) as the etch-stop layer. For further example, the substrate and support layer may be silicon and the fin layer 600 may be a III-V material such as GaN and AlGaN.

[0039] Referring back to FIG. 1, a second hard mask may be formed over the fin material at 135. The second hard mask may be formed by depositing and subsequently patterning a material, such as SiO_x, SiN, HSQ or another material. The second hard mask formed at 135 may be the same material or a different material from the first hard mask deposited at 115. The second hard mask may be deposited and patterned as previously described with respect to the first hard mask.

[0040] FIG. 7 shows a top view and cross-sectional view A-A of the same portion of the substrate 200 as previously shown in FIG. 2 to FIG. 6. In FIG. 7 and subsequent figures, section A-A is a cross-section through the channel (or what will become the channel) of the additive-fin FET. The second hard mask 700 may completely cover the surface of the fin layer 600 in the

areas that will become the channel of the additive-fin FET. The second hard mask 700 may fill the interstitial spaces between the fin layer 600 in the areas that will become the channel of the additive-fin FET. The surfaces (such as surface 705) of the fin layer 600 may be exposed in areas that will become the source and drain contacts of the additive-fin FET.

[0041] Referring back to FIG. 1, a source/drain contact layer may be deposited at 140. The source/drain contact layer may be, for example, the same material as the fin material with the addition of N or P doping. The source/drain contact layer may be deposited, for example, by metalorganic chemical vapor deposition (MOCVD) or metalorganic vapor phase epitaxy (MOVPE). FIG. 8 shows a top view and a cross-sectional view B-B of the same portion of the substrate 200 (as shown previously in FIG. 2 to FIG. 7) after deposition of the source/drain contact layer 800. In FIG. 8 and subsequent figures, section B-B is a cross-section through a drain or source contact (or what will become a drain or source contact) of the additive-fin FET. The source/drain contact layer 800 may completely fill the interstitial spaces between the fins except for the areas already filled by the second hard mask 700. Depending on the process used to deposit the source/drain contact layer 800, the source/drain contact layer may also cover the external surfaces of the second hard mask 700 (not shown).

[0042] Referring again to FIG. 1, the first and second hard masks and the remaining support layer may be removed at 145. The first and second hard masks may be removed using a wet or dry etching process suitable for the material or materials used for the first and second hard masks. The support layer may be removed using the same highly selective wet or dry etch

previously used to create elongated trenches in the support material at 125. FIG. 9 shows a top view and cross-sectional views A-A and B-B of the same portion of the substrate 200 (as shown previously in FIG. 2 to FIG. 8) after removal of the first and second hard masks and the support layer. At this point, the fin layer 600 is no longer supported by the support layer, but is supported by the source/drain contact layer 800 (see section B-B) except in the areas previously covered by the channel mask. In the regions previously covered by the channel mask, fins 900 stand unsupported (see Section A-A). The unsupported fins 900 may be, for example, 10 nanometers thick and extend 200 nanometers out from the substrate 200.

[0043] Referring back to FIG. 1, a gate oxide layer and a gate metal layer may be deposited at 150. The gate oxide layer may be, for example, SiO2 or another suitable dielectric material. The gate metal may be a metal such as aluminum, a conductive ceramic such as TiN (titanium nitride), or some other conductive material. Both the gate oxide layer and the gate metal layer may be deposited using processes, such as atomic layer deposition (ALD), that ensure conformal coating of the underlying structures. FIG. 10 shows a top view and cross-sectional views A-A and B-B of the same portion of the substrate 200 (as shown previously in FIG. 2 to FIG. 9) after deposition of the gate oxide layer 1000 and the gate metal layer 1010. The gate metal layer 1010 may be deposited to fill the interstitial spaces between the fins, as shown in Section A-A.

[0044] Referring back to FIG. 1, the gate electrodes of the additive-fin FET may be defined at 155 by patterning the gate oxide layer and the gate metal layer. For example, the gate metal layer may be selectively etched using a photomask and the gate oxide layer may be subsequently

etched using the gate metal as a hard mask. Conventional wet or dry etch processes may be used for patterning. One or more additional conductor layers and insulator layers may be deposited and patterned at 160 to define gate, source, and drain interconnections. Conventional semiconductor processes may be used for deposition and patterning. The process 100 may then end at 195.

[0045] FIG. 11 shows a top view and cross-sectional views A-A and B-B of the same portion of the substrate 200 (as shown previously in FIG. 2 to FIG. 10) after patterning the gate oxide layer 1000 and the gate metal layer 1010. In the channel region of the additive-fin FET (see Section A-A), the gate oxide layer 1000 and gate metal layer 1010 cover both sides of each fin 900, thus providing excellent gate control of the channel.

[0046] Description of Apparatus

[0047] FIG. 12 shows a top view and cross-sectional views A-A and B-B of an additive-fin FET fabricated by the process 100 of FIG. 1. The additive-fin FET includes five fins 900 that extend essentially orthogonal to the substrate 200. An additive-fin FET may include more or fewer that five fins, with the number of fins selected to provide a desired total channel cross-sectional area. A channel region of each fin (Section A-A) is covered on both sides by a gate oxide layer 1000 and a gate metal layer 1010. Outside of the channel regions (Section B-B), a source/drain contact layer 800 provides an electrical contact to, and mechanical support for, at least one side of each fin 900. Interconnections between the source, drain, and gate contacts of the additive-fin FET may be made by one or more additional conductor layers 1200.

[0048] Closing Comments

[0049] Throughout this description, the embodiments and examples shown should be considered as exemplars, rather than limitations on the apparatus and procedures disclosed or claimed. Although many of the examples presented herein involve specific combinations of method acts or system elements, it should be understood that those acts and those elements may be combined in other ways to accomplish the same objectives. With regard to flowcharts, additional and fewer steps may be taken, and the steps as shown may be combined or further refined to achieve the methods described herein. Acts, elements and features discussed only in connection with one embodiment are not intended to be excluded from a similar role in other embodiments.

[0050] As used herein, "plurality" means two or more. As used herein, a "set" of items may include one or more of such items. As used herein, whether in the written description or the claims, the terms "comprising", "including", "carrying", "having", "containing", "involving", and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of", respectively, are closed or semi-closed transitional phrases with respect to claims. Use of ordinal terms such as "first", "second", "third", etc., in the claims to modify a claim element does not by itself connote any priority, precedence, or order of one claim element over another or the temporal order in which acts of a method are performed, but are used merely as labels to distinguish one claim element having a certain name from another element having a same name (but for use of the

ordinal term) to distinguish the claim elements. As used herein, "and/or" means that the listed items are alternatives, but the alternatives also include any combination of the listed items.

CLAIMS

It is claimed:

1. A process, comprising:

forming an elongate trench having opposed side walls in a sacrificial support layer on a substrate;

depositing a semiconductor layer on at least one side wall of the trench;

removing the support layer leaving the semiconductor layer as a fin extending from the substrate;

creating a field effect transistor in the semiconductor layer.

2. The process of claim 1, wherein the semiconductor layer is deposited on at least one side wall of the trench using by atomic layer epitaxy.

3. The process of claim 1, wherein forming an elongate trench further comprises:

depositing the support layer on the substrate;

depositing and patterning a first hard mask; and

etching the support layer using a material-selective and orientation-selective wet etch.

4. The process of claim 3, further comprising:

depositing an etch-stop layer on the substrate before depositing the support layer.

5. The process of claim 4, wherein a depth of the elongate trench extends from a surface of the support layer to the etch-stop layer.

6. The process of claim 4, wherein the semiconductor layer is the same material as the etch-stop layer.

7. The process of claim 6, wherein

the substrate and the support layer are InP, and

the etch-stop layer and the semiconductor layer are InGaAs.

8. The process of claim 1, further comprising, after depositing the semiconductor layer and before removing the support layer:

depositing a second hard mask over portions of the semiconductor layer to be a channel of the field effect transistor; and

at least partially filling portion of the elongate trench not covered by the second hard mask with doped source/drain contact material,

wherein the deposited doped source/drain contact material is configured to provide mechanical support to the semiconductor layer after the support layer is removed.

9. The process of claim 8, further comprising, after depositing the source/drain contact material:

removing the second hard mask and remaining support layer;

forming a gate dielectric layer and a gate metal layer over the portions of the semiconductor layer to be the channel of the field effect transistor.

10. A device, comprising:

a field effect transistor formed in a fin extending from a substrate, the fin formed by a process comprising:

depositing a semiconductor layer onto a side wall of a trench formed in a sacrificial support layer on the substrate, and

subsequently removing the support layer.

11. The device of claim 12, the process further comprising:

depositing the support layer on the substrate;

depositing and patterning a first hard mask; and

etching the support layer using a material-selective and orientation-selective wet etch to form the trench.

12. The device of claim 13, the process further comprising:

depositing an etch-stop layer on the substrate before depositing the support layer.

13. The device of claim 13, wherein a depth of the trench extends from a surface of the support layer to the etch-stop layer.

14. The device of claim 11, the process further comprising, after depositing the semiconductor layer and before removing the support layer:

depositing a second hard mask over portions of the semiconductor layer to be a channel of the field effect transistor; and

at least partially filling portions of the trench not covered by the second hard mask with doped source/drain contact material,

wherein the deposited doped source/drain contact material is configured to provide mechanical support to the semiconductor layer after the support layer is removed.

15. The device of claim 12, wherein

the substrate and the support layer are InP, and

the semiconductor layer is InGaAs.

16. A field effect transistor, comprising:

a semiconductor fin extending from a substrate, the fin having two opposing surfaces, the fin divided into a channel region disposed between a source contact region and a drain contact region;

a gate dielectric layer deposited on both surfaces of the fin in the channel region;

a gate metal layer deposited over the gate dielectric layer; and

doped source/drain contact material disposed to provide electrical contact and mechanical support to at least one surface of the fin in the source contact region and the drain contact region.

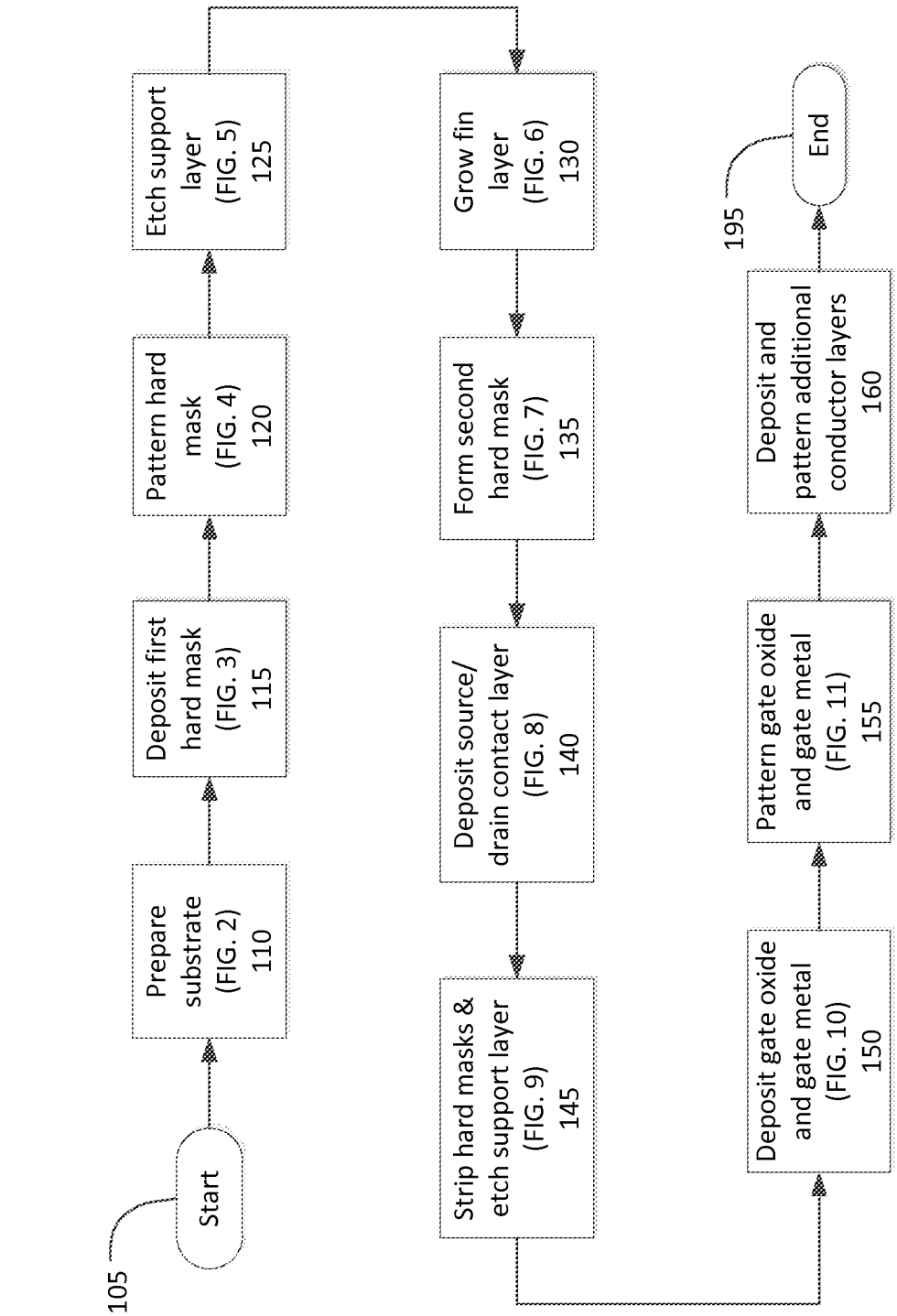

100
105
Start
Prepare substrate (FIG. 2) 110
Deposit first hard mask (FIG. 3) 115
Pattern hard mask (FIG. 4) 120
Etch support layer (FIG. 5) 125
Grow fin layer (FIG. 6) 130
Form second hard mask (FIG. 7) 135
Deposit source/ drain contact layer (FIG. 8) 140
Strip hard masks & etch support layer (FIG. 9) 145
Deposit gate oxide and gate metal (FIG. 10) 150
Pattern gate oxide and gate metal (FIG. 11) 155
Deposit and pattern additional conductor layers 160
195
End

FIG. 1

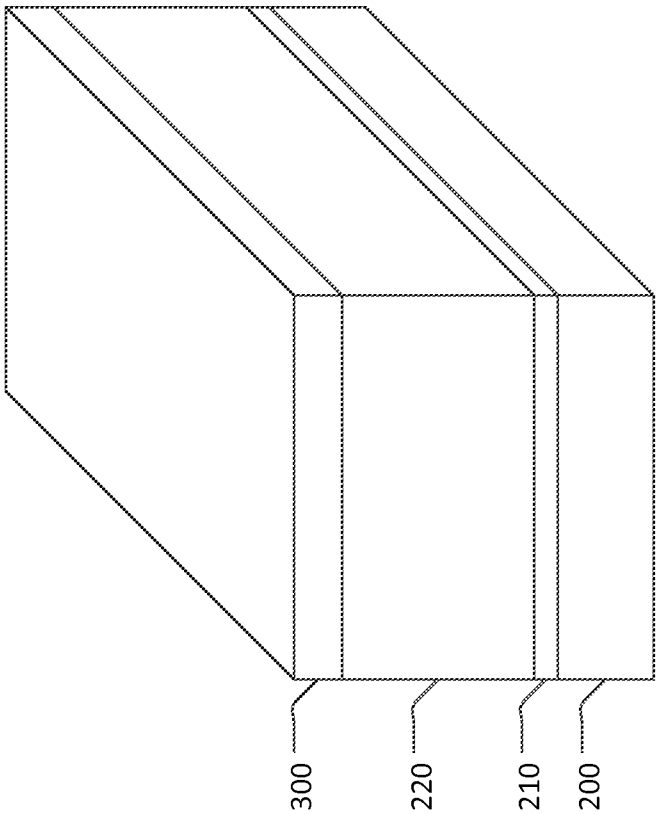


FIG. 3

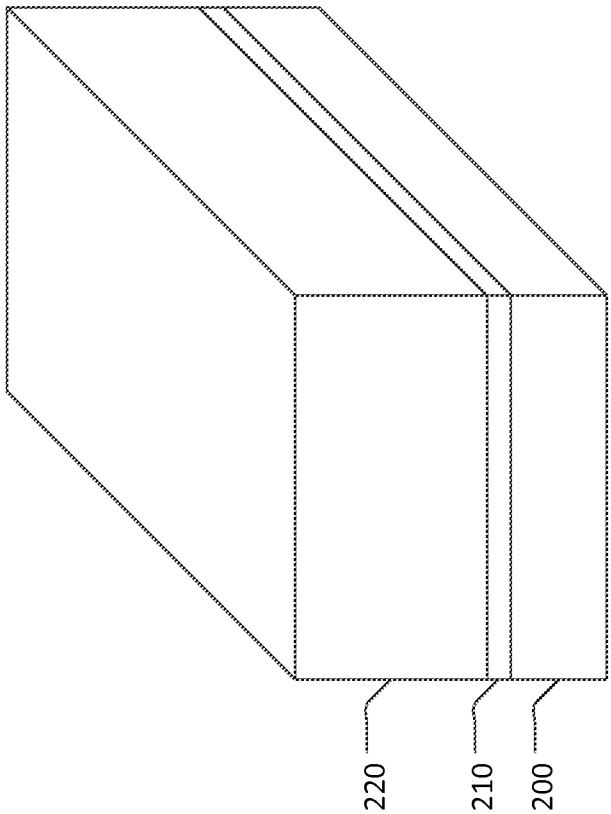


FIG. 2

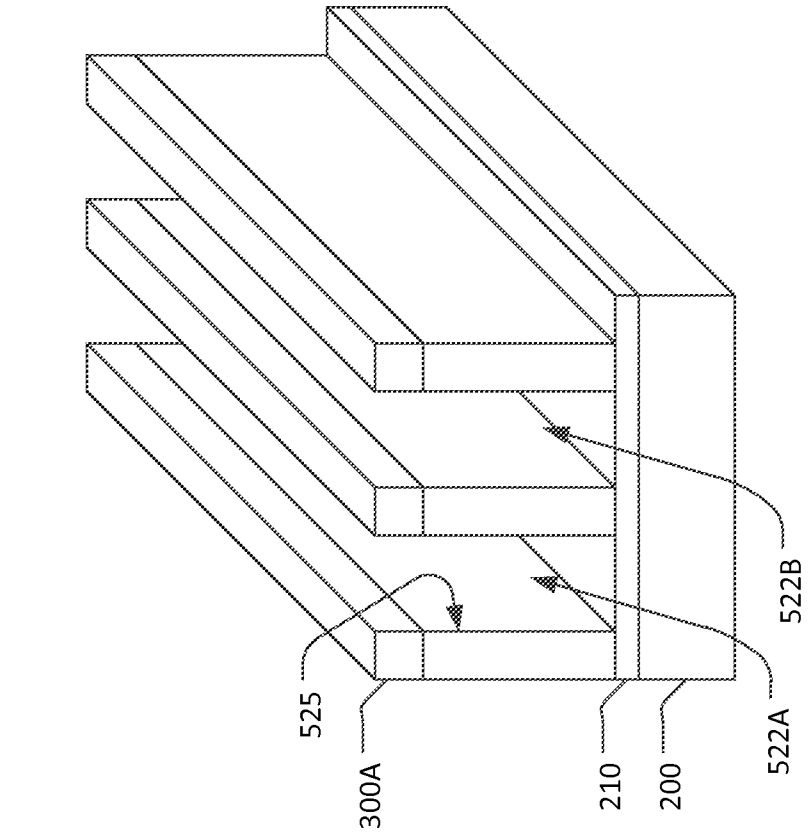


FIG. 5

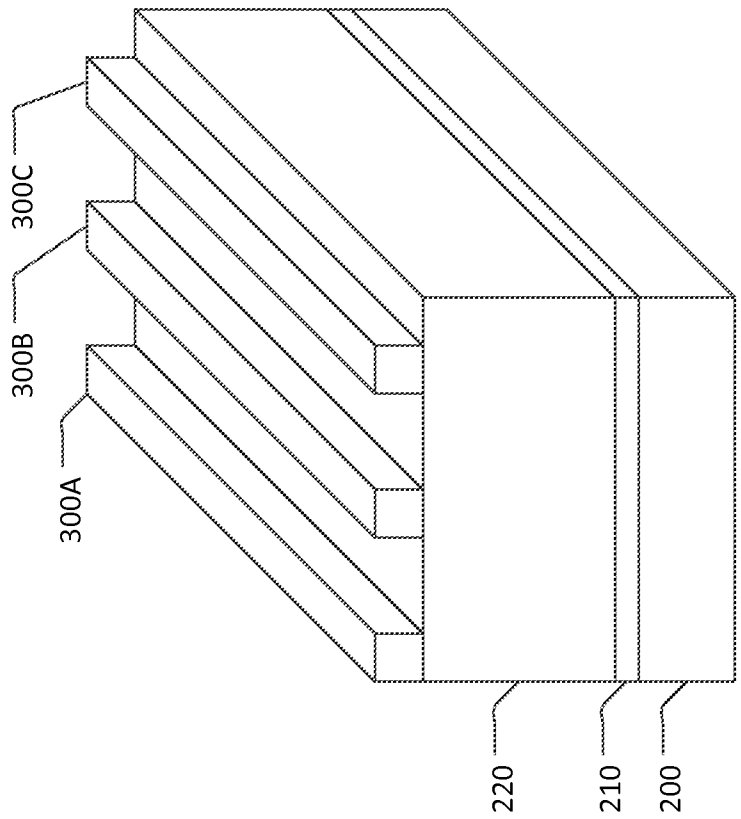


FIG. 4

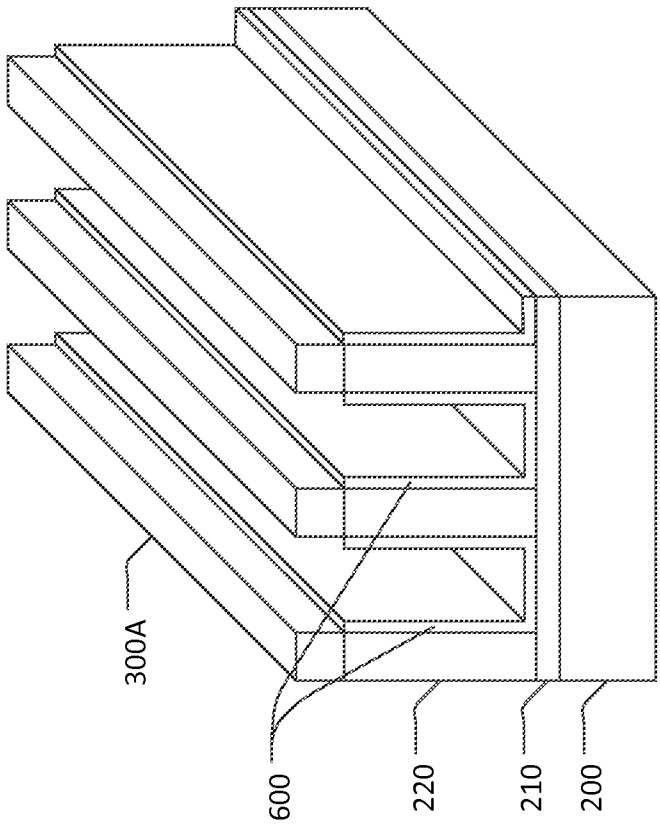
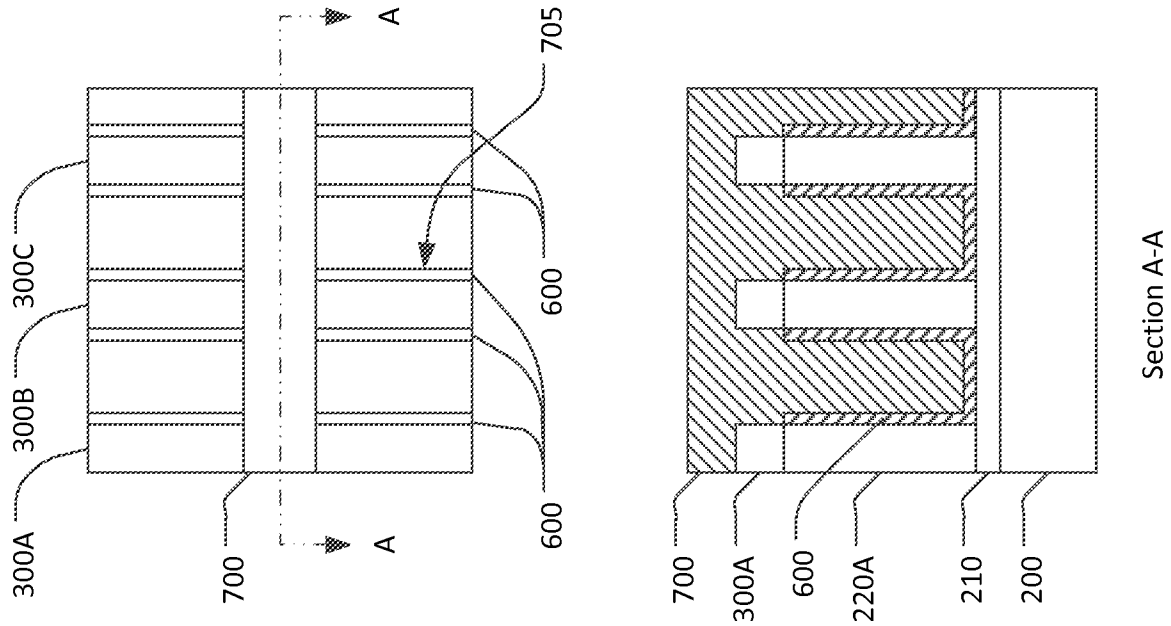


FIG. 6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Section A-A

FIG. 7

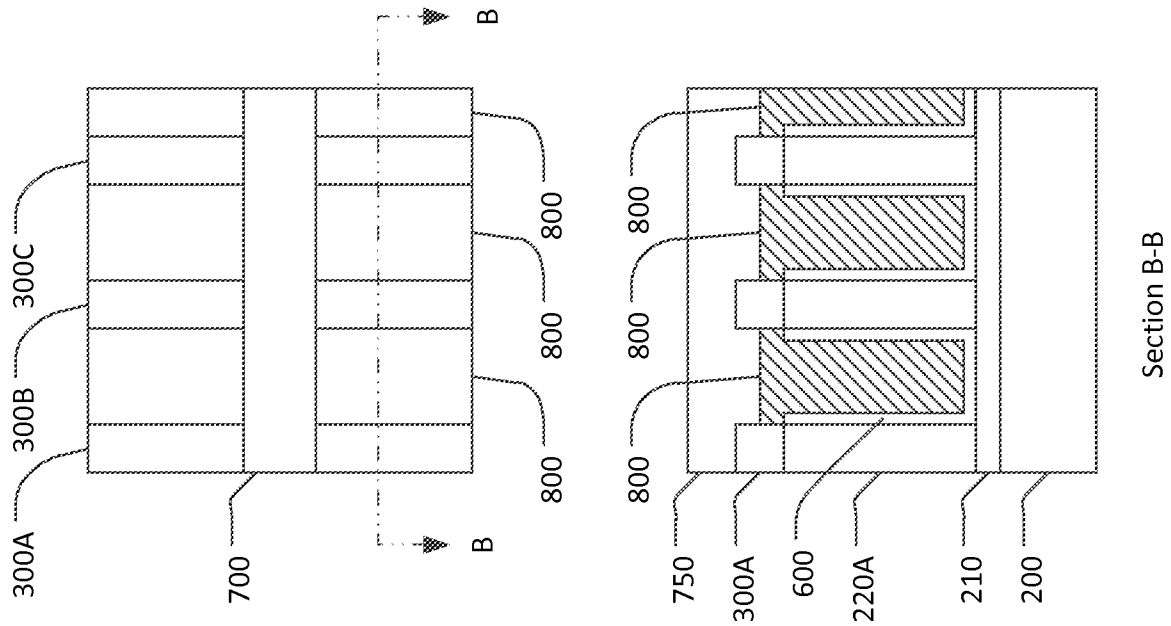
300A
300B
300C
700
800
800
800
800
B
B
750
300A
600
220A
210
200
800
800
800
800
Section B-B

FIG. 8

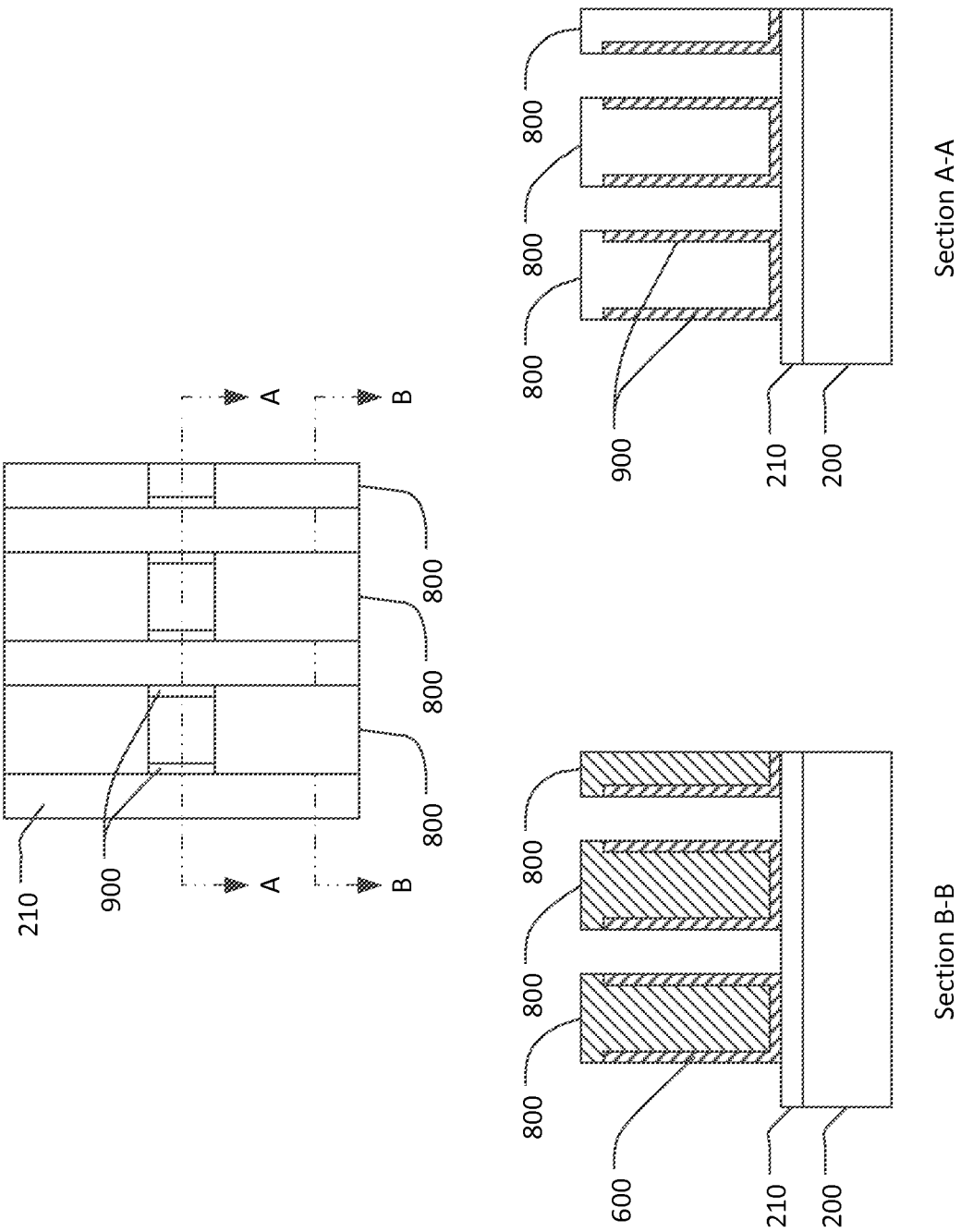
A
B
800
800
800
210
900
A
B
800
800
800
900
210
200
Section A-A
800
800
800
600
210
200
Section B-B

FIG. 9

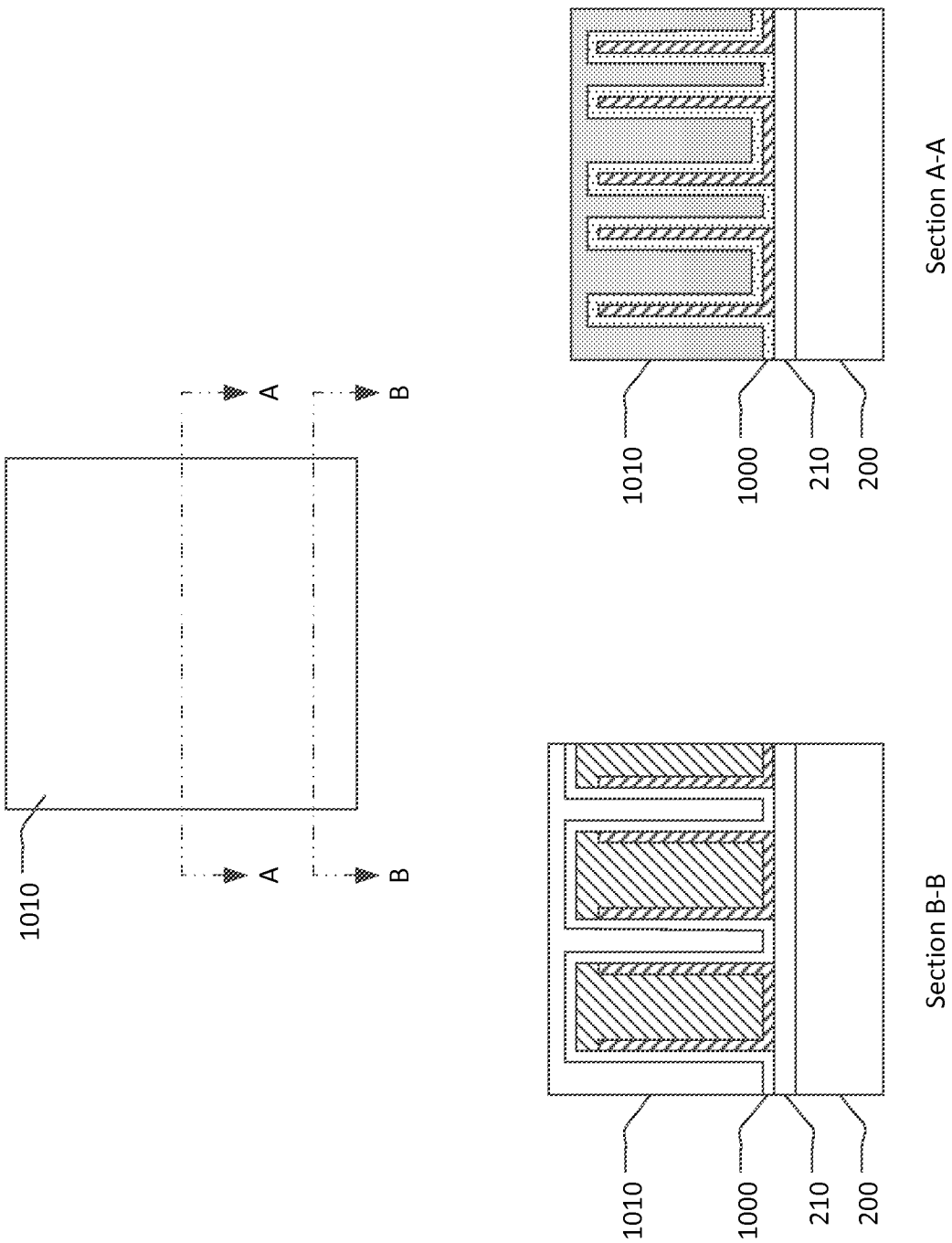
A
B
A
B
1010
Section A-A
1010
1000
210
200
Section B-B
1010
1000
210
200

FIG. 10

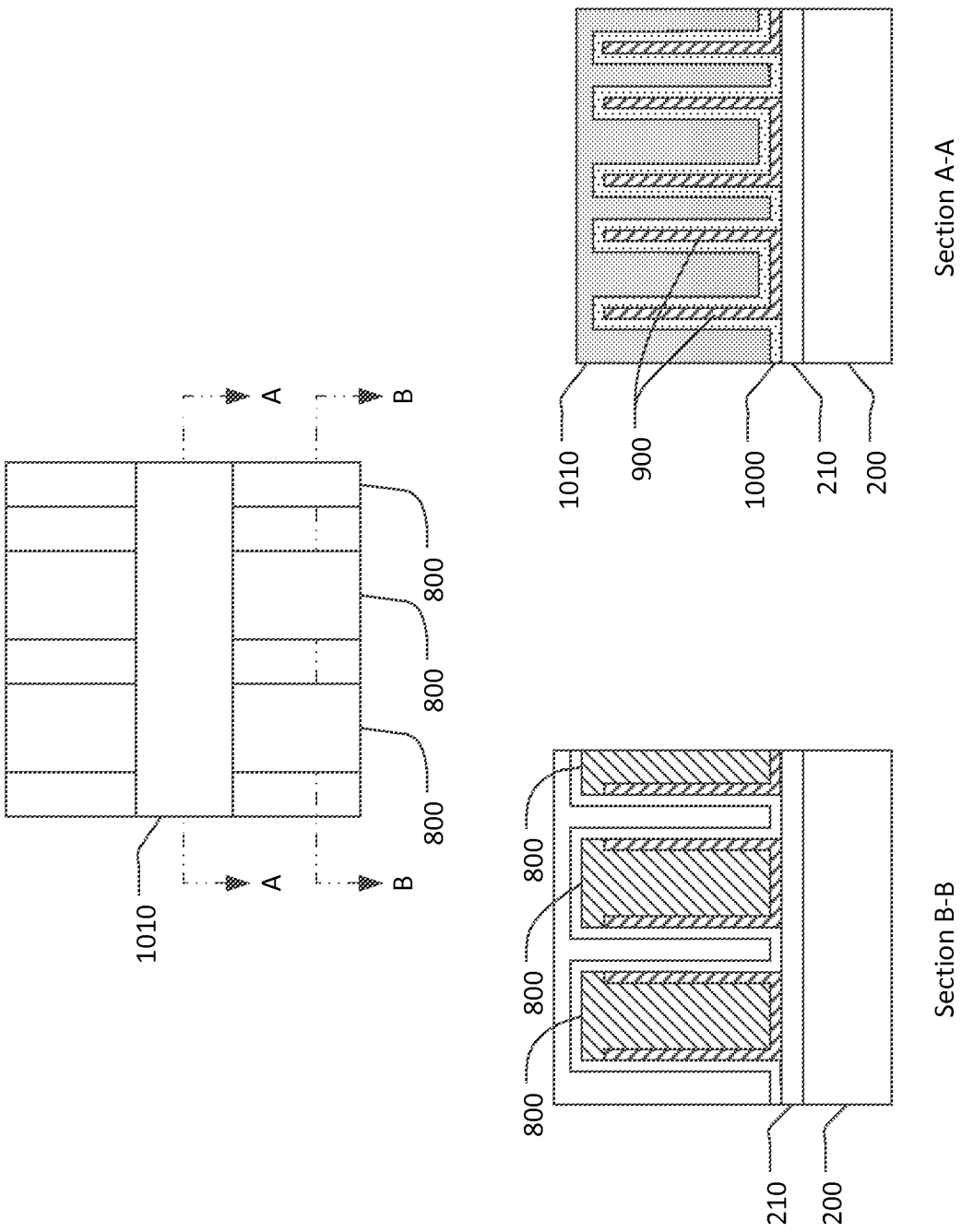
A
B
1010
800
800
800
A
B
Section A-A
1010
900
1000
210
200
Section B-B
800
800
800
210
200

FIG. 11

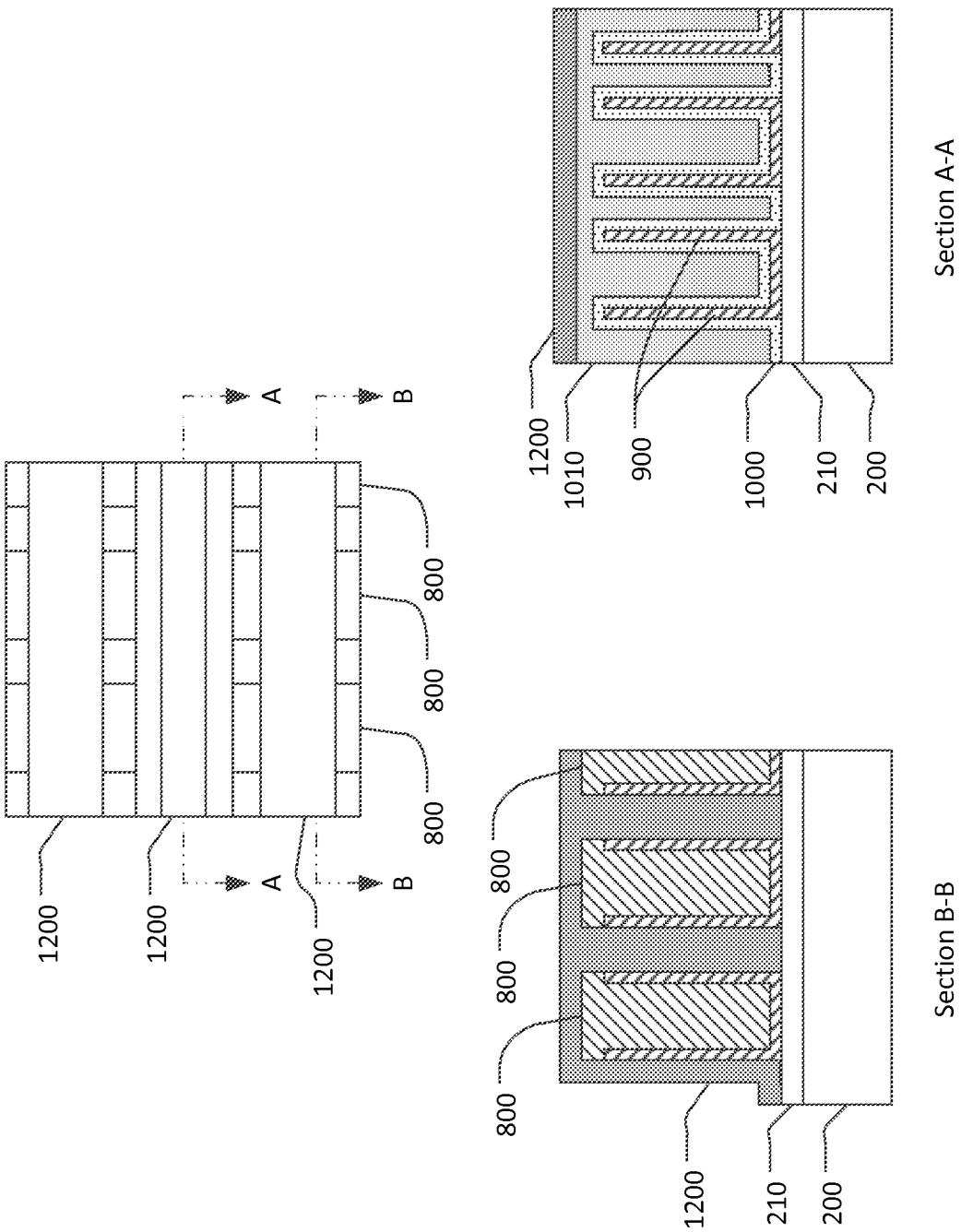
A
B
800
800
800
1200
1200
1200
A
B
1200
1010
900
1000
210
200
Section A-A
800
800
800
1200
210
200
Section B-B

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US14/41403

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/772, 29/20, 21/18 (2014.01)
CPC - H01L 29/7783, 29/41791, 29/41783
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 29/772, 29/20, 21/18 (2014.01)
CPC - H01L 29/7783, 29/41791, 29/41783; USPC - 257/213, E21.409, E29.249; 438/156, 268, 269, 300

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; ProQuest; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used:transistor, FET, field effect transistor, FinFET, chhanel, vertical channel, vertical FinFET, gate oxide, gate electrode, source, doped source, drain, doped drain, InP, Indium phosphide, InGaAs, etch stop.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------ Y	US 2011/0012085 A1 (DELIGIANNI H et al.) January 20, 2011, Figures 3B-3D; paragraphs [0061]-[0063].	1, 10-13, 16 ---------- 2-9, 14-15
Y	US 2010/0038679 A1 (CHAN K et al.) February 18, 2010, paragraph [0045].	2-7
Y	US 2003/0197193 A1 (PIERSON JR, R et al.) October 23, 2003, Abstract; Figure 1; paragraphs [0016], [0017].	6-7, 15
Y	US 2005/0124099 A1 (BEINTNER J et al.) June 09, 2005, Figures 8C, 9C; paragraphs [0045]-[0049].	8-9, 14

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2014 (31.08.2014)	09 OCT 2014

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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