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GB 1520452
GB 1403059
GB 1368929
GB 1016444
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(54) **Improvements in or relating to display processors**

(57) In order to enable an image of a scene, comprising one or more regions each enclosed by a respective set of planes defined by a boolean expression relating the planes of the set one to another, to be generated on a raster scan display, a processor is used to produce, from the boolean description of the scene, an electrical signal capable of generating that image. The processor is adapted to determine what is to be shown in each part of the display from depth values indicative of the distance of each plane from the display screen, first and second increment values respectively indicative of depth value changes between two raster points in two mutually non-parallel directions, and property codes indicative of whether each plane is a front surface or a back surface of the image and of the positions of the planes in the boolean expression of the set of planes including that plane. The processor may be used to generate a projection of a three-dimensional image on the screen, or alternatively it may be used to generate a cross-section through such an image.

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

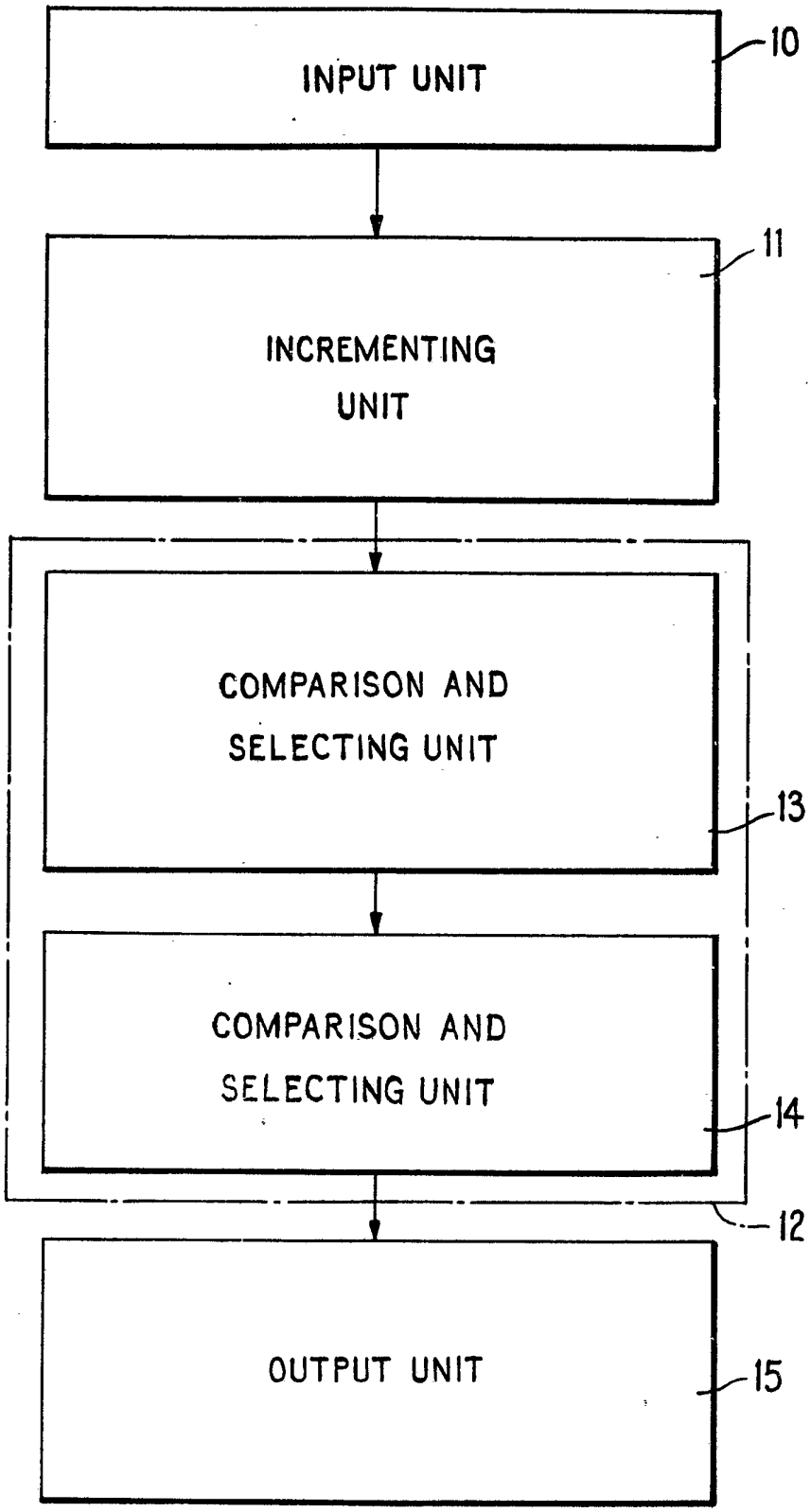
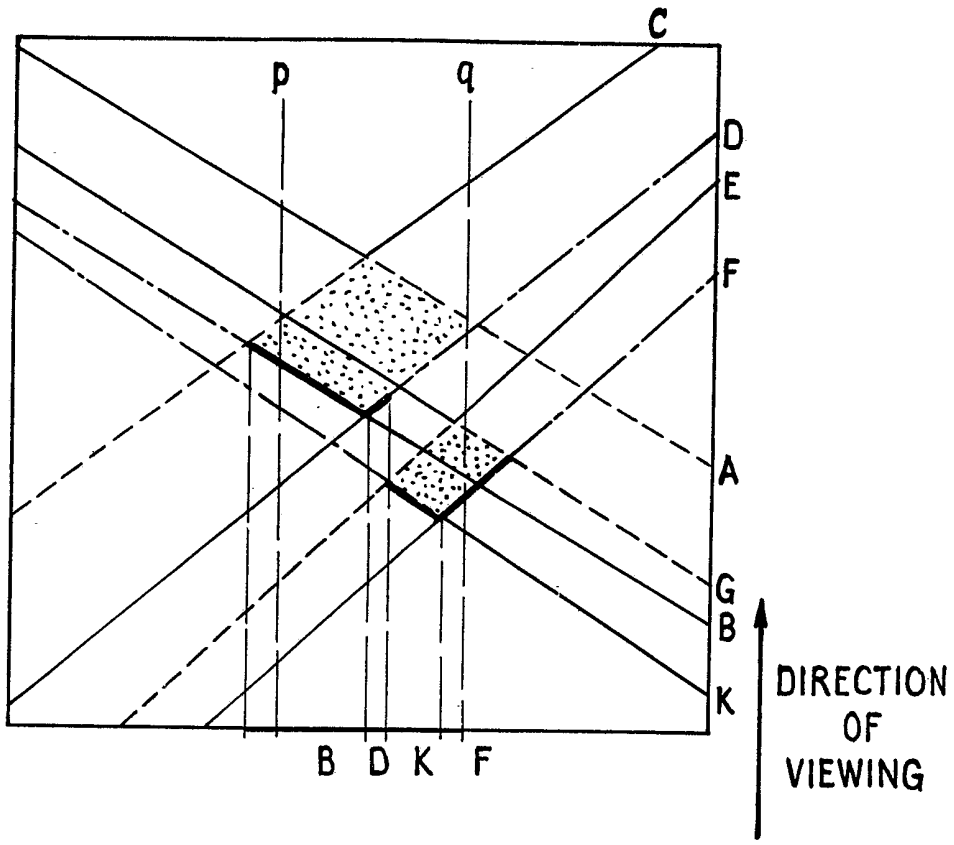

INPUT UNIT
10
INCREMENTING UNIT
11
COMPARISON AND SELECTING UNIT
13
COMPARISON AND SELECTING UNIT
14
12
OUTPUT UNIT
15

Fig. 1

2043972



SCENE = A. B. C. D + E. F. G. K.

MINIMUM OF BACK PLANES ---------

MAXIMUM OF FRONT PLANES ——-——-——

VISIBLE FRONT SURFACES ————————

MINIMUM OF VISIBLE SURFACES ————

Fig. 2

Fig. 3

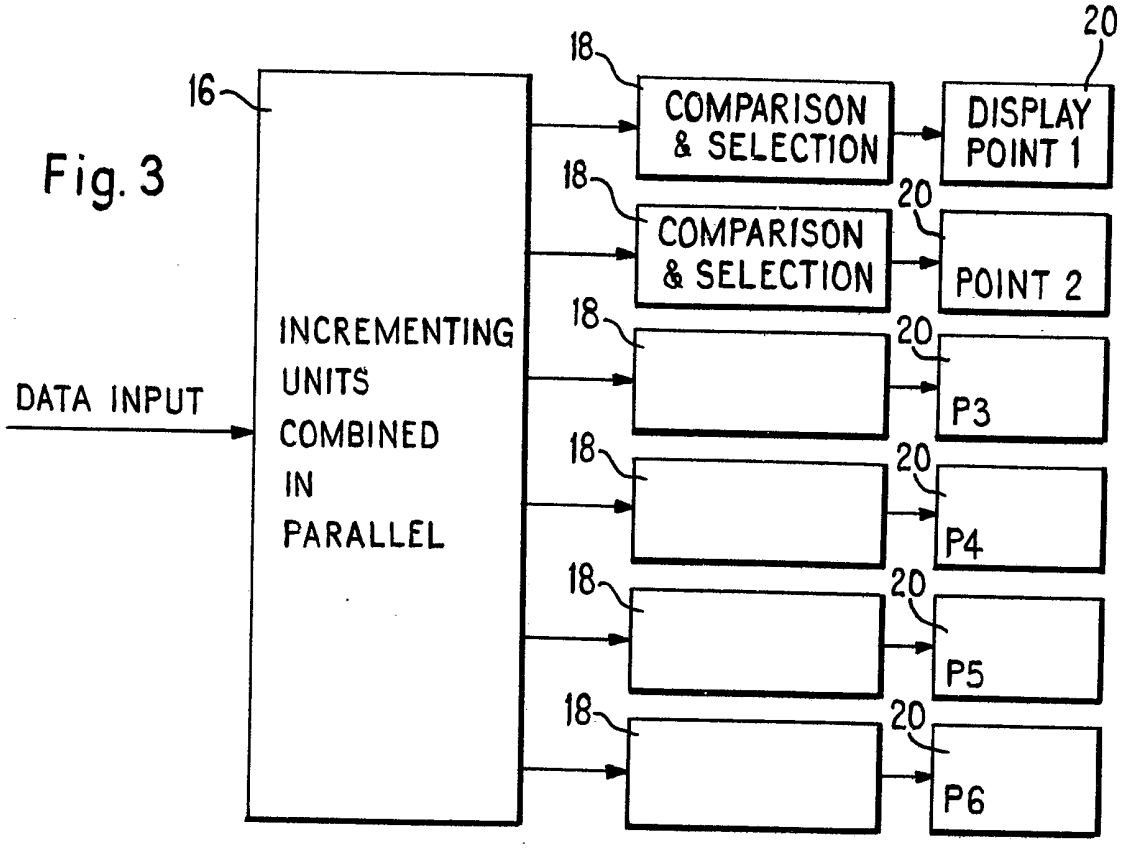

16
INCREMENTING UNITS COMBINED IN PARALLEL
DATA INPUT
18
COMPARISON & SELECTION
18
COMPARISON & SELECTION
18
18
18
18
20
DISPLAY POINT 1
20
POINT 2
20
P3
20
P4
20
P5
20
P6

Fig. 4

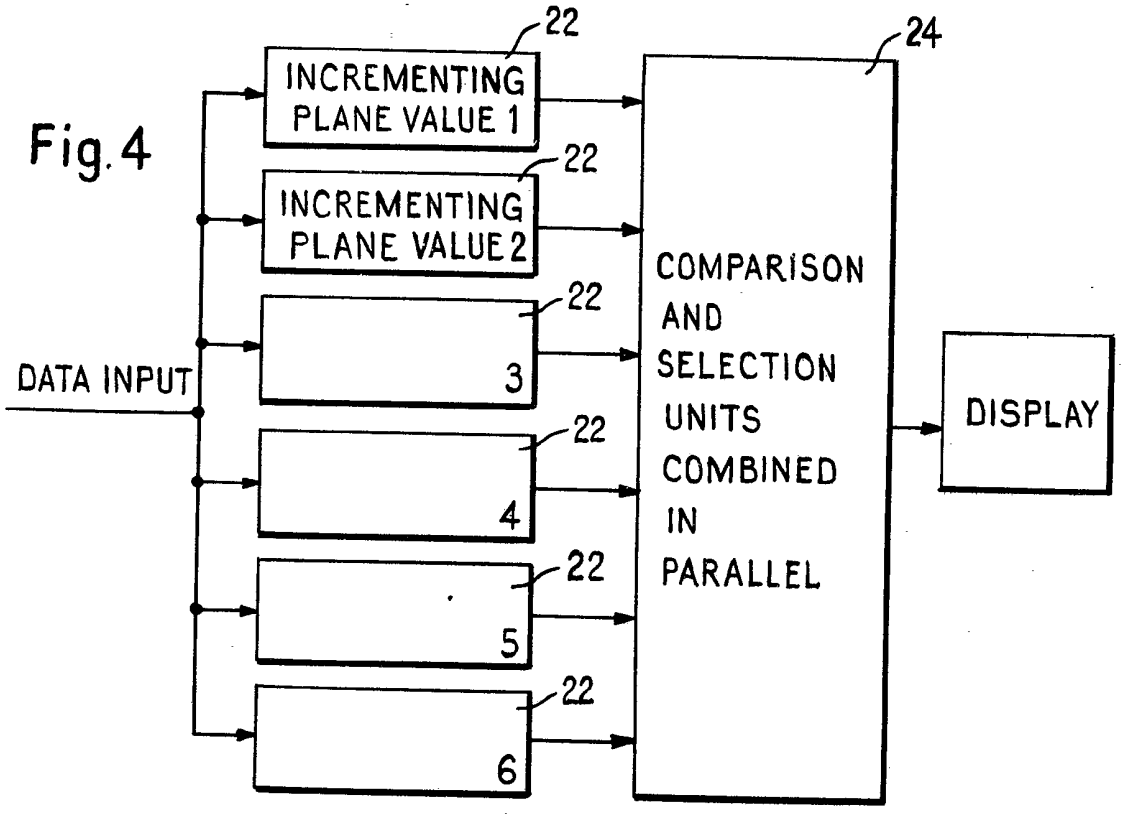

22
INCREMENTING PLANE VALUE 1
22
INCREMENTING PLANE VALUE 2
22
3
22
4
22
5
22
6
DATA INPUT
24
COMPARISON AND SELECTION UNITS COMBINED IN PARALLEL
DISPLAY

Fig. 5

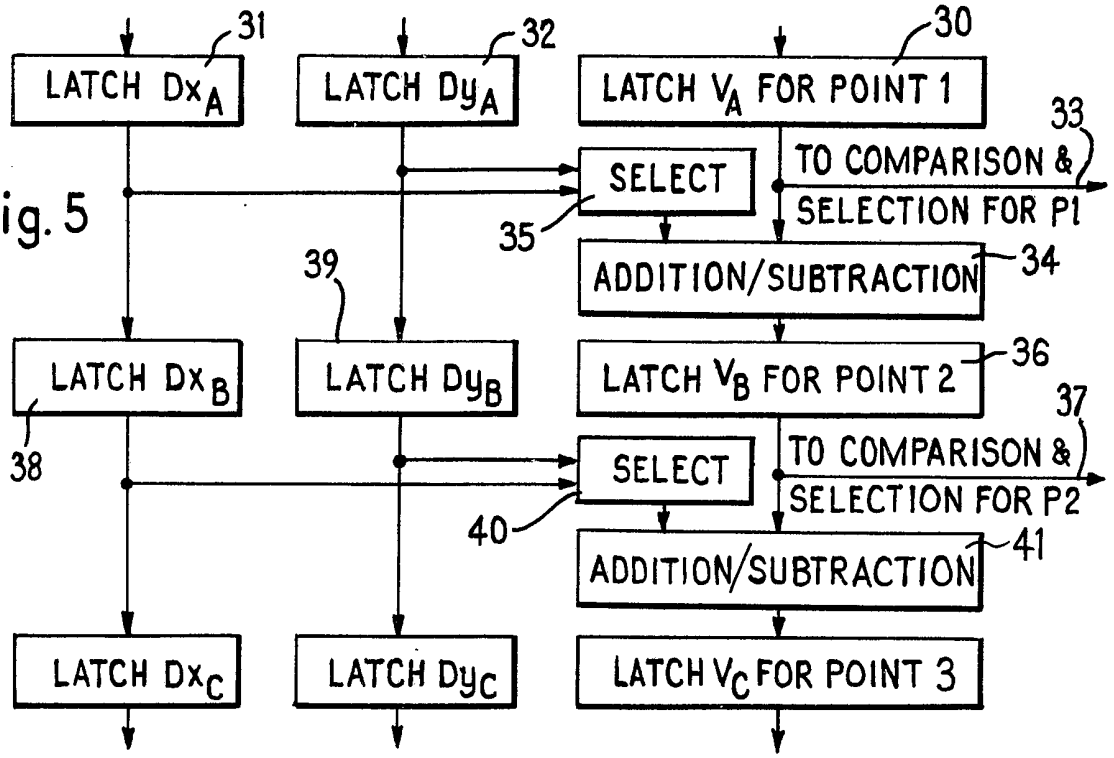
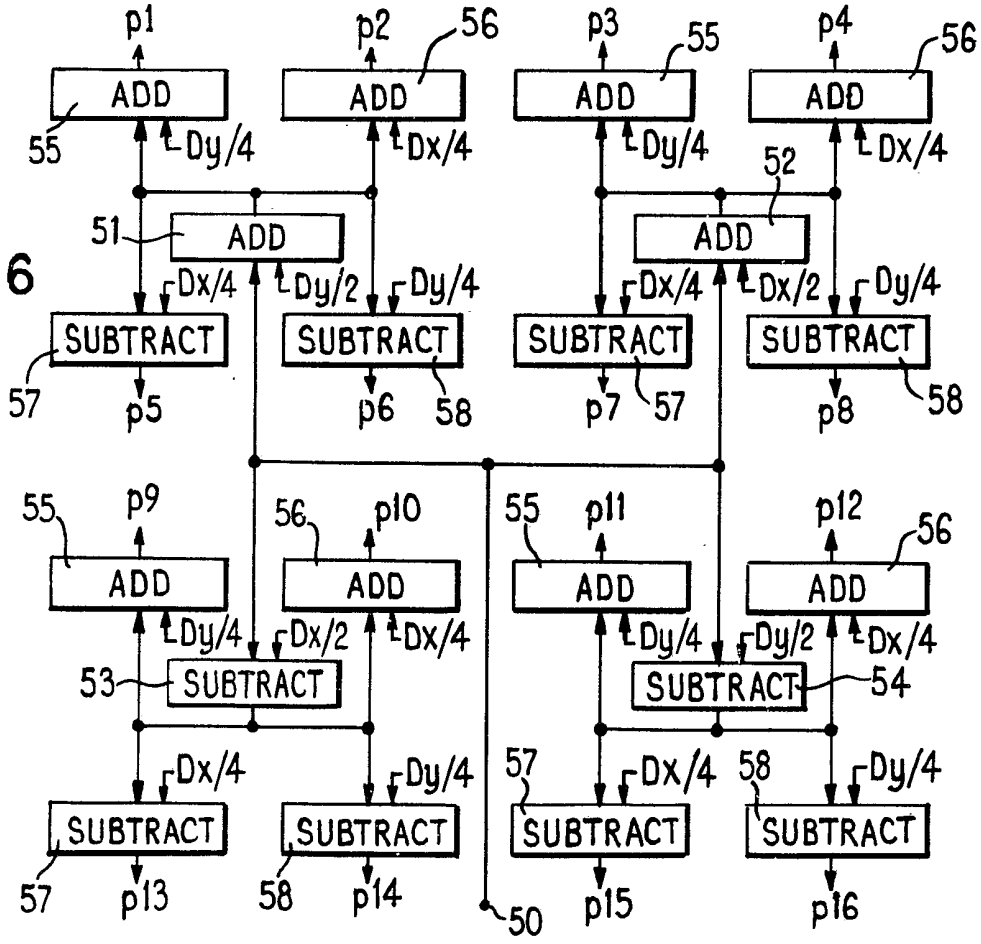

LATCH Dx$_A$
LATCH Dy$_A$
LATCH V$_A$ FOR POINT 1
31
32
30
33
SELECT
TO COMPARISON & SELECTION FOR P1
35
ADDITION/SUBTRACTION
34
39
LATCH Dx$_B$
LATCH Dy$_B$
LATCH V$_B$ FOR POINT 2
36
38
37
SELECT
TO COMPARISON & SELECTION FOR P2
40
ADDITION/SUBTRACTION
41
LATCH Dx$_C$
LATCH Dy$_C$
LATCH V$_C$ FOR POINT 3

Fig. 6


p1
p2
56
p3
55
p4
56
ADD
55
Dy/4
Dx/4
Dy/4
Dx/4
52
51
ADD
ADD
Dx/4
Dy/2
Dy/4
Dx/4
Dx/2
Dy/4
SUBTRACT
SUBTRACT
SUBTRACT
SUBTRACT
57
p5
p6
58
p7
57
p8
58
55
p9
56
p10
55
p11
p12
56
ADD
ADD
ADD
ADD
Dy/4
Dx/2
Dx/4
Dy/4
Dy/2
Dx/4
53
SUBTRACT
SUBTRACT
54
Dx/4
Dy/4
57
Dx/4
58
Dy/4
SUBTRACT
SUBTRACT
SUBTRACT
SUBTRACT
57
p13
58
p14
50
p15
p16

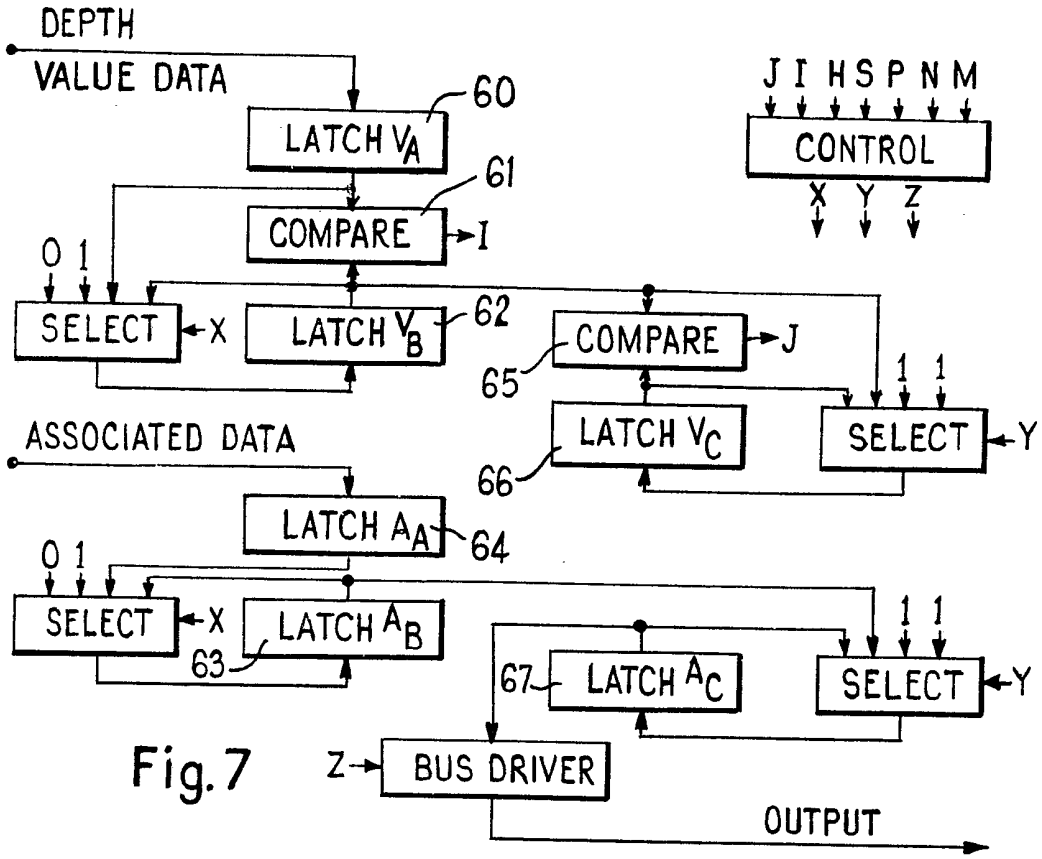

DEPTH
VALUE DATA
60
LATCH V_A
61
COMPARE
I
J I H S P N M
CONTROL
X Y Z
0 1
SELECT
X
LATCH V_B
62
COMPARE
J
65
1 1
LATCH V_C
66
SELECT
Y
ASSOCIATED DATA
LATCH A_A
64
0 1
SELECT
X
LATCH A_B
63
1 1
67
LATCH A_C
SELECT
Y
Z
BUS DRIVER
OUTPUT

Fig. 7

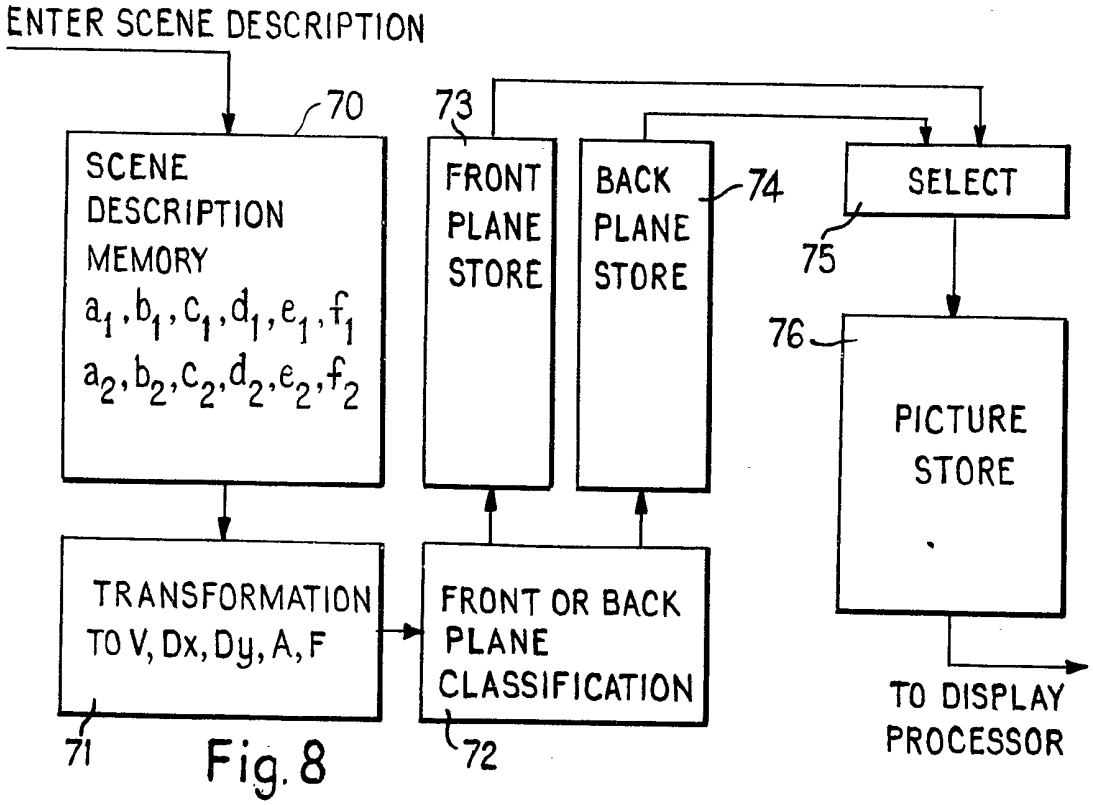

ENTER SCENE DESCRIPTION
70
SCENE DESCRIPTION MEMORY
$a_1, b_1, c_1, d_1, e_1, f_1$
$a_2, b_2, c_2, d_2, e_2, f_2$
73
FRONT PLANE STORE
BACK PLANE STORE
74
SELECT
75
76
PICTURE STORE
TRANSFORMATION TO V, Dx, Dy, A, F
71
FRONT OR BACK PLANE CLASSIFICATION
72
TO DISPLAY PROCESSOR

Fig. 8

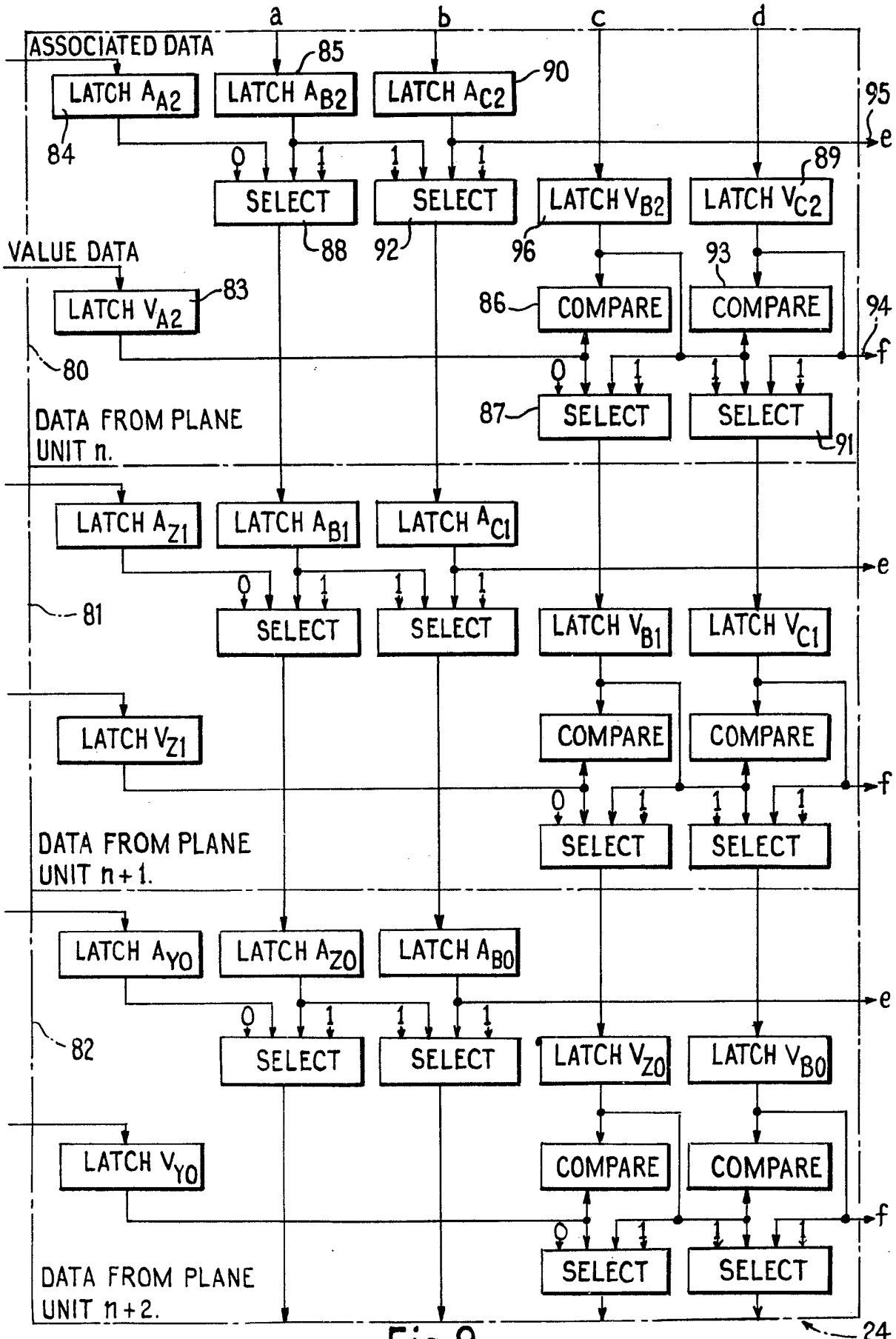

a
b
c
d
ASSOCIATED DATA
LATCH A_{A2}
LATCH A_{B2}
LATCH A_{C2}
85
90
95
e
84
SELECT
SELECT
LATCH V_{B2}
LATCH V_{C2}
89
88
92
96
VALUE DATA
LATCH V_{A2}
83
86
COMPARE
COMPARE
93
94
f
80
87
SELECT
SELECT
91
DATA FROM PLANE UNIT n.
LATCH A_{Z1}
LATCH A_{B1}
LATCH A_{C1}
81
SELECT
SELECT
LATCH V_{B1}
LATCH V_{C1}
LATCH V_{Z1}
COMPARE
COMPARE
DATA FROM PLANE UNIT n+1.
LATCH A_{Y0}
LATCH A_{Z0}
LATCH A_{B0}
82
SELECT
SELECT
LATCH V_{Z0}
LATCH V_{B0}
LATCH V_{Y0}
COMPARE
COMPARE
DATA FROM PLANE UNIT n+2.
SELECT
SELECT
24

Fig.9

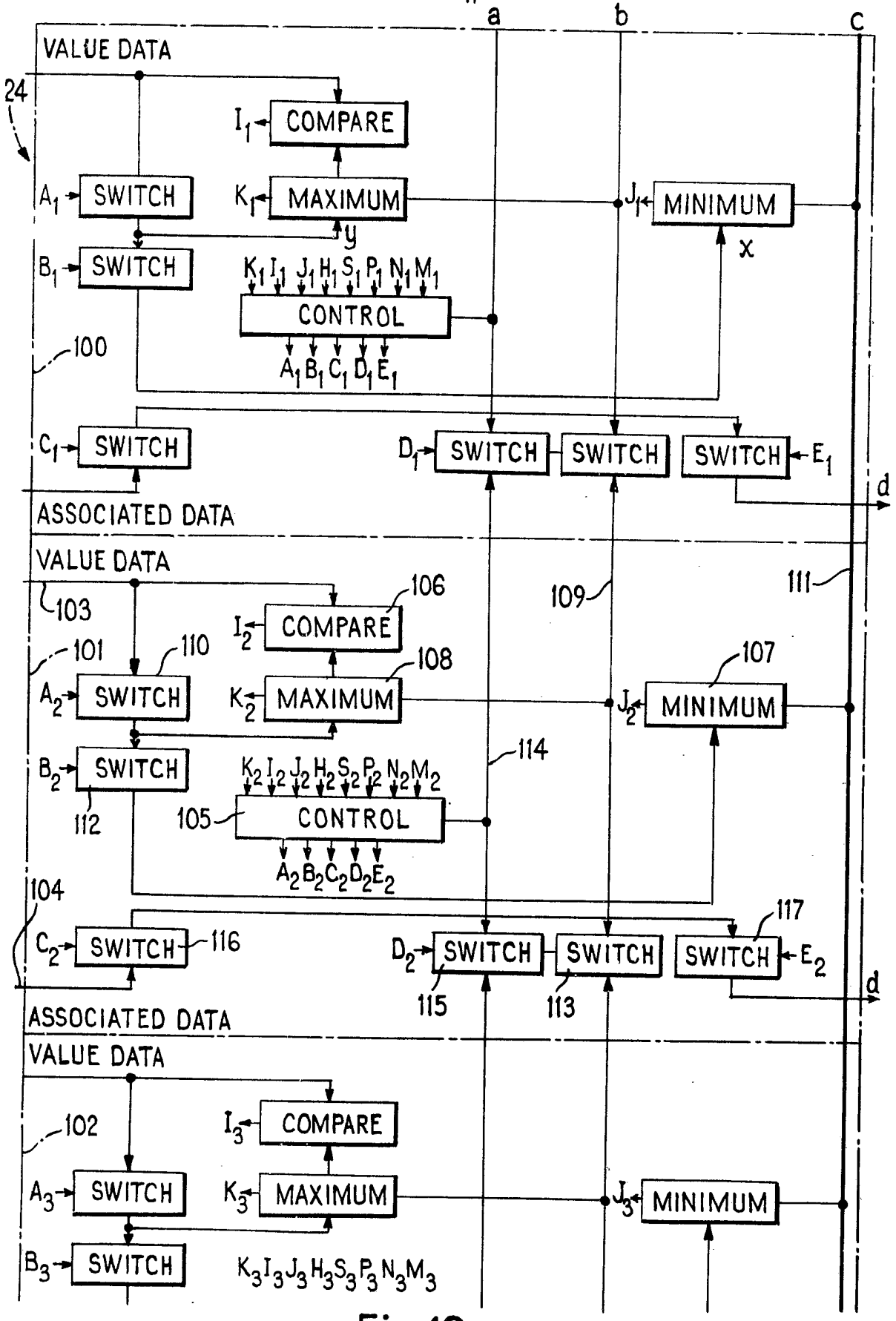

a
b
c
VALUE DATA
24
I1 COMPARE
A1 SWITCH
K1 MAXIMUM
J1 MINIMUM
y
x
B1 SWITCH
K1 I1 J1 H1 S1 P1 N1 M1
CONTROL
A1 B1 C1 D1 E1
100
C1 SWITCH
D1 SWITCH
SWITCH
SWITCH
E1
d
ASSOCIATED DATA
VALUE DATA
103
106
I2 COMPARE
109
111
101
110
108
107
A2 SWITCH
K2 MAXIMUM
J2 MINIMUM
B2 SWITCH
K2 I2 J2 H2 S2 P2 N2 M2
114
112
105
CONTROL
A2 B2 C2 D2 E2
104
117
C2 SWITCH
116
D2 SWITCH
SWITCH
SWITCH
E2
d
115
113
ASSOCIATED DATA
VALUE DATA
102
I3 COMPARE
A3 SWITCH
K3 MAXIMUM
J3 MINIMUM
B3 SWITCH
K3 I3 J3 H3 S3 P3 N3 M3

Fig. 10

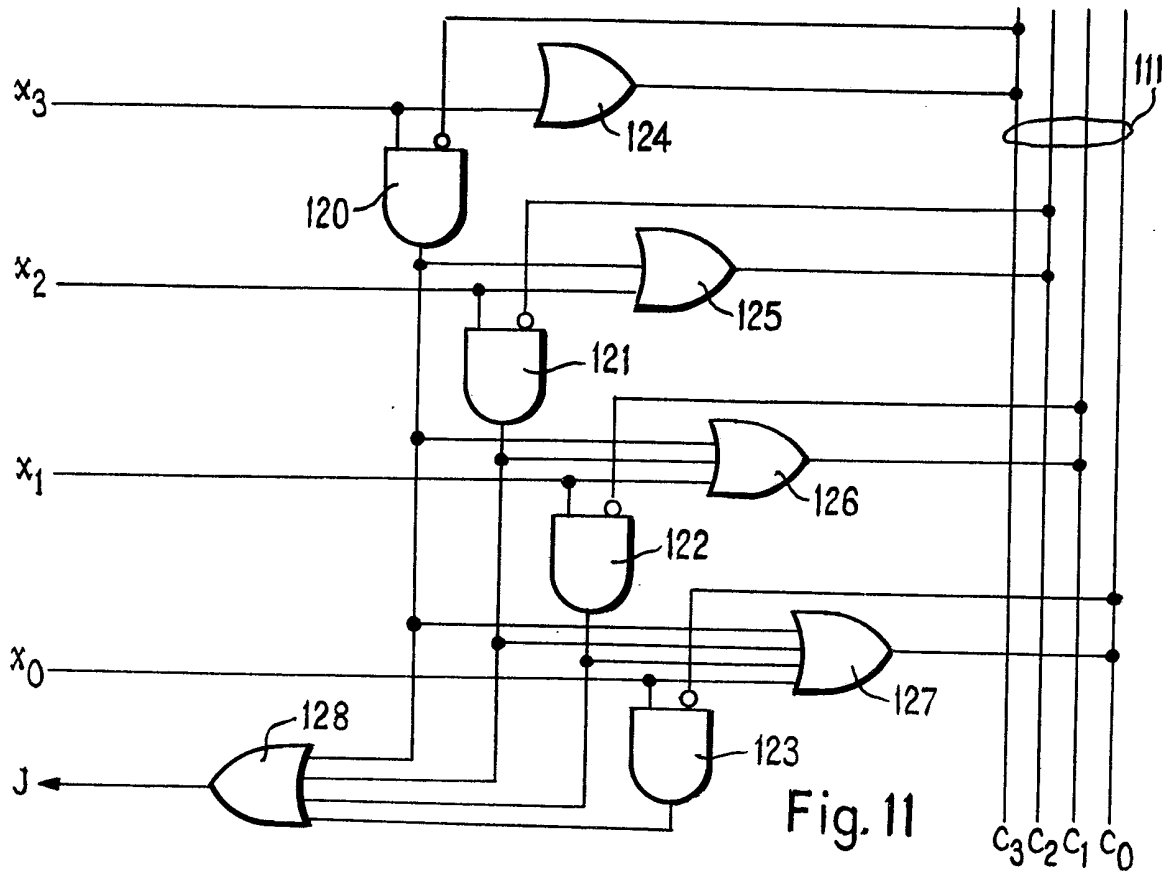

x3
x2
x1
x0
J
120
121
122
123
124
125
126
127
128
111
c3 c2 c1 c0

Fig. 11

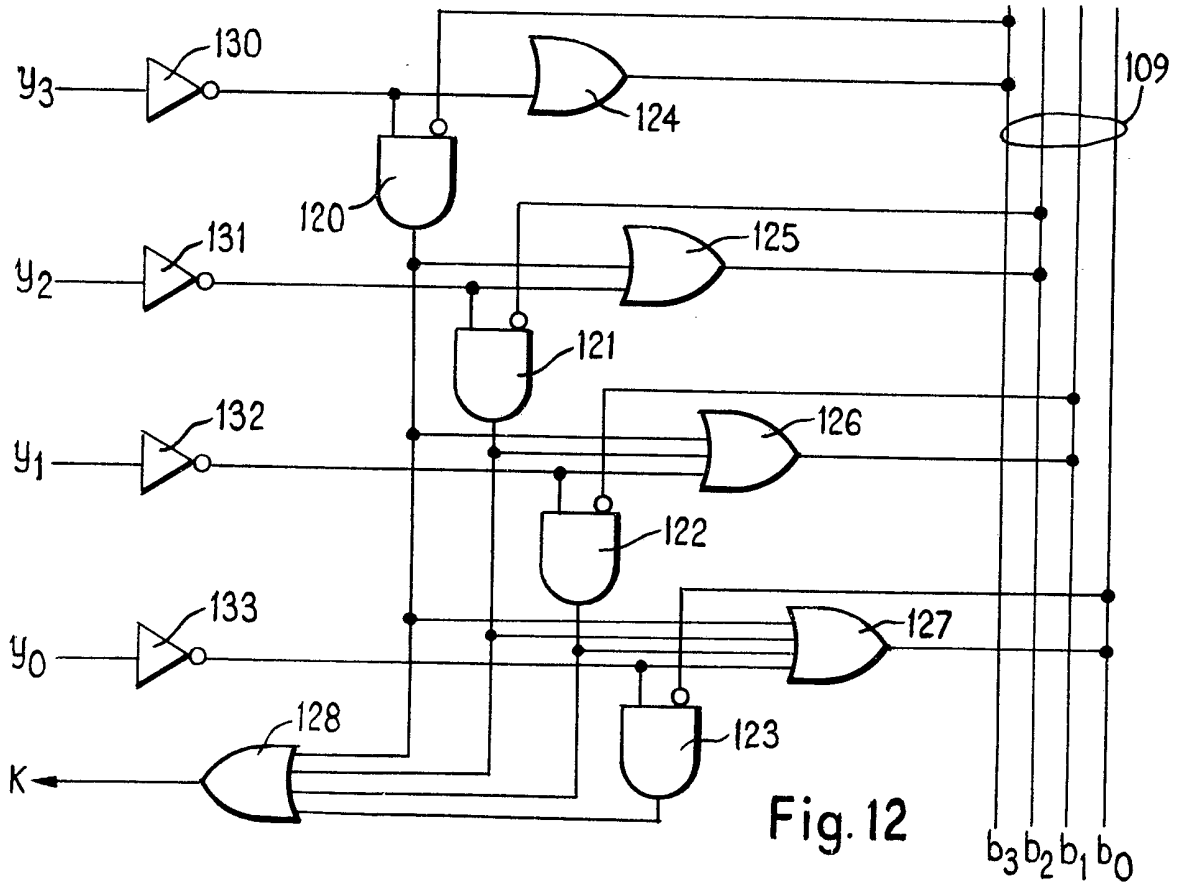

y3
y2
y1
y0
K
130
131
132
133
120
121
122
123
124
125
126
127
128
109
b3 b2 b1 b0

Fig. 12

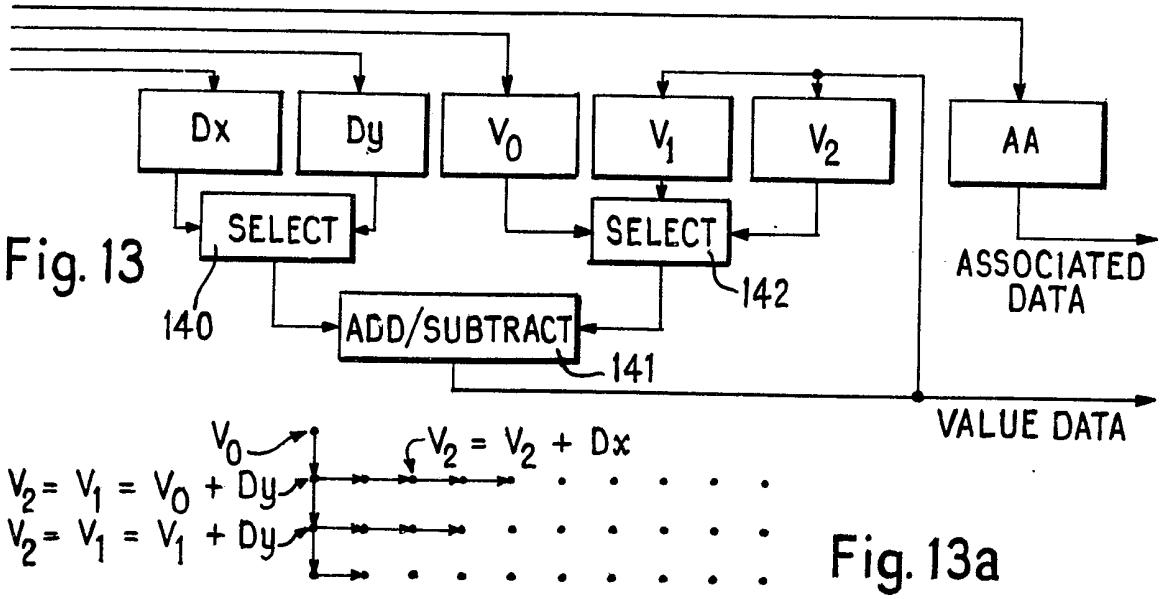


Fig. 13

Fig. 13a

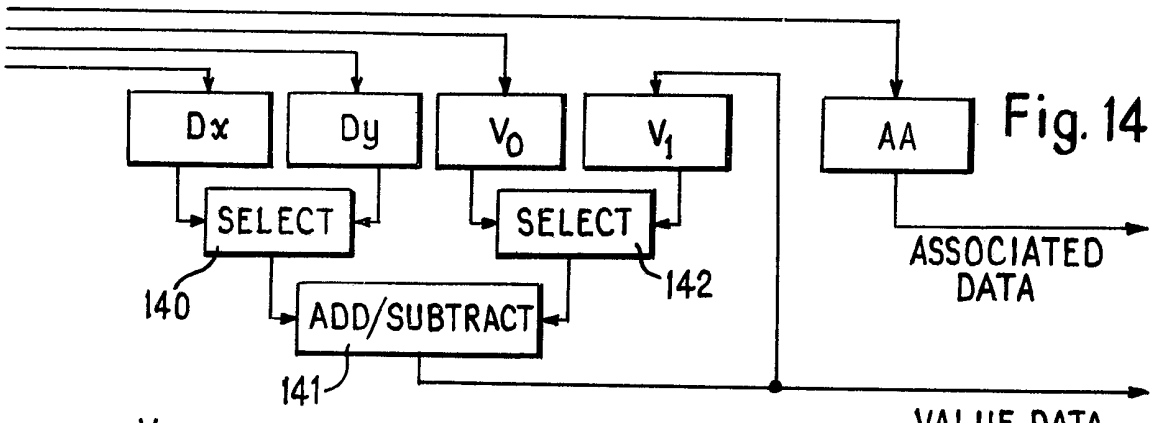
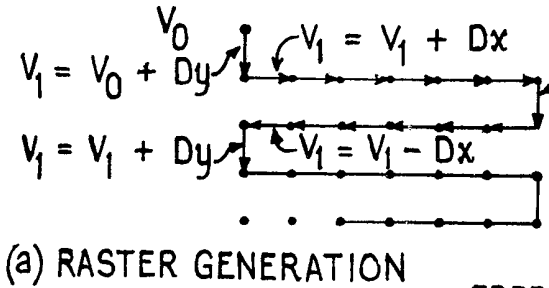


Fig. 14



(a) RASTER GENERATION

Fig. 14a

FREE FORM

(4) LINE GENERATION

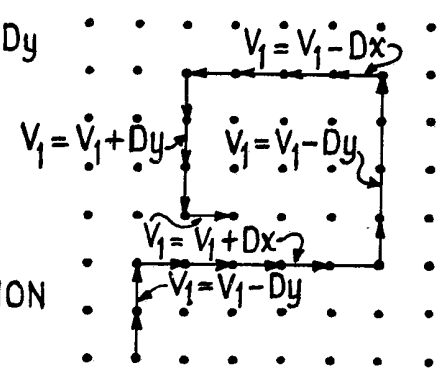
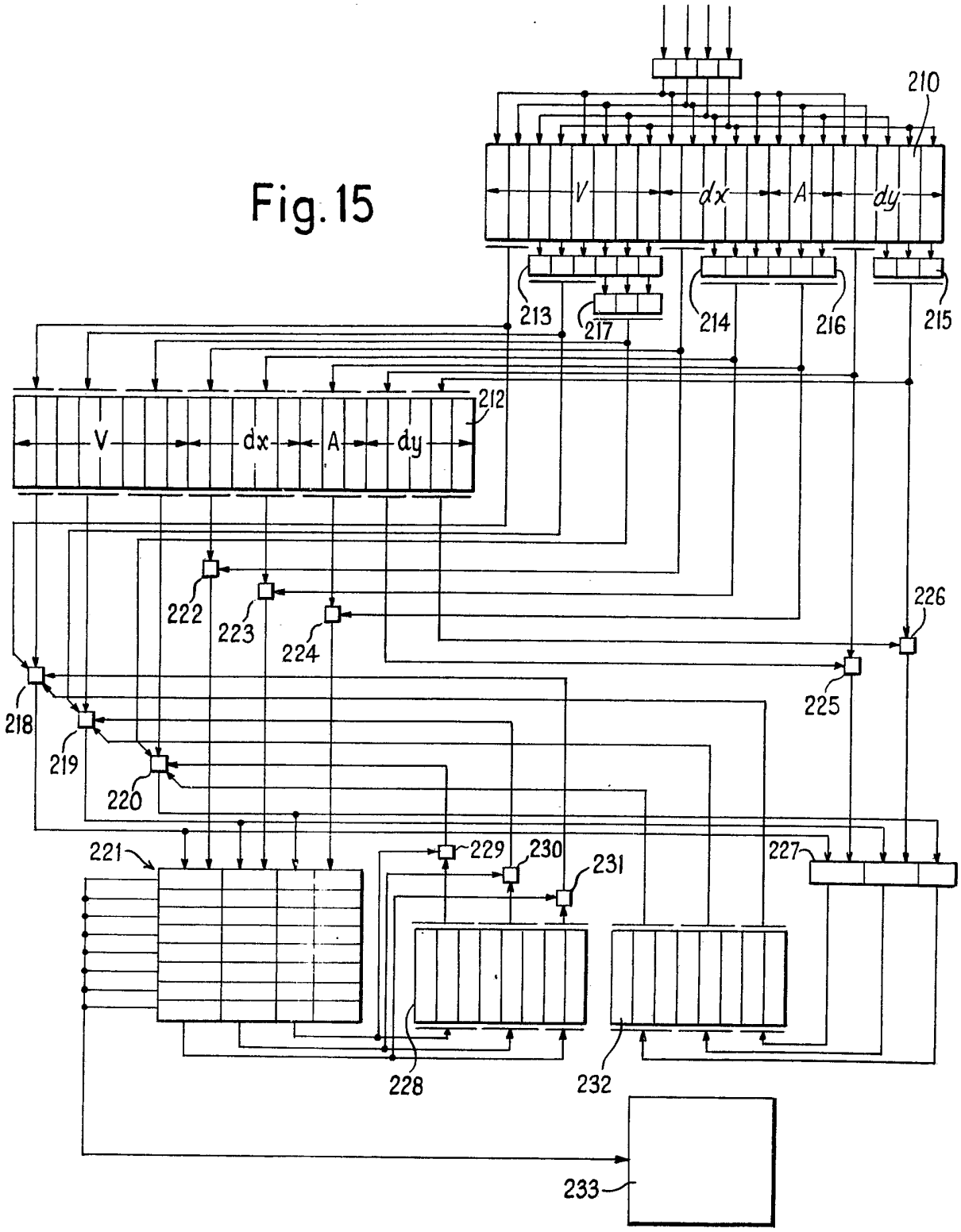


Fig. 14b

Fig. 15


210
V
dx
A
dy
213
217
214
216
215
212
V
dx
A
dy
222
223
224
226
225
218
219
220
221
229
230
231
227
228
232
233

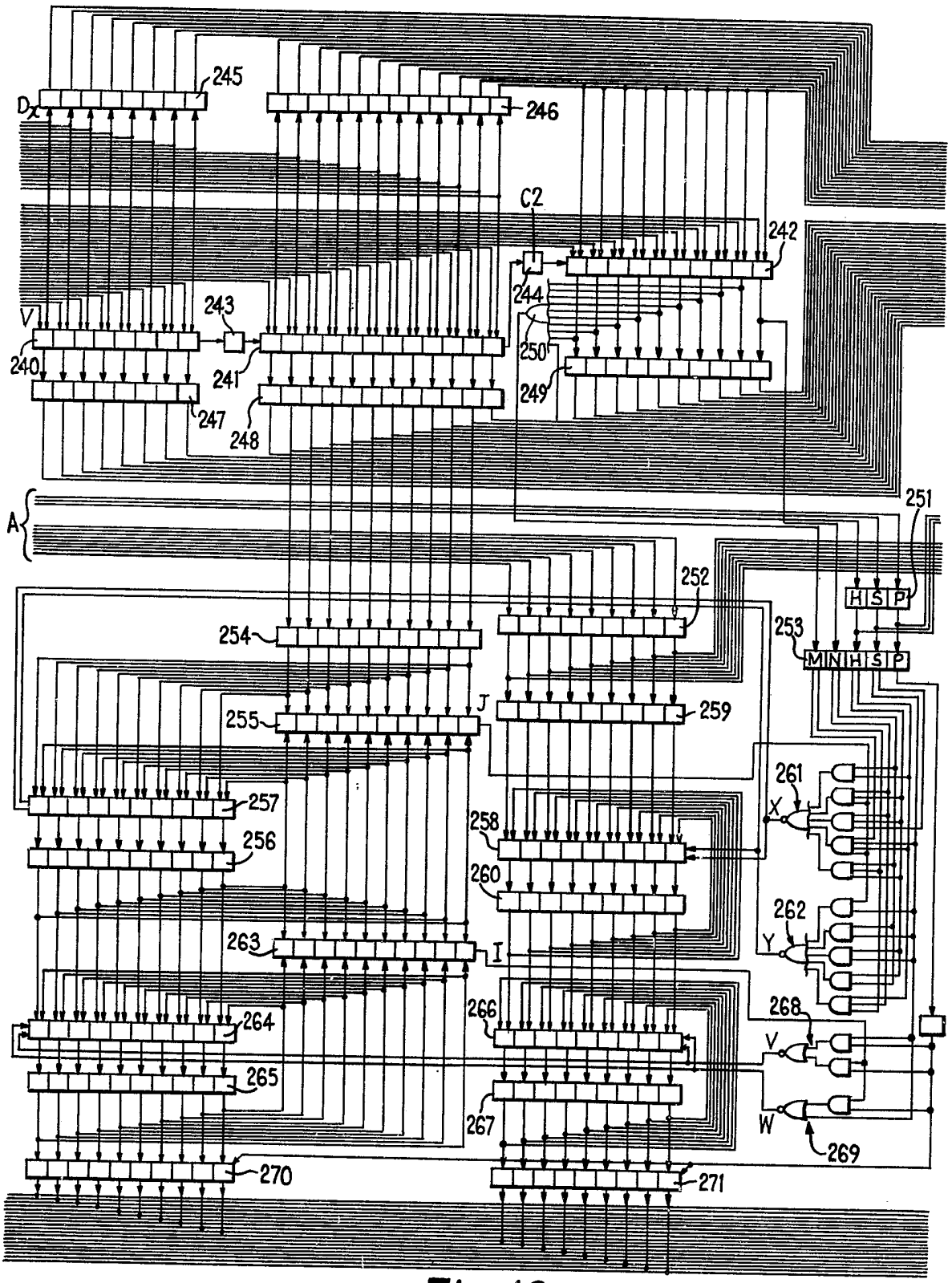

245
246
C2
242
244
243
V
240
241
250
249
247
248
A
251
252
H S P
254
253
M N H S P
J
259
255
261
X
257
258
256
260
262
Y
263
I
264
266
268
V
265
267
W
269
270
271

Fig. 16

Fig. 17

J = 0

NM \ SH	00	01	11	10
00	B	A	A	0s
01	B	1s	1s	0s
11	1s	B	0s	1s
10	1s	B	0s	1s

NM \ SH	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

NM \ SH	00	01	11	10
00	0	1	1	1
01	0	0	0	1
11	0	0	1	0
10	0	0	1	0

J = 1

NM \ SH	00	01	11	10
00	1s	B	A	0s
01	B	1s	1s	0s
11	1s	B	0s	1s
10	1s	B	0s	1s

NM \ SH	00	01	11	10
00	1	0	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

X

NM \ SH	00	01	11	10
00	0	0	1	1
01	0	0	0	1
11	0	0	1	0
10	0	0	1	0

Y

I \ SP	00	01	11	10
0	0	0	1	1
1	0	0	0	1

W

I \ SP	00	01	11	10
0	1	0	1	1
1	1	0	0	1

V

Fig. 18

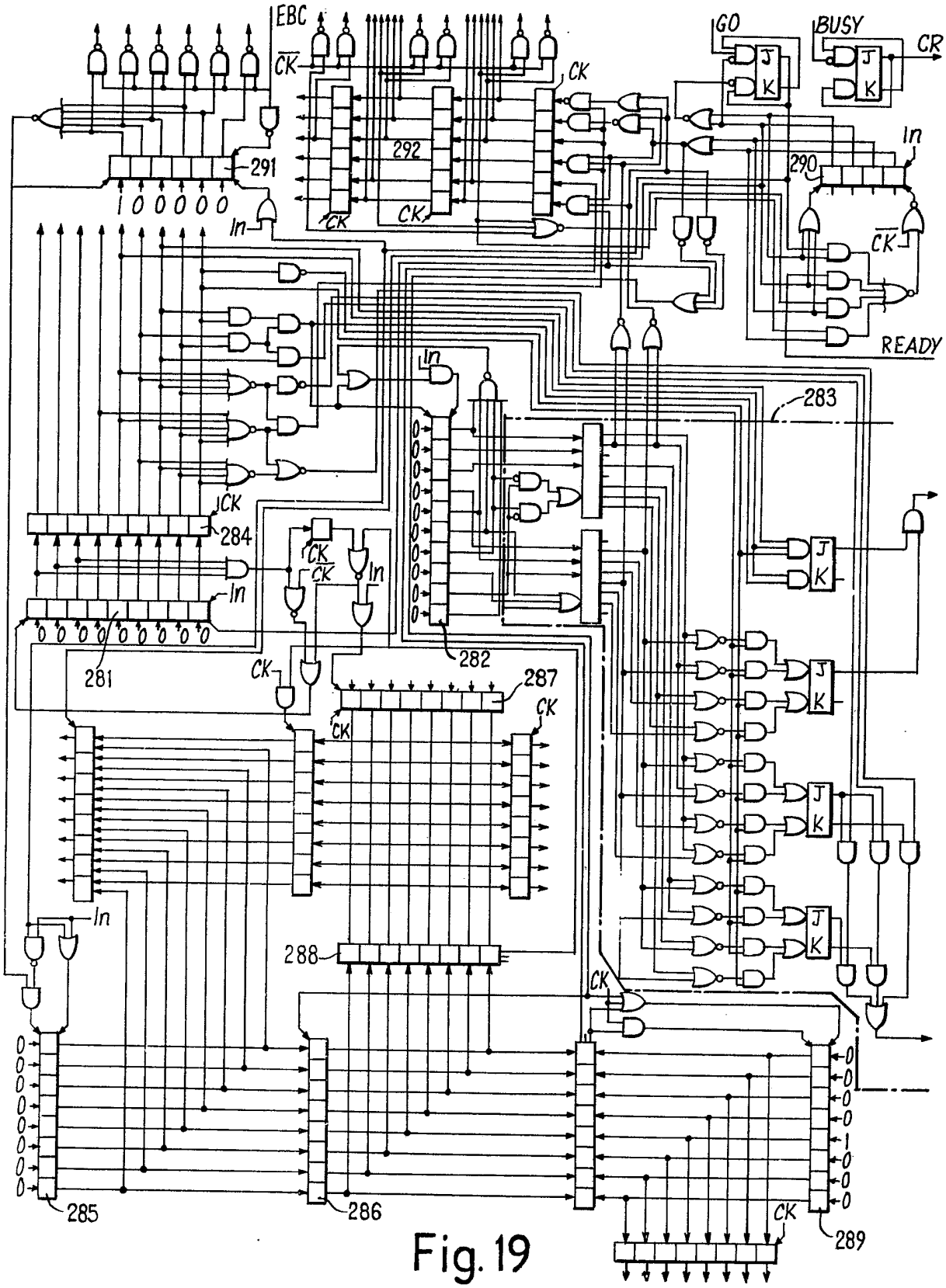

EBC
GO
BUSY
CR
READY
291
292
290
283
284
281
282
287
288
285
286
289
In
CK

Fig. 19

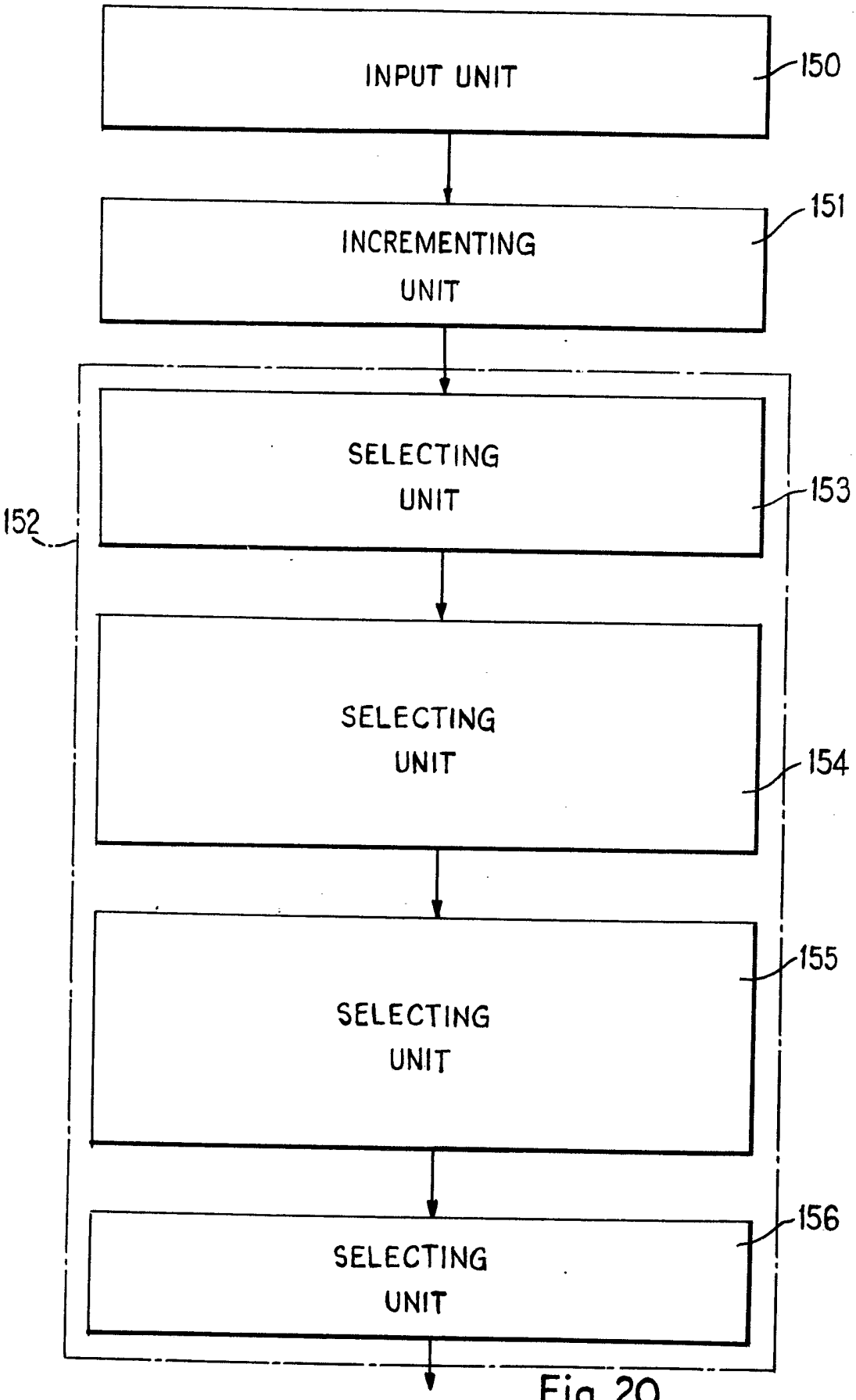
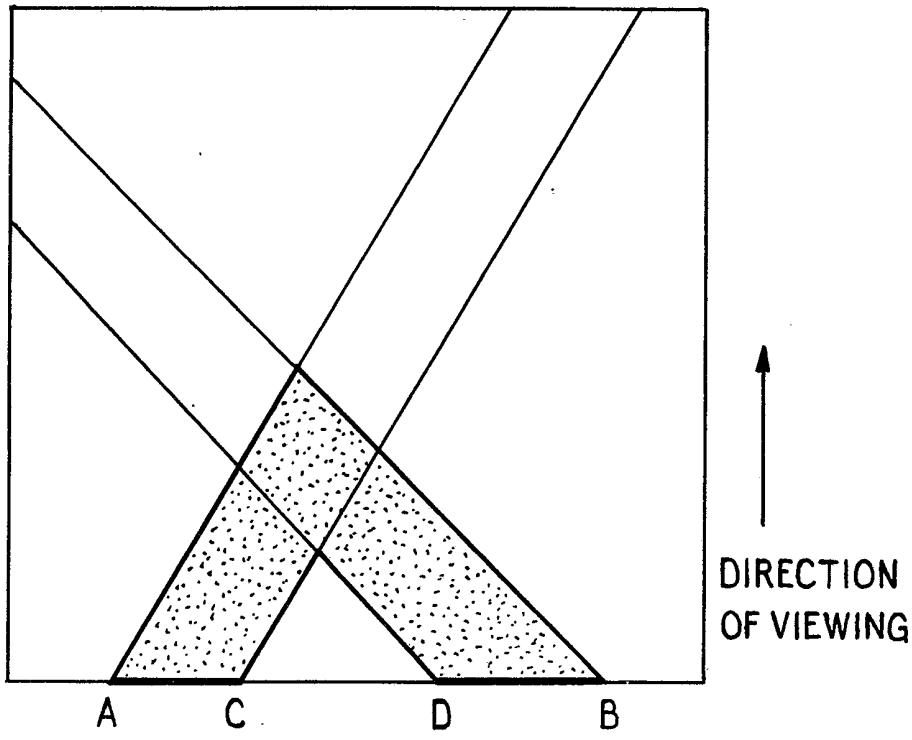

INPUT UNIT
150
INCREMENTING UNIT
151
SELECTING UNIT
153
152
SELECTING UNIT
154
SELECTING UNIT
155
SELECTING UNIT
156

Fig. 20



SCENE = A. B. $(C.D)^1$

SURFACE OF OBJECT ———

DISPLAYED SECTION ——

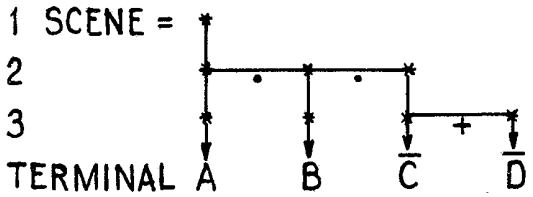


Fig. 21

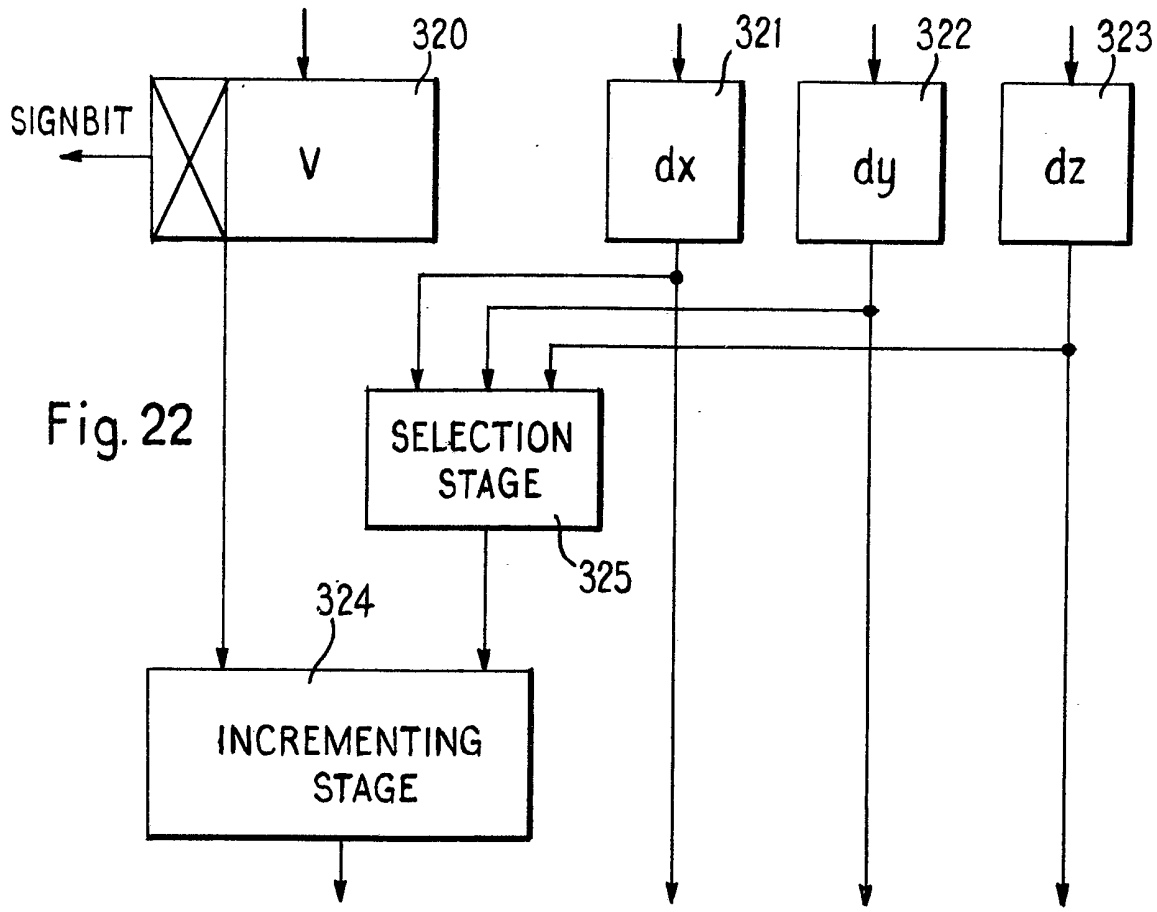

320
321
322
323
SIGNBIT
V
dx
dy
dz
SELECTION STAGE
325
324
INCREMENTING STAGE

Fig. 22

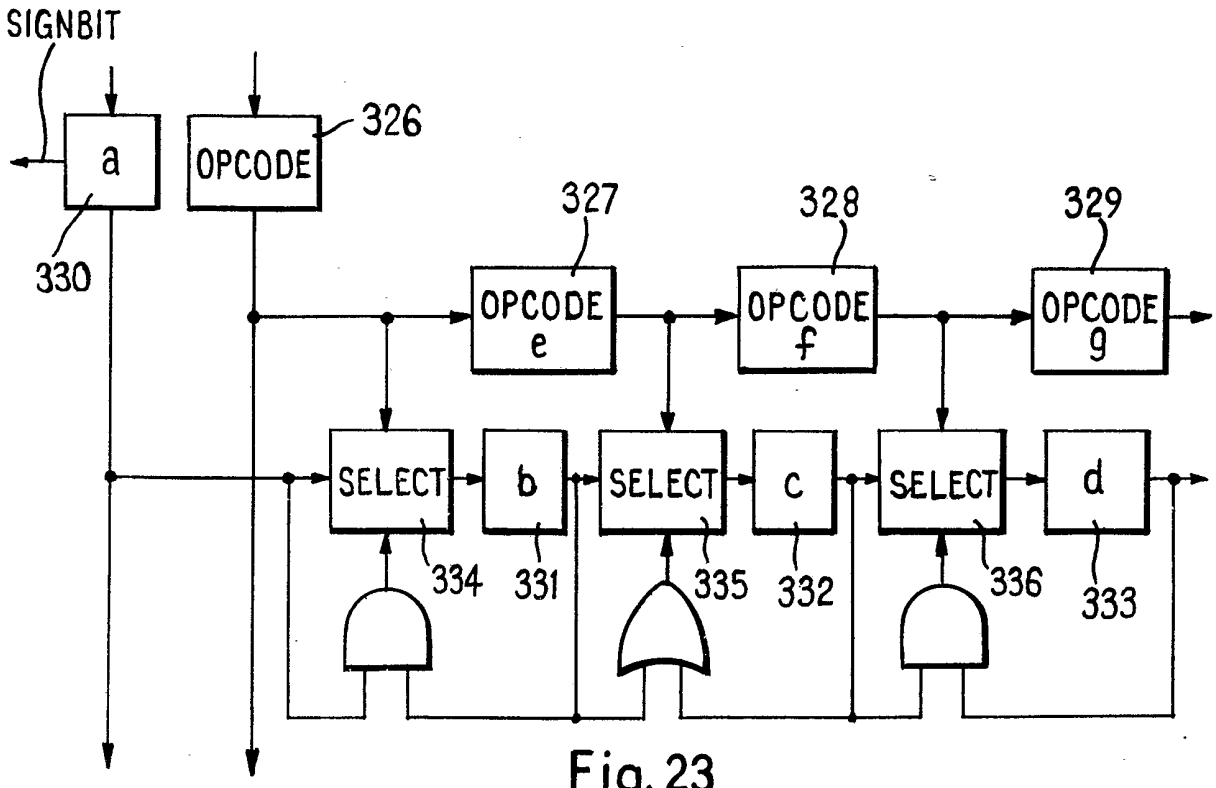

SIGNBIT
a
OPCODE
326
330
327
328
329
OPCODE e
OPCODE f
OPCODE g
SELECT
b
SELECT
c
SELECT
d
334
331
335
332
336
333

Fig. 23

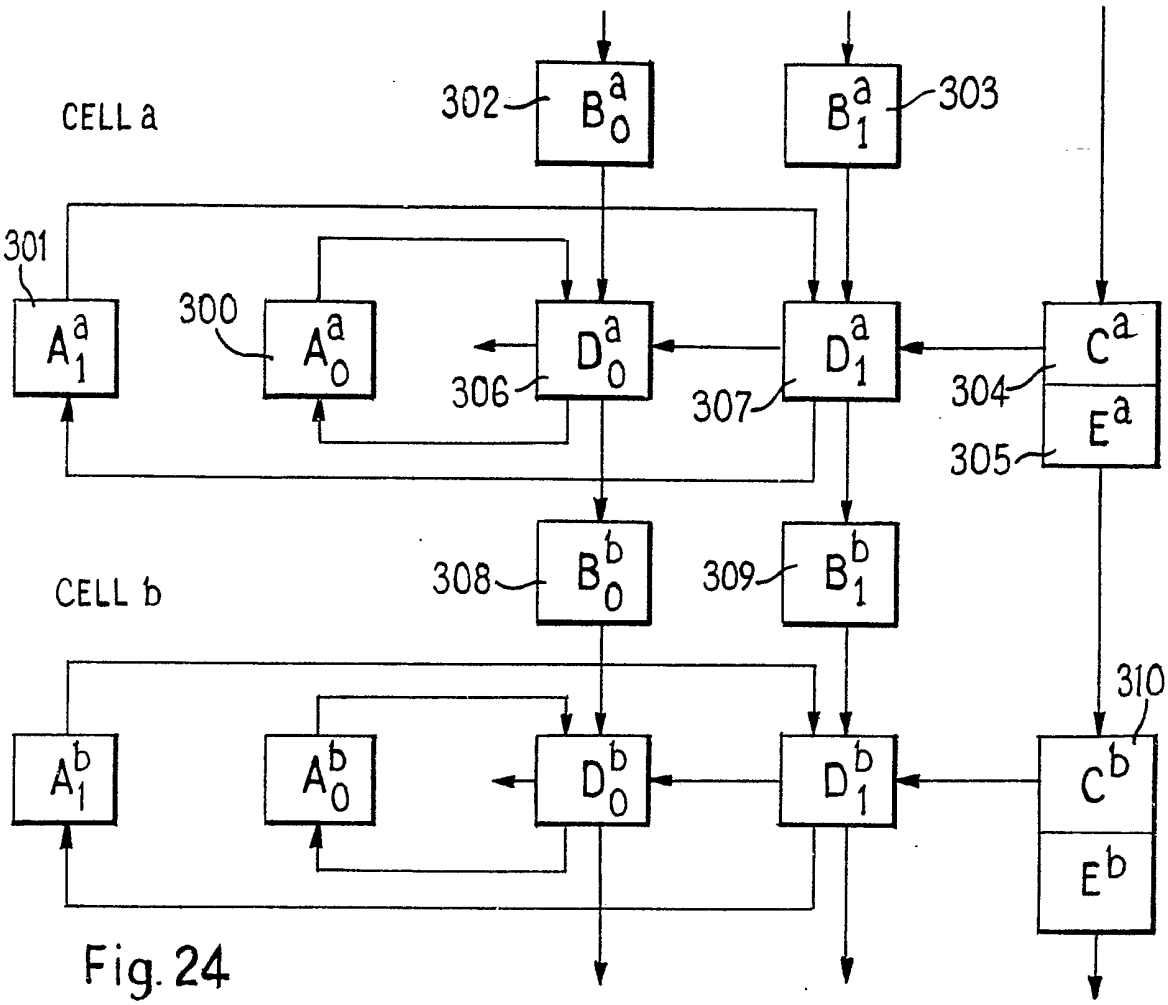

CELL a
CELL b
302
303
301
300
306
307
304
305
308
309
310

Fig. 24

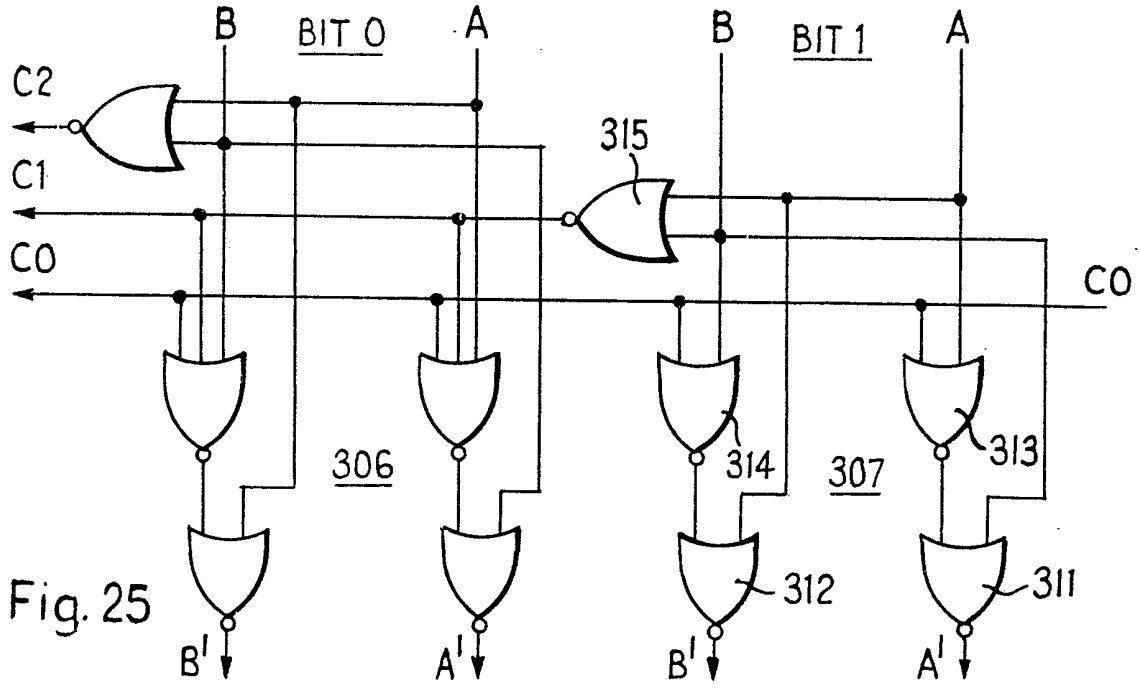

B
BIT 0
A
B
BIT 1
A
C2
C1
C0
315
C0
306
307
314
313
312
311

Fig. 25

SPECIFICATION

Improvements in or relating to Display Processors

This invention relates to display processors which can be used to generate raster scan and line displays from a data-structure where planes forming the facets of a volume or lines bounding a zone in two dimensions are related by a boolean expression, the structure of the boolean expression controlling the display operations.

The primitive elements used in the construction of objects in three dimensional scenes are orientated planes. Similarly the primitive elements used in the construction of zones in two dimensional displays are orientated lines. The orientation of the line or plane defines which side of it is to be considered inside, in other words where the property inside is "true". The boolean expression is used to define more complex regions made up from the intersection or union of the inside regions of named planes or straight lines, the boolean product of a collection of surfaces defining the convex volume which is the intersection of their interiors, the boolean summation of a collection of products denoting the union of these convex objects. In order to carry out each of the display operations in accordance with this invention it is usually necessary to employ a boolean expression in a fully expanded form, in other words without bracketted subexpressions.

There are two kinds of display operation. The first creates a "projected display", the second a "cross-sectional display". The first kind of display operation comprises the following sequence of actions at each display point. Within each product phrase of the boolean expression, the front face furthest from the display surface is selected within the same phrase, the back face nearest the display surface is also selected, and the distance of the display surface from the nearest back face is compared with the distance of the display surface from the furthest front face to determine which is the less, in other words whether the front face is possibly visible. Within the total boolean expression the furthest front faces from those of the product phrases whose furthest front faces are possibly visible are compared, the nearest to the display surface is selected and its associated property data used to create a display.

The second kind of display operation is based on classifying the display point as inside or outside an object. In this mode the boolean expression can be evaluated to give an overall result by entering the separate inside or outside value for each plane into the expression as either true or false. The result in its simplest form is a two valued cross-sectional display. All the foregoing is already known.

The invention provides a processor for producing an output capable of generating an image of a scene on a raster scan display, which scene comprises one or more regions each enclosed by a respective set of planes defined by a boolean expression relating the planes of the set one to another, the processor being adapted to determine what is to be shown in each part of the display from a depth value indicative of the distance of each plane from the display screen, first and second increment values respectively indicative of the depth value change between two raster points in two mutually non-parallel directions, and a property code indicative of whether the plane is a front surface or a back surface of the image and of the position of the plane in the boolean expression of the set of planes including that plane.

When operating in the "cross-sectional display" mode, the processor is arranged to determine whether each part of the display is inside or outside an area bounded by a set of planes.

When operating in the "projected display" mode, the processor is arranged to determine which plane is to be shown in each part of the display. In addition to indicating whether a plane is a front surface or a back surface, the surface value may also be arranged to indicate the colour of such surface.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram illustrating the flow of data through a processing system which will carry out the required display algorithm,

Figure 2 is a diagram illustrating the production of a display in accordance with the processor system described with reference to Figure 1,

Figures 3 and 4 are block diagrams illustrating alternative ways of implementing the system shown in Figure 1,

Figures 5 and 6 are block diagrams illustrating alternative ways of implementing the incrementing units of the system shown in Figure 3.

Figure 7 is a block diagram showing a comparison and selection unit for the system shown in Figure 3,

Figure 8 is a block diagram of apparatus for re-ordering planes in a boolean expression,

Figures 9 and 10 are block diagrams illustrating alternative forms of comparison and selection units for use in the processing system shown in Figure 4,

Figures 11 and 12 are schematic diagrams of minimum and maximum generating circuits respectively for use in the comparison and selection unit shown in Figure 10,

Figure 13 is a block diagram of an incrementing unit for use with the processing system shown in Figure 4,

Figure 14 is a block diagram of a simplified form of incrementing unit for use in the processing system shown in Figure 4,

Figure 15 is a block diagram illustrating the processor system of Figure 3 in more detail,

Figure 16 is a schematic diagram illustrating a single processor of the system shown in Figure 15,

Figures 17 and 18 are Karnaugh Maps of the control functions for the first stage selection and second stage selection respectively,

Figure 19 is a block diagram of the control circuit for use with the processor system shown in Figure 15,

Figure 20 is a block flow diagram of a processing system for operation in a "cross-sectional display" mode,

Figure 21 is a diagram illustrating the production of a display in accordance with the processor system illustrated in Figure 20,

Figure 22 is a block diagram showing an incrementing unit for the system shown in Figure 20,

Figure 23 is a block diagram of a selection circuit for the system shown in Figure 20,

Figure 24 is a block diagram of a smallest-out-first sorting circuit for use in a modified processing system, and

Figure 25 is a schematic diagram of comparison, selection and switching elements for use in the sorting circuit shown in Figure 24.

Figure 1 illustrates the basic essential features of a processing system in accordance with the invention. The input data consists of a value V indicating the depth of the plane behind the display screen at a reference point, for example, the corner from which the scan of the screen begins, a first incremental value dx indicating the change in depth value between successive raster points in the line scan direction, a second incremental value by indicating the change in depth value between successive lines of the raster, and a property code consisting of three bits H, S and P together with an associated value representing a property such as the colour of the surface. The three bits H, S and P indicate whether the surfaces are front or back surfaces, whether it is to be multiplied or added to the previous plane in the boolean expression and whether or not it is the first surface in the boolean expression respectively.

In Figure 1, an input unit 10 receives each new scene description from a main computer. The data is applied to an incrementing unit 11 where the depth value of each surface is incrementing unit 11 where the depth value of each surface is incremented to give the depth value for the next display point. The incremented values from the incrementing unit 11 are applied to a comparison and selection unit 12 which operates in two stages 13 and 14. In the first stage 13, the various surfaces within each product phrase of the boolean expression are compared to identify a possible visible surface, if any, at the display point. Each successive front plane is compared with the current plane having the maximum depth value at the point. If the depth value of the new plane is greater than this intermediate results, then it replaces it. The depth value of each back plane is then successively compared with that of the maximum distance front plane. There is a possible visible surface at the display point only if all such back plane distances are greater than the distance of the maximum distance front plane. The results of these operations at the end of each product phrase are passed to the second stage 14 where a similar comparison process is carried out between the possible visible surfaces of successive product phrases in the overall scene description. The possible visible surface having minimum depth value is selected, along with its property code, to be stored as an intermediate value ready for comparison with the next result from the first stage 13. At the end of the boolean expression, the output from the second stage 14 of the comparison selection unit 12 is passed to a display unit 15.

Figure 2 illustrates the display of a scene represented by the boolean expression A.B.C.D + E.F.G.K, i.e. two objects one of which is bounded by the planes, A, B, C, and D and the other by the planes E, F, G and H. For example, at the point P, after the depth value for each plane has been incremented in turn in the incrementing unit 11, the depth values for the front planes B and D in the phrase A.B.C.D are applied to the first stage 13 of the comparison and selection unit 12 where it is established that, at the point P, the depth value for the plane B is greater than that for the plane B is greater than that for the plane D so that the plane B is selected. Next, the depth values for the back planes A and C are applied to the first stage 13 where it is established that both such values are greater than the depth value of the plane B because both back planes are behind the plane B. Plane B is therefore selected by the first stage 13 as a possible visible surface. A similar operation is then performed on the front planes F and K and the back planes E and G of the phrase E.F.G.K, thereby ascertaining that, although the plane K has a greater depth value than the other front plane F, the back plane E has a smaller depth value, indicating that no plane of the phrase E.F.G.K is visible at the point P. Consequently, since the plane B is the only visible surface, it is selected for display by the second stage 14 of the comparison and selection unit 12. On the other hand, at the point q, where both product phrases yield possible visible surfaces D and F respectively, the second stage 14 of the comparison and selection unit 12 compares the depth values of these two front surfaces and establishes that that of the surface F is smaller than that of the surface D with the result that the surface F is selected for display because the object bounded by the second product phrase is in front of that bounded by the first product phrase.

Figure 3 illustrates a first type of parallel processor in which the incrementing stage comprises a multiple incrementing unit 16 in which, for each plane, the depth values for the plane at a number of different points on the display screen are generated and applied in parallel to a respective one of a corresponding number of comparison and selection units 18, each associated with a respective one of such points. The comparison and selection units 18 compare the depth values for successive surfaces, as received from the multiple incrementing unit 16, in order to determine which front surface, if any, is possibly visible at that point. In other words, the comparison and selection operation for a number of points in the display are carried out in parallel. The display unit 15 has a separate section 20 for each point. Processors of this kind are hereinafter called point processors.

In the second alternative illustrated in Figure 4, the value incrementing stage 11 comprises a plurality of plane incrementing units 22. Each plane incrementing unit 22 products successive depth values for a respective plane at each raster point in turn and applies such values to a multiple comparison and selection unit 24 where, for each raster point in turn, the possible visible plane, if any, is identified and applied to the display unit 15. In other words, the depth values for a number of planes are calculated in parallel. Processors of this kind are hereinafter called plane processors.

The incrementing units and the comparison and selection units of both the point processor of Figure 3 and the plane process of Figure 4 can be implemented in two different ways. One of these is simultaneous processing and the other is an offset form parallel calculation hereinafter called pipelining.

Figure 5 shows part of a pipelined incrementing unit which can be used as the multiple incrementing unit 16 of the point processing system shown in Figure 3. The parts illustrated in Figure 5 comprise the processors for two points P1 and P2. The depth value V_A at the point P1, which is the original depth value V, if the point P1 is at the beginning of the raster scan, or the previously incremented depth value, if the point P1 is some other part of the display, is applied to a latch 30. Similarly the increments dx and dy are applied to latches 31 and 32. The output of the latch 30 supplies the depth value V_A for use at point P1 of the display on output line 33. At the same time, the output for latch 30 is applied to one input of an addition unit 34 the other input of which is supplied, via a selector 35, with the output of one or other of the latches 31 and 32. The selector 35 selects the output of the appropriate latch 31 or 32 depending on whether the change in the depth value between the points P1 and P2 is dx or dy. The output of the addition unit 34 is applied to a latch 36, the output of which, on line 37, forms the depth value V_B at point P2. The outputs of the latches 31 and 32 are also applied to latches 38 and 39 respectively which have their outputs connected, via a selector 40 to the second input of an addition unit 41, the first input of which is connected to the output of the latch 36 so as to further increment the depth value in a similar manner to that previously described.

Thus, it will be seen that the depth value V for a particular point will be supplied sequentially to the appropriate comparison and selection unit 18 (Figure 3). The same sequence of values is applied to the next processor in the pipeline except that each value is incremented to give the value appropriate to the next point in the display. The time at which a value for a particular point is passed to the appropriate comparison and selection unit 18 is offset by one clock period when comparing a processor with its neighbour. Since a supply of outputs from the comparison and selection units 18 is triggered by the bit P in the first plane in the next boolean expression to be processed, the output takes the form of a continuous stream of values from consecutive processors, one from each for each consecutive clock period.

Figure 6 shows a simultaneous multiple incrementing unit 16 for a sixteen point display. In this embodiment the increments Dx and Dy are the increments to the depth value of a plane which occur when half the screen is traversed in the x direction and the y direction respectively. The depth value of a point at the centre of the display is applied via an input terminal 50 to adders 51 and 52 and to subtractors 53 and 54. The increment $\frac{1}{2}$dy is applied to the second inputs of the adder 52 and the subtractor 53. The output of each of the adders 51 and 52 and each of the subtractors 53 and 54 is applied to a respective pair of adders 55 and 56 and a respective pair of subtractors 57 and 58. The increment $\frac{1}{4}$dy is applied to the second inputs of each of the adders 55 and subtractors 58 and the increment $\frac{1}{4}$dx is applied to the second inputs of each of the adders 56 and subtractors 57. The outputs of the various adders 55 and 56 and subtractors 57 and 58 are the depth value for the sixteen points P1 to P16 of the display.

Figure 7 shows a comparison and selection unit which can create either type of display and which can be used with either of the incremeting units shown in Figures 5 and 6. The data is entered so that the depth value of a particular plane and the corresponding externally defined code bits H, S and P, two code bits N and M generated in the incrementing unit and the associated data all arrive at the same time. The bit N represents the sign of the depth value and the bit M indicates whether it is greater than the maximum value used in the comparison and selection unit. The new depth value of the intermediate visible surface of the current product phrase from the boolean expression, which is stored in a latch 62, to give a signal I which, with the other control bits, sets up a selection control signal X. This signal X determines whether the next value to be stored in the latch 62, and also the associated data value to be stored in a latch 63, are the existing stored values, corresponding to the previous intermediate visible surface, or the values in the latches 60 and 64 respectively, which are the values of the new surface. If no visible surface exists at a particular point in the

display, then the value stored in the latch 62 is all 1's. If the surface of the display cuts through an object then the value stored is all 0's. At the end of each product phrase, the value then in the latch 62 is compared, by a comparator 65, with the value, if any, in the latch 66 resulting from previous product phrases, to give a signal J which, with the other control bits, sets up a selection control signal Y. This signal Y determines whether the next value to be stored in the latch 66, and also the associated data in a latch 67, are the existing stored values, corresponding to the intermediate visible surface from previous product phrases, or the values in the latches 62 and 63 respectively, i.e. the value of the visible surface from the most recent product phrase.

The comparison and selection unit shown in Figure 7 requires the data to be organised in such a way that all the front surfaces in a product phrase are processed before any of the back surfaces therein. Consequently, when displaying the rotation and translation of objects in real time, a re-ordering of planes in the boolean expression defining the object may be necessary between each frame of the display. This can be conveniently done by using the apparatus shown in Figure 8. The scene description is entered into a scene description memory 70, the output of which is connected to a transformation unit 71 which transforms the scene description to the form V, Dx, Dy etc. The output of the transformation unit 71 is connected to a classification unit 72 which applies the data relating to front planes to a front plane store 73 and the data relating to back planes to a back plane store 74. The outputs of the stores 73 and 74 are applied via a selector 75 to a picture store 76, the output of which constitutes the input to the display processor. The selector 75 is arranged to enter the data for all the front planes of a product phrase from the front plane store 73 into the picture store 76 before the data for any of the back planes of such phrase from the back store 74.

Figure 9 shows part of a pipelined version of the multiple comparison and selection unit 24 of Figure 4, the drawing showing three sections 80, 81 and 82 for processing the data from three of the incrementing units 22. As already explained, each of the incrementing units 22 process all the data for a respective single plane. The manner in which the units work on a pipeline basis is that, while the section 81 is processing the data for a particular point in the display, the section 80 is processing the data for the next following point and the section 82 is processing the data for the previous point. The planes are allotted to the various incrementing units 22, and therefore to the various sections of the comparison and selection unit 24, in the order in which they appear in the boolean expression. The operation of the section 80 will be described by way of example. The current depth value fo the plane which is to be processed is entered in a latch 83 from the corresponding incrementing unit 22 and the associated data of the plane is entered in a latch 84. The depth vlaue of the intermediate visible plane in the same product phrase is applied from the previous stage of the unit 24 to a latch 96 and the corresponding associated data is applied to a latch 85.

The values in the latches 83 and 96 are compared by a comparator 86 which operates selector 87 and 88, for the depth values and the associated data respectively, so as to apply the new value, associated with the plane processed by the section 80 to the next section 81 if the plane concerned is a front plane and if the depth value is greater than that of the previous intermediate depth value. If the plane being processed is a back plane and its depth value is less than the value in the latch 96, the selector 87 selects all 1's for application to the next stage 81, to indicate that no object exists at the points being processed. It will be recalled that the data has been organised so that all front planes in a product phrase are processed before any back plane.

The intermediate depth value from the previous product phrase is entered in a latch 89 and the corresponding associated data in a latch 90. If the plane processed by the section 80 is not the first plane in a product phrase, then selectors 91 and 92 pass this data to the next section 81 unchanged. On the other hand, if the plane being processed by the section 80 is the first plane of a product phrase, the output of the latches 83 and 84 are applied, by the selectors 87 and 88 directly to the next section 81 and the contents of the latch 96, which is the intermediate depth value from the previous product phrase, is compared with the depth value in the latch 89 by a comparator 93 and the smaller depth value, being that of the plane nearer to the display, is applied, by the selector 91, and the corresponding associated data is applied by the selector 92, to the next section 81.

If the section 81 is to process the first plane of a scene description, all 0's are applied to the latches 96 and 85 and all 1's to the latches 89 and 90. If the section next but one prior to the section 80 is to process the data of the last plane of a scene description, then the section prior to the section 80 compares the intermediate value of the last product phrase with the intermediate value resulting from the other product phrases and applies the resulting depth value to the latch 89 of the section 80 and the corresponding associated data to the latch 90 thereof. The resulting final depth value and associated data for the particular point of the display then appear at outputs 94 and 95 respectively.

Figure 10 illustrates part of a simultaneous comparison and selection unit 24 which can be used in place of the pipelined unit of Figure 9. The drawing shows two sections 100 and 101 for processing the data for two successive planes in the boolean expression, together with part of a third section 102. The operation of the section 101 will be described by way of example. The depth values of the plane to be processed by the section 101 at successive points are applied serially to an input 103 while the corresponding associated data is applied to an input 104, all the values for the various places at the same point being applied to their respective sections of

the comparison and selection unit simultaneously. A control signal generator 105 receives the bits H S P of the property code, a bit N indicating the sign of the depth value V and a bit M, indicating whether the depth value exceeds a predetermined threshold. It will be appreciated that if the sign bit N is negative, the plane is, at the point in question, in front of the plane of the display screen and therefore cannot be seen at the point in question. If the bit M indicates that the depth value exceeds the threshold and the bit N indicates that the depth value is positive, then, at the point in question, the plane is so far behind the plane of the display screen as not to be distinguishable, the particular depth value of the threshold being determined by the capacity of the processing system. The control signal generator 105 also receives bits I, J and K from a comparator 106, a minimum generation unit 107 and a maximum generation unit 108. The comparator 106 is arranged to compare the depth value on the input 103 with the value on a first stage selection bus 109. The maximum generation unit 108 is arranged to make the same comparison when a switch 110 is on and also to replace the value on the bus 109 with the depth value at the input 103 if the latter is greater. The minimum generation unit 107 is arranged to compare the depth value at the input 103 with the value on a second stage selection bus 111 when both switches 110 and 112 are on and to replace the value on the buss 111 with the depth value 103 when the latter is the smaller. A switch 113 is connected in series with the bus 109 between the section 101 and the next section 102 of the comparison and selection unit 24. The switch 113 opens when the data applied to the section 101 is that of the last plane in a product phrase. In other words, the switch 113 and the corresponding switches in the other units are used to divide the bus 109 into a respective separate section for each product phrase. The bus 111 is permanently connected to all sections of the entire unit.

When the section 101 is processing the data for a plane at a particular point in the display, the control unit 105 produces a signal A to turn the switch 110 on if the plane is a front plane. Initially, there is no value on the bus 109 but the maximum generation units 108 in the various sections rapidly establish the depth value of the furthest front plane in each product phrase on the relevant section of the bus 109. For back planes, the switch 110 remains closed but the comparator 106 establishes whether such a back plane has a smaller depth value than the front plane whose depth value is on the bus 109 and, if so, applies a signal to one-bit bus 114 to inhibit the passing of any value in the product phrase to the second stage of comparison because there is no visible surface from the product phrase at the point of the display being processed. The bus 114 is splitable into respective sections for each product phrase by switches 115 which are connected to receive the same signal B from the control unit 105 as the switches 113.

If the plane being processed by the section 101 is the front plane in its product phrase generating the maximum value and the inhibit signal on the bus 114 is not present, the control unit 105 generates a signal B to turn the switch 112 on so that the depth value is applied to the minimum generation unit 107. The control unit 105 also produces a signal C to open a switch 116 to forward the associated data on the input 104. If the minimum generation unit 107 indicates that the depth value on the input 103 is the minimum in the boolean expression at the point being processed, the control unit 105 generates a signal E to open a switch 117 to forward the associated data from the output of the switch 117 to the display unit.

Figure 11 is a schematic circuit diagram of a version of the minimum generation unit 107 capable of handling four-bit depth values. Each of the bits x_3 to x_0 of the depth value of the plane being processed is applied to a first, direct input of a respective AND gate 120 to 123 while the corresponding bit from the bus 111 is applied to a second, inverting input of the corresponding AND gate. The most significant bit conductor of the bus 111 is connected to the output of an OR gate 124 having its single input connected to receive the bit x_3. The next most significant bit conductor of the bus 111 is connected to the output of an OR gate 125 having two inputs, one connected to receive the bit x_2 and the other to the output of the AND gate 120. The next bit conductor of the bus 111 is connected to the output of an OR gate 126 having three inputs, one connected to receive the bit x_1 and the other two to the outputs of the AND gates 120 and 121 respectively. The least significant bit conductor of the bus 111 is connected to the output of an OR gate 127 having four inputs, one connected to receive the bit x_0 and the other three to the outputs of the AND gates 120, 121 and 122. In addition, the outputs of all four AND gates 120 to 123 are connected to respective inputs of an OR gate 128, the output of which constitutes the control signal J.

Since logic 0 is represented by an earth condition, 0 predominates if both 0 an 1 are applied to the same conductor. Consequently, starting from the most significant bit downwards, if the bits applied at x are the same as the bits on the bus 111, no change takes place. If a 0 is already present on the bus, then a 1 applied from one of the OR gates 124 to 127 does not cause any change to take place. On the other hand, if one of these OR gates applies a 0 to a bit conductor of the bus which was previously at logic 1, the output of such OR gate pulls the bus down to logic 0.

A signal 1 at the non-inverting input of any of the AND gates 120 to 123 and a signal 0 at the inverting input thereof causes the OR gates for all less significant bit positions to apply logic 1 to the bus, with the result that, if logic 1 is already present at any of such less significant bit positions, it remains but if logic 0 is already present, the logic 0 condition predominates. In other words, the bit outputs of a minimum generating unit which are of less significance than the most significant bit at logic

1 to differ from the corresponding bit on the bus can have no effect on the corresponding less significant bits on the bus, with the result that the bit values of these less significant bits are determined by the minimum generating unit producing the minimum overall value.

The circuit of the maximum generating unit illustrated in Figure 12 is identical with that of the minimum generating unit illustrated in Figure 11 except that the input bits y_3 to y_0 of the plane being processed are connected via respective inverters 130 to 133. The result of this is that the value on the bus 109 is the complement of the maximum value at theinput of the corresponding maximum generating unit.

Figure 13 shows an incrementing unit 22 for the plane processing system shown in Figure 4. As stated above, one such incrementing unit is provided for each plane. The initial depth value V for the plane at the beginning of the raster scan, together with the values of the increment in the x and y directions and the associated data are entered into the stores V_0, Dx, Dy and AA respectively. Additional stores V_1 and V_2 are provided for storing the incremented depth value obtained by moving along a raster line and the incremented depth value at the beginning of the current raster line respectively. The outputs from the stores V_0, V_1 and V_2 are applied via a first selector 140 to one input of an add/subtract unit 141 and the outputs of the stores Dx and Dy are applied to the other input thereof by a selector 142. Since the depth value at the beginning of the current raster line is stored in the store V_2, the incrementing unit can provide a direct output to a conventional television raster in which each line is scanned from left to right, as shown in Figure 13a.

Figure 14 shows a simplified version of the incrementing unit 22 which is the same as the version shown in Figure 13 except that the store V_2 is omitted. The effect of this is that there is no record of the depth value at the beginning of the current raster line and consequently the system can only operate in a manner in which the change between successive points involves an increment in either the x direction or the y direction. Examples of incrementing patterns which can be produced by this simplified form of incrementing unit are the raster patterns shown in Figure 14a, in which alternate lines are scanned in opposite directions, and the free form line generation procedure illustrated in Figure 14b.

Figures 15 to 19 illustrate a parallel processor using the pipelined incrementing system and providing a "projected display", in more detail.

Referring to Figure 15, the values V, dx, dy and A for each plane, are fed from a computer interface to a buffer store 210, each word of which constitutes the data for a single plane. The buffer store has the capacity of thirty two bits for the depth value V, and twenty bits each for the increments dx and dy. In the drawing these values are shown in units of four bits. The associated data A comprises twelve bits of which three bits are used to hold the operation codes H, S and P which indicate whether the plane is a front or back surface whether it is the first plane of a product phrase or not, and whether it is the first plane of a new scene description. The remaining nine bits of A constitute colour bits C the three colours red, green and blue, the level of each colour being indicated by three bits.

Each word in the buffer store 210 is transferred in turn to a picture store 212, once a complete scene description has been received. The eight least significant bits of the values V, dx and dy are applied directly from the buffer store, while the twelve next most significant bits of the value V, the twelve most significant bits of the values dx and dy and all twelve bits of A are transferred via respectively latches 213, 214, 215 and 216, so as to give a delay of one clock cycle. The twelve most significant bits of the value V which are also applied to the latch 213 are subsequently applied to a further latch 217 so as to be subject to a two cycle delay. The effect of this is that, when either of the increments dx or dy is added to V, the eight least significant bits are added in the first clock cycle, the next twelve in the second cycle and the effect of any carrying or the adding of negative increments on the twelve most significant bits of V is taken into account in the third cycle. Consequently the duration of a clock cycle need not be as long as it takes to perform a thirty two bit addition, but need only be sufficiently long to complete a twelve bit addition.

The output from the parts of the picture store 212 containing the values of V are applied, by respective selectors 218, 219 and 220 to respective inputs of a processor bank 221 consisting of eight processors. The selector 218 is also connected directly to the output of the buffer store 210 containing the least significant eight bits of the value V, while the selector 219 is also connected to the output of the latch 213 and the selector 220 to the output of the latch 217. Similarly selectors 222 and 223 control the supply of the increment values dx to the processors 221 while the selector 224 controls the supply of the values A thereto. The outputs of the part of the picture store 212 containing the increment values dy are connected by selectors 225 and 226 to a line increment processor 227. The selector 225 is also connected directly to the buffer store 210 and the selector 226 to the output of the latch 215.

The construction and operation of the eight processors forming the processor bank 221 will be described in more detail hereinafter. Briefly, the function of each processor is to compare, at a particular raster point, each plane with all the other planes in a scene description in order to ascertain which is the front face furthest from the display surface, which is the back face nearest to the display surface and whether the nearest back face is nearer to the display surface than the furthest front surface. As the data is passed from one processor to the next, the value V is increased by the increment dx so that, at the output of the eighth processor, the value V has been incremented by 8dx. The incremented value of V is applied both to the point store 228 and the respective inputs of the selectors 229, 230 and 231. The

second inputs to the selectors 229, 230 and 231 are connected to the outputs of the point store 228 and the outputs of these selectors are connected to the respective inputs of selectors 218, 219 and 220. Thus as the processing of the raster points in a line continues the incremented values of V are successively passed through the processor bank.

At the beginning of the first raster line, the line increment processor 227 adds the increment dy to the value V and the incremented value is applied to line store 232. Though for the first point in the first raster line the processors obtain their depth values V from the picture store 212 and for subsequent points in the raster line from the point store 228, for each new line they obtain their depth values from the line store 232. To permit this, the outputs of the line store 232 are applied to the selectors 218, 219 and 220 and the outputs of these selectors are linked to the line increment processor 227 to allow the depth values for the beginning of subsequent lines to be evaluated. When the last plane in a scene description passes through one of the processors then the associated data representing the colour of the visible surface is output onto a nine bit bus linking each processor in the bank 221 to a TV monitor unit 233. Only one processor will contain the last plane at any clock cycle so only one processor will be passing output to the TV display at any one time.

Figure 16 shows the first processor of the processor bank 221 in more detail. This processor is in two parts, an incrementing section and a comparison and selection section. The incrementing section consists of three adders 240, 241 and 242, the carry output of the adder 240 being connected to the carry input of the adder 241 via latch 243 and the carry output of the adder 241 being connected to the carry input of adder 242 via a latch 244. The digits of the value V from the selector 218 are applied to the adder 240, those from the selector 219 to the adder 241 and those from the selector 220 to adder 242. Similarly the digits of the increment dx from the selector 222 are applied to the second inputs of the adder 240 and those from selector 223 to the second inputs of the adder 241. The two groups of digits of the increment dx are also applied to respective latches 245 and 246, the output of which form the dx input to the next processor in the bank 221. The output of the addres 240, 241 and 242 are applied to respective latches 247, 248 and 249, the output of which, consisting of the value V incremented by dx, forms the V input to the next processor. The most significant bit of the output of the latch 246 is applied to each of the second inputs to the adder 42.

The 30th bit of the input V is transferred to the comparison stage as bit N indicating the sign of the value V. The two most significant bits of the original thirty two bit value are ignored, these two unused bits result from constructing the memory as a collection of four bit slices through the machine. The thirty bit value is made up from four fields. The first ten bits are called the fractional part, the next nine bits are called the comparison part, the next ten bits are called the overflow part and as already indicated the thirtieth bit is the sign bit. The ten bits of the overflow part are connected to an OR gate 250 to give a value M which is passed to the control of the comparison section.

The bits H, S and P of the associated data signal A are entered into a latch 251 and the colour bits C into a latch 252. The outputs of the latches 251 and 252 are used to transfer the associated data to the next processor and also form inputs to the comparison and selection section of the processor illustrated in Figure 18. The bits H, S and P from the latch 251 are entered into a latch 253 together with the bits M and N from the OR gate 250 and the most significant bit output of the adder 242 respectively.

The comparison and selection section consists of two stages each in two parts. The two stages correspond to the selection within a product phrase of a visible surface and the selection of the dominant visible surface from all the product phrases in the boolean expression. The two parts handle the depth values V, and the associated property data A.

In Figure 16 the tenth to nineteenth bits from the thirty bit value V is the field which is transferred to the comparison and selection unit from the incrementing unit, the first bit being the least significant bit. This ten bit value is entered into a latch 254. The output of the latch 254 is passed to a first level comparator 255, and also to a first level selector 257. The second set of inputs to the comparator 255 are obtained from a latch 256, the inputs which are from a selector 257. This arrangements allows the new depth value to be compared with a previously stored depth value held in the latch 256, and where required substituted for it by the appropriate setting of the selector 257. The selector in this first stage of the comparison unit is also used to enter the value all 1's or all 0's into the latch 256. The all 1's value is created when there is no visible surface at the display point, and all 0's is created when the display point lies within the interior of an object being displayed. The condition which determines which new input is to be entered into the latch 256 is a logical function of the data signals H, S, N and M, which are stored in a latch 253, and the output J of the comparator 255. The relation between these control values and the required selection is as follows:—

N=0	Positive depth value
N=1	Negative depth value
H=0	Back surface

H=1 Front surface

M=0 Overflow part of depth value is zero.

M=1 Overflow part of depth value is greater than zero.

S=0 Boolean product operation

S=1 Boolean summation operation

J=0 New value is greater than the old value.

J=1 New value is less than or equal to the old depth value.

The values selected for entry into the latch 254 are as follows:—

		J=1, S=0, H=0
J=0, S=0, H=0		
N=0, M=0	Enter old value	Enter all 1's
N=0, M=1	Enter old value	Enter old value
N=1, M=1	Enter all 1's	Enter all 1's
N=1, M=0	Enter all 1's	Enter all 1's
J=0, S=1, H=0		**J=1, S=1, H=0**
N=0, M=0	Enter all 0's	Enter all 0's
N=0, M=1	Enter all 0's	Enter all 0's
N=1, M=1	Enter all 1's	Enter all 1's
N=1, M=0	Enter all 1's	Enter all 1's
J=0, S=1, H=1		**J=1, S=1, H=1**
N=0, M=0	Enter new value	Enter new value
N=0, M=1	Enter all 1's	Enter all 1's
N=1, M=1	Enter all 0's	Enter all 0's
N=1, M=0	Enter all 0's	Enter all 0's
J=0, S=0, H=1		**J=1, S=0, H=1**
N=0, M=0	Enter new value	Enter old value
N=0, M=1	Enter all 1's	Enter all 1's
N=1, M=1	Enter old value	Enter old value
N=1, M=0	Enter old value	Enter old value

A corresponding selection of the colour bits C corresponding to each depth value is performed by a selector 258. The output of the latch 252 is applied, via a latch 259 to one input of the selector 258. The output of the selector 258 is connected to a latch 260, the output of which forms the second input of the selector 258.

Two data networks 261 and 262 generate two control signals X and Y for controlling the selector 257 and 258. The precise details of these networks depend on the particular components used to carry out the selection operation. Using SN74 153 four-way selectors, the control signals are as follows:—

X	Y		
0	0	Select input 1; old value from latches 256 and 260	B
0	1	Select input 2; all 0's	L
1	0	Select input 3; all 1's	H
1	1	Select input 4; new value from latches 254 and 259	A

The logic to generate the two signals X and Y is defined in the Karnaugh Maps given in Figure 17, and the control function is:—

$$X = \overline{N.H. + \overline{J}.\overline{H}.\overline{N}. + S.\overline{H}.\overline{N} + \overline{N}.M.\overline{H} + J.\overline{S}.H.\overline{M}}$$

$$Y = \overline{N.\overline{H} + J.\overline{S} + N.\overline{S} + \overline{S}.\overline{H} + \overline{N}.M.H}$$

Referring again to Figure 16, the second stage of comparison and selection is similar to the first stage but with different selection functions. The outputs of the latch 256 are applied to one input of the comparator 263 and to one input of a selector 264. The outputs of the selector 264 are applied to a latch 265, the outputs of which are applied to the second inputs of the comparator 263 and the selector 264 respectively. Similarly for the colour bits C, the outputs of the latch 264 are applied to one set of inputs of a selector 266, the outputs of which are connected to a latch 267. The outputs of the latch 267 are connected to the second inputs of the selector 266. The control functions of the selectors 264 and 266 select either the new values from the latches 256 and 260 or the old values from the latches 265 and 267, or sets the selectors 264 and 266 to all 1's when initialising. Control signals W and V for the selectors 264 and 266 are produced by the respective data networks 268 and 269 from the signals S and P in the latch 253 and the output signal I of the comparator 263, where;

I=0	New value is less than the old value
I=1	New value is greater than or equal to the old value
S=0	Boolean product operation
S=1	Boolean summation operation
P=0	Generate output, end of expression
P=1	Not the end of expression

I=0	I=1
S=0, P=0 Enter all 1's	Enter all 1's
S=0, P=1 Enter old value	Enter old value
S=1, P=1 Enter new value	Enter old value
S=1, P=0 Enter new value	Enter new value

Using the same selector for convenience:

W	V	
0	0	Select input 1, old value
0	1	Select input 2, all 1's
1	0	Select input 3, all 1's
1	1	Select input 4, new value

which gives the control functions:—

$$W = \overline{\overline{S} + I.P} \qquad V = \overline{P.\overline{S} + I.P}$$

the Karnaugh maps for which are given in Figure 20.

The final output from the processor is controlled by the signal P enabling output bus-buffers 270 and 271, which transfer the data in latches 265 and 267 on to the output buses for one clock cycle.

Figure 19 shows a control signal generation unit for providing the basic control signals need by the system shown in Figures 15 and 16. This unit generates the memory enable signals for reading and writing, the various addresses for the different blocks of memory, and the selector control signals for routing the data through the machine in the correct way. There are four sections to the control signal generation unit, namely a TV monitor control signal generator, a computer interface control, an address generator, and a selection and enable signal generator.

The unit operates at a clock frequency of 8 MHz, which allows a display to be created with a resolution of 512 points in each TV raster line scan. This frequency controls the rate of data transfers within the system, and, with the design shown in Figure 15, can only be changed by halving the frequency to 4 MHz and removing the least significant bit of the point counter 281. The exception to this rate of data transfer is the entry of data into the buffer store, which is regulated by the bus cycle pulses of the host computer which may be a PDP 11/45. The Sync signals to the TV are generated from multiples of the base frequency and are coordinated with the internal data transfers in the processor.

The main clock (not shown) drives the least significant bit of a point counter 281. Logic on the output of the point counter 281 gives the various components used in the TV control signal, and also a clock signal to increment a line counter 282. The output from the line counter 282 is passed through logic 283 which generates the Video Gate signal and the final composite Sync signal for the TV. The output of the point counter 281 is also applied in a latch 284 to the TV monitor 233.

When data is received by the buffer store it arrives in groups of six sixteen bit words from the host computer, each group defining a new plane. The number of planes received is recorded in a counter 285, and the output of this counter is selected to give the buffer store address while new data is being entered into the buffer store. Once a new set of data has been received by the buffer store the total number of planes in the set is transferred from the counter 285 to a latch 286 where it is used to control the addressing of the other blocks of memory. The addresses to the picture store and the line store are generated in a counter 287 controlled by using a comparator 288 to compare its output to the total number of planes in the picture stored in the latch 286. This counter 287 also generates the address selected to drive the buffer store when its contents are being transferred to the picture store. The point store address is generated by a separate counter 289, since if there are 'n' planes, the main address cycle used for the picture store must be 1 to n but if there are 'm' processors the point store addresses must cycle from m to n, and if $m \geqslant n$ then the point store will be bypassed.

The overall control of the data transfers is carried out by the action of a shift register 290 in the interface control section. This shift register 290 can represent four states. The first is when the machine is displaying its current data from the picture store but is ready to receive data from the host computer. The second state is, while still displaying the current picture, when the new data values are being transferred into the buffer store. The third state is entered when this transfer is complete and the control is waiting to transfer the data in the buffer store across to the picture store for display, which can only be initiated at the beginning of a new TV scan. The interlace frame is treated as a refresh picture so the maximum rate at which new pictures can be displayed is once every twenty fifth of a second. The final stage is when the buffer store is providing data for display and transferring it into the picture store for future display. Once this transfer is complete then the machine changes back into the initial state where it is ready to receive new data.

The enable signals to the different memory units control the reading cycle of the memory. The outputs of a shift register 291 control the sixteen bits of memory receiving each new word from the host computer. The read enable signals to the other blocks of memory are generated by a group of latches 292 linked as shift registers. This arrangement allows the control signals to be offset to match the offset caused by the way the incrementing operation is pipelined in the processor bank. Also passing through these latches are the selection control signals which govern the flow of data through the selectors 218, 219, 220, 222, 223, 224, 225, 226, 229, 230 and 231 shown in Figure 15.

In order to determine whether the increment to be added to a depth value to obtain the next depth value is to be dx or dy in a pipelined incrementing unit, it is necessary to provide two lines which pass through all the incrementing units of the incrementing circuit and present the same information to each at the same time. The values on these lines determine whether the increment is to be dx or dy and whether this increment is to be added or subtracted to the previous depth value. The appropriate increment is latched into an incrementing unit which currently holds the end of expression marker, and so defines the next point which is to be processed by the incrementing unit. The processor need not be limited to four incrementing directions obtained from the increments dx and dy. A more complex processor having three lines extending through all the incrementing units may process the points along

six directions obtained from increments dx, dy and dz or alternatively along eight directions obtained from the increments dx, dy, dx + dy and dx — dy.

The processors described with reference to Figures 1 to 19 can be used in the "cross-sectional display" mode as well as in the "projected display" mode. A simplified form of processor which can be used in the "cross-sectional display" mode only is illustrated schematically in Figure 20 and the display of a scene represented by the boolean expression A.B.(C.D) is shown in Figure 21. In this system, the depth value is used to define the perpendicular distance from the plane to the display point rather than the perpendicular distance taken from the picture plane. Since the range of values of perpendicular distance from the display point would be less than the range of values from the perpendicular distance from the picture plane, the size of depth value which the processing system can handle may be reduced. In addition, at the comparison and selection stage, it is merely necessary to determine whether any particular point is within the cross-section to be displayed. This is evaluated by substituting into the boolean expression the truth value for each plane, i.e. 0 for outside and 1 for inside, and thence determining whether the point is true, i.e. inside, for the whole expression.

The foregoing approach allows the boolean expression structure to be evaluated as a series of logical operations on the truth values for each plane. The boolean expression defining a scene can be compacted by nesting and the use of brackets. Figure 20 illustrates a processor which can accept up to three levels of nesting which is adequate for two dimensional data, where planes are replaced by lines on the picture plane. Referring to Figure 20, the processor comprises an input unit 150 which receives each new scene description from a main computer. The data is applied therefrom to an incrementing unit 151 where the depth value of each surface is incremented to give the depth value for the next display point. The incremented values from the incrementing unit 151 are applied to a selection unit 152 which has four stages. The first stage 153 selects the associated data for the terminal elements of the tree of the boolean expression for which the values are negative. The second stage 154 selects, at the lowest level in the tree, the associated data of those elements which are true. A similar operation is performed at the next level of the tree by the next stage 155 and the associated data of the true components received from the stage 155 are selected by the final stage 156 for display.

The process illustrated in Figure 20 may be expanded to deal with an additional level, so as to be able to display three dimensional data more conveniently, by inserting an extra selection stage before the selection stage 153.

Figure 23 shows a pipelined incrementing unit for such a cross-sectional display for use with three dimensional scene descriptions. This incrementing unit comprises a store 320 for the initial depth value and respective stores 321, 322 and 323 for the three increments dx, dy and dz. In the case of such a processor for two dimensional scene descriptions only two increments are necessary. Furthermore the unit comprises an incrementing stage 324 similar to the pipelined incrementing unit already described with reference to the processor capable of being used in the projected display mode and a selection stage 325. In operation the initial depth value V which represents the distance from the plane to a reference point in a direction perpendicular to the plane is supplied to the incrementing stage together with whichever of the increments dx, dy and dz is selected by the selection stage 325. The increments dx, dy and dz define the change in the distance from the reference point perpendicular to the plane in moving from point to point on a regular grid based on the reference point. Which increment is selected depends on the direction of the next point to be processed with respect to the direction of the previous point processed in the incrementing stage 324. However, in contrast to the processor capable of being used in the projected display mode, this processor need only determine whether the vector from the point to the plane perpendicular to the plane is positive, meaning that the point is inside the plane, or negative, meaning that the point is outside the plane, with respect to a reference direction for that plane.

Figure 23 shows three levels of a four level selection circuit for selecting the points to be displayed from the boolean expression supplied to such a processor. Latches 326, 327, 328 and 329 are provided in this circuit for holding opcodes enabling the overall process to be controlled by means of the boolean expression. The selection circuit comprises further latches 330, 331, 332 and 333 for holding the depth values of the points being processed, as well as selectors 334, 335 and 336 disposed between these latches.

In operation of this selection circuit the opcodes associated with the boolean expression are supplied to the latches 326, 327, 328 and 329, each plane having a respective opcode associated with it. These opcodes serve to control the selectors 334, 335 and 336. As an example the operation of this circuit will be considered under the control of the boolean expression:

$$R + S + (A + B.C + D).E.F + G.H$$

Indicating the sign bits of a particular point with respect to each plane by the letters A, B, C, D, E, F, G, H, R and S denoting that plane, H will first be entered into the latch 330. It will then be passed directly to the following latch 331 by the selector 334 and, as the first value of a new expression, will sweep all previous values before it (due to the presence of a suitable opcode marker). The value G, which has meanwhile been entered into the latch 350, will enter the latch 331 and the value H will be

passed to the latch 332 on the next clock pulse. Similarly, on the next clock pulse, F will enter the latch 331, G will enter the latch 332 and H will enter the latch 333. At this point the opcode of G will correspond with its position in the circuit so that, when E is entered into the latch 331, F will enter into the latch 332 and the function (G.H) will enter into the latch 333. In the next clock period, F will enter into the latch 333 and the value (G.H) will be outputted to the final stage. The processing of the remainder of the expression will continue in a similar manner with the latch 331 holding the functions such as (B.C), the latch 332 holding the functions such as (A + D. .) and the latch 33 holding the functions such as (E.F. . . .). The final level (R + F + . . .) is carried out in the final stage. In the final stage the data associated with each phrase is selected and processed. If the output from the previous stage of the circuit is true this means that the point is inside the current zone being processed and the associated data is selected. There are two ways in which this selection may be done. Firstly the data associated with each new zone within which the point is found to lie may be substituted for the data associated with the previous zone in which the point has been found to lie. Alternatively, where a point is found to lie in several zones, the data associated with each of these zones may be combined in some way. For example, where a colour code is associated with each zone, the colour codes may be combined together to form zones of mixed colour.

Such a processor may be used with any level of nesting in the input expression, as long as the selection circuit includes the same number of stages as there are levels in the expression. It is convenient to provide four levels for three dimensional scenes and three levels for two dimensional scenes.

The processors described with reference to Figures 1 to 23 are capable of changing the image displayed each frame. However, in practice, there has to be some degree of coherence between frames in order to render the display intelligible. This coherence can be used to reduce the amount of computation which is necessary between one frame and the next and especially the amount of computation which is required to remove hidden regions of the scene from the display. Figure 24 illustrates two bits of two cells of a sorting circuit which may be used in a processing system utilising volume, facet or edge coherence to reduce the volume of computation or alternatively which may be used in a processing system similar to those described with reference to Figures 1 to 23 as a way of providing a packed frame store. This sorting circuit is capable of sorting a plurality of values supplied sequentially to the input of the circuit and of outputting these values sequentially with the smallest value being outputted first, the next smallest value being outputted second and so on, the last value to be outputted being the largest value. Such a sorting circuit may be termed a "smallest-out-first" sorting circuit. A "largest-out-first" sorting circuit, that is a circuit which sorts the values and outputs them in order of descending value, may be produced by a simple modification of the circuit of Figure 24. Whilst only two bits of two cells of a sorting circuit are shown in Figure 20, the circuit will in practice comprise as many cells as are necessary to sort the values, each cell comprising as many bits as there are bits in the largest value to be sorted.

Considering cell *a* shown in Figure 24, the elements 300, 301, 302, 303, 304 and 305 are each one-bit latches. The elements 306 and 307 are combinational logic elements which will be described in more detail below with reference to Figure 25. The operation of the cell is as follows. The first value of a set of values to be sorted is entered into the latches 302, 303 and at the same time a 1 is inserted into the latch 304. The presence of the 1 in the latch 304 causes the elements 306, 307 to transfer the value in the latches 302, 303 directly to the latches 300, 301 in the next clock period. At the same time any value present in the latches 300, 301 as a result of a previous sorting process is transferred to the latches 308, 309 of the cell *b*. Furthermore the value 1 in the latch 304 is transferred to the latch 305, and a second value is entered into the latches 302, 303. the value in the latch 304 will be 0 and therefore, in the next clock period, the value in the latches 302, 303 will only be transferred to the latches 300, 301 if it is greater than the value already in those latches, that is the first value entered into the circuit. If it is not greater than that value, the second value is passed to the latches 308, 309 of the cell *b*. If the second value replaces the first value in the latches 300, 301, the first value is passed to the latches 308, 309 of the cell *b*. At the same time the 1 in the latch 305 is passed to the latch 310 of the cell *b* so as to serve in a similar manner to previously to ensure that the values of the new set being sorted are not mixed up with the values of the set previously being sorted. It will thus be appreciated that, due to the comparison, selection and switching operation of the elements 306, 307 and the corresponding elements of the following cells, the values of the set will gradually be sorted as they progress through the circuit with the smallest value finally being outputted first at the output of the final cell of the circuit. Furthermore as the values of this set progress through the circuit they will automatically sweep the values of the previous set before them. Such a sorting circuit is therefore capable or ordering the values of a plurality of sets of values sequentially with the values of each set themselves being outputted sequentially. The comparison, selection and switching elements 306, 307 will now be described in more detail. Again it will be appreciated that each cell will comprise further elements similar to the elements 306, 307 for comparing the higher order bits of the values to be compared. In use of these elements to compare the value A from the latches such as 300, 301 and the new value B from the latches such as 302, 303 the most significant bit of each value will first be compared. If the most significant bit of B is greater than the most significant bit

of A, then the new value B will be transferred to the latches such as 300, 301 and the value A will be passed to the next cell, and it is not necessary to compare the other bits of these values. Similarly, if the most significant bit of A is greater than the most significant bit of B, the new value B will be passed to the next cell and it is not necessary to compare the other bits of these values. However, if the most significant bits of these two values are the same, a carry bit will be compared. Again, if one of the bits is greater or less than the other, the selection and switching operation will be enabled and it is not necessary to compare any further bits. However, if these bits are the same, a carry bit will be supplied to the element for comparing the next most significant bits and these bits will be compared. This process continues for as long as is necessary to determine which of the two values is the greater. It will be noted that the carry is in the opposite direction to the carry in a normal addition operation.

Considering the bit 1 element of Figure 25 (which has been shown as though it is the element of the most significant bit of the values to be compared), the value A is supplied to a NOR gate 311 by way of a NOR gate 313 and directly to a NOR gate 312, and the value B is supplied to the NOR gate 312 by way of a NOR gate 314 and directly to the NOR gate 311. Assuming that CO has the value O the value of A will be outputted at B′ and the value of B will be outputted at A′ where B is greater than A. Alternatively where A is greater than B the value of B will be outputted at B′ and the value of A will be outputted at A′. Where the values of A and B are the same a further NOR gate 315 will supply a carry bit C1 to the element of the next most significant bit (bit 0) so as to initiate comparison of the next most significant bits. Where the value of CO is 1 when a new set of values is being entered into the circuit, the value of A will be outputted at A′ and the value of B will be outputted at B′, that is the element will act as though A is greater than B, even though this may not actually be the case.

The operation of such a comparison, selection and switching element may be summarised as follows:—

$$A' = \overline{B + (\overline{A + C})}$$

$$B' = \overline{A + (\overline{B + C})}$$

$$C' = C + (\overline{A + B})$$

where C is the carry from the preceding element and C′ is the carry to the next element.

In order to produce a largest-out-first sorting circuit a similar circuit to that described with reference to Figures 24 and 25 may be used except that inverters must be provided on each of the B inputs and each of the B′ outputs so that the value B is inverted to produce a value $D = \overline{B}$ and the value B′ is produced by inverting a value D′ so that $B' = \overline{D}'$. The operation of this circuit can then be summarised as follows:—

$$A' = \overline{D + (\overline{A + C})}$$

$$D' = \overline{A + (\overline{D + C})}$$

$$C' = C + (\overline{A + D})$$

Whichever sorting circuit is used n-1 cells are required to order n numbers. Furthermore there is a latent period between entering the first value of a set into the circuit and obtaining the value of that set which is outputted first at the output of the circuit, in view of the fact that the set has to work its way through the circuit. However, once the values start to emerge at the output, they do so one each clock period. It is this ability to maintain a steady flow of data which makes this circuit particularly useful in a display processor.

CLAIMS

1. A processor for producing an output capable of generating an image of a scene on a raster scan display, which scene comprises one or more regions each enclosed by a respective set of planes defined by a boolean expression relating the planes of the set one to another, the processor being adapted to determine what is to be shown in each part of the display from a depth value indicative of the distance of each plane from the display screen, first and second increment values respectively indicative of the depth value change between two raster points in two mutually non-parallel directions, and a property code indicative of whether the plane is a front surface or a back surface of the image and of the position of the plane in the boolean expression of the set of planes including that plane.

2. A processor according to claim 1, wherein incrementing means are provided for determining the depth values of the plane at a plurality of points on the display from the depth value at a reference point and the first and second increment values.

3. A processor according to claim 1 or 2, wherein selecting means are provided for determining

the front plane having the maximum depth value at a point and the back plane having the minimum depth value at that point and for comparing the depth value of the front plane having the maximum depth at that point with the depth value of the back plane having the minimum depth value at that point, so as to identify a possible visible surface at that point.

4. A processor according to claim 3, wherein the selecting means is further adapted to compare the depth value of the front plane having the maximum depth value at that point for a first set of planes with the depth value of the front plane having the maximum depth value at that point for a second set of planes, so as to identify a possible visible surface which is hidden at that point.

5. A processor according to claim 2 and 3, wherein the incrementing means comprises a plurality of incrementing units disposed in parallel for determining, for each plane in turn, the depth values of the plane at a plurality of points, and the selecting means comprises a plurality of selecting circuits each provided for comparing the depth values of the various planes obtained from a respective one of the incrementing units.

6. A processor according to claim 2 and 3, wherein the incrementing means comprises a plurality of incrementing circuits, each provided for determining, for each point in turn, the depth value of a respective plane at that point, and the selecting means comprises a plurality of selecting units disposed in parallel for comparing, for each point in turn, the depth values of the various planes at that point obtained from the incrementing circuits.

7. A processor according to claim 5, wherein each incrementing unit comprises adding means for determining the depth value of the plane at each point other than the first from the depth value of the plane at the preceding point and either the first or second increment value, whereby the depth values are produced sequentially.

8. A processor according to claim 5, wherein each incrementing unit comprises a plurality of adders and a corresponding plurality of subtractors for adding and subtracting the first and second increment values and multiples of those values to and from a reference value to simultaneously produce the depth values of the plane at a plurality of evenly spaced points.

9. A processor according to claim 5, 7 or 8, wherein each selecting circuit comprises first means for holding an intermediate value, second means for holding a new depth value, and comparison means for comparing the new depth value to the intermediate value and replacing the intermediate value or maintaining the intermediate value in the first means, in accordance with the result of the comparison.

10. A processor according to claim 9, wherein each selecting circuit further comprises means for determining whether the criteria for the replacement of the intermediate value in the first means by the new depth value is to be that the latter is greater than the former or that the latter is less than the former, in dependence on whether the plane is a front surface or a back surface of the image as indicated by the property code.

11. A processor according to claim 9 or 10, wherein each selecting circuit also comprises third means for holding a previous intermediate value obtained from a comparison of the depth values of all the planes of a previous set at a point and further comparison means for comparing a new intermediate value obtained from a comparison of the depth values of all the planes of a new set at that point to the previous intermediate value and replacing the previous intermediate value in the third means by the new intermediate value or maintaining the previous intermediate value in the third means, in accordance with the result of the comparison.

12. A processor according to claim 9, 10 or 11, wherein means are provided for ordering the data concerning the various planes so that the data concerning the front planes is supplied to the incrementing means prior to the data concerning the back planes.

13. A processor according to claim 6, wherein the selecting units are arranged such that, whilst one unit is processing the data concerning its associated plane at a particular point, another unit is processing the data concerning its associated plane at the next following point and a third unit is processing the data concerning its associated plane at the previous point.

14. A processor according to claim 13, wherein each selecting unit comprises first means for holding an intermediate value, second means for holding a new depth value, and comparison means for comparing the new depth value to the intermediate value and transferring either the new depth value or the intermediate value to the first means of the selecting unit associated with the next following point, in accordance with the result of the comparison.

15. A processor according to claim 6, wherein the selecting units are interconnected by a maximum comparison bus and a minimum comparison bus, and each unit incorporates maximum generation means, minimum generation means and control means, the arrangement being such that, when the plane is a front plane, the depth value is compared to an intermediate maximum value on the maximum comparison bus and is substituted for the intermediate maximum value if it is greater than that value, and, when the plane is a back plane, the depth value is compared to an intermediate minimum value on the minimum comparison bus and is substituted for the intermediate minimum value if it is less than that value.

16. A processor according to claim 15, wherein the selecting units are interconnected by a third bus, and each unit incorporates means for comparing the depth values for the back planes with the

maximum value for the various planes on the maximum comparison bus and for applying a signal to indicate that there is no visible surface at that point when a depth value is less than said maximum value.

17. A processor according to claim 6 or any one of claims 13 to 16, wherein each incrementing circuit comprises means for storing the initial depth value of the associated plane at the beginning of the raster scan, the first and second increment values, the property code and the incremented depth value obtained by moving along a raster line, and adding means for determining the depth value at each point from the stored values.

18. A processor according to claim 17, wherein each incrementing circuit further comprises means for storing the incremented depth value at the beginning of the current raster line.

19. A processor according to any preceding claim adapted to generate an image in the form of a projection of a three-dimensional scene on the display screen, except where the scene intercepts the screen, when a cross-section through the intercepting portion of the scene is shown.

20. A processor according to claim 1, adapted to generate an image in the form of a cross-section through a three-dimensional scene, wherein means are provided for determining whether the vector from a point to a plane perpendicular to the plane is positive or negative with respect to a reference direction for that plane, so as to determine whether the point is inside or outside the plane.

21. A processor according to claim 20, wherein a selecting circuit is provided comprising a plurality of selecting units arranged in series, each selecting unit comprising a respective first latch for containing an opcode determined by the boolean expression, a respective second latch for containing a value indicative of whether a point is inside or outside one or more planes, and a respective selector for either replacing the value in the associated second latch with a new value or replacing the value in the associated second latch with a function of that value and the new value, in dependence on the value in the first latch.

22. A processor substantially as hereinbefore described with reference to Figures 1 to 23 of the accompanying drawings.

23. A circuit for sorting a set of values into ascending or descending order, which circuit comprises a plurality of cells arranged in series, each cell including latch means for holding one of said values, and comparison means for comparing a new value entered into the cell to said one value and either replacing said one value in the latch means by the new value and outputting said one value from the cell or maintaining said one value in the latch means and outputting the new value from the cell, in accordance with result of the comparison, whereby the ordered values are outputted sequentially from the last cell of the circuit.

24. A circuit according to claim 23, wherein the comparison means of each cell includes a respective element for comparing each bit of the new value with the corresponding bit of said one value, the comparison means being arranged to compare the most significant bits of these values first.

25. A circuit according to claim 24, wherein the elements of the comparison means include carry means for initiating comparison of the next most significant bits of the new value and said one value where the result of the previous comparison is that the bits compared are equal.

26. A circuit according to claim 23 or 24, wherein the comparison means includes selection means for supplying the new value and said one value to their new locations when the result of a comparison indicates that the compared bits are not equal and in accordance with the result of the comparison.

27. A circuit for sorting a set of values into ascending or descending order, which circuit is substantially as hereinbefore described with reference to Figures 24 and 25 of the accompanying drawings.

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