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Europäisches Patentamt
European Patent Office
Office européen des brevets

11

Publication number:

**0 228 745
A2**

12

EUROPEAN PATENT APPLICATION

21

Application number: **86202315.7**

51

Int. Cl. 4: **G09G 1/16**

22

Date of filing: **18.12.86**

30

Priority: **30.12.85 US 815361**

43

Date of publication of application:
15.07.87 Bulletin 87/29

84

Designated Contracting States:
DE FR GB

71

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Raster scan video controller provided with an update cache, update cache for use in such video controller, and CRT display station comprising such controller.

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A raster scan video controller is provided with an update cache for selective updating of a display memory under control of an updating device. The display has a larger bit width than the updating device. The update cache is full-width connected to the display memory. Each display memory connection is paired to a corresponding connection to the updating device. The updating device has random-access facility to the update cache for accessing only a selective part thereof for receiving, transmitting and latching data with respect to the update cache. Corresponding functions are available with respect to the memory.

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Raster scan video controller provided with an update cache, update cache for use in such video controller, and CRT display station comprising such controller.

BACKGROUND TO THE INVENTION:

The invention relates to a raster scan video controller. In particular, such video controllers are used in bit-mapped alphanumeric and or graphic image processing. In particular, the invention is directed to the control logic and to circuits necessary to overcome a mismatch between the number of data lines in display memory and the number of data lines on a raster scan video controller. The invention is useful for high performance CRT systems, black/white or color, especially those capable of accessing display memory to create and update an image on a video display.

An update data cache is a mechanism by which a CRT controller with a smaller number of data lines can update a display memory with a larger number of data lines. Especially, in high performance color CRT systems, the multiple bits accessed in a display memory cycle can be quite large both because the pixel rate is much faster than the memory time and because each pixel may be represented by a multiplicity of bits. This multiplicity is determined both by the number of bits of an actually displayed pixel, and by the number of pixels that can be displayed on a particular screen position. The latter number may relate to multiple windowing features, hidden objects in a graphics system, and others.

DESCRIPTION OF THE PRIOR ART:

Most presently available video display systems typically include a processor, a video controller, a display memory containing a single current screen image, other system memory, and a raster scan video display. In normal (steady-state) operation, the video controller continually reads out the contents of the display memory and transforms the information read out to the signalling necessary to control the raster scan beam while it is in its active display time. The video controller also provides the horizontal and vertical retrace signalling at appropriate intervals, and blanking of the raster scan beam during retrace.

The processor also has access to the display memory, so that it can change the current screen image. This access may be "through" the video controller or "around" it. The invention applies to the former type of system. In either case, use of the display memory is typically carefully controlled between updating and display accesses, to prevent breakup of the video image while it is being changed.

Depending on the timing of the various parts of the system, the display memory may be available for updating a) only during vertical retrace periods, or b) during both horizontal and vertical retrace periods, or c) during retrace periods plus alternating memory cycles during the active display time of scan lines. In any of these cases, however, updating of display memory typically proceeds at a rate slower than could be achieved without interference from the video controller's display accesses because of the time division among both access types.

With high performance color CRT systems, the number of bits accessed in display memory cycles can be quite large. All CRT controllers are pin constrained to a limited number of data bits by means of which they update or change the memory. This invention provides a mechanism by which a CRT controller with a smaller number of data lines, for example 16, can update a display memory with a larger number of data lines, for example 128. Alternatives to this would include limiting the display access to the number of data lines on the CRT controller, for a low performing system; employing a large number of data pins on the CRT controller, which drastically increases its cost; paralleling several CRT controllers, which is complex and expensive; or addressing memory differently in video versus update accesses, which causes a serious software problem.

Another object of the present invention is to improve performance because the update and video operations can occur simultaneously in many cases.

SUMMARY OF THE INVENTION:

The improved video controller according to the invention is recited in Claim 1. The invention also relates to an update cache for use in such improved video controller. Various advantageous aspects are recited in the dependent Claims. The improved video controller incorporating the present invention has two types of chips, to wit, an address module and at least one data module. The chip set, known as BMAP, is designed to work with an external processor which generates the instructions for the set. The major function of the address module is to generate both video addresses and update addresses, while the data modules are used to collect and integrate video data that had been read out from the display memory. The video data output from the data module passes through high speed shift registers and a look-up table to the CRT display. The major parts of the address module are a synchronous signal generator, a window controller, an update controller and an interface controller. The address module also has the ability to update the contents of the display memory according to instructions passed from the host system. Thus, the host system does not have to access display memory when it wants to insert some characters or graphic elements into display memory. It only passes the appropriate instructions and/or data to the BMAP.

The structure of the display memory is related to the operating frequency of the CRT controller and the complexity of the system. This can result in a mismatch in data width between the video controller, display memory and the host system.

The invention provides an update cache for selective updating of a memory in a computer system wherein the data width of the memory is greater than the data width of the devices performing or controlling the updating. Such a system usually includes one or more updating devices each having a number of signal connections on which they read and write data. For high-performance memories, this number can be less than the number of signals provided by the memory. The invention provides a set of transceivers provided with register storage for each updating device, such transceivers hereinafter being called registered transceivers. Each transceiver has a number of paired data signal connections, and each has control inputs which control the driving, receiving and latching of the states of these data signals. The total number of pairs in the set is greater than or equal to the number of data signals provided by the memory. A set of data lines connect each data signal of the memory to one and only one data signal connection in each set of registered transceivers, such that each registered transceiver treats all of its memory data signals identically in response to its control inputs. Another set of data lines connects each data signal of each updating device to a data signal of one or more registered transceivers in its set. Each pair which has one data signal connected to a memory signal has the other data signal of the pair connected to one and only one data signal of its updating device. The control logic provides the appropriate control signals to select any of a number of subsets of the set of registered transceivers associated with an updating device, each subset having a number of data signal pairs that is less than or equal to the number of data signals provided by the updating device. For each update access, the address module provides an address for the memory and the control signals to transfer data from memory to the set of registered transceivers or from the set of the registered transceivers to the memory. Control signals are also provided to control the transfer of data from an updating device to a selected subset of its registered transceivers or from the selected subset to the updating device. The control signals further provide the ability to latch data from an updating device in a selected subset of its registered transceivers. The control logic further provides for the simultaneous execution of a video access and a transfer between the updating device and the selected subset, where necessary and convenient.

Basically the invention uses of a set of bidirectional registered transceivers plus the logic and signals to control them. The interface controller of the address module contains the logic and directs the distribution of control signals. The registered transceivers are placed between the data lines of the display memory and the data lines used for update accesses by the CRT controller or the host processor. For memory updating, the video controller (BMAP) can read the display memory, in a fashion similar to a normal video access and latch a whole block of data into the registered transceivers. It can then modify the data word by word. After all the modifications are completed, it can use a write cycle to write the (wholly or partially) updated data from the registered transceivers back to the display memory. Random accesses related to the updating process can be done without changing the latched data. The transceivers/registers function as a data cache, with write operation being handled in a write-back fashion.

The registered transceivers are logically grouped according to their width vs. the width of the data accesses. The total number of devices used is determined by the display memory access width. With BMAP, update accesses are 16 bits, so octal devices are paired, one pair being selected on any given update access.

For high performance systems, if video and update operations can be overlapped in time, this increases the memory update speed. By using the external transceivers/registers video accesses can be overlapped with update accesses.

With the implementation of the invention, the video controller has sufficient output signalling to allow
 5 update operations involving latched data to be carried out simultaneously with video accesses to memory.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Figure 1 is a block diagram of a bit-mapped alphanumeric and graphic display controller with which the present invention can be used.

Figure 2 is a block diagram of a sophisticated display system using the controller of Figure 1 and the present invention.

Figure 3 is a block diagram of the structure of a display memory system illustrating the present
 15 invention.

Figure 4 is a block diagram of the interface controller used with the present invention.

Figure 5 is a block diagram of the update address output controller used with the present invention.

20 DESCRIPTION OF THE PREFERRED EMBODIMENT:

The bit-mapped raster scan video (CRT) controller chip set illustrated in Figure 1, has an address module 10 and a multiple data module 12. The address module 10 has as principal subsystem a synchronous signal generator 30, an update controller 32, a window controller 40 and an interface controller
 25 34. Apart from usual connections for power (VCC, Gnd), clock (CLK) and Reset, the following synchronization connections are provided: Vertical Sync 100 (VSsync/CSync), H(orizontal) Synch 102, CBLANK/HBLANK(ing) signal 104, alternating line/vertical blank (ACLL/VBLANK) signal 106. Interface controller 34 has an attachment 108 for a system bus, and two memory interface connections 110, 112. The window controller faces the data module side, and the interface controller side, the update controller only
 30 faces the interface controller side. The multiplying of the data module 12 may be chosen according to needs and facilities. The chip set shown provides hardware support for windows in a bit-mapped alphanumeric and graphic raster scan video (CRT) display system used in a computer system having one or more main processors and is particularly advantageous for use with multi-tasking operating systems. The hardware support includes logic circuits whereby a description of a plurality of overlapping windows can be
 35 programmed into the chip set. This feature allows the CPU to maintain a multi-window bit-mapped display almost as easily as it maintains a conventional alphanumeric display.

In this specification the term "video access" is used to indicate an access that reads out the display memory contents to be displayed on the screen. The term "update access", on the other hand, indicates a memory access that is used to update the contents of the display memory. The term "update operation"
 40 refers to the transfer of information between the updating device and the registered transceivers. In the embodiment used to illustrate the present invention, each video access and update access consist of 16 to 256 bits, while an update operation always consists of a 16-bit word. Of course, more extended systems could have a minimum access width of 32 bits and an update operation also relating to 32 bits. The video access operates straightforwardly as follows. Upon presentation of the display address, the display memory
 45 (item 13 in Figure 2) will output the whole block of information stored at the display memory address. Then, either the data read out will go to data accumulator modules not shown or to shift registers 15 directly.

During an update operation that does not access data already present in the registered transceivers 14, the BMAP address module outputs a "local address" together with the display address to select a 16-bit word from the display memory. The local address is used to select the desired word from the correspond-
 50 ing video access. All 4 bits in the local address are needed when the BMAP is used in a system that has 8 bits per pixel and 32 pixels per video access. The 18 most significant bits in the pixel address represent the 18 bit video address.

Since a 16-bit word may consist of 16 one-bit pixels for a monochrome display system, and consist of 2 pixels for a system that has 8 bits per pixel, the pixel address offset can have a length that varies from 1 to
 55 4 bits. Various operating possibilities exist that are not described for brevity.

Figure 2 is a block diagram of a sophisticated system that includes an address module 10 and several data modules 12. The address module generates both video addresses and update addresses, while the data modules are used to collect and integrate the display patterns that have been read out from the display memory 13. The data output by the data module(s) then goes through the high speed shift register(s) 15 and color look-up table 17 to the video display 19.

The address module 10 also has the ability to update the contents of the display memory 13 according to the instructions passed from the host system that has one or more host processors 11 and system memory 114 (I/O has not been shown for brevity). Therefore, host processor 11 does not have to access the display memory 13 when it wants to insert some characters or graphic elements into the display memory. Instead, it only needs to pass appropriate instructions to the address module 10. To this effect, the system is provided with a data transceiver 116 for interfacing the address module to the system bus and an address transceiver 118 for interfacing address module and display memory to the system bus.

After receiving the instructions passed from the host system, the address module 10 executes them one by one just like a special purpose microprocessor. Since the whole procedure is controlled by the internal hardware, instructions can be done within a very short time. Typically the insertion speed is 5 to 50 times faster than a software procedure on the host processor.

To do a block transfer, the host processor can also use the address module 10 in the DMA/BitBlt mode. The DMA/BitBlt procedure is similar to the character insertion procedure.

The data module 12 has 32 data inputs on the side of display memory 13 and 8 data outputs on the side of shift registers 15. By setting the appropriate control inputs, one or more data modules can be used in various kinds of applications. All system that apply sequential memory access to increase the data read out speed, have to include the data module (or equivalent hardware) in the back-end.

Since the structure of the display memory 13 is related to the operating frequency of the raster scan video controller and the complexity of the system, Figure 3 shows a typical memory structure that can be used with the BMAP chip set.

For memory updating, the address module 10 can read the display memory similarly to a video access and latch the whole block of data into a set of bidirectional transceivers/registers 14. These transceivers/registers 14 (e.g. 74F646) are placed in the data path used to update the display memory, and function as an update cache for the video controller. The address module can then modify the data word by word. As the last word is modified, the address module 10 writes the updated data from the transceivers/registers 14 back to the display memory 13. "Random" update accesses can also be done without latching the data. This operation is useful when a single word (e.g., "Source" data) is needed during updating.

The number of transceivers/register devices used is determined by the display memory access width. In the embodiment described herein (BMAP) this can be from 16 to 256 bits, and four to 32 octal devices - (e.g., 74F646) are used correspondingly. The registered transceivers are logically grouped according to their width vs. the width of update operations. With BMAP, update operations are 16 bits, so the octal devices are paired, one pair being selected on any given update operation.

By using the external transceivers/registers, video access can be overlapped with the update operations. That means under certain circumstances the BMAP can do two things at once. Table 2 shows the need for registered transceivers for various applications.

Table 2

5						*		# of	
			Ave.		Memory Width			Trans/Regs.	
			Addr.	Pixel					
10		# of	Rate	freq.	non-	inter	non-	inter	
	Resolution	colors	(MHz)	(MHz)	inter.	leave	inter.	leave	
15	1024*1024	1	5.7	91	1	2	0	4	
	512 * 512	16	5.7	23	1	2	0	4	
	1024*1024	4	5.7	91	2	4	4	8	
	800 * 480	16	4.2	34	2	4	4	8	
20	1024*1024	16	5.7	91	4	8	8	16	
	800 * 480	256	4.2	34	4	8	8	16	
	1024*1024	256	5.7	91	8	16	16	32	
25									

*: Memory width is in number of 16-bit words.

30 The control logic must of course provide the control signals needed by the particular registered transceivers chosen. These may vary in detail, but basically serve to control any of the following operations:

(a) capture/latch the number of data bits in display access from display memory, and pass a selected set of the number of bits in the update operation on to the CRT controller or host processor;

(b) pass a selected set of the number of bits in the update operation from the latched data, to the CRT controller or host processor;

35 (c) capture/latch data from the CRT controller or host processor, into a selected set of the number of bits in the update operation width;

(d) pass a selected set of the number of bits in the update operation, from the CRT controller or host processor to the display memory, along with the latched data for the balance of the number of bits in the memory. The latched data could have been from previous operations of type (a) or type (c);

40 (e) pass a selected set of the number of bits in the update access, from display memory to the CRT controller or host processor, without latching them or affecting previously-latched data;

(f) optionally, pass a set of the numbers of bits in the update access, from the CRT controller or host processor to the display memory without latching them or affecting previously-latched data;

45 (g) optionally, write back the number of bits in the display access, from previously-latched data to display memory; the latched data could have been from previous operations of type (a) or type (c). (f) and (g) represent extensions to the set of functions necessary for the invention, which may or may not be provided by a particular embodiment.

50 With the optimal implementation of the invention, the video display controller has sufficient output signalling to allow update operations of type b) and c) to be carried out simultaneously with display accesses to memory. Thus, updating speed is improved if the occurrence of type b) and c) accesses are maximized. This means that update operations by the video display controller should be ordered/grouped so that several consecutive update operations fall within the same display memory access.

55 To some extent, such ordering or grouping is typical of the procedures for updating a bit-mapped video display image, but actual update operations tend to be interspersed/alternated with accesses that read information which directs the updating process. For example, virtually all bit-mapped video display controllers access information at "source" and "destination" areas of display memory, the latter represent-

ing the actual updating of the image, the former being access to information that directs the updating. To these types the BMAP adds "instruction" accesses, which also direct updating. With the invention, these interspersed accesses to other areas are handled by type e) and f) operations, in which the latched data in the registered transceivers 14 is not affected.

5 In the BMAP embodiment shown in Figure 3, control information is output by four local address lines and three status lines 52 from the interface controllers 34 which are shown in Figures 1, 4 and 5. The local address lines serve to select one pair of registered transceivers among the 2 to 16 pairs. The status lines indicate the type of access being done, video access or update operation.

In this embodiment, external logic in the form of a programmed logic array (PLA) 54 is used to transform these signals into the control signals required by the specific registered transceivers used. A decoder on the four local address lines is also required.

Regardless of the specific embodiment, the information output by the control logic must include, for each update operation;

- 1) Direction (read/write access);
- 15 2) Selection for registered transceivers 14 (local address);
- 3) For read, whether the source of data is the display memory 13 or the registered transceivers 14;
- 4) For a read from display memory 13, whether the data should be latched in the registered transceivers 14;
- 5) For a write, whether the registered transceivers 14 should output data to display memory 13; and
- 20 6) For a write, whether data from the video controller 10 should be latched in the registered transceiver 14.

Because the data is cached in a write-back rather than write-thru fashion, the control logic must include a provision to write data back to display memory at appropriate times (point 5 above). In the present embodiment this is known explicitly, when the appropriate number of low order bits (1-4) of the destination local address 50 are all ones, or when the access is the last one of a block at the destination (see left OR gate 56 in Figure 5). That a new access to display memory 13 is needed for the destination (points 3, 4 above) is also known explicitly. It is indicated when the appropriate number of low-order bits (1-4) of the destination local address 50 are all zero, or when the access is the first one of a block of data at the destination (OR gate 58 in Figure 5). A single write operation is handled by signalling both first and last, so that the block of bits of display memory width is first read. The block is then rewritten with a number of bits equal to the update operation width, bits being changed by the video display controller or host processor.

The mask register 60 in Figure 5 is programmed during system initialization, to correspond to the width of display memory 13 accesses and the number of registered transceiver pairs 14. It controls how many low order local address bits must be 1 to force a write-back, and how many low order bits must be 0 to cause a new read from display memory 13.

A generalized variation would be to include a set of latches for the display memory address (i.e. for the high order part of the update address), plus a comparator between the contents of this latch and each new address, and a single-bit flag to record whether or not the data in the registered transceivers has been updated. An algorithm of the following form can then be used to control the cache, where n is the ratio of the number of bits in the display access, divided by the number of bits in the update access.

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new_memory_address: = update_address DIV n
5   local_address: = update_address MOD n
   IF access_type .NEQ. "destination" THEN
       READ_BLOCK (new_memory_address)
10  ELSE
       IF new_memory_address .NEQ. old_memory_address THEN
           IF update_flag THEN
15             WRITE_BLOCK (old memory address)
               update_flag: = FALSE
           ENDIF
           READ_BLOCK (new_memory_address)
20           LATCH_BLOCK
               Old_memory_address: = new_memory_address
           ENDIF
25       ENDIF
       IF access_type = "WRITE" THEN
           LATCH_TRANSCEIVER (local address)
           update_flag: = TRUE
30       ELSE READ_TRANSCEIVER (local_address)
       ENDIF

```

35 INTERFACE FOR UPDATE OPERATION:

40 The update operation is controlled by an 18-bit address, supplied by the window controller of the address module, the local address and the "TYPE2" outputs. The need for the 18-bit address depends on whether the update operation requires an update access. The update controller 32 generates three kinds of operations. Two of them have to access either the display memory or the system memory. The hardware that is used to generate the local address and the "TYPE2" outputs is shown in Figure 5.

45 As shown in Figure 5, the 4-bit address port is used to output one of the local addresses stored in the PC (program counter), DC (destination counter) and SC (source counter). The 4-bit mask register 60 is used to define the address boundary for the external transceivers/registers 14. If the operation refers to the "first" word of an update access, the BMAP has to read the destination pattern from the display memory, latch the data in the transceivers/registers 14 and read the required 16 bits of the latched data.

If the update operation refers to the "last" word of an update access, the BMAP has to combine the write operation with the access that writes the whole data block from the transceivers/registers 13.

50 If the update operation is the first and the last operation to a certain update access, the BMAP performs a read-modify-write operation to the display memory 13 directly. Table 2 shows 8 kinds of access that relate to the output controllers.

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	TYPE2	Type of	Address	
	OUTPUT	Access	Port	Description
5				
	000	R-M-W	B	Intermediate Destination
		to T/R		Access
10	001	R-M-W	A,B	First Destination Access
		to Memory		
	010	R-M-W	A,B	Last Destination Access
		to memory		
15	011	R-M-W	A,B	First and Last Destination Access
		to Memory		
	100	R-M-W	A,B	Read Instruction
20		from Memory		
	101	R-M-W	A,B	Write Instruction
		to Memory		
25	110	Read	A,B	Source Pattern Access
		from Memory		
	111	Read	A,B	Vertical Resync Access
30		from Memory		

Table 2 TYPE2 Control Output

The three TYPE2 outputs are also connected with the external PLA 54, such that the corresponding
 35 DRAM 13 (display memory) and transceiver/register 14 control signals can be generated to do the update
 access. Both the "TYPE2" and "local address" outputs are qualified by the LAS* (local address strobe)
 signal and negate by the LDTACK* (local address acknowledge) signal, as in the display memory access
 cycle.

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Claims

1. A raster scan video controller provided with an update cache for selective updating of a display
 memory having a first bit width under control of an updating device having a second bit width that is smaller
 45 than said first bit width, said controller comprising
 a set of registered transceivers, each having a number of pairs of data signal connections, and each having
 control inputs controlling driving, receiving, and latching of the states of these data signal connections, such
 that the total number of pairs in the set is at least equal to the number of data signals provided by said
 memory;
 50 a plurality of data lines connecting each data signal of said memory to one and only data signal in each set
 of registered transceivers, such that each registered transceiver treats all of its memory data signal
 connections identically in response to its control inputs;
 a plurality of data lines connecting each data signal connection of the updating device, to a data signal of
 one or more registered transceivers in its set, such that each pair that has one data signal connected to a
 55 memory data signal connection has the other data signal connection of that pair connected to one and only
 data signal connection of the updating device;
 means to select any of a number of subsets of the set of registered transceivers associated with the
 updating device, each subset having a number of data signal connection pairs that is at most equal to the

number of data signal connections provided by said updating device;

means to address said memory and transfer data from said memory to a set of registered transceivers;

means to address said memory and transfer data from a set of registered transceivers to said memory;

means to transfer data from an updating device to the selected subset of its registered transceivers;

5 means to transfer data to an updating device from the selected subset of its registered transceivers;

means to latch data from an updating device in the selected subset of its registered transceivers;

means to latch data from said memory in a set of registered transceivers.

2. A controller as claimed in Claim 1 wherein the registered transceivers are replaced by a functionally-equivalent set of drivers, receivers, and latches if necessary.

10 3. A controller as claimed in Claim 1 or 2 including means to simultaneously read data from said memory and provide the selected subset of the data to an updating device, without latching the data.

4. A controller as claimed in Claim 1 or 2 including means to simultaneously read data from said memory, latch the data in a set of registered transceivers, and provide the selected subset of the data to the updating device.

15 5. A controller as claimed in Claims 1 or 2 including means to simultaneously transfer data from the updating device to the selected subset of its registered transceivers, combine that data with latched data from other transceivers of the set, address said memory and transfer said combined data to said memory.

6. A controller as claimed in Claims 1 or 2 including means to address memory and transfer data to or from it, while simultaneously transferring unrelated data between one or more updating devices and the latches of the selected subsets of their registered transceivers.

7. An update cache for use in a controller as claimed in any of Claims 1 to 6, wherein said first bit width is an integer multiple of said second bit width.

8. A CRT display station comprising a raster scan video controller as claimed in any of Claims 1 through 6, wherein said display memory has multi-pixel storage facility for each on-screen pixel location.

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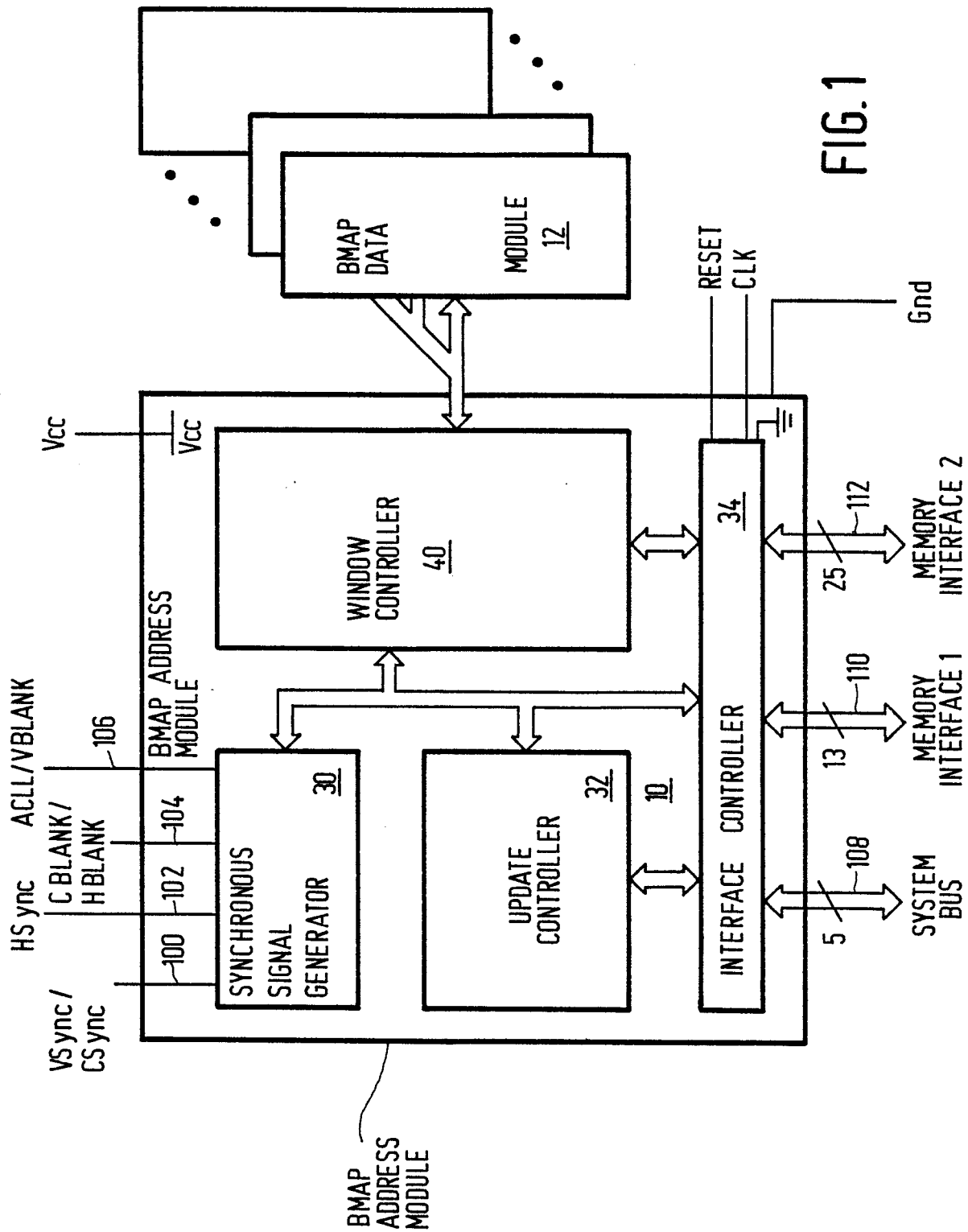


FIG. 1

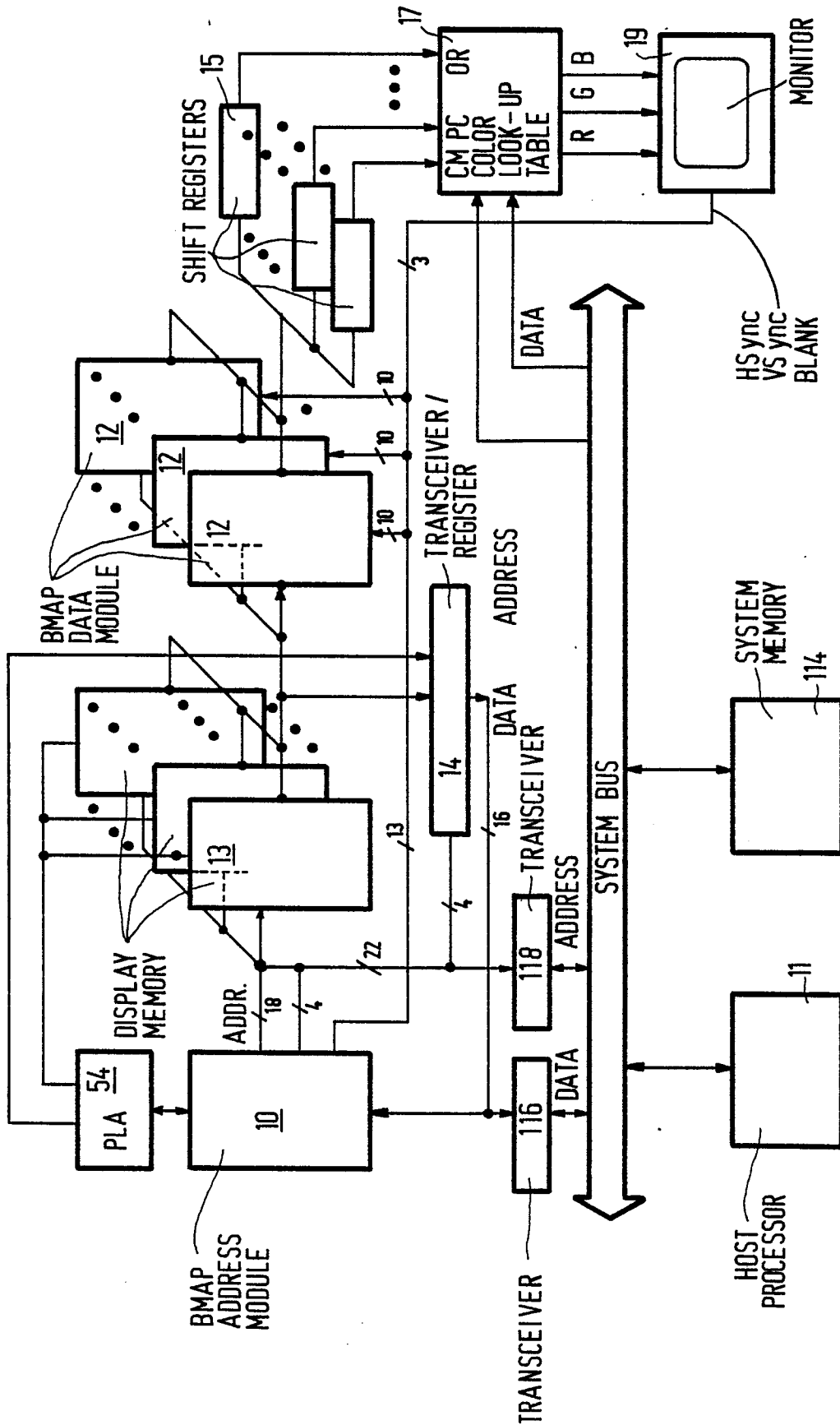


FIG. 2

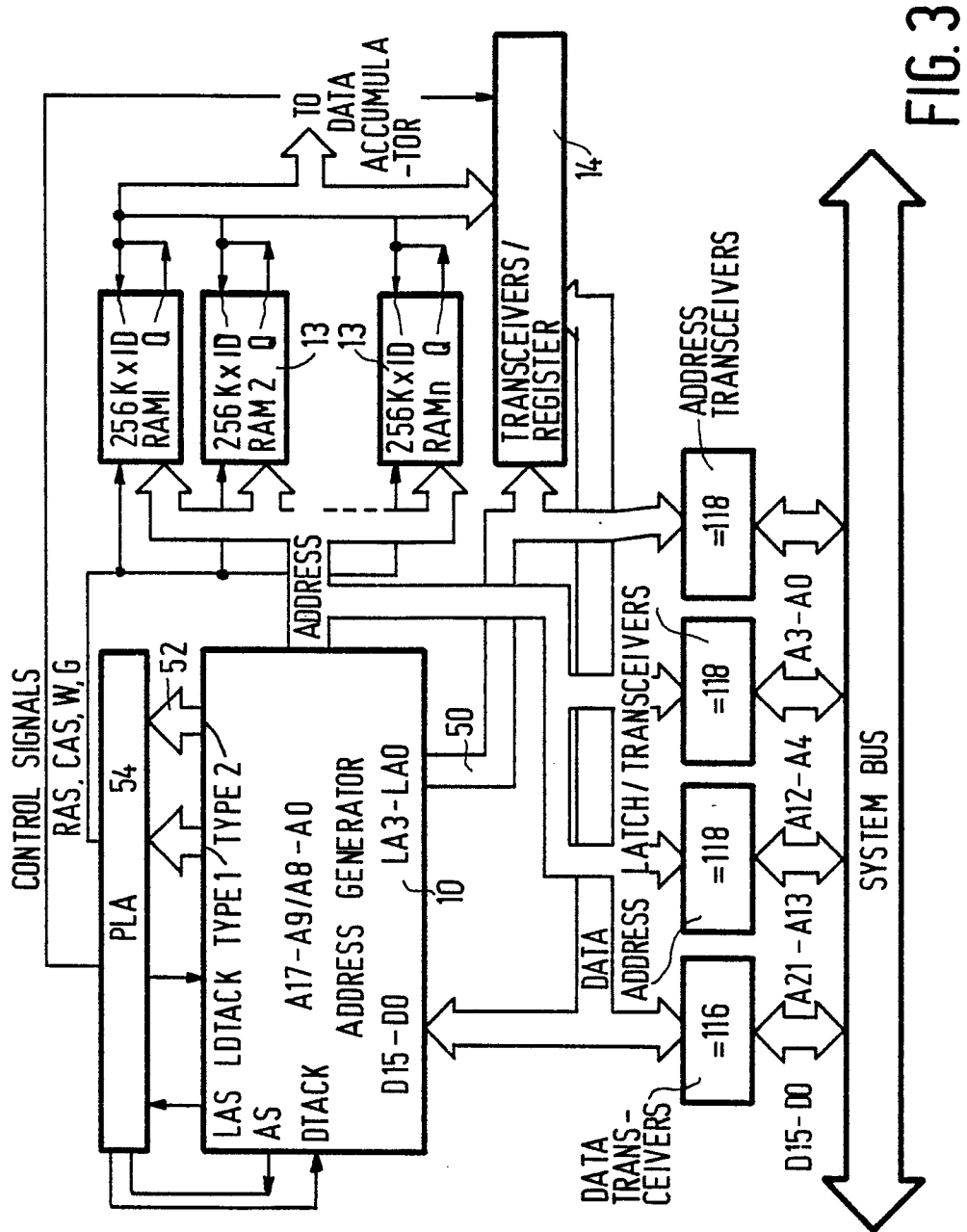


FIG. 3

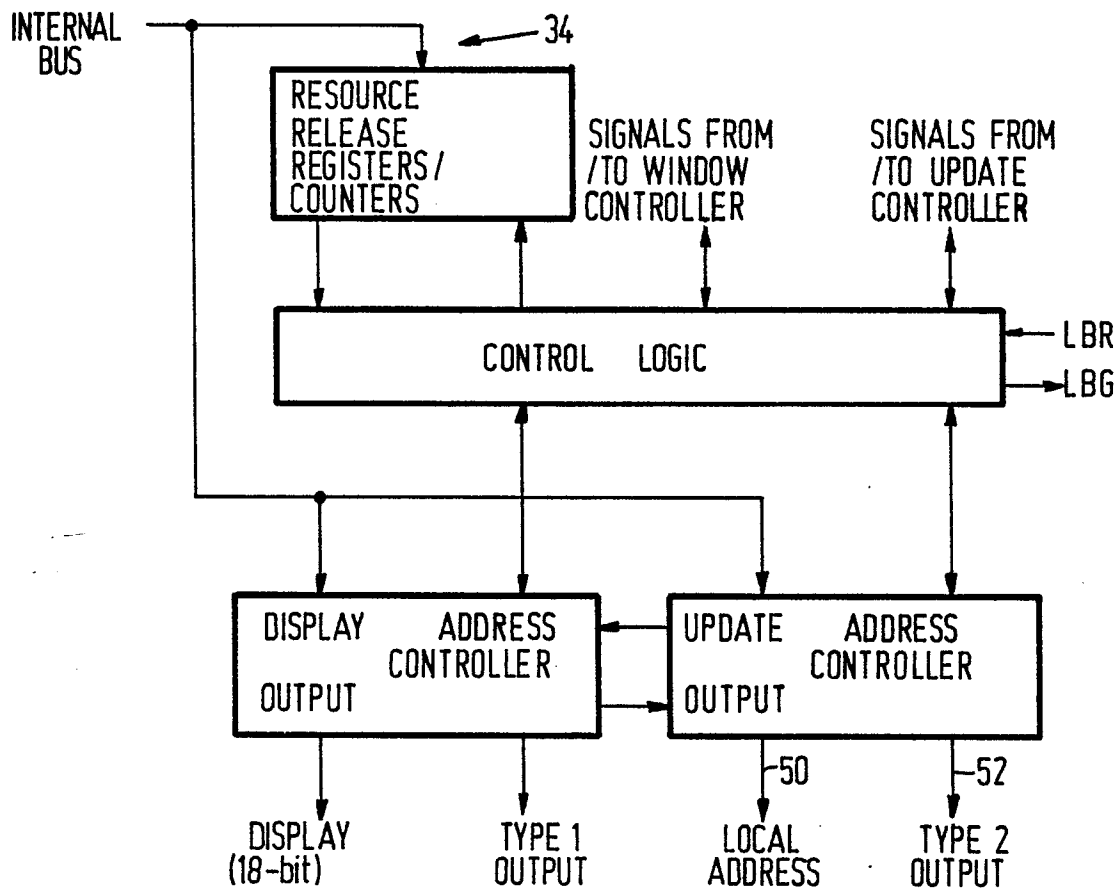


FIG. 4

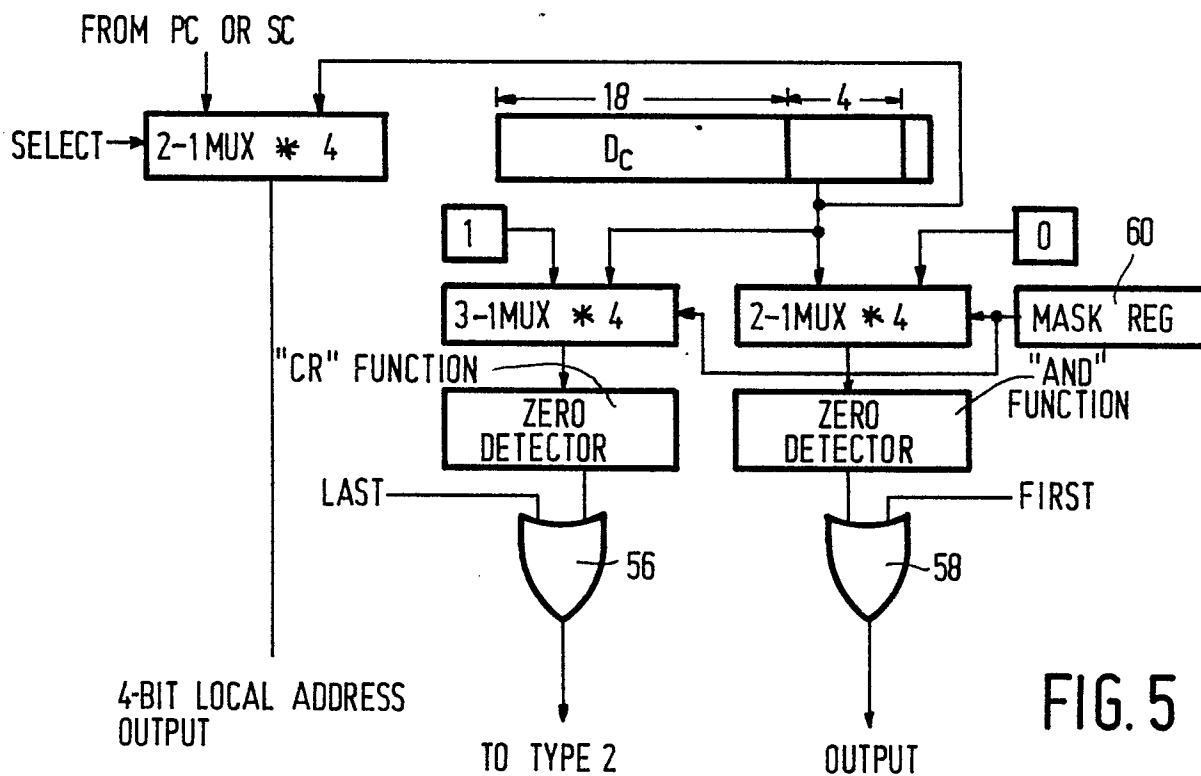


FIG. 5