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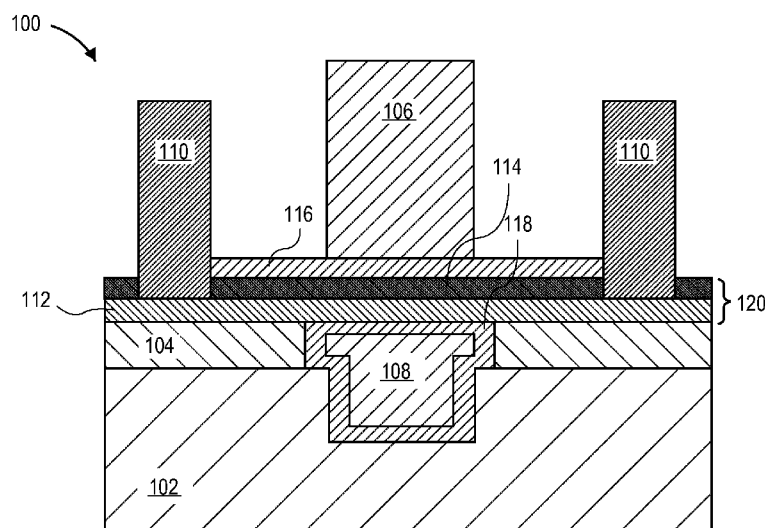


FIG. 1B

(57) Abstract: A multi-gate high electron mobility transistor (HEMT) and its methods of formation are disclosed. The multi-gate HEMT includes a substrate and an adhesion layer on top of the substrate. A channel layer is disposed on top of the adhesion layer, and a first gate electrode is disposed on top of the channel layer. The first gate electrode has a first gate dielectric layer in between the first gate electrode and the channel layer. A second gate electrode is embedded within the substrate and beneath the channel layer. The second gate electrode has a second gate dielectric layer completely surrounding the second gate electrode. A pair of source and drain contacts are disposed on opposite sides of the first gate electrode.

MULTI-GATE HIGH ELECTRON MOBILITY TRANSISTORS AND METHODS OF FABRICATION

TECHNICAL FIELD

[0001] Embodiments of the present invention relate generally to semiconductor transistors and their methods of fabrication. More particularly, embodiments of the present invention relate to multi-gate high electron mobility transistors (HEMT) and their methods of fabrication.

BACKGROUND

[0002] Compound nitride semiconductors, such as III-V semiconductors, are gaining popularity as promising alternatives or complements beyond silicon due to their large band gap electrical properties. Using large band gap materials in semiconductor technology yields semiconductor devices with high breakdown voltages and high electron mobility. Conventional devices utilizing wide band gap semiconductors are formed with a planar semiconductor structure including a single gate electrode and a pair of source and drain regions. In order to fabricate conventional planar wide band gap transistors, thick buffer layers of III-V semiconductor material are initially formed on a bulk substrate to minimize threading dislocation defects. Practically speaking, growing thick buffer layers can be costly and time consuming, thereby limiting flexibility in the design process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIGS. 1A-1B illustrate cross-sectional views of multi-gate HEMTs, in accordance with an embodiment of the invention.

[0004] FIGS. 2A-2J illustrate cross-sectional views of a method of forming an enhancement mode multi-gate HEMT, in accordance with an embodiment of the invention.

[0005] FIGS. 2K-2M illustrate cross-sectional views of a method of forming a depletion mode multi-gate HEMT as continued from FIG. 2G-1, in accordance with an embodiment of the invention.

[0006] FIG. 3 illustrates an interposer implementing one or more embodiments of the invention.

[0007] FIG. 4 illustrates a computing device built in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

[0001] Multi-gate HEMTs and their methods of fabrication are disclosed. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0008] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0009] Embodiments of the invention are directed to multi-gate HEMTs and their methods of fabrication. In an embodiment, a multi-gate HEMT includes a channel layer disposed on top of a substrate. A first gate electrode is disposed above the channel layer and a second gate electrode is disposed beneath the channel layer. On opposite sides of the first and second gate electrodes are source and drain contacts. In embodiments, the first and second gate electrodes control current flow from above and below the channel layer, respectively. Therefore, the multi-gate HEMT has maximum control of the current flow.

[0010] FIG. 1A illustrates a cross-sectional view of a multi-gate HEMT 100, in accordance with an embodiment of the invention. In an embodiment, the multi-gate HEMT 100 is formed on a carrier substrate 102. The carrier substrate 102 may be formed of any suitable substrate for semiconductor fabrication, such as a bulk monocrystalline silicon substrate. An adhesion layer 104 is formed on top of the carrier substrate 102. The adhesion layer 104 may be used to attach the carrier substrate 102 to another substrate as will be discussed below. Any suitable adhesive material, such as silicon dioxide (SiO_2) or aluminum oxide (Al_2O_3), may be used to form the adhesion layer 104.

[0011] As shown in FIG. 1A, a channel layer 120 is disposed on the adhesion layer 104. In an embodiment, the channel layer 120 is a heterogeneous structure that includes a polar semiconductor

layer 114 and a polarization layer 112. In embodiments, the polar semiconductor layer 114 is disposed directly on top of the polarization layer 112. The polar semiconductor layer 114 may be formed of a wide band gap +c polar semiconductor material, such as, but not limited to, gallium nitride (GaN) or indium gallium nitride (InGaN). In embodiments, the polarization layer 112 is formed of any suitable material that induces a two dimensional electron gas (2DEG) when disposed directly adjacent to the polar semiconductor layer 114. For instance, the polarization layer 112 may be formed of aluminum gallium nitride (AlGaN), aluminum indium nitride (AlInN), or aluminum nitride (AlN).

[0012] In an embodiment of the invention, the multi-gate HEMT 100 has two gate electrodes: a first gate electrode 106 and a second gate electrode 108. The first gate electrode 106 may be disposed above the channel layer 120 and the second gate electrode 108 may be disposed beneath the channel layer 120. In an embodiment, the second gate electrode is disposed beneath the polar semiconductor layer 114. In an embodiment, the second gate electrode 108 is further disposed beneath the polarization layer 112. As shown in FIG. 1A, the second gate electrode 108 may be vertically aligned with the first gate electrode 106. Having two gate electrodes allows a gate voltage to be applied to the top and bottom surfaces of the polar semiconductor layer 114. As such, the multi-gate HEMT 100 has maximum control of the current that flows through the polar semiconductor layer 114. The first and second gate electrodes 106 and 108 may be formed of a conductive material typically used for gate electrodes. In an embodiment, the conductive material is a metal. In a particular embodiment, the conductive material is formed of nickel (Ni), titanium nitride (TiN), platinum (Pt), or tungsten (W).

[0013] The multi-gate HEMT 100 also includes two gate dielectric layers. A first gate dielectric layer 116 may be disposed between the polar semiconductor layer 114 and the first gate electrode 106. A second gate dielectric layer 118 may be disposed around a circumference of the second gate electrode 108. In an embodiment, the second gate dielectric layer 118 completely encloses the second gate electrode 108. The first and second gate dielectric layers 116 and 118 may be formed of an insulating material such as, but not limited to, silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material.

[0014] The multi-gate HEMT includes source and drain contacts formed on opposite sides of the first and second gate electrodes 106 and 108. In embodiments, source and drain contacts 110 are disposed over the carrier substrate 102 and on top of the channel layer 120. The source and drain contacts 110 are positioned to be electrically coupled to the channel layer 120. In an embodiment,

the source and drain contacts 110 are disposed directly on top of the polarization layer 112. Any suitable conductive material may be used to form the source and drain contacts 110. In embodiments, the source and drain contacts 110 are epitaxial semiconductor structures formed of n-doped GaN, InGaN, or indium nitride (InN).

[0015] In the embodiment depicted in FIG. 1A, the multi-gate HEMT 100 is an enhancement mode multi-gate HEMT. The enhancement mode multi-gate HEMT 100 has the polar semiconductor layer 114 disposed between the first and second gate electrodes 106 and 108. In this embodiment, the polarization layer 112 is not disposed between the first and second gate electrodes 106 and 108. Absence of the polarization layer 112 between the first and second gate electrodes 106 and 108 prevents formation of a 2DEG between the first and second gate electrodes 106 and 108. As such, the enhancement mode multi-gate HEMT 100 does not have a 2DEG between the first and second gate electrodes 106 and 108. In this embodiment, the polar semiconductor layer 114 is effectively the channel layer 120. The polar semiconductor layer 114 may be formed of a wide band gap semiconductor material, such as GaN or InGaN.

[0016] To operate the enhancement mode multi-gate HEMT 100, a gate bias is applied to the first and second gate electrodes 106 and 108 to induce an accumulation of electrons within the polar semiconductor layer 114. The accumulation of electrons forms an inversion layer within the polar semiconductor layer 114. The inversion layer allows current to flow through the polar semiconductor layer 114 between the source and drain contacts 110. Accordingly, applying the gate bias turns ON the enhancement mode multi-gate HEMT 100. However, if no gate bias is applied, the enhancement mode multi-gate HEMT 100 does not induce an inversion layer within the polar semiconductor layer 114. Without an inversion layer, no current flows through the polar semiconductor layer 114 and the enhancement mode multi-gate HEMT 100 is therefore OFF. According to embodiments of the invention, applying the gate bias to the first and second gate electrodes 106 and 108 controls the channel layer 120 from above and below the polar semiconductor layer 114. Therefore, the enhancement mode multi-gate HEMT 100 has maximum control of the current that flows through the polar semiconductor layer 114.

[0017] In an alternative embodiment, as depicted in FIG. 1B, a depletion mode multi-gate HEMT is illustrated. The depletion mode multi-gate HEMT 100 has both the polar semiconductor layer 114 and the polarization layer 112 disposed between the first and second gate electrodes 106 and 108. Interactions between the polar semiconductor layer 114 and the polarization layer 112 create a two-dimensional electron gas (2DEG) at an interface between the polar semiconductor layer 114 and

the polarization layer 112. In embodiments, the mere presence of the polarization layer 112 forms the 2DEG at the interface. In an embodiment, the 2DEG is induced at a distance of 1-2 nm away from the interface and within the polar semiconductor layer 114. In an embodiment, the polar semiconductor layer 114 is formed of a wide band gap +c polar semiconductor material. In a particular embodiment, the polar semiconductor layer 114 is formed of GaN or InGaN. The polarization layer 112 may be formed of any suitable material that induces a 2DEG when disposed directly adjacent to the polar semiconductor layer 114. For instance, the polarization layer 112 may be formed of AlGa_N, AlIn_N, or AlN. In a particular embodiment, the polarization layer 112 is formed of AlGa_N and the polar semiconductor layer 114 is formed of GaN.

[0018] To operate the depletion mode multi-gate HEMT 101, a gate bias is not applied to the first and second gate electrodes 106 and 108. The naturally forming 2DEG allows current to freely travel between the source and drain contacts 110. Accordingly, the depletion mode multi-gate HEMT 101 is constantly ON when no gate bias is applied to the first and second gate electrodes 106 and 108. When a gate bias is applied, electrons are prevented from entering the channel layer 120 between the first and second gate electrodes 106 and 108. Without electrons in the channel layer, the channel is pinched off and no current can flow through the channel layer. Accordingly, applying a gate bias turns OFF the enhancement mode multi-gate HEMT 100. According to embodiments of the invention, applying the gate bias to the first and second gate electrodes 106 and 108 controls the channel layer 120 from above and below the polar semiconductor layer 114. As such, the depletion mode multi-gate HEMT 101 has maximum control of the current that flows through the channel layer 120.

[0019] FIGS. 2A-2M illustrate an exemplary method of forming the multi-gate HEMT according to embodiments of the invention. More specifically, FIGS. 2A-2J illustrate cross-sectional views of a method of forming an enhancement mode multi-gate HEMT, in accordance with an embodiment of the invention. FIGS. 2K-2M illustrate cross-sectional views of a method of forming a depletion mode multi-gate HEMT as continued from FIG. 2G-1, in accordance with an embodiment of the invention.

[0020] With reference to FIG. 2A, a donor substrate 200 having a donor top surface 208 is provided. In an embodiment, the donor substrate 200 includes a thick polar semiconductor layer 113 disposed on top of a template substrate 202. The donor substrate 200 further includes a first adhesion layer 104A disposed on a polarization layer 112. In embodiments, the polarization layer 112 is disposed on the thick polar semiconductor layer 113.

[0021] An exemplary process flow to form the donor substrate 200 may begin by providing the template substrate 202. The template substrate 202 provides a base upon which other layers may form. Any suitable substrate may form the template substrate 202, such as, but not limited to, a bulk monocrystalline silicon substrate or a sapphire substrate.

[0022] Next, the thick polar semiconductor layer 113 is formed on top of the template substrate 202. Any suitable growth process, such as atomic layer deposition (ALD), chemical vapor deposition (CVD), and molecular beam epitaxy (MBE), may be used to form the thick polar semiconductor layer 113. The thick polar semiconductor layer 113 may have a thickness sufficient to minimize defects created during its fabrication. For instance, a thick polar semiconductor layer 113 formed of GaN may form threading dislocation defects when grown on a non-native substrate. The defects propagate vertically and may eventually terminate after a certain height. Therefore, the thickness of the polar semiconductor layer 113 may need to be sufficient enough to form a high quality material having low defect density in an upper region of the thick polar semiconductor layer 113. The high quality material in the upper region of the thick polar semiconductor layer 113 may be later used as part of a channel layer 120, as will be discussed below. In an embodiment, the thickness of the thick polar semiconductor layer 113 is at least 20 μm . In a particular embodiment, the thickness is around 30 μm .

[0023] Next, the polarization layer 112 is formed on top of the thick polar semiconductor layer 113 by any suitable growth technique, such as epitaxial growth. The polarization layer 112 may be formed to a thickness sufficient to induce a 2DEG at the interface between the polarization layer 112 and the thick polar semiconductor layer 113. For instance, the thickness of the polarization layer 112 may range from 10 to 30 nm. In a particular embodiment, the thickness is about 20 nm. The polarization layer 112 may be formed of any suitable material having an intrinsic charge polarity that interacts with the thick polar semiconductor layer 113 to induce a 2DEG at the interface between the polarization layer 112 and the thick polar semiconductor layer 113. Exemplary materials for the polarization layer 112 include AlGa_xN_{1-x}, AlInN, and AlN.

[0024] The first adhesion layer 104A is then formed on top of the polarization layer 112, thereby completing formation of the donor substrate 200. Any suitable deposition process may be used to form the first adhesion layer 104A, such as chemical vapor deposition (CVD) and physical vapor deposition (PVD). The first adhesion layer 104A attaches the donor substrate 200 to a separate substrate, such as the receiver substrate 201 illustrated in FIG. 2B-1. The first adhesion layer 104A may be designed to have a thickness sufficient to form a strong bond when fused with another

adhesion layer, such as a second adhesion layer 104B illustrated in FIG. 2B-1. In embodiments, the thickness of the first adhesion layer 104A ranges from 10-20 nm. The first adhesion layer 104A may be formed of any suitable material with adhesive properties, such as SiO₂ or Al₂O₃. In a particular embodiment, the donor substrate 200 includes a template substrate 202 formed of silicon, a thick polar semiconductor layer 113 formed of GaN, a polarization layer 112 formed of AlGaN, and a first adhesion layer 104A formed of SiO₂.

[0025] An optional perforation layer 204 may be formed within the thick polar semiconductor layer 113 in preparation for an ion cleaving process. In an embodiment, the perforation layer 204 is implanted anytime after growing the thick polar semiconductor layer 113. In an embodiment, the perforation layer 204 is implanted after depositing the first adhesion layer 104A. In an embodiment, the perforation layer 204 is created by hydrogen implantation to a depth D from the top surface 115 of the thick polar semiconductor layer 113. The perforation layer 204 may determine the point at which the donor substrate 200 will be cut by the ion cleaving process. In embodiments, the depth D of the hydrogen implantation is a target thickness of a polar semiconductor layer 114 to be formed as part of the channel layer 120 as shown in FIG. 1A. A portion of the thick polar semiconductor layer 113 disposed above the depth D may be high-quality semiconductor material later used as part of the channel layer 120. In an embodiment, the depth D is at least 2 nm. In a particular embodiment, the depth D is in the range of 20 to 100 nm.

[0026] Next, in FIG. 2B-1, a receiver substrate 201 having a receiver top surface 210 is provided. In an embodiment, the receiver substrate 201 includes a carrier substrate 102 formed of any suitable substrate for semiconductor fabrication, such as a bulk monocrystalline silicon substrate.

[0027] A sacrificial layer 206 is formed within the receiver substrate 201. The sacrificial layer 206 may be completely embedded within the receiver substrate 201. As shown in a top-view perspective of the receiver substrate 201 in FIG. 2B-2, the sacrificial layer 206 may extend down a portion of the carrier substrate 102 within a second adhesion layer 104B. With reference back to the embodiment depicted in FIG. 2B-1, the sacrificial layer 206 is formed within a trench of the carrier substrate 102 and completely surrounded by the second adhesion layer 104B. The second adhesion layer 104B may immediately surround the sacrificial layer 206 within the trench of the carrier substrate 102. In embodiments, the sacrificial layer 206 is formed from a sacrificial material that can be selectively removed relative to the adhesion layer 104B. Further, the sacrificial layer 206 is formed of a sacrificial material that does not diffuse into the adhesion layer 104B. The sacrificial layer 206 may also withstand subsequent processing conditions used to form other features of the

multi-gate HEMT. In an embodiment, the sacrificial layer 206 may be formed from a metal, such as tungsten, or a nitride, such as titanium nitride (TiN) or silicon nitride (SiN).

[0028] As illustrated in FIG. 2B-1, a portion of the second adhesion layer 104B is disposed on top of the carrier substrate 102. The second adhesion layer 104B may attach the receiver substrate 201 to a separate substrate, such as the donor substrate 200. In an embodiment, the second adhesion layer 104B has a thickness sufficient to form a strong bond when fused with another adhesion layer, such as the first adhesion layer 104A in FIG. 2A. In embodiments, the thickness of the second adhesion layer 104B ranges from 15-20 nm. Any suitable material with adhesive properties may form the second adhesion layer 104B. For example, the second adhesion layer 104B may be formed of SiO₂ or Al₂O₃.

[0029] The receiver substrate 201 may be formed by well-known deposition and etch processes. An exemplary process flow to form the receiver substrate 201 may begin by initially etching a trench within the carrier substrate 102 with an anisotropic etch process. Thereafter, an initial adhesion layer may be deposited within the trench and on a top surface 103 of the carrier substrate 102. Next, the sacrificial layer 206 is formed on the initial adhesion layer and within the trench. A planarization process may then remove portions of the sacrificial layer 206 and a portion of the initial adhesion layer disposed above the top surface 103 of the carrier substrate 102. Finally, a subsequent adhesion layer may be deposited on the top surface 103 of the carrier substrate 102, on top of the initial adhesion layer, and on top of the sacrificial layer 206. A remaining portion of the initial adhesion layer together with the subsequent adhesion layer form the second adhesion layer 104B as illustrated in FIG. 2B-1.

[0030] After the donor substrate 200 and the receiver substrate 201 are provided, the donor substrate 200 is then attached to the receiver substrate 201 to form a bonded substrate 203 as illustrated in FIG. 2C. In an embodiment, attaching the donor substrate 200 to the receiver substrate 201 is performed by bonding the first adhesion layer 104A to the second adhesion layer 104B. Bonding of the first adhesion layer 104A to the second adhesion layer 104B may occur by a direct wafer bonding process. In an embodiment, the direct wafer bonding process forms a chemical bond between the top surfaces of the two adhesion layers 104A and 104B. The direct wafer bonding process may be an oxide fusion bonding process. The oxide fusion bonding process may include temporarily holding the top surfaces of the two adhesion layers 104A and 104B in place with electrostatic forces, such as van der Waals forces. A thermal anneal may then chemically bond the two layers together.

[0031] In embodiments, the adhesion layers 104A and 104B are fused together to form the bonded adhesion layer 104. The bonded adhesion layer 104 may have a thickness determined by the sum of the first and second adhesion layers 104A and 104B. The thickness of the bonded adhesion layer 104 should not be too thick for a via to be formed through it. Further, the thickness of the bonded adhesion layer 104 should be thick enough to form a bond sufficient to withstand wafer handling and subsequent semiconductor processing. In an embodiment, the thickness of the bonded adhesion layer 104 ranges from 30 to 40 nm.

[0032] Next, as shown in FIG. 2D, the bonded substrate 203 is separated at a point within the thick polar semiconductor layer 113 to remove a portion 209 of the bonded substrate 203. A remaining portion of the bonded substrate 203 forms a device substrate 205. The device substrate 205 will be used to form the multi-gate HEMT according to embodiments of the invention. The thick polar semiconductor layer 113 is separated into a portion 114x and a polar semiconductor layer 114. The portion 114x may be discarded or reused for subsequent surface donations with the portion 209. The polar semiconductor layer 114 may remain as part of the device substrate 205 for fabrication of the multi-gate HEMT. In embodiments, the polar semiconductor layer 114 is disposed in a top portion of the device substrate 205 where a channel layer 120 is disposed. The polar semiconductor layer 114 may be formed of the high quality material in the upper region of the thick polar semiconductor layer 113 discussed above with respect to FIG. 2A.

[0033] In embodiments, the polar semiconductor layer 114 is used to form a channel layer for the multi-gate HEMT according to embodiments of the invention. The polar semiconductor layer 114 may have a thickness sufficient for current flow during operation of the multi-gate HEMT. In an embodiment, the thickness of the polar semiconductor layer 114 is equivalent to the depth D of the implanted hydrogen atoms discussed in FIG. 2A. In one embodiment, the thickness of the polar semiconductor layer 114 is at least 2 nm. In a specific embodiment, the thickness of the polar semiconductor layer 114 is in the range of 20 to 100 nm.

[0034] In an embodiment, the bonded substrate 203 is separated by ion cutting at the perforation layer 204 within the thick polar semiconductor layer 113 where hydrogen atoms were implanted as discussed in FIG. 2A. Ion cutting may be performed by an initial thermal anneal that forms voids where the hydrogen atoms are implanted. Once the voids are formed, the portion 209 may be easily separated due to structural weakness caused by the voids. Alternative separation methods include any conventional cutting technique, such as spalling, or any suitable selective etch release technique. One skilled in the art would understand the processes required to implement the selective etch

release technique to separate the bonded substrate 203. A polishing process, such as chemical mechanical polishing (CMP), may then be used to smooth the top surface and thin the layer 114 to desired thickness.

[0035] After separating and removing the portion 209 of the bonded substrate 203, the device substrate 205, as shown in FIG. 2E, is used to form the multi-gate HEMT 100 according to embodiments of the invention. In an embodiment, the device substrate 205 includes the carrier substrate 102, the sacrificial layer 206, the bonded adhesion layer 104, and the channel layer 120. In an embodiment, the channel layer 120 is a heterogeneous structure formed of the polar semiconductor layer 114 and the polarization layer 112. In embodiments, the polar semiconductor layer 114 is disposed directly on top of the polarization layer 112.

[0036] Next, as shown in FIG. 2F, source and drain contacts 110 are formed on opposite sides of the sacrificial layer 206 and over the carrier substrate 102. The source and drain contacts 110 may be formed by epitaxial growth from the polar semiconductor layer 114. For instance, the source and drain contacts 110 may be formed by ALD or CVD. In an embodiment, the source and drain contacts 110 extend through the polar semiconductor layer 114 and are formed directly on top of the polarization layer 112. As such, the source and drain contacts 110 are coupled to the polar semiconductor layer 114 and the polarization layer 112. Additionally, the source and drain contacts 110 may be coupled to the 2DEG layer formed within the polar semiconductor layer 114. The source and drain contacts 110 are formed of any suitable semiconductor material. In an embodiment, the source and drain contacts 110 are formed of n-doped GaN, InGaN, or InN.

[0037] Thereafter, as shown in FIG. 2G-1, the sacrificial layer 206 is selectively removed to form a void 210. In an embodiment, the sacrificial layer 206 is removed by a first etch process that substantially removes only the sacrificial layer 206. In an embodiment, the first etch process is an isotropic wet etch process using an etchant that selectively removes the sacrificial layer 206 relative to the surrounding bonded adhesion layer 104. That is, the etchant substantially removes the sacrificial layer 206 while leaving the surrounding bonded adhesion layer 104 substantially intact. In an embodiment, the etchant is phosphoric acid (H_3PO_4) or a mixture of ammonium hydroxide and hydrogen peroxide ($\text{NH}_4\text{OH}+\text{H}_2\text{O}_2$).

[0038] To remove the sacrificial layer 206, at least one or more openings 211 may be formed through a region 209 directly over the sacrificial layer 206 as shown in a top-view perspective illustrated in FIG. 2G-2. The openings 211 do not interfere with the channel layer 120. In an embodiment, the openings 211 expose the sacrificial layer 206 and provide a tunnel through which

etchants may flow. The etchants may be used to selectively remove the sacrificial layer 206. In embodiments, the openings 211 may be formed by any suitable etch process, such as a plasma etch process.

[0039] Next, the void 210 is expanded to form an enlarged void 212 as shown in FIG. 2H. In an embodiment, a portion of the polarization layer 112 is removed to form the enlarged void 212. Accordingly, the enlarged void 212 may expose a bottom surface 222 of the polar semiconductor layer 114. The enlarged void 212 may also expose other surfaces within the device substrate 205. For example, the enlarged void 212 may further expose sidewalls 214 of the polarization layer 112, sidewalls 216 of the bonded adhesion layer 104, and surfaces 218 and 220 of the carrier substrate 102. The enlarged void 212 may define the gate length of the bottom gate electrode 108 shown in FIGS. 1A-1B. In an alternative embodiment, the enlarged void 212 does not expose the polar semiconductor layer 114, as will be discussed further below in FIGS. 2K-2M.

[0040] In embodiments, the enlarged void 212 is formed by two etch processes. For example, the enlarged void 212 may be formed by a second etch process and a third etch process. In an embodiment, the second etch process substantially removes only a portion of the bonded adhesion layer 104. The second etch process may be an isotropic wet etch process that uses an etchant to selectively remove the bonded adhesion layer 104 relative to the surrounding layers (i.e., 112, and 102). That is, the etchant substantially removes the bonded adhesion layer 104 while leaving the surrounding layers substantially intact. In an embodiment, the etchant is hydrofluoric acid (HF).

[0041] In an embodiment, the third etch process removes a portion of the polarization layer 112. The third etch process may be a wet etch process that selectively removes the polarization layer 112 relative to the surrounding layers (i.e., 114, 104, and 102). That is, the etchant substantially removes the polarization layer 112 while leaving the surrounding layers 114, 104, and 102 substantially intact. In an embodiment, the etchant is potassium hydroxide (KOH), sodium hydroxide (NaOH), or AZ400K photoresist developer.

[0042] Next, as shown in FIG. 2I, a first gate dielectric layer 116 and a second gate dielectric layer 118 are formed. In embodiments, the first gate dielectric layer 116 is formed on top of the channel layer 120 and in between the source and drain contacts 110. Further, the second gate dielectric layer 118 is formed on surfaces 222, 214, 216, 218, and 220 of the enlarged void 212. In embodiments, the second gate dielectric layer 118 does not completely fill the enlarged void 212. The first and second gate dielectric layers 116 and 118 are formed to have a thickness sufficient for transistor operation. In an embodiment, the first and second gate dielectric layers 116 and 118 have a

thickness between 2-4 nm. The first and second gate dielectric layers 116 and 118 electrically isolate the surfaces upon which they are formed from subsequently formed gate electrodes. The first and second gate dielectric layers 116 and 118 may be formed of any suitable high-k dielectric material. In an embodiment, the first and second gate dielectric layers 116 and 118 are formed from an insulating material such as, but not limited to, SiO_2 , HfO_2 , and ZrO_2 .

[0043] In embodiments, any suitable conforming deposition process, such as CVD or ALD, may form the first and second gate dielectric layers 116 and 118. In an embodiment, the first and second gate dielectric layers 116 and 118 are formed simultaneously. In an embodiment, the second gate dielectric layer 118 is formed by ALD through the openings 211, which is discussed above in FIG. 2G-2. As such, the openings 211 should be designed to have a diameter that is wide enough to allow sufficient deposition material to flow into the enlarged void 212 to deposit the second gate dielectric layer 118. In an embodiment, the openings 211 have a diameter of at least 10 nm. In a particular embodiment, the openings 211 have a diameter in the range of 15-20 nm.

[0044] Thereafter, as depicted in FIG. 2J, a first gate electrode 106 and a second gate electrode 108 are formed, thereby completing the construction of the enhancement mode multi-gate HEMT 100 according to an embodiment of the invention. The first gate electrode 106 is formed on top of the first gate dielectric layer 116 and above the polar semiconductor layer 114. Additionally, the second gate electrode 108 is formed within the enlarged void 212 below the polar semiconductor layer 114. In an embodiment, the second gate electrode 108 completely fills the enlarged void 212. In an embodiment, the second gate electrode 108 is entirely enclosed within the second gate dielectric layer 118. The first and second gate electrodes 106 and 108 may be formed to have a gate length according to design requirements. In embodiments, the first and second gate electrodes may have a gate length depending on the depth D of the polar semiconductor layer 114. For example, if the depth D of the polar semiconductor layer 114 is around 20 nm, the first and second gate electrodes 106 and 108 may have the same gate length. In an embodiment, the first second gate electrodes 106 and 108 may have a gate length between 1 and 3 μm . In a particular embodiment, the first and second gate electrodes 106 and 108 have a gate length of 2 μm . In another example, if the depth D of the polar semiconductor layer 114 is around 100 nm, the first and second gate electrodes 106 and 108 may have different gate lengths. For instance, the second gate electrode 108 may have a wider gate length than the first gate electrode 106. In an embodiment, the first gate electrode 106 may have a gate length between 0.5 and 3 μm and the second gate electrode may have a gate length

between 1 and 3 μm . In a particular embodiment, the first gate electrode 106 has a gate length of 1 μm and the second gate electrode 108 has a gate length of 2 μm .

[0045] In an embodiment, the first gate electrode 106 and the second gate electrode 108 are vertically aligned to one another. Additionally, in an embodiment, the first gate electrode 106 and the second gate electrode 108 are electrically coupled to one another such that when voltage is applied to one gate, the other gate is also applied with the same voltage. As such, both sides of a channel layer 120 can be used to control current flow through the polar semiconductor layer 114. The first gate electrode 106 may be formed by any suitable gate formation process. For example, the first gate electrode 106 may be formed by a blanket deposition of a conductive material followed by an anisotropic etch of the deposited conductive material. In another example, the first electrode 106 may be formed by a replacement gate process or a damascene process. The second gate electrode 108 may be formed by any suitable deposition technique that can deposit material within a void embedded within a substrate. For example, the second gate electrode 108 may be formed by CVD, PVD, or ALD. In a particular embodiment, the first and second gate electrodes 106 and 108 are formed simultaneously. The first and second gate electrodes 106 and 108 may be formed by CVD, PVD, or ALD, followed by an anisotropic etch to form the first gate electrode 106. The first and second gate electrodes 106 and 108 may be formed of a conductive material, such as a metal. Exemplary metals include Ni, TiN, Pt, and W.

[0046] According to an embodiment of the invention, the enhancement mode multi-gate HEMT 100 illustrated in FIG. 2J has the polar semiconductor layer 114 disposed between the first and second gate electrodes 106 and 108. In this embodiment, the polarization layer 112 is not disposed between the first and second gate electrodes 106 and 108. Absence of the polarization layer 112 between the first and second gate electrodes 106 and 108 prevents formation of a 2DEG between the first and second gate electrodes 106 and 108. According to embodiments of the invention, applying the gate bias to the first and second gate electrodes 106 and 108 controls the channel layer 120 from above and below the polar semiconductor layer 114. As such, the enhancement mode multi-gate HEMT 100, according to an embodiment of the invention, has maximum control of the current that flows through the polar semiconductor layer 114.

[0047] In an alternative embodiment, the polarization layer 112 may be left intact between the first and second gate electrodes 106 and 108 to form a depletion mode multi-gate HEMT. The method of forming the depletion mode multi-gate HEMT is illustrated in FIGS. 2K-2M, which continues from FIG. 2G-1 described above.

[0048] In FIG. 2K, the void 210 from FIG. 2G-1 is expanded to form an enlarged void 212. In this embodiment, the enlarged void 212 does not expose the polar semiconductor layer 114. The enlarged void 212 may expose a bottom surface 223 of the polarization layer 112. In embodiments, the enlarged void 212 may further expose sidewalls 216 of the bonded adhesion layer 104, and surfaces 218 and 220 of the carrier substrate 102. The enlarged void 212 may be formed by a second etch process that substantially removes only the bonded adhesion layer 104, as discussed above with regard to FIG. 2H. Next, as shown in FIG. 2L, a first gate dielectric layer 116 and a second gate dielectric layer 118 are formed. In this embodiment, the first gate dielectric layer 116 is formed on top of the channel layer 120 and in between the source and drain contacts 110. Further, the second gate dielectric layer 118 is formed on the surfaces 223, 216, 218, and 220 of the enlarged void 212. The second gate dielectric layer 118 does not completely fill the enlarged void 212. In an embodiment, a portion of the second gate dielectric 118 is formed directly below the polarization layer 112. The first and second gate dielectric layers 116 and 118 have thicknesses, dimensions, and formation process techniques similar to those described above in FIG. 2I.

[0049] Thereafter, as depicted in FIG. 2M, a first gate electrode 106 and a second gate electrode 108 are formed, thereby completing the construction of the depletion mode multi-gate HEMT 101 according to an embodiment of the invention. In embodiments, the first gate electrode 106 is formed on top of the first gate dielectric layer 116 and above the channel layer 120. The second gate electrode 108 is formed within the enlarged void 212. The second gate electrode 108 may be disposed beneath the channel layer 120 formed of the polar semiconductor layer 114 and the polarization layer 112. In an embodiment, the second gate electrode 108 is entirely enclosed by the second gate dielectric layer 118. In an embodiment, the first gate electrode 106 and the second gate electrode 108 are vertically aligned to one another. Additionally, in an embodiment, the first gate electrode 106 and the second gate electrode 108 are electrically coupled to one another such that when voltage is applied to one gate, the other gate is also applied with the same voltage. As such, both sides of the channel layer 120 can be used to control current flow through the channel layer 120. In an embodiment, the first and second gate electrodes 106 and 108 are formed by the process techniques and according to the structural dimensions disclosed above in FIG. 2J.

[0050] According to an embodiment of the invention, the depletion mode multi-gate HEMT 101 has both the polar semiconductor layer 114 and the polarization layer 112 disposed between the first and second gate electrodes 106 and 108. The depletion mode multi-gate HEMT 101 therefore has a 2DEG between the first and second gate electrodes 106 and 108. In an embodiment, the 2DEG is 1-

2 nm away from the interface within the polar semiconductor layer 114. According to embodiments of the invention, applying the gate bias to the first and second gate electrodes 106 and 108 controls the channel layer 120 from above and below the polar semiconductor layer 114. As such, the depletion mode multi-gate HEMT 101, according to an embodiment of the invention, has maximum control of the current that flows through the channel layer 120.

[0051] FIG. 3 illustrates an interposer 300 that includes one or more dies fabricated with embodiments of the invention. The interposer 300 is an intervening substrate used to bridge a first substrate 302 to a second substrate 304. The first substrate 302 may be, for instance, an integrated circuit die. The second substrate 304 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 300 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 300 may couple an integrated circuit die to a ball grid array (BGA) 306 that can subsequently be coupled to the second substrate 304. In some embodiments, the first and second substrates 302/304 are attached to opposing sides of the interposer 300. In other embodiments, the first and second substrates 302/304 are attached to the same side of the interposer 300. And in further embodiments, three or more substrates are interconnected by way of the interposer 300.

[0052] The interposer 300 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0053] The interposer may include metal interconnects 308 and vias 310, including but not limited to through-silicon vias (TSVs) 312. The interposer 300 may further include embedded devices 314, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 300.

[0054] In accordance with embodiments of the invention, multi-gate HEMTs or methods of forming the multi-gate HEMTs disclosed herein may be used in the fabrication of interposer 300.

[0055] FIG. 4 illustrates a computing device 400 in accordance with one embodiment of the invention. The computing device 400 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 400 include, but are not limited to, an integrated circuit die 402 and at least one communication chip 408. In some implementations the communication chip 408 is fabricated as part of the integrated circuit die 402. The integrated circuit die 402 may include a CPU 404 as well as on-die memory 406, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

[0056] Computing device 400 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 410 (e.g., DRAM), non-volatile memory 412 (e.g., ROM or flash memory), a graphics processing unit 414 (GPU), a digital signal processor 416, a crypto processor 442 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 420, an antenna 422, a display or a touchscreen display 424, a touchscreen controller 426, a battery 428 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 428, a compass 430, a motion coprocessor or sensors 432 (that may include an accelerometer, a gyroscope, and a compass), a speaker 434, a camera 436, user input devices 438 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 440 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0057] The communications chip 408 enables wireless communications for the transfer of data to and from the computing device 400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 408 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 400 may include a plurality of communication chips 408. For instance, a first

communication chip 408 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 408 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0058] The processor 404 of the computing device 400 may include one or more multi-gate HEMT devices of embodiments of the present invention and which may be formed in accordance with embodiments of the invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0059] The communication chip 408 may also include one or more multi-gate HEMT devices of embodiments of the present invention and which may be formed in accordance with embodiments of the invention.

[0060] In further embodiments, another component housed within the computing device 400 may contain one or more multi-gate HEMT devices of embodiments of the present invention and which may be formed in accordance with embodiments of the invention.

[0061] In various embodiments, the computing device 400 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 400 may be any other electronic device that processes data.

[0062] In an embodiment, a semiconductor device includes a substrate, and an adhesion layer on top of the substrate, a channel layer on top of the adhesion layer, a first gate electrode on top of the channel layer, the first gate electrode having a first gate dielectric layer in between the first gate electrode and the channel layer, a second gate electrode beneath the channel layer, the second gate electrode having a second gate dielectric layer completely surrounding the second gate electrode, and a pair of source and drain contacts on opposite sides of the first electrode.

[0063] In an embodiment, the channel layer is a heterogeneous structure. The channel layer may include a polarization layer and a polar semiconductor layer directly on top of the polarization layer. The polarization layer may be formed of AlGaN and the polar semiconductor layer may be formed of GaN. In an embodiment, the polarization layer is not disposed between the first and second gate electrodes. In an embodiment, the polar semiconductor layer and the polarization layer are disposed between the first and second gate electrodes. In an embodiment, the polarization layer induces a

two-dimensional electron gas (2DEG) at the interface between the polarization layer and the polar semiconductor layer. The 2DEG may be 1-2 nm away from the interface within the polar semiconductor layer. In an embodiment, the pair of source and drain contacts are formed on the polarization layer through the polar semiconductor layer. In an embodiment, the first gate dielectric layer is formed between the pair of source and drain contacts. The second gate electrode may extend into a trench of the carrier substrate. In an embodiment, the first gate electrode is vertically aligned to the second gate electrode.

[0064] In an embodiment, a method of forming a semiconductor device includes providing a donor substrate and a receiver substrate, the receiver substrate having an embedded sacrificial layer, transferring a portion of the donor substrate onto the receiver substrate to form a device substrate, a top portion of the device substrate forms a channel layer, forming a pair of source and drain regions on the channel layer and on opposite sides of the embedded sacrificial layer, removing the embedded sacrificial layer to form a void beneath the channel layer, forming a first gate dielectric layer on top of a portion of the channel layer and a second gate dielectric layer on sidewalls within the void; and forming a first gate electrode on the first gate dielectric layer above the channel layer and a second gate electrode on the second gate electrode beneath the channel layer within the void.

[0065] In an embodiment, forming the void includes first and second selective etch processes. The first selective etch process may substantially remove only the sacrificial layer. The second selective etch process may substantially remove only the adhesion layer. In an embodiment, the second selective etch process further includes a third selective etch process. The third selective etch process may substantially remove a portion of the bottom layer. In an embodiment, forming the void exposes the bottom layer within the gate void. Forming the void may expose the top layer within the void. In an embodiment, selectively removing the sacrificial layer includes etching openings into the device substrate to expose the sacrificial layer and removing the sacrificial layer with a selective etchant applied through the openings. The selective etchant may selectively remove the sacrificial layer relative to surrounding materials. In an embodiment, transferring a portion of the donor substrate onto the receiver substrate includes attaching the donor substrate to the receiver substrate, bonding the donor substrate to the receiver substrate to form a bonded substrate, and separating the bonded substrate to form the device substrate. The device substrate may include the receiver substrate and a portion of the donor substrate on top of the receiver substrate. In an embodiment, transferring a portion of the donor substrate onto the receiver substrate further includes performing fusion bonding to adhere the donor substrate to the receiver substrate.

[0066] In an embodiment, a computing device includes a motherboard, a processor mounted on the motherboard, and a communication chip fabricated on the same chip as the processor or mounted on the motherboard. The processor includes a substrate, an adhesion layer on top of the substrate, a channel layer on top of the adhesion layer, a first gate electrode on top of the channel layer, the first gate electrode having a first gate dielectric layer in between the first gate electrode and the channel layer, a second gate electrode embedded within the substrate and beneath the channel layer, the second gate electrode having a second gate dielectric layer completely surrounding the second gate electrode, and a pair of source and drain contacts on opposite sides of the first gate electrode.

[0067] In an embodiment, the channel layer is a heterogeneous structure. In an embodiment, the channel layer includes a polarization layer and a polar semiconductor layer directly on top of the polarization layer. The polarization layer may induce a two-dimensional electron gas (2DEG) at the interface between the polarization layer and the polar semiconductor layer. The polarization layer may be formed of AlGaN and the polar semiconductor layer may be formed of GaN. In an embodiment, the first gate electrode is vertically aligned to the second gate electrode.

[0068] The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[0069] These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
 - a substrate;
 - an adhesion layer on top of the substrate;
 - a channel layer on top of the adhesion layer;
 - a first gate electrode on top of the channel layer, the first gate electrode having a first gate dielectric layer in between the first gate electrode and the channel layer;
 - a second gate electrode beneath the channel layer, the second gate electrode having a second gate dielectric layer completely surrounding the second gate electrode; and
 - a pair of source and drain contacts on opposite sides of the first electrode.
2. The semiconductor device of claim 1, wherein the channel layer is a heterogeneous structure.
3. The semiconductor device of claim 2, wherein the channel layer comprises a polarization layer and a polar semiconductor layer directly on top of the polarization layer.
4. The semiconductor device of claim 3, wherein the polarization layer is formed of AlGaN and the polar semiconductor layer is formed of GaN.
5. The semiconductor device of claim 3, wherein the polarization layer is not disposed between the first and second gate electrodes.
6. The semiconductor device of claim 3, wherein the polar semiconductor layer and the polarization layer are disposed between the first and second gate electrodes.
7. The semiconductor device of claim 6, wherein the polarization layer induces a two-dimensional electron gas (2DEG) at the interface between the polarization layer and the polar semiconductor layer.

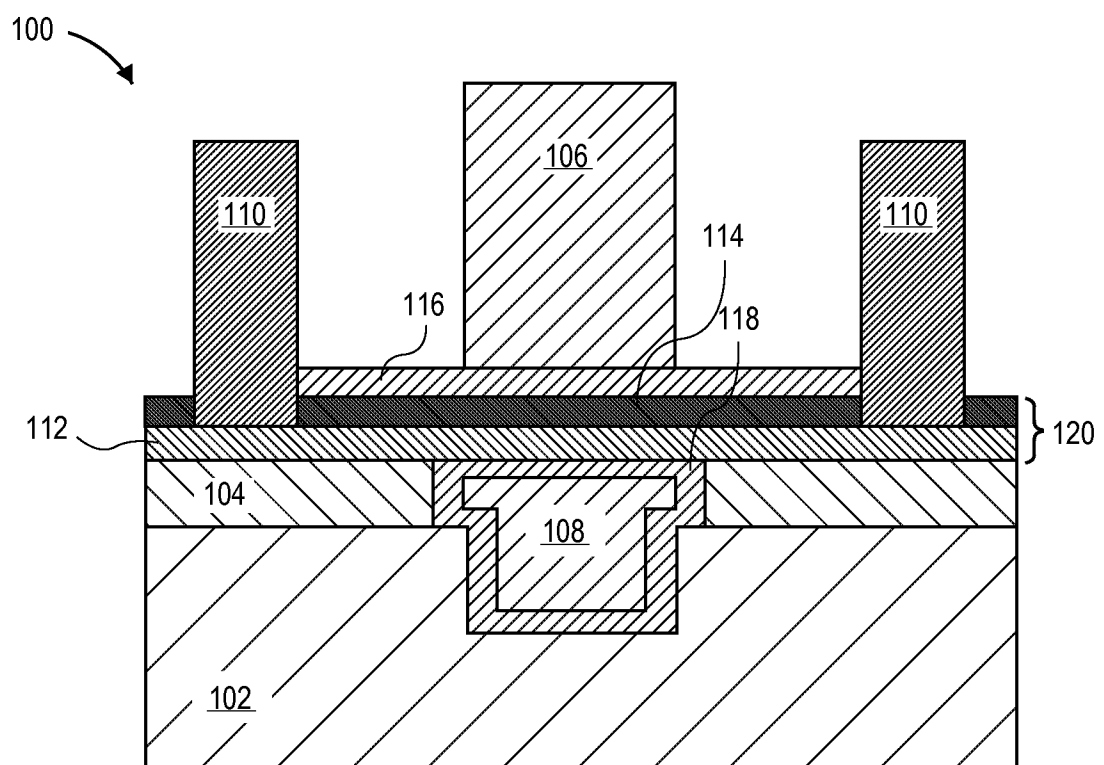
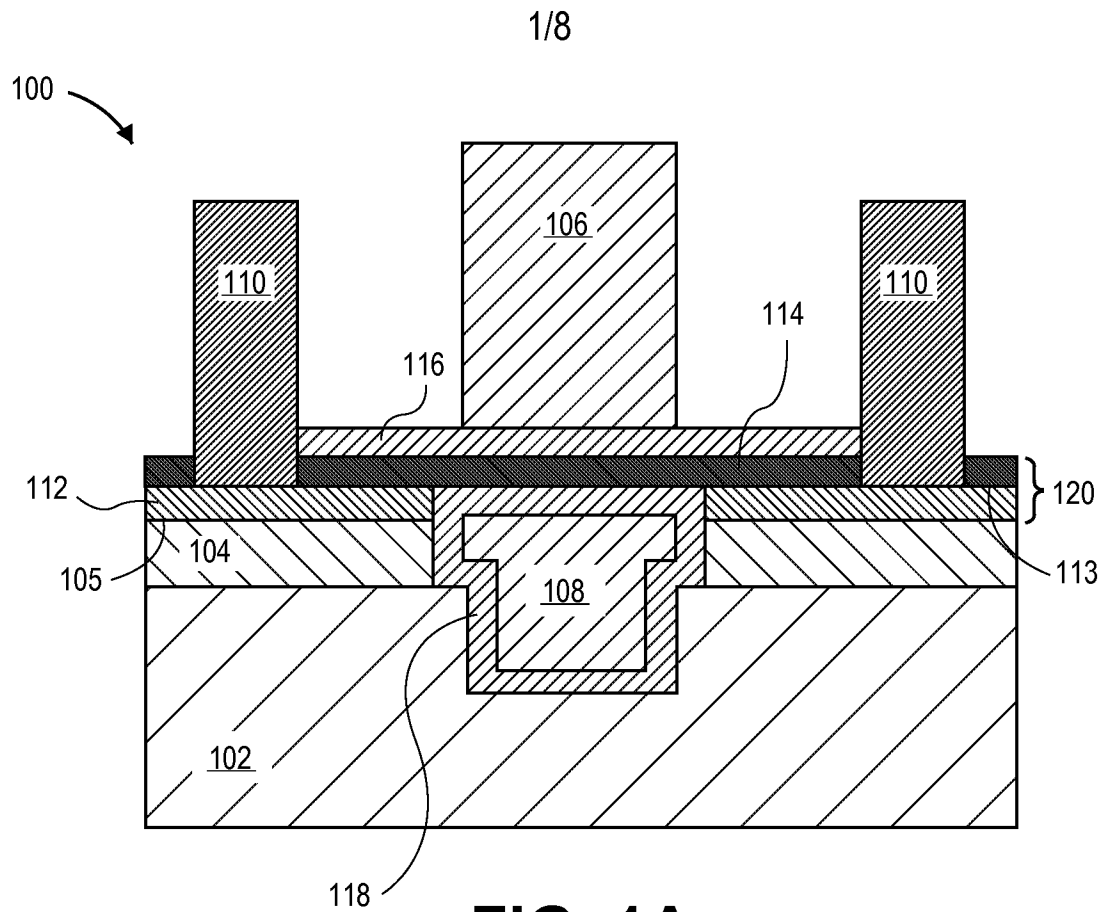
8. The semiconductor device of claim 7, wherein the 2DEG is 1-2 nm away from the interface within the polar semiconductor layer.
9. The semiconductor device of claim 1, wherein the second gate electrode extends into a trench of the carrier substrate.
10. The semiconductor device of claim 1, wherein the first gate electrode is vertically aligned to the second gate electrode.
11. A method of forming a semiconductor device, comprising:
 - providing a donor substrate and a receiver substrate, the receiver substrate having an embedded sacrificial layer;
 - transferring a portion of the donor substrate onto the receiver substrate to form a device substrate, a top portion of the device substrate forms a channel layer;
 - forming a pair of source and drain regions on the channel layer and on opposite sides of the embedded sacrificial layer;
 - removing the embedded sacrificial layer to form a void beneath the channel layer;
 - forming a first gate dielectric layer on top of a portion of the channel layer and a second gate dielectric layer on sidewalls within the void; and
 - forming a first gate electrode on the first gate dielectric layer above the channel layer and a second gate electrode on the second gate electrode beneath the channel layer within the void.
12. The method of claim 11, wherein forming the void comprises first and second selective etch processes.
13. The method of claim 12, wherein the first selective etch process substantially removes only the sacrificial layer.
14. The method of claim 12, wherein the second selective etch process substantially removes only the adhesion layer.
15. The method of claim 12, further comprising a third selective etch process.

16. The method of claim 15, wherein the third selective etch process substantially removes a portion of the bottom layer.
17. The method of claim 11, wherein selectively removing the sacrificial layer comprises etching openings into the device substrate to expose the sacrificial layer and removing the sacrificial layer with a selective etchant applied through the openings.
18. The method of claim 17, wherein the selective etchant selectively removes the sacrificial layer relative to surrounding materials.
19. The method of claim 11, wherein transferring a portion of the donor substrate onto the receiver substrate comprises:
- attaching the donor substrate to the receiver substrate;
 - bonding the donor substrate to the receiver substrate to form a bonded substrate; and
 - separating the bonded substrate to form the device substrate, the device substrate comprises the receiver substrate and a portion of the donor substrate on top of the receiver substrate.
20. The method of claim 19, further comprising performing fusion bonding to adhere the donor substrate to the receiver substrate.
21. A computing device, comprising:
- a motherboard;
 - a processor mounted on the motherboard; and
 - a communication chip fabricated on the same chip as the processor or mounted on the motherboard;
- wherein the processor comprises:
- a substrate;
 - an adhesion layer on top of the substrate;
 - a channel layer on top of the adhesion layer;
 - a first gate electrode on top of the channel layer, the first gate electrode having a first gate dielectric layer in between the first gate electrode and the channel layer;

a second gate electrode embedded within the substrate and beneath the channel layer, the second gate electrode having a second gate dielectric layer completely surrounding the second gate electrode; and

a pair of source and drain contacts on opposite sides of the first gate electrode.

22. The computing device of claim 21, wherein the channel layer is a heterogeneous structure.
23. The computing device of claim 22, wherein the channel layer comprises a polarization layer and a polar semiconductor layer directly on top of the polarization layer.
24. The computing device of claim 23, wherein the polarization layer induces a two-dimensional electron gas (2DEG) at the interface between the polarization layer and the polar semiconductor layer.
25. The computing device of claim 24, wherein the polarization layer is formed of AlGaN and the polar semiconductor layer is formed of GaN.



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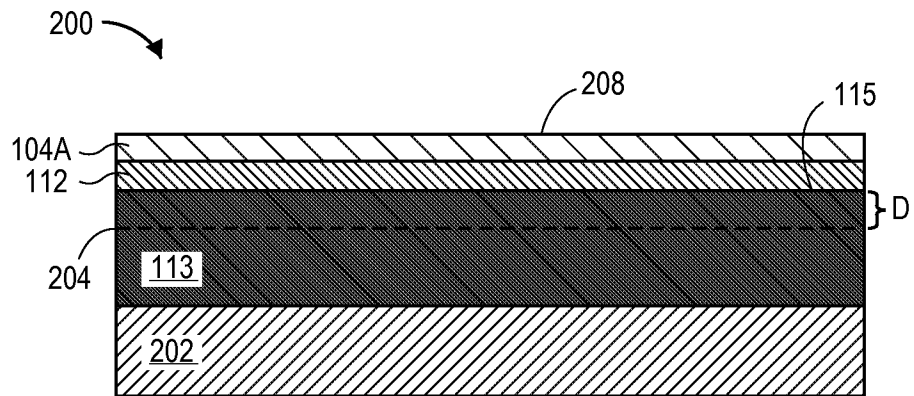


FIG. 2A

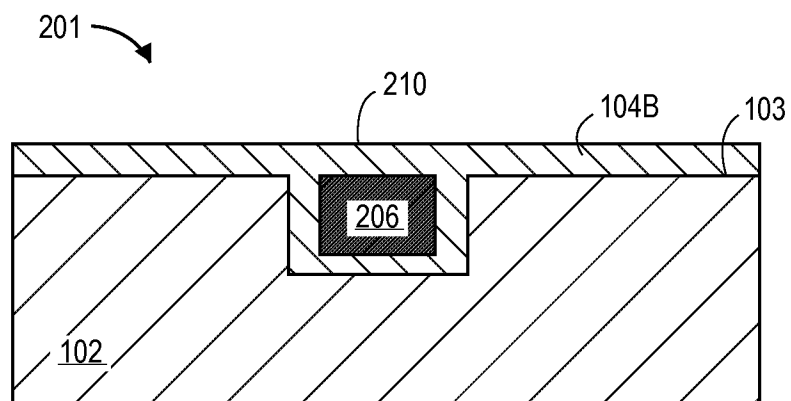


FIG. 2B-1

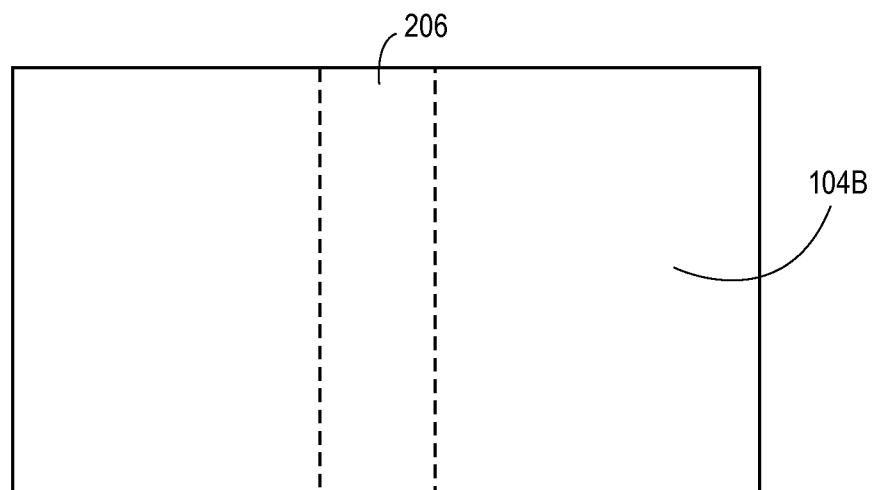


FIG. 2B-2

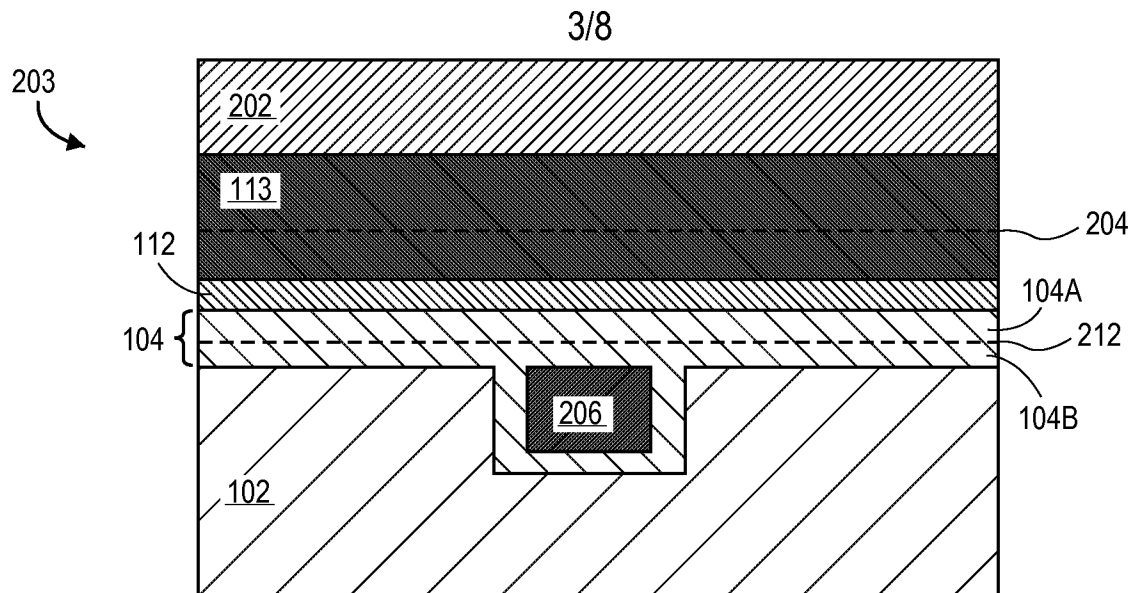


FIG. 2C

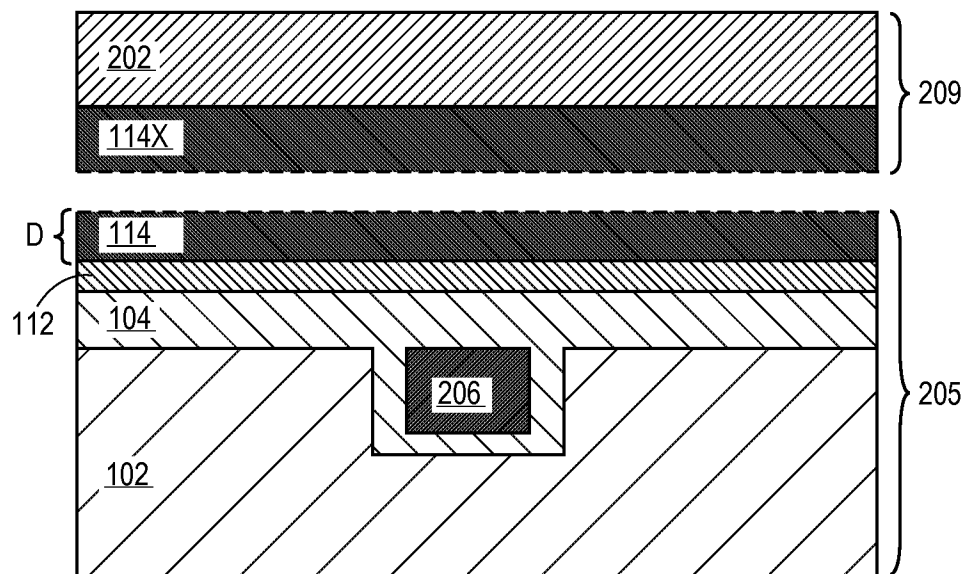


FIG. 2D

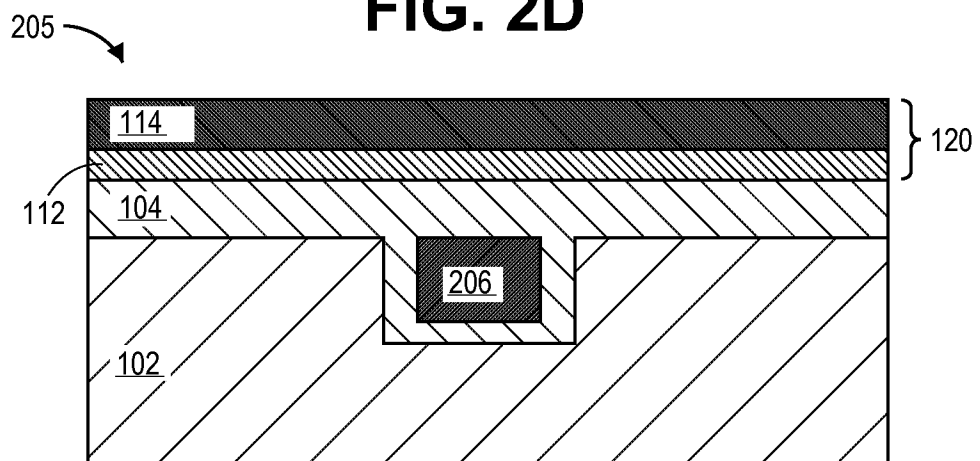


FIG. 2E

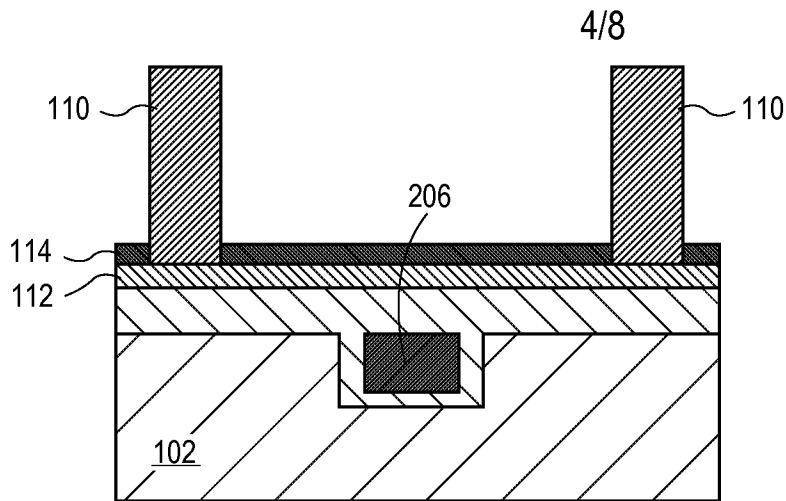


FIG. 2F

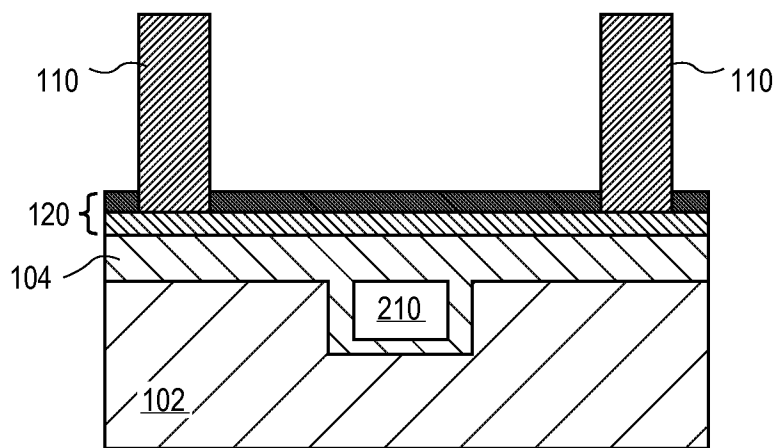


FIG. 2G-1

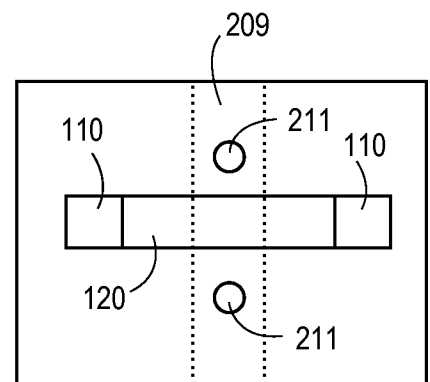


FIG. 2G-2

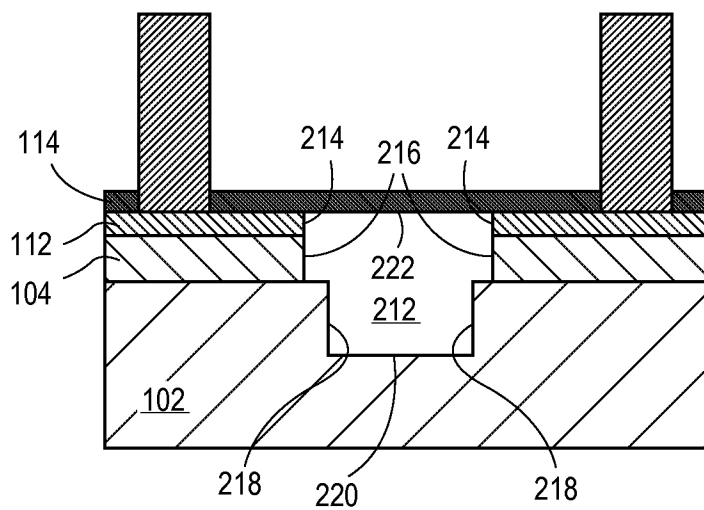


FIG. 2H

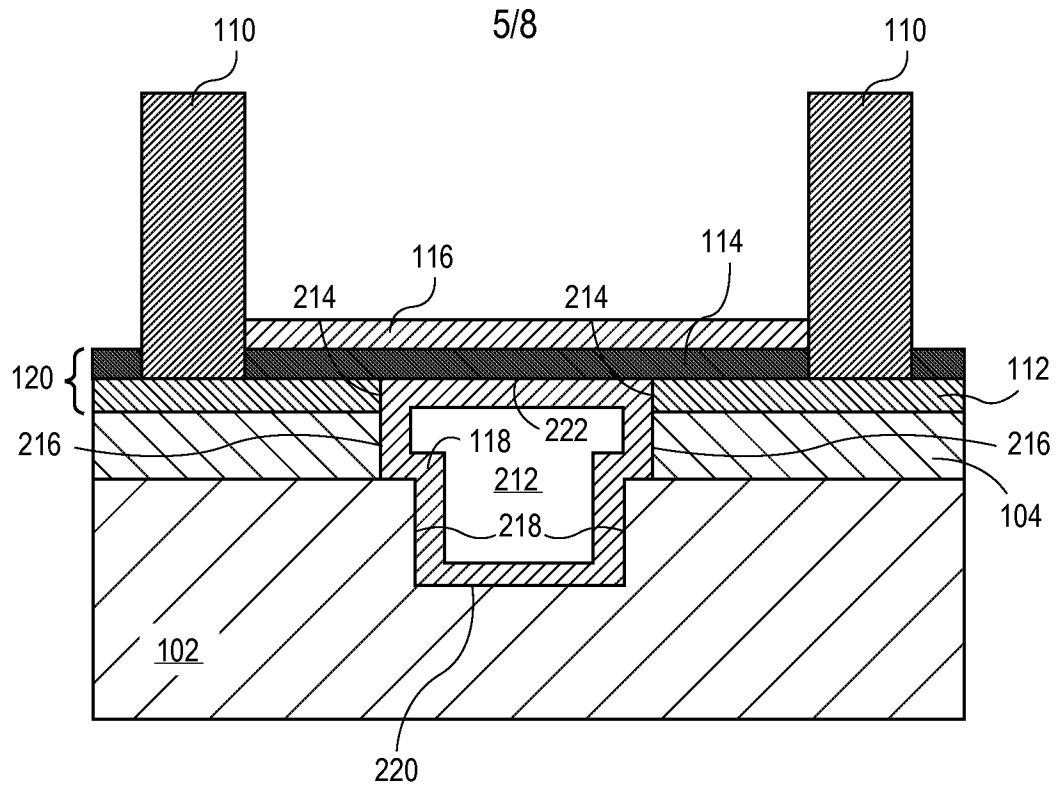


FIG. 21

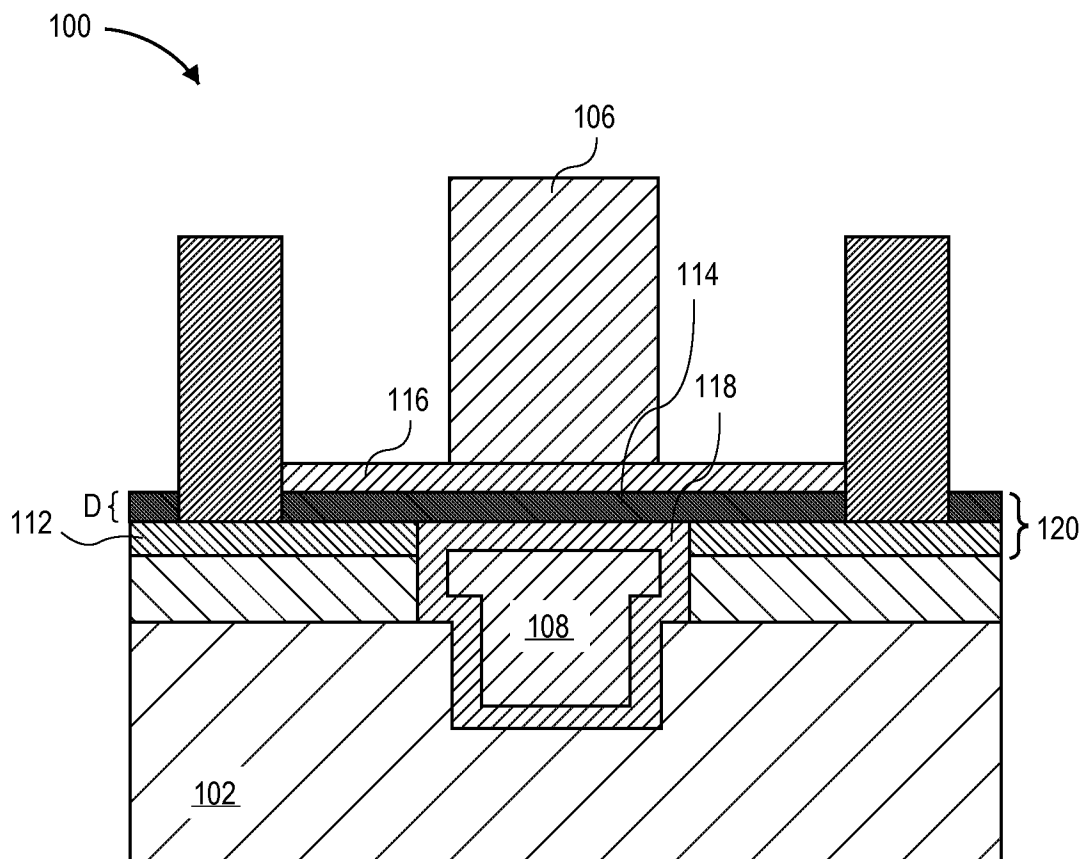


FIG. 2J

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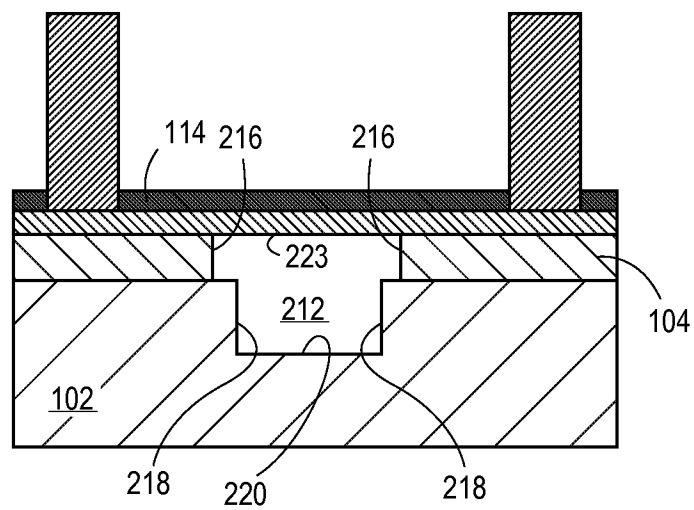


FIG. 2K

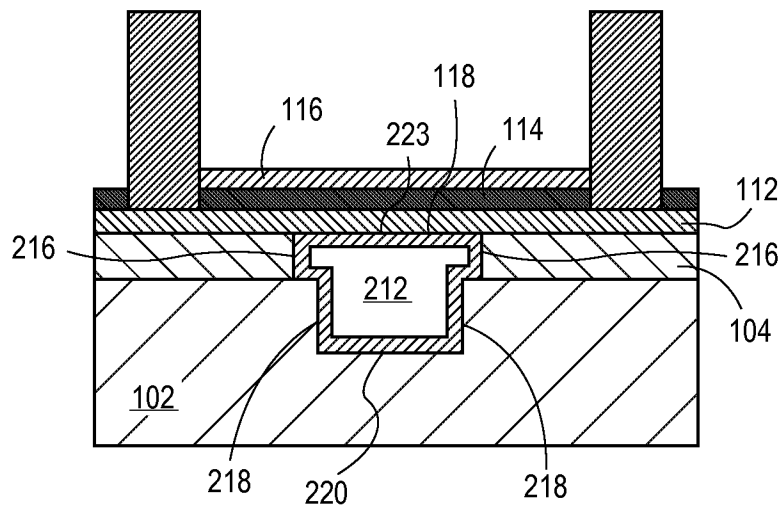


FIG. 2L

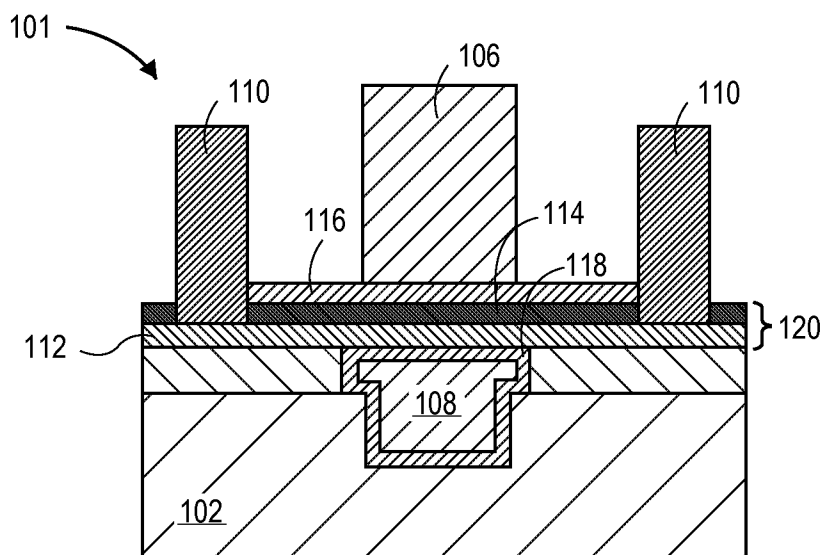


FIG. 2M

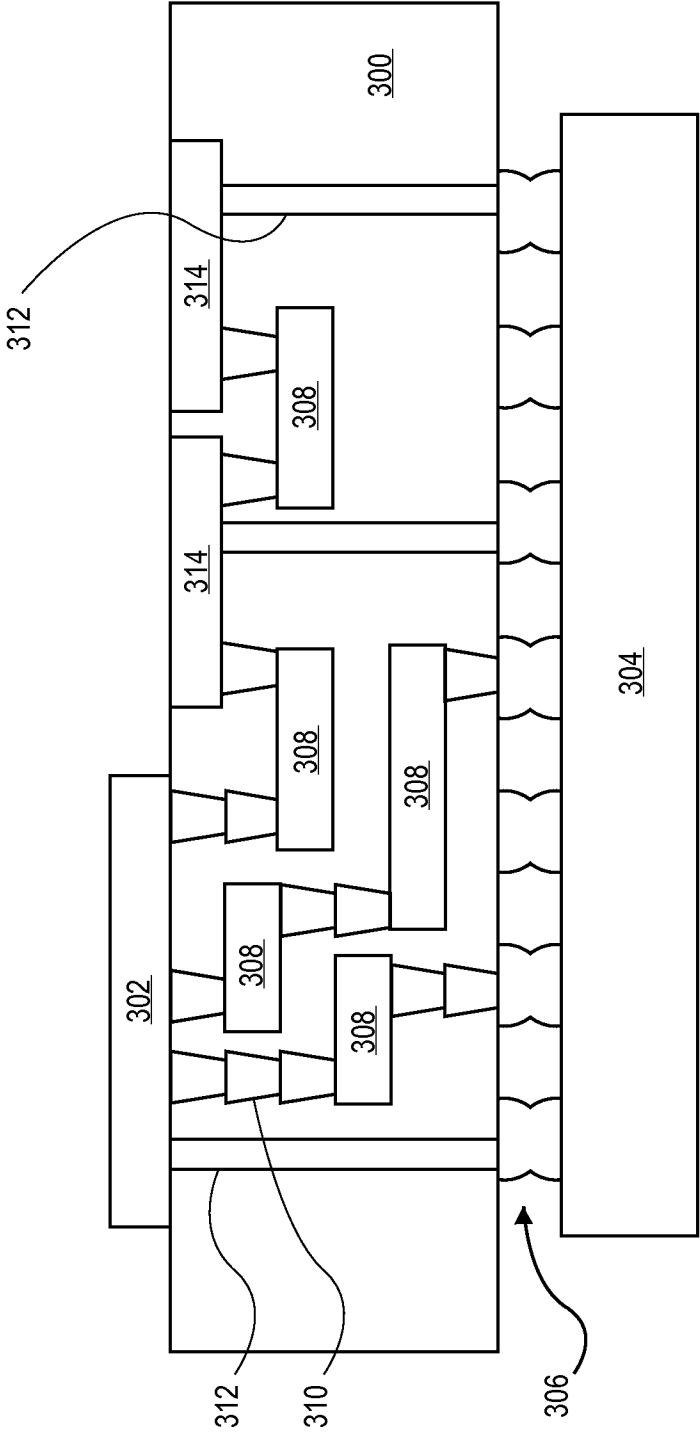
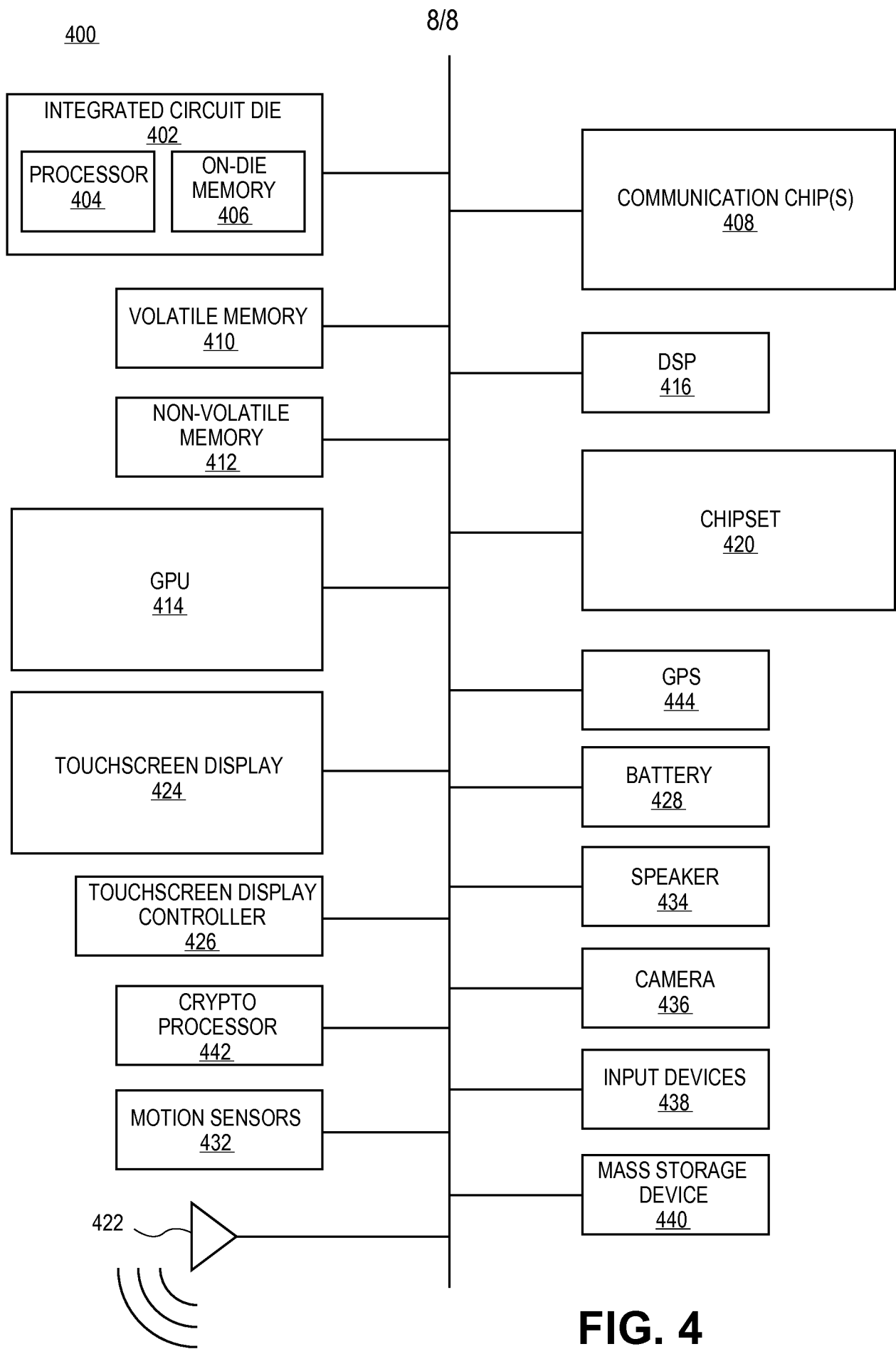


FIG. 3



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/054823**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/778(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/778; H01L 21/336; H01L 21/762; H01L 21/336; H01L 29/12; H01L 29/78; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: adhesion layer, first gate, second gate, beneath, channel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0161698 A1 (FABIO ALESSIO MARINO et al.) 27 June 2013 See abstract, paragraphs [0011]-[0105] and figures 1-18.	1-10, 21-25
A		11-20
Y	US 2009-0117707 A1 (AKIHISA SHIMOMURA et al.) 07 May 2009 See abstract, paragraphs [0131]-[0136], [0401], [0402] and figures 1A-4C, 14A, 14B.	1-10, 21-25
A	KR 10-2007-0061841 A (FREESCALE SEMICONDUCTOR, INC.) 14 June 2007 See abstract, claims 1-20 and figures 20, 21.	1-25
A	US 2010-0140589 A1 (MIHAI ADRIAN IONESCU) 10 June 2010 See abstract, paragraphs [0016]-[0023] and figure 1(a).	1-25
A	US 2012-0115296 A1 (WILLIAM G. VANDENDERGHE et al.) 10 May 2012 See abstract, claims 1-4 and figures 1-12.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 May 2015 (28.05.2015)

Date of mailing of the international search report

28 May 2015 (28.05.2015)

Name and mailing address of the ISA/KR

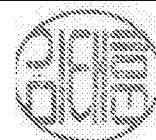
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