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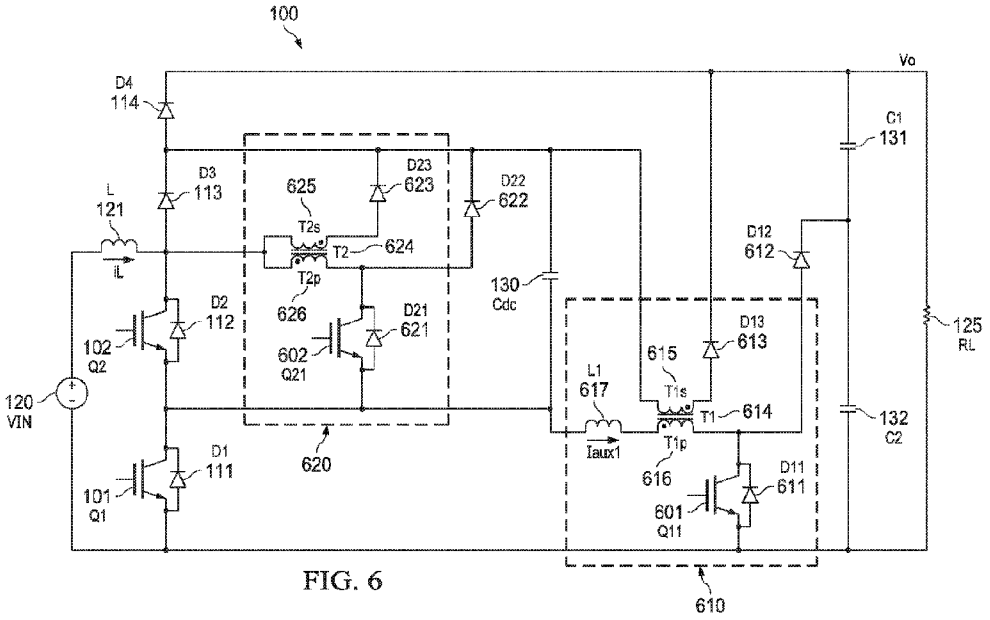


FIG. 6

(57) Abstract: An apparatus includes comprises an auxiliary switch, a transformer and an auxiliary diode. The auxiliary switch is configured to be turned on prior to turning on a first power switch of a multi-level boost converter. The transformer has a primary winding connected between the first power switch and the auxiliary switch. The auxiliary diode is coupled between a secondary winding of the transformer and an output terminal of the multi-level boost converter. The transformer and the auxiliary switch are configured such that the first power switch is of zero voltage switching, and the auxiliary switch is of zero current switching.

[Continued on next page]

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Boost Converter and Control Method

TECHNICAL FIELD

[0001] The present disclosure relates to an apparatus and method for achieving zero voltage switching in a multi-level power converter, and, in particular embodiments, to an apparatus and method for achieving zero voltage switching in a three-level boost converter.

BACKGROUND

[0002] Renewable energy sources include solar energy, wind power, tidal wave energy and the like. A solar power conversion system may include a plurality of solar panels connected in series or in parallel. The output of the solar panels may generate a variable dc voltage depending on a variety of factors such as time of day, location and sun tracking ability. In order to regulate the output of the solar panels, the output of the solar panels may be coupled to a power regulator so as to achieve a regulated output voltage at the output of the solar power conversion system. In addition, the solar panels may be connected with a backup battery system through a battery charge control apparatus. During the day, the backup battery is charged through the output of the solar panels. When the power utility fails or the solar panels are an off-grid power system, the backup battery provides electricity to the loads coupled to the solar panels.

[0003] To achieve an optimized solar power conversion system, boost converters may be used to get the maximum power out of the solar panels of the solar power conversion system. For example, a boost converter may be coupled between the output of a solar panel and an input of a solar inverter. The boost converter is controlled such that the output of the boost converter generates a suitable voltage source for the solar inverter coupled to the boost converter.

[0004] A boost converter comprises a switching element, a blocking device, at least one energy storage element and an output filter. The switching element may be implemented as a power transistor. The blocking device may be implemented as a diode. The energy storage element may be implemented as an inductor. The output filter may be implemented as a capacitor. The diode and the power transistor are connected in series across the capacitor. The inductor is coupled between an input power source and the common node of the diode and the power transistor. The boost converter is used to provide an output voltage higher than an input voltage from the input power source by modulating the width of a pulse applied to the power transistor.

SUMMARY

[0005] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present disclosure which provide an apparatus and method for achieving zero voltage switching in a three-level boost converter.

[0006] In accordance with an embodiment, a power converter comprises a first soft switching network and a second soft switching network. The first soft switching network is coupled to a low-side switch of the power converter. The first soft switching network comprises a first magnetic device and a first auxiliary switch. The first soft switching network is configured such that the low-side switch is of zero voltage switching, and the first auxiliary switch is of zero current switching. The second soft switching network is coupled to a high-side switch of the power converter. The second soft switching network comprises a second magnetic device and a second auxiliary switch. The second soft switching network is configured such that the high-side switch is of zero voltage switching, and the second auxiliary switch is of zero current switching.

[0007] The power converter comprises a first diode, a second diode, the high-side switch and the low-side switch connected in series between an output terminal of the power converter and ground. The power converter further comprises a flying capacitor connected between a common node of the first diode and the second diode, and a common node of the high-side switch and the low-side switch, and an inductor connected to a common node of the second diode and the high-side switch, and an input terminal of the power converter.

[0008] The power converter further comprises a first output capacitor and a second output capacitor connected in series between the output terminal of the power converter and ground, a first voltage clamping diode between the first soft switching network, and a common node of the first output capacitor and the second output capacitor, and a second voltage clamping diode between the second soft switching network and a positive terminal of the flying capacitor.

[0009] The first soft switching network comprises a transformer, the first auxiliary switch and a first auxiliary diode. A first terminal of a primary winding of the transformer is connected to the low-side switch. A second terminal of the primary winding of the transformer is connected to the first auxiliary switch. A first terminal of a secondary winding of the transformer is connected to a common node of the first diode and the second diode. A second terminal of the secondary winding of the transformer is connected to the output terminal of the power converter through the first auxiliary diode. The first terminal of the primary winding and the second terminal of the secondary winding share a same polarity. The power converter is a three-level boost converter.

[0010] In accordance with another embodiment, an apparatus comprises an auxiliary switch, a transformer and an auxiliary diode. The auxiliary switch is configured to be turned on prior to turning on a first power switch of a multi-level boost converter. The transformer has a primary winding connected between the first power switch and the auxiliary switch. The auxiliary diode is coupled between a secondary winding of the transformer and an output terminal of the multi-level boost converter. The transformer and the auxiliary switch are configured such that the first power switch is of zero voltage switching, and the auxiliary switch is of zero current switching.

[0011] In accordance with yet another embodiment, a method comprises providing a first soft switching network coupled to a low-side switch of a multi-level boost converter, wherein the first soft switching network comprises a first magnetic device and a first auxiliary switch. The method further comprises prior to a zero voltage turn-on transition of the low-side switch, turning on the first auxiliary switch, and after the zero voltage turn-on transition of the low-side switch, turning off the first auxiliary switch.

[0012] The method further comprises providing a second soft switching network coupled to a high-side switch of the multi-level boost converter, wherein the second soft switching network comprises a second magnetic device and a second auxiliary switch, prior to a zero voltage turn-on transition of the high-side switch, turning on the second auxiliary switch, and after the zero voltage turn-on transition of the high-side switch, turning off the second auxiliary switch.

[0013] An advantage of an embodiment of the present disclosure is achieving zero voltage switching for a three-level boost converter, thereby improving the efficiency, reliability and cost of the three-level boost converter.

[0014] The foregoing has outlined rather broadly the features and technical advantages of the present disclosure in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the disclosure will be described hereinafter which form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0016] Figure 1 illustrates a schematic diagram of a multi-level boost converter in accordance with various embodiments of the present disclosure;

[0017] Figure 2 illustrates a current flow of the three-level boost converter in the first operating mode in accordance with various embodiments of the present disclosure;

[0018] Figure 3 illustrates a current flow of the three-level boost converter 100 in the second operating mode in accordance with various embodiments of the present disclosure;

[0019] Figure 4 illustrates a current flow of the three-level boost converter in the third operating mode in accordance with various embodiments of the present disclosure;

[0020] Figure 5 illustrates a current flow of the three-level boost converter 100 in the fourth operating mode in accordance with various embodiments of the present disclosure;

[0021] Figure 6 illustrates a schematic diagram of the three-level boost converter comprising a first soft switching apparatus and a second soft switch apparatus in accordance with various embodiments of the present disclosure;

[0022] Figure 7 illustrates a timing diagram of various signals during a ZVS turn-on of the switch Q1 101 in accordance with various embodiments of the present disclosure; and

[0023] Figure 8 illustrates a timing diagram of various signals during a ZVS turn-on of the switch Q2 102 in accordance with various embodiments of the present disclosure.

[0024] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the various embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0025] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosure, and do not limit the scope of the disclosure.

[0026] The present disclosure will be described with respect to preferred embodiments in a specific context, namely a zero voltage switching three-level boost converter. The present disclosure may also be applied, however, to a variety of power converters. Hereinafter, various embodiments will be explained in detail with reference to the accompanying drawings.

[0027] Figure 1 illustrates a schematic diagram of a multi-level boost converter in accordance with various embodiments of the present disclosure. The multi-level boost converter 100 comprises an input inductor L 121, a first switch Q1 101, a second switch Q2 102, a first blocking device, a second blocking device, a flying capacitor Cdc 130 and two output capacitors C1 131 and C2 132. As shown in Figure 1, the multi-level boost converter 100 is coupled between an input power source VIN 120 and a load RL 125. The multi-level boost converter 100 shown in Figure 1 is a three-level boost converter. Throughout the description, the multi-level boost converter 100 is alternatively referred to as a three-level boost converter.

[0028] In some embodiments, the first blocking device is implemented as a first diode D3 113 as shown in Figure 1. The second blocking device is implemented as a second diode D4 114. Throughout the description, the first blocking device and the second blocking device are alternatively referred to as the first diode D3 113 and the second diode D4 114 respectively.

[0029] In comparison with a conventional boost converter, the second switch Q2 102, the first diode D3 113 and the flying capacitor Cdc 130 are employed to reduce voltage stresses on the switches and diodes. For example, the voltage rating of Q2 102 is one half of the voltage rating of Q1 101. Likewise, the voltage rating of D3 113 is one half of the voltage rating of D4 114.

[0030] As shown in Figure 1, the second diode D4 114, the first diode D3 113, the second switch Q2 102 and the first switch Q1 101 are connected in series between the positive output terminal of the three-level boost converter 100 and ground. Throughout the description, the first switch Q1 101 may be alternatively referred to as a low-side switch. The second switch Q2 102 may be alternatively referred to as a high-side switch.

[0031] The first output capacitor C1 131 and the second output capacitor C2 132 are connected in series. The input inductor L 121 is coupled between the input power source VIN 120 and a common node of the first diode D3 113 and the second switch Q2 102. The flying Cdc 130 has a first terminal connected to a common node of diodes D3 113 and D4 114, and a second terminal connected to a common node of switches Q1 101 and Q2 102 as shown in Figure 1.

[0032] In accordance with an embodiment, the switches (*e.g.,* switches Q1 101 and Q2 102) may be an insulated gate bipolar transistor (IGBT) device. Alternatively, the switching element can be any controllable switches such as metal oxide semiconductor field-effect transistor (MOSFET) devices, integrated gate commutated thyristor (IGCT) devices, gate turn-off thyristor (GTO) devices, silicon controlled rectifier (SCR) devices, junction gate field-effect transistor (JFET) devices, MOS controlled thyristor (MCT) devices, silicon carbide (SiC) devices, gallium nitride (GaN) devices and the like.

[0033] It should be noted that when switches Q1 101 and Q2 102 are implemented by MOSFET devices, the body diodes of switches Q1 101 and Q2 102 can be used to provide a freewheeling channel. On the other hand, when switches Q1 101 and Q2 102 are implemented by IGBT devices, a separate freewheeling diode (*e.g.,* D1 111 and D2 112) is required to be connected in parallel with its corresponding switch.

[0034] As shown in Figure 1, diodes D1 111 and D2 112 are required to provide reverse conducting paths for the three-level boost converter 100. In other words, diodes D1 111 and D2 112 are anti-parallel diodes. In some embodiments, diodes D1 111 and D2 112 are co-packaged with their respective IGBT devices. In alternative embodiments, didoes D1 111 and D2 112 are placed outside their respective IGBT devices.

[0035] The three-level boost converter 100 includes four different operating modes according to the on/off statuses of switches Q1 101 and Q2 102. In a first operating mode, switch Q1 101 is turned on and switch Q2 102 is turned off. The power from the input power source VIN

120 is used to charge the flying capacitor Cdc 130. The detailed operating principles of the first operating mode will be described below with respect to Figure 2.

[0036] It should be noted that, in the first operating mode, the current flowing through the input inductor L may ramp up or down depending on different combinations of the input voltage, the voltage across the flying capacitor and the output voltage.

[0037] In a second operating mode, switch Q2 102 is turned on and switch Q1 101 is turned off. The energy stored in the flying capacitor Cdc 130 is discharged to the output capacitors C1 131 and C2 132. It should be noted that, in the second operating mode, the current flowing through the input inductor L 121 may ramp up or down depending on different combinations of the input voltage, the voltage across the flying capacitor and the output voltage.

[0038] In a third operating mode, both switches Q1 101 and Q2 102 are turned off. The energy stored in the input inductor L 121 is used to charge the output capacitors C1 131 and C2 132. The detailed operating principles of the third operating mode will be described below with respect to Figure 4.

[0039] In a fourth operating mode, both switches Q1 101 and Q2 102 are turned on. The current flowing through the input inductor L 121 ramps up and energy is stored in the input inductor L 121 accordingly. The detailed operating principles of the fourth operating mode will be described below with respect to Figure 5.

[0040] Figure 2 illustrates a current flow of the three-level boost converter in the first operating mode in accordance with various embodiments of the present disclosure. During the first operating mode, switch Q2 102 is turned off as indicated by the arrow placed on top of the symbol of Q2 102. Since switch Q1 101 is turned on, a conductive path is established as indicated by the dashed line 202 shown in Figure 2. The conductive path is formed by L 121, D3 113, Cdc 130 and Q1 101. The current flows from the positive terminal of the input power source VIN 120 to the negative terminal of the input power source VIN 120 through the conductive path shown in Figure 2.

[0041] During the first operating mode, the flying capacitor Cdc 130 is charged and energy is stored in the flying capacitor Cdc 130 accordingly. The current flowing through the inductor L 121 may ramp up or down depending on the voltage applied across the inductor L 121. More particularly, when VIN 120 is greater than the voltage across Cdc 130, the current flowing through the inductor L 121 ramps up and the energy stored in the inductor L 121 increases accordingly. When the voltage across Cdc 130 is greater than VIN 120, the current flowing through the inductor L 121 ramps down and the energy stored in the inductor L 121 decreases accordingly.

[0042] Figure 3 illustrates a current flow of the three-level boost converter 100 in the second operating mode in accordance with various embodiments of the present disclosure. During the second operating mode, switch Q1 101 is turned off as indicated by the arrow placed on top of the symbol of Q1 101. Since switch Q2 102 is turned on, a conductive path is established as indicated by the dashed line 302 shown in Figure 3. The conductive path is formed by inductor L 121, Q2 102, Cdc 130, D4 114 and C1 131/C2 132. The current flows from the positive terminal of the input power source VIN 120 to the negative terminal of the input power source VIN 120 through the conductive path shown in Figure 3.

[0043] During the second operating mode, the flying capacitor Cdc 130 is discharged to the load RL 125 and the output capacitors C1 131/C2 132. The current flowing through the inductor L 121 may ramp up or down depending on the voltage applied across the inductor L 121. More particularly, when the sum of VIN 120 and the voltage across Cdc 130 is greater than the output voltage Vo, the current flowing through the inductor L 121 ramps up and the energy stored in the inductor L 121 increases accordingly. When the sum of VIN 120 and the voltage across Cdc 130 is less than the output voltage Vo, the current flowing through the inductor L 121 ramps down and the energy stored in the inductor L 121 decreases accordingly. It is understood that current does not flow through D3 113 as a result of reverse bias within the three-level boost converter 100.

[0044] Figure 4 illustrates a current flow of the three-level boost converter in the third operating mode in accordance with various embodiments of the present disclosure. During the third operating mode, both switches Q1 101 and Q2 102 are turned off as indicated by the arrows placed on top of the symbols of Q1 101 and Q2 102. A conductive path is established as indicated by the dashed line 402 shown in Figure 4. The conductive path is formed by inductor L 121, D3 113, D4 114 and C1 131/C2 132. The current flows from the positive terminal of the input power source VIN 120 to the negative terminal of the input power source VIN 120 through the conductive path shown in Figure 4. During the third operating mode, the energy stored in the inductor L 121 is discharged to the load RL 125 and the output capacitor C1 131/C2 132. As a result, the current flowing through the inductor L 121 ramps down.

[0045] Figure 5 illustrates a current flow of the three-level boost converter 100 in the fourth operating mode in accordance with various embodiments of the present disclosure. During the fourth operating mode, both switches Q1 101 and Q2 102 are turned on. A conductive path is established as indicated by the dashed line 502 shown in Figure 5. The conductive path is formed by inductor L 121, Q2 102 and Q1 101. The current flows from the positive terminal of the input power source VIN 120 to the negative terminal of the input power source VIN 120 through the conductive path shown in Figure 5. During the fourth operating mode, the current flowing

through the inductor L 121 ramps up and the energy stored in the inductor L 121 increases accordingly.

[0046] Referring back to Figure 1, during steady operation, the duty cycle of Q1 101 is equal to the duty cycle of Q2 102. According to the volt-second balance principle, the voltage at the output of the three-level boost converter 100 is given by the following equation:

$$Vo = \frac{Vin}{1 - D} \qquad (1)$$

where D is the steady state duty cycle of switches Q1 101 and Q2 102, Vo is the output voltage, and VIN 120 is the input voltage.

[0047] In some embodiments, the voltage across the capacitor Cdc 130 is adjustable through changing the duty cycles of Q1 101 and Q2 102. More particularly, the voltage across Cdc 130 may increase by operating the converter under a condition satisfying the duty cycle of Q1 101 is greater than the duty cycle of Q2 102. On the other hand, the voltage across Cdc 130 may decrease by operating the converter under a condition satisfying the duty cycle of Q1 101 is less than the duty cycle of Q2 102.

[0048] While the voltage across Cdc 130 is adjustable, during steady operation the voltage across Cdc 130 may stay a stable voltage and the duty cycle of Q1 101 is equal to the duty cycle of Q2 102. A controller (not shown) including a feedback loop may be used to monitor the voltage across Cdc 130 so as to maintain the voltage across Cdc 130 stable during steady operation. For example, if the voltage across Cdc 130 is not stable, the controller may slightly adjust the duty cycle of Q1 101 and/or the duty cycle of Q2 102 to achieve a stable voltage across Cdc 130. The feedback loop may comprise a predetermined threshold. The controller may regulate the voltage across Cdc 130 through increasing a duty cycle of the second switch when the voltage across the capacitor Cdc 130 is greater than the predetermined threshold and increasing a duty cycle of the first switch when the predetermined threshold is greater than the voltage across the capacitor Cdc 130.

[0049] It should be noted that while the example throughout the description is based upon a non-isolated boost converter, the three-level boost converter 100 shown in Figure 1 may have many variations, alternatives, and modifications. For example, the three-level boost converter 100 shown in Figure 1 may include a transformer to achieve an isolated three-level boost converter. The non-isolated topology illustrated herein is limited solely for the purpose of clearly illustrating the aspects of the various embodiments. The present disclosure is not limited to any particular power topology.

[0050] As example embodiments, in different voltage applications Q1 101 and D3 114 in the three-level boost converter 100 may be implemented using different ratings. For example, in a 1000 V solar application, Q1 101 and D3 114 can be implemented as semiconductor devices having a voltage rating of 1200 V. Q2 102 and D3 113 can be implemented as semiconductor devices having a voltage rating of 600 V.

[0051] In another example, in a 1200 V solar application, the voltage across Cdc 130 is set to 500 V. As a result, the voltage stresses across Q2 102 and D3 113 are about 500 V. Q2 102 and D3 113 can be implemented as semiconductor devices having a voltage rating of 650 V. The voltage stresses across Q1 101 and D3 114 are equal to the difference between the output voltage (1200 V) of the three-level boost converter and the voltage across Cdc 130. In other words, the voltage stresses across Q1 101 and D3 114 are about 700 V. Since the voltage stresses across Q2 102 and D3 113 are low, the switching losses are reduced accordingly.

[0052] One advantageous feature of having low voltage rating devices (*e.g.,* Q2 102 and D3 113) is the low voltage stresses on Q2 102 and D3 113 help to reduce conduction losses as well as switching losses. As a result, the efficiency of the three-level boost converter 100 is improved.

[0053] Figure 6 illustrates a schematic diagram of the three-level boost converter comprising a first soft switching apparatus and a second soft switch apparatus in accordance with various embodiments of the present disclosure. The three-level boost converter 100 comprises a first soft switching apparatus 610 and a second soft switching apparatus 620. The three-level boost converter 100 further comprises a first voltage clamping diode D12 612 and a second voltage clamping diode D22 622. In some embodiments, by employing the first soft switching apparatus 610 and the second soft switching apparatus 620, the power switches (*e.g.*, Q1 101 and Q2 102) are able to achieve zero voltage switching (ZVS). The power diodes (*e.g.*, D3 113 and D3 114) are able to achieve zero current switching (ZCS). The ZVS operation of the power switches and the ZCS operation of the diodes help to reduce the switching losses of the three-level boost converter 100.

[0054] As shown in Figure 6, the first voltage clamping diode D12 612 is connected between the first soft switching apparatus 610, and a common node of output capacitors C1 131 and C2 132. The first voltage clamping diode D12 612 is employed to clamp the voltage of the first soft switching apparatus 610 to a voltage level approximately equal to one half of the output voltage of the three-level boost converter 100, thereby preventing the first soft switching apparatus 610 from being damaged by excessive voltages.

[0055] As shown in Figure 6, the second voltage clamping diode D22 622 is connected between the second soft switching apparatus 620 and the positive terminal of the flying capacitor Cdc 130. The second voltage clamping diode D22 622 is employed to clamp the voltage of the

second soft switching apparatus 620 to a voltage level approximately equal to one half of the output voltage of the three-level boost converter 100, thereby preventing the second soft switching apparatus 620 from being damaged by excessive voltages.

[0056] The first soft switching apparatus 610 is coupled to the switch Q1 101. In operation, the first soft switching apparatus 610 is employed to achieve ZVS during the turn-on process of the switch Q1 101. The second soft switching apparatus 620 is coupled to the switch Q2 102. In operation, the second soft switching apparatus 620 is employed to achieve ZVS during the turn-on process of the switch Q2 102.

[0057] The first soft switching apparatus 610 comprises a first magnetic device, a first auxiliary switch Q11 601 and a first auxiliary diode D13 613. In some embodiments, the first magnetic device is implemented as a first transformer T1 614 comprising a primary winding T1p 616 and a secondary winding T1s 615 as shown in Figure 6.

[0058] A first terminal of the primary winding T1p 616 is connected to a common node of switches Q1 101 and Q2 102. A second terminal of the primary winding T1p 616 is connected to a common node of the first auxiliary switch Q11 601 and the first voltage clamping diode D12 612. A first terminal of the secondary winding T1s 615 is connected to a common node of diodes D3 113 and D3 114. A second terminal of the secondary winding T1s 615 is connected to an output terminal of the three-level boost converter 100 through the first auxiliary diode D13 613.

[0059] The transformer T1's polarities are indicated in Figure 6 as dots next to the terminals of the primary winding T1p 616 and the secondary winding T1s 615. In particular, the transformer T1 614 has polarity dots at opposing terminals of the primary winding T1p 616 and the secondary winding T1s 615. Such a polarity dot arrangement indicates the currents flowing through two windings are instantaneously out-of-phase with respect to a common ground. In other words, the dot notation indicates the primary side T1p 616 and the secondary side T1s 615 are out of phase by 180 degrees. The operation of a transformer is well known in the art, and hence is not discussed in further detail herein.

[0060] The second soft switching apparatus 620 comprises a second magnetic device, a second auxiliary switch Q21 602, a second auxiliary diode D23 623. In some embodiments, the second magnetic device is implemented as a second transformer T2 624 comprising a primary winding T2p 626 and a secondary winding T2s 625 as shown in Figure 6.

[0061] A first terminal of the primary winding T2p 626 is connected to a common node of switch Q2 102 and diode D3 113. A second terminal of the primary winding T2p 626 is connected to a common node of the second auxiliary switch Q21 602 and the second voltage clamping diode D22 622. A first terminal of the secondary winding T2s 625 is connected to the first terminal of

the primary winding T2p 626. A second terminal of the secondary winding T2s 625 is connected to a common node of diodes D3 113 and D3 114 through the second auxiliary diode D23 623.

[0062] The second transformer T2's polarities are indicated in Figure 6 as dots next to the terminals of the primary winding T2p 626 and the secondary winding T2s 625. In particular, the transformer T2 624 has polarity dots at opposing terminals of the primary winding T2p 626 and the secondary winding T2s 625. Such a polarity dot arrangement indicates the currents flowing through two windings are instantaneously out-of-phase with respect to a common ground.

[0063] In accordance with an embodiment, the auxiliary switches (*e.g.,* switches Q11 601 and Q21 602) may be IGBT devices. Alternatively, the auxiliary switches can be any controllable switches such as MOSFET devices, IGCT devices, GTO devices, SCR devices, JFET devices, MCT devices, SiC devices, GaN devices and the like.

[0064] As shown in Figure 6, auxiliary switches Q11 601 and Q21 602 are implemented as IGBT devices. Separate freewheeling diodes (*e.g.,* D11 611 and D21 621) are required to be connected in parallel with respective switches. In some embodiments, diodes D11 611 and D21 621 are co-packaged with their respective IGBT devices. In alternative embodiments, didoes D11 611 and D21 621 are placed outside their respective IGBT devices.

[0065] In operation, the first auxiliary switch Q11 601 is turned on before turning on the switch Q1 101. In response to the turn-on of Q11 601, an auxiliary current Iaux1 flows through the primary winding T1p 616. The input voltage VIN 120 is applied to the leakage inductance L1 617 of the transformer T1 614. As a result of applying the input voltage to the leakage inductance L1 617 of the transformer T1 614, the auxiliary current Iaux1 ramps up. Once the auxiliary current Iaux1 reaches the load current iL, the collector-emitter capacitance of Q1 101 and the leakage inductance L1 617 of the transformer T1 614 form a resonant circuit. The resonant current generated by the resonant circuit discharges the voltage across the collector-emitter capacitance of the switch Q1 101 to a voltage level approximately equal to zero. After a suitable delay, the switch Q1 101 is turned on under a collector-emitter voltage approximately equal to zero. As such, the switch Q1 101 is able to achieve ZVS during a turn-on process.

[0066] After the switch Q1 101 has been turned on and before the first auxiliary switch Q11 601 is turned off, the primary winding T1p 616 is shorted by the turned-on switches Q1 101 and Q11 601. At the secondary side of the transformer T1 614, the current flows through the first auxiliary diode D13 613. The turned-on D13 613 pulls the voltage at the second terminal of T1s 615 to a voltage level approximately equal to the output voltage Vo. The voltage across the flying capacitor Cdc 130 is equal to one half of the output voltage Vo. In addition, the switch Q1 101 is turned on. As such, the voltage at the first terminal of T1s 615 is equal to one half of the output voltage Vo. In sum, a negative voltage is across the first terminal and the second terminal of T1s

615. Such a negative voltage is reflected to the primary side T1p 616 and applied to the leakage inductance L1 617 of T1 614. In response to this reflected voltage applied to the leakage inductance L1 617, the auxiliary current Iaux1 reduces in a linear manner. After the auxiliary current Iaux1 reaches zero, the first auxiliary switch Q11 601 can be turned off under ZCS.

[0067] The operating principle of the second soft switching apparatus 620 is similar to that of the first soft switching apparatus 610, and hence is not discussed again to avoid repetition. It should be noted that the auxiliary switches Q11 601 and Q21 602 are able to achieve ZCS during the turn-on and the turn-off processes of these two switches. Furthermore, the auxiliary diodes D13 613 and D23 623 are able to achieve ZCS during the turn-on and the turn-off processes. The ZCS turn-on and turn-off of the auxiliary components (*e.g.*, Q11 601, Q21 602, D13 613 and D23 623) help to reduce the switching losses of the three-level boost converter 100.

[0068] During a startup process of the three-level boost converter 100, the first voltage clamping diode D12 612 may function as a charging diode. More particularly, the output capacitors (*e.g.*, C2 132) may be charged by a current flowing through the first voltage clamping diode D12 612. When the capacitance values of the output capacitors C1 131 and C2 132 are much greater than the capacitance value of the flying capacitor Cdc 130, the voltage balance between the output capacitors C1 131 and C2 132 is determined by the capacitance values of the output capacitors C1 131 and C2 132. When the capacitance values of the output capacitors C1 131 and C2 132 are similar to the capacitance value of the flying capacitor Cdc 130, the voltage balance between the output capacitors C1 131 and C2 132 can be achieved by adjusting the capacitance values of the output capacitors C1 131 and C2 132.

[0069] Figure 7 illustrates a timing diagram of various signals during a ZVS turn-on of the switch Q1 101 in accordance with various embodiments of the present disclosure. The horizontal axis of Figure 7 represents intervals of time. There may be five vertical axes. The first vertical axis Y1 represents the voltage across the gate and emitter of Q1 101 (gate drive voltage of Q1 101). The second vertical axis Y2 represents the voltage across the collector and emitter of Q1 101. The third vertical axis Y3 represents the voltage across the gate and emitter of Q11 601 (gate drive voltage of Q11 601). The fourth vertical axis Y4 represents the auxiliary current flowing through the primary winding of the transformer T1 614. The fifth vertical axis Y5 represents the current flowing through the inductor L 121.

[0070] Referring back to Figure 6, both the switch Q1 101 and the auxiliary switch Q11 601 are implemented as IGBT devices. As such, the voltage across the switch Q1 101 is referred to as V_{CE_Q1}. The gate-to-emitter voltage of the switch Q1 101 is referred to as V_{GE_Q1}. The gate-to-emitter voltage of the auxiliary switch Q11 601 is referred to as V_{GE_Q11}. The current flowing

through the primary winding of the transformer T1 614 is referred to as Iaux1. The current flowing through the inductor of the output filter is referred to as iL (a.k.a. load current).

[0071] During the time interval from t0 to t1, the switch Q1 101 is turned off. The auxiliary switch Q11 601 is turned off. At the time instant t1, the auxiliary switch Q11 601 is turned on in response to a voltage applied to the gate of the auxiliary switch Q11 601. The current flowing into the auxiliary switch Q11 601 may not change instantaneously since the auxiliary switch Q11 601 is connected in series with the primary side T1p 616 of transformer T1 614. As shown in Figure 7, the current Iaux1 ramps up from zero to a value of about iL at the time instant t2. The ramp-up slope exhibits an approximately linear behavior as shown in Figure 7. The ramp-up slew rate is determined by the value of the leakage inductance L1 617. The ramp-up slew rate can be adjusted by changing the value of the leakage inductance L1 617.

[0072] During the time interval from t2 to t3, the voltage V_{CE_Q1} across the switch Q1 101 may be discharged by a resonant process generated by the leakage inductance L1 617 of the transformer T1 614 and the collector-to-emitter capacitance of Q1 101. As shown in Figure 7, the voltage V_{CE_Q1} across the switch Q1 101 drops to a voltage level approximately equal to zero at the time instant t3. After a suitable delay, at the time instant t4, the switch Q1 101 is turned on. As shown in Figure 7, the voltage V_{CE_Q1} across the switch Q1 101 is equal to zero at the time instant t4. The switch Q1 101 is able to achieve ZVS during the turn-on process.

[0073] During the time interval from t4 to t5, a negative voltage is applied to the secondary winding of the transformer T1 614. Such a negative voltage is reflected to the primary side of the transformer T1 614. The reflected voltage is applied to the leakage inductance L1 617. In response to the reflected voltage applied to the leakage inductance L1 617, the current flowing through the leakage inductance reduces in a linear manner as shown in Figure 7. At the time instant t5, the auxiliary current Iaux1 drops to a current level approximately equal to zero. After a suitable delay, at the time instant t6, the auxiliary switch Q11 601 is turned off. As shown in Figure 7, the current flowing through the auxiliary switch Q11 601 is equal to zero at the time instant t6. The auxiliary switch Q11 601 is able to achieve ZCS during the turn-off process.

[0074] One advantageous feature of the first soft switching network is that the switch Q1 101 may achieve a zero voltage turn-on and the auxiliary switches (*e.g.*, Q11 601) are of a zero current turn-off. Such zero voltage switching and zero current switching help to reduce the total power losses of the three-level boost converter 100 shown in Figure 1.

[0075] Referring back to Figure 6, the semiconductor devices shown in Figure 6 may comprise parasitic capacitance and/or inductance. For example, the first voltage clamping diode D12 612 may have a parasitic inductance of about 300 nH, which is connected in series with the first voltage clamping diode D12 612. The first auxiliary switch Q11 601 may have a collector-to-

emitter capacitance of 100 pF. The leakage inductance of the first transformer T1 614 is about 100 uH. The first switch Q1 101 may have a collector-to-emitter capacitance of 600 pF. The load current is about 19.2 A. The RMS value of the auxiliary current is about 1.6 A. The average value of the auxiliary current is about 0.8 A. Under the operating conditions above, the parasitic inductance of the first voltage clamping diode D12 612 does not have a negative impact on the voltage stresses of the three-level boost converter 100.

[0076] Figure 8 illustrates a timing diagram of various signals during a ZVS turn-on of the switch Q2 102 in accordance with various embodiments of the present disclosure. The horizontal axis of Figure 8 represents intervals of time. There may be five vertical axes. The first vertical axis Y1 represents the voltage across the gate and emitter of Q2 102 (gate drive voltage of Q2 102). The second vertical axis Y2 represents the voltage across the collector and emitter of Q2 102. The third vertical axis Y3 represents the voltage across the gate and emitter of Q21 602 (gate drive voltage of Q11 601). The fourth vertical axis Y4 represents the auxiliary current flowing through the primary winding of the transformer T2 624. The fifth vertical axis Y5 represents the current flowing through the inductor L 121.

[0077] The turn-on process of the switch Q2 102 and the turn-off process of the auxiliary switch Q21 602 are similar to the turn-on process of the switch Q1 101 and the turn-off process of the auxiliary switch Q11 601 shown in Figure 8, and hence are not discussed in detail herein.

[0078] Although embodiments of the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims.

[0079] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. The specification and drawings are, accordingly, to be regarded simply as an illustration of the disclosure as defined by the appended claims, and are contemplated to cover any and all modifications, variations, combinations or equivalents that fall within the scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A power converter comprising:

a first soft switching network coupled to a low-side switch of the power converter, wherein the first soft switching network comprises a first magnetic device and a first auxiliary switch, and wherein the first soft switching network is configured such that the low-side switch is of zero voltage switching, and the first auxiliary switch is of zero current switching; and

a second soft switching network coupled to a high-side switch of the power converter, wherein the second soft switching network comprises a second magnetic device and a second auxiliary switch, and wherein the second soft switching network is configured such that the high-side switch is of zero voltage switching, and the second auxiliary switch is of zero current switching.

2. The power converter of claim 1, wherein the power converter comprises:

a first diode, a second diode, the high-side switch and the low-side switch connected in series between an output terminal of the power converter and ground;

a flying capacitor connected between a common node of the first diode and the second diode, and a common node of the high-side switch and the low-side switch; and

an inductor connected to a common node of the second diode and the high-side switch, and an input terminal of the power converter.

3. The power converter of any one of claims 1-2, wherein the power converter further comprises:

a first output capacitor and a second output capacitor connected in series between the output terminal of the power converter and ground;

a first voltage clamping diode between the first soft switching network, and a common node of the first output capacitor and the second output capacitor; and

a second voltage clamping diode between the second soft switching network and a positive terminal of the flying capacitor.

4. The power converter of any one of claims 1-3, wherein:

the first magnetic device is a transformer.

5. The power converter of any one of claims 1-4, wherein:

the first soft switching network comprises the transformer, the first auxiliary switch and a first auxiliary diode.

6. The power converter of any one of claims 1-5, wherein:

a first terminal of a primary winding of the transformer is connected to the low-side switch;

a second terminal of the primary winding of the transformer is connected to the first auxiliary switch;

a first terminal of a secondary winding of the transformer is connected to a common node of the first diode and the second diode; and

a second terminal of the secondary winding of the transformer is connected to the output terminal of the power converter through the first auxiliary diode, and wherein the first terminal of the primary winding and the second terminal of the secondary winding share a same polarity.

7. The power converter of any one of claims 1-5, wherein:

the high-side switch and the low-side switch are IGBT devices.

8. The power converter of any one of claims 1-7, wherein:

an anode of the first diode is connected to a cathode of the second diode; and

an emitter of the high-side switch is connected to a collector of the low-side switch.

9. The power converter of any one of claims 1-7, wherein:

the first auxiliary switch is an IGBT.

10. The power converter of any one of claims 1-9, wherein:

the power converter is a three-level boost converter.

11. An apparatus comprising:

an auxiliary switch configured to be turned on prior to turning on a first power switch of a multi-level boost converter;

a transformer having a primary winding connected between the first power switch and the auxiliary switch; and

an auxiliary diode coupled between a secondary winding of the transformer and an output terminal of the multi-level boost converter, wherein the transformer and the auxiliary switch are configured such that the first power switch is of zero voltage switching, and the auxiliary switch is of zero current switching.

12. The apparatus of claim 11, wherein the multi-level boost converter is a three-level boost converter comprising:

a first diode, a second diode, a second power switch and the first power switch connected in series between the output terminal of the three-level boost converter and ground;

a flying capacitor connected between a common node of the first diode and the second diode, and a common node of the second power switch and the first power switch;

an inductor connected to a common node of the second diode and the second power switch, and an input terminal of the three-level boost converter; and

a first output capacitor and a second output capacitor connected in series between the output terminal of the three-level boost converter and ground.

13. The apparatus of any one of claims 11-12, wherein:

the primary winding is connected between a collector of the first power switch and a collector of the auxiliary switch; and

the secondary winding is connected to the output terminal of the multi-level boost converter through the first diode and the auxiliary diode respectively.

14. The apparatus of any one of claims 11-13, wherein:

a first terminal of the primary winding is connected to the collector of the first power switch;

a second terminal of the primary winding is connected to the collector of the auxiliary switch;

a first terminal of the secondary winding is connected to a common node of the first diode and the second diode; and

a second terminal of the secondary winding is connected to the output terminal of the multi-level boost converter through the auxiliary diode.

15. The apparatus of any one of claims 11-15, wherein:

the first terminal of the primary winding and the second terminal of the secondary winding share a same polarity.

16. A method comprising:

providing a first soft switching network coupled to a low-side switch of a multi-level boost converter, wherein the first soft switching network comprises a first magnetic device and a first auxiliary switch;

prior to a zero voltage turn-on transition of the low-side switch, turning on the first auxiliary switch; and

after the zero voltage turn-on transition of the low-side switch, turning off the first auxiliary switch.

17. The method of claim 16, further comprising:

providing a second soft switching network coupled to a high-side switch of the multi-level boost converter, wherein the second soft switching network comprises a second magnetic device and a second auxiliary switch;

prior to a zero voltage turn-on transition of the high-side switch, turning on the second auxiliary switch; and

after the zero voltage turn-on transition of the high-side switch, turning off the second auxiliary switch.

18. The method of any one of claims 16-17, wherein the multi-level boost converter comprises:

a first diode, a second diode, the high-side switch and the low-side switch connected in series between an output terminal of the multi-level boost converter and ground;

a flying capacitor connected between a common node of the first diode and the second diode, and a common node of the high-side switch and the low-side switch;

an inductor connected to a common node of the second diode and the high-side switch, and an input terminal of the multi-level boost converter; and

a first output capacitor and a second output capacitor connected in series between the output terminal of the multi-level boost converter and ground.

19. The method of any one of claims 16-18, wherein the first magnetic device is a first transformer, and the first soft switching network further comprises a first auxiliary diode, and wherein:

a primary winding of the first transformer is connected between the low-side switch and the first auxiliary switch; and

the first auxiliary diode is coupled between a secondary winding of the first transformer and the output terminal of the multi-level boost converter, and wherein the first transformer and the first auxiliary switch are configured such that the low-side switch is of zero voltage switching, and the first auxiliary switch is of zero current switching.

20. The method of any one of claims 16-18, wherein the second magnetic device is a second transformer, and the second soft switching network further comprises a second auxiliary diode, and wherein:

a primary winding of the second transformer is connected between the high-side switch and the second auxiliary switch; and

the second auxiliary diode is coupled between a secondary winding of the second transformer and a common node of the first diode and the second diode, and wherein the second transformer and the second auxiliary switch are configured such that the high-side switch is of zero voltage switching, and the second auxiliary switch is of zero current switching.

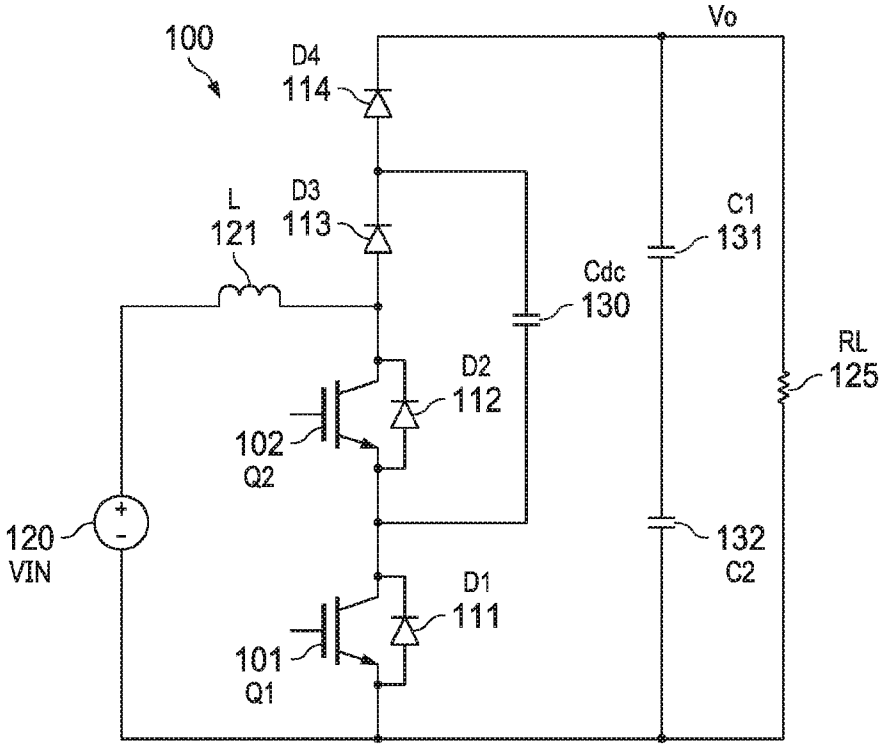

100
Vo
D4
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L
121
D3
113
C1
131
Cdc
130
RL
125
D2
112
102
Q2
120
VIN
132
C2
D1
111
101
Q1

FIG. 1

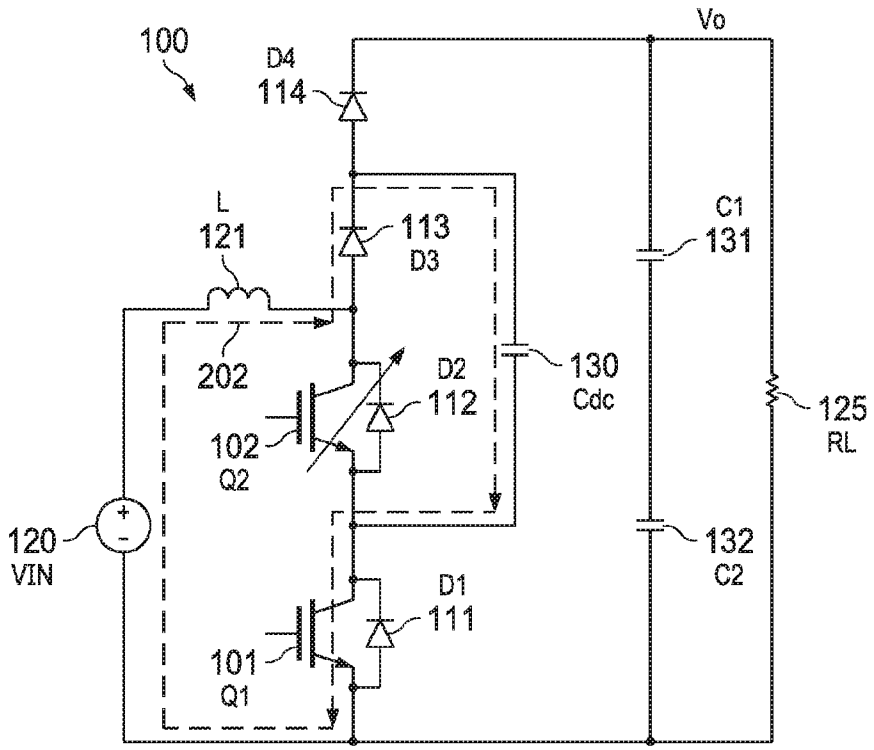

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D2
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Q2
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VIN
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C2
D1
111
101
Q1

FIG. 2

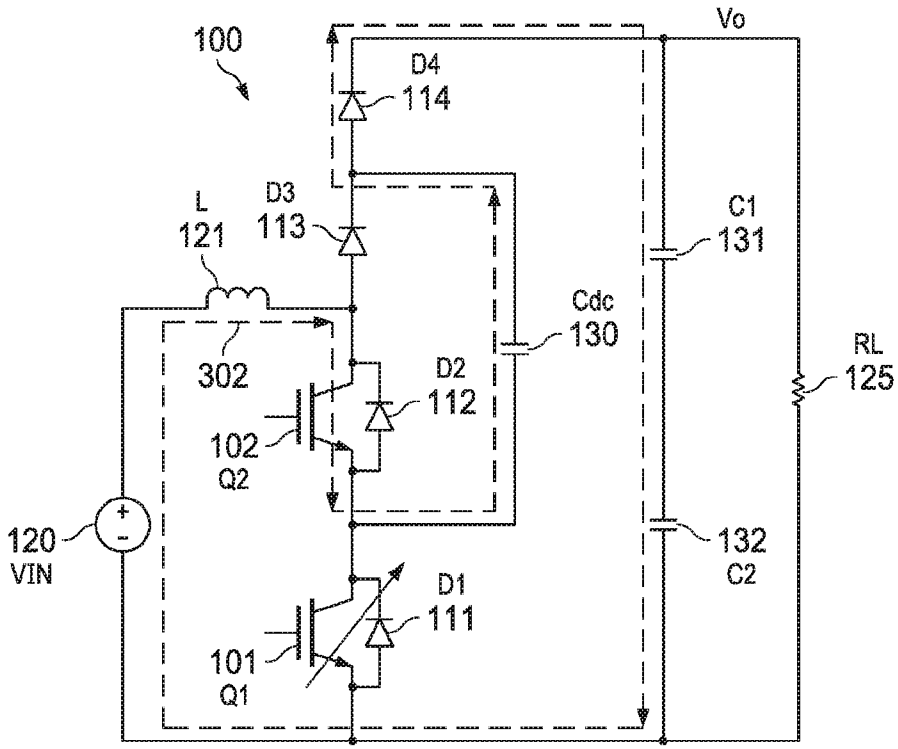

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VIN
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101
Q1

FIG. 3

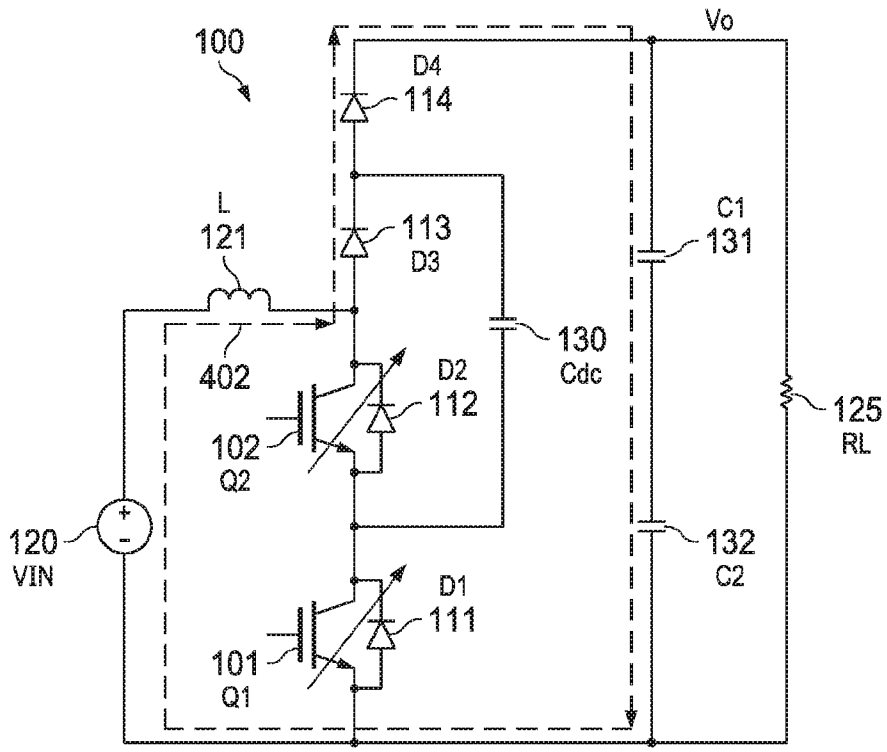

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131
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Cdc
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Q2
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C2
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Q1

FIG. 4

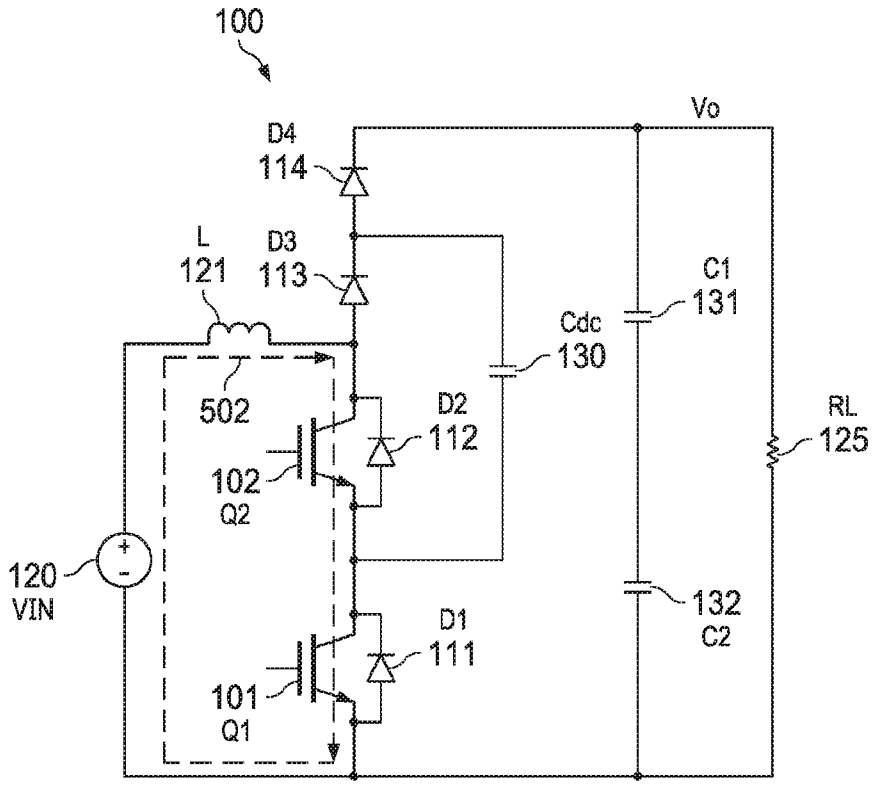

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Q1

FIG. 5

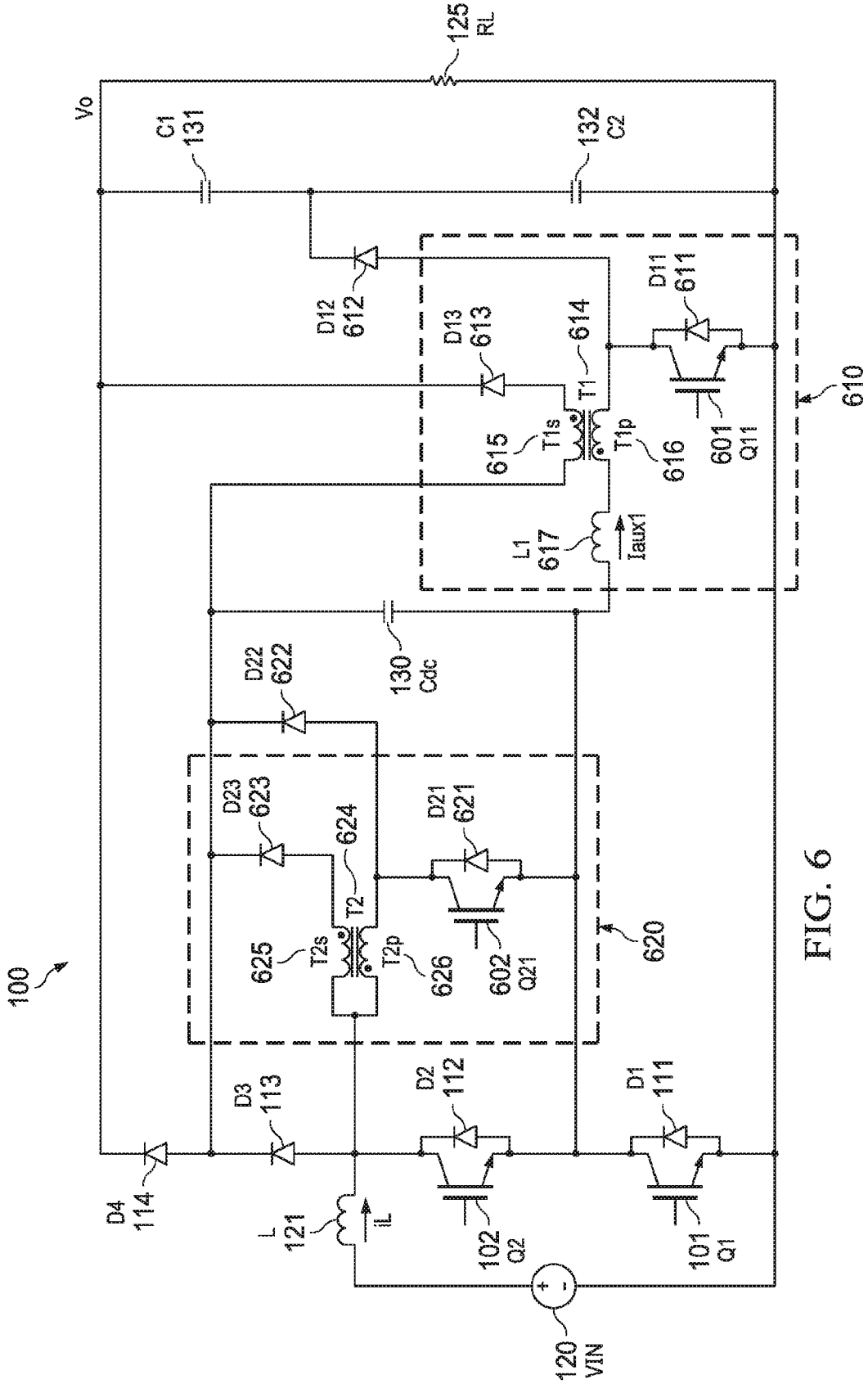

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Vo
125
RL
C1
131
132
C2
D12
612
D13
613
614
T1
D11
611
610
615
T1s
T1p
616
601
Q11
L1
617
Iaux1
130
Cdc
D22
622
D23
623
624
T2
D21
621
625
T2s
T2p
626
602
Q21
620
D3
113
D2
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D1
111
D4
114
L
121
iL
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Q2
101
Q1
120
VIN

FIG. 6

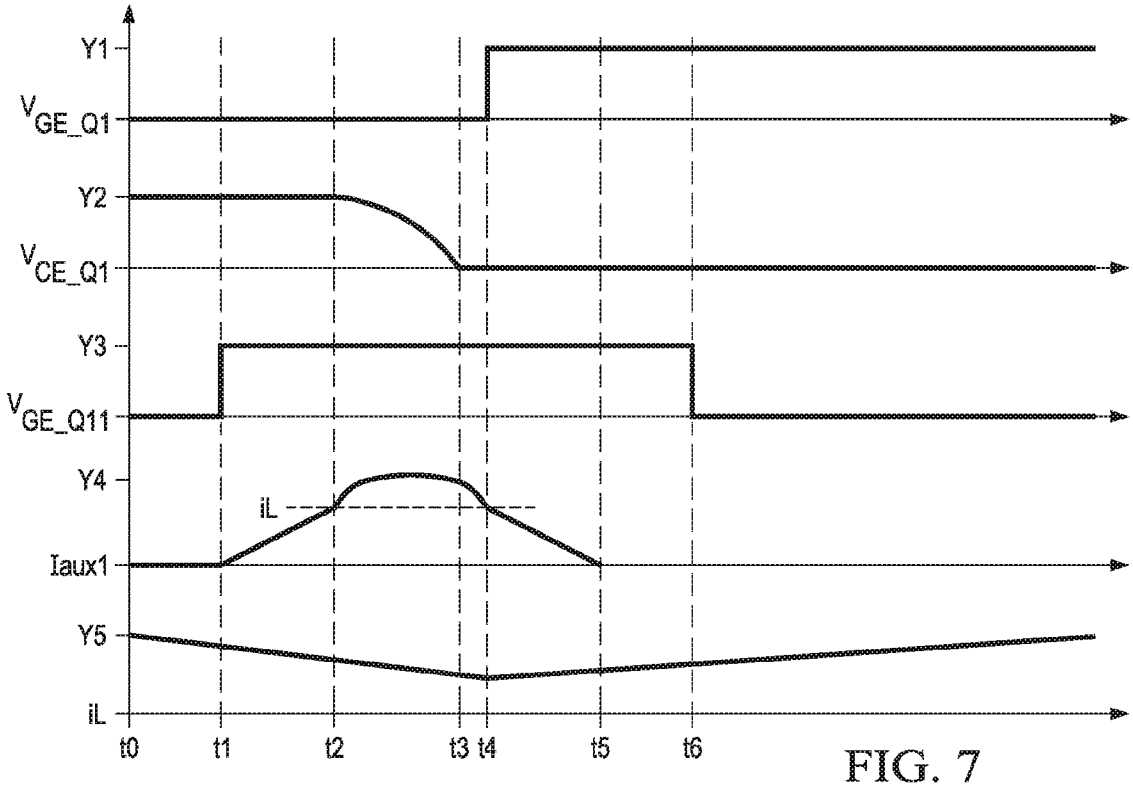

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Y2
VCE_Q1
Y3
VGE_Q11
Y4
iL
Iaux1
Y5
iL
t0
t1
t2
t3
t4
t5
t6

FIG. 7

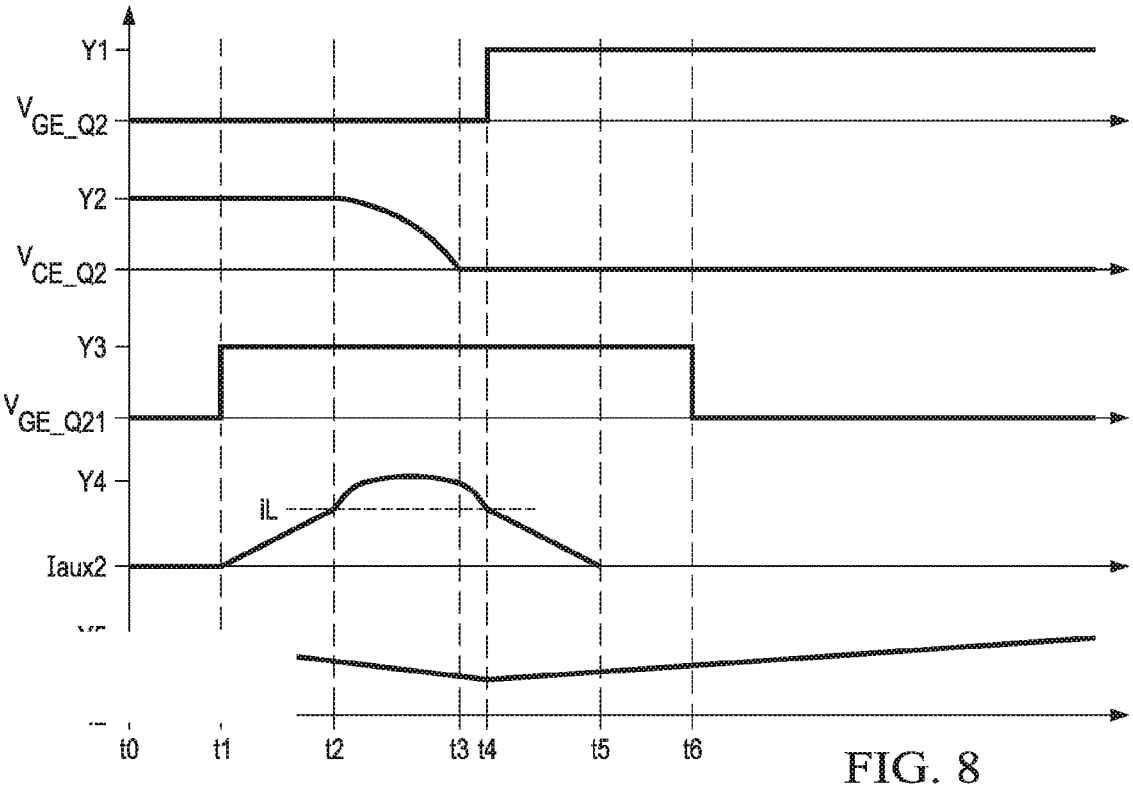

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Y2
VCE_Q2
Y3
VGE_Q21
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Iaux2
t0
t1
t2
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t4
t5
t6

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/033230

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158 H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2018/069490 A1 (FU DIANBO [US]) 8 March 2018 (2018-03-08) figure 3 paragraph [0005] - paragraph [0007] paragraph [0055] paragraph [0072] - paragraph [0075] paragraph [0089] -----	1,2,11, 12,16-18 3-10, 13-15, 19,20
X A	US 2017/163163 A1 (JANG YUNGTAEK [US] ET AL) 8 June 2017 (2017-06-08) figure 2 figure 3b figure 14 paragraph [0032] - paragraph [0034] paragraph [0036] - paragraph [0037] ----- -/--	1,2,11, 12,16-19 3-10, 13-15,20

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 January 2020	29/01/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Riehl, Philippe

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/033230

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2014/313627 A1 (LI TIN-HO [CN] ET AL) 23 October 2014 (2014-10-23) figures 4a-4b figure 7j paragraph [0031] - paragraph [0037] paragraph [0067] paragraph [0071]	1,2,11, 12,16-18 3-10, 13-15, 19,20
A	ASMARASHID BIN PONNIRAN ET AL: "Size Reduction of DC-DC Converter using Flying Capacitor Topology with Small Capacitance", IEEJ JOURNAL OF INDUSTRY APPLICATIONS, vol. 3, no. 6, 1 January 2014 (2014-01-01) , pages 446-454, XP055660180, ISSN: 2187-1094, DOI: 10.1541/ieejjia.3.446 figure 1	1-20
A	US 2015/244284 A1 (FU DIANBO [US]) 27 August 2015 (2015-08-27) figure 8	1-20
A	US 2005/226012 A1 (JOVANOVIC MILAN M [US] ET AL) 13 October 2005 (2005-10-13) figure 1	1-20

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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