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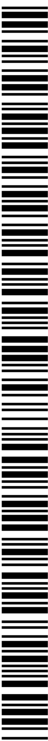

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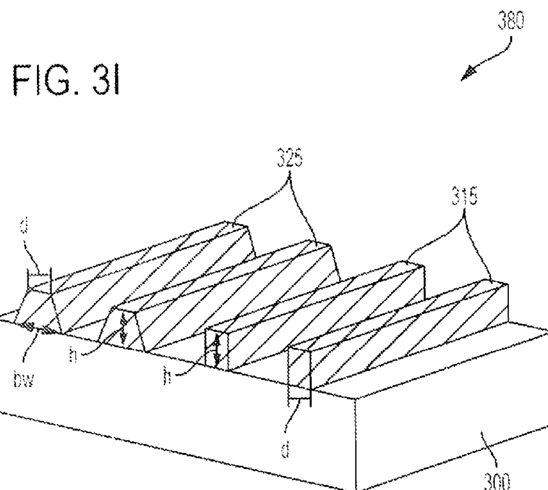


**(57) Abstract**: A technique for forming a semiconductor device is provided. Sacrificial mandrels are formed over a hardmask layer on a semiconductor layer. Spacers are formed on sidewalls of the sacrificial mandrels. The sacrificial mandrels are removed to leave the spacers. A masking process leaves exposed a first set of spacers with a second set protected. In response to the masking process, a first fin etch process forms a first set of fins in the semiconductor layer via first set of spacers. The first set of fins has a vertical sidewall profile. Another masking process leaves exposed the second set of spacers with the first set of spacers and the first set of fins protected. In response to the other masking process, a second fin etch process forms a second set of fins in semiconductor layer using the second set of spacers. The second set of fins has a trapezoidal sidewall profile.

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# DUAL FIN INTEGRATION FOR ELECTRON AND HOLE MOBILITY ENHANCEMENT

## TECHNICAL FIELD

**[0001]** The present disclosure relates generally to electron and hole mobility in integrated circuit device manufacturing, and more specifically to dual fin integration for electron and hole mobility enhancement.

## BACKGROUND ART

**[0002]** In solid-state physics, the electron mobility characterizes how quickly an electron can move through a metal or semiconductor, when pulled by an electric field. In semiconductors, there is an analogous quantity for holes, called hole mobility. The term carrier mobility refers in general to both electron and hole mobility in semiconductors.

**[0003]** Electron and hole mobility are special cases of electrical mobility of charged particles under an applied electric field. For example, when an electric field E is applied across a piece of material, the electrons respond by moving with an average velocity called the drift velocity.

**[0004]** Conductivity is proportional to the product of mobility and carrier concentration. For example, the same conductivity could come from a small number of electrons with high mobility for each, or a large number of electrons with a small mobility for each. For semiconductors, the behavior of transistors and other devices can be very different depending on whether there are many electrons with low mobility or few electrons with high mobility. Therefore, mobility is a very important parameter for semiconductor materials. Almost always, higher mobility leads to better device performance, with other things being equal.

**[0005]** Therefore, there is a need in the art to improve the aforementioned behaviour.

## BRIEF SUMMARY

**[0006]** Embodiments include a method of forming a semiconductor device. The method includes forming a plurality of sacrificial mandrels over a hardmask layer, in which the hardmask layer is disposed over a semiconductor layer, forming a plurality of spacers on sidewalls of the plurality of sacrificial mandrels, removing the plurality of sacrificial mandrels to leave the plurality of spacers, and performing a masking process to leave exposed a first set of the plurality of spacers with a second set of the plurality of spacers protected. In response to the masking process, a first fin etch process is performed to form a first set of fins in the semiconductor layer using the first set of the plurality of spacers, where the first set of fins has a vertical sidewall profile. Another masking process is performed to leave exposed the second set of the plurality of spacers with the first set of the plurality of spacers and the first set of fins protected. In response to the other masking process, a second fin etch process is performed to form a second set of fins in the semiconductor layer using the second set of the plurality of spacers, where the second set of fins has a trapezoidal sidewall profile.

**[0007]** Embodiments include a method of forming a semiconductor device. The method includes forming trapezoidal shaped fins on a substrate, where a trapezoidal shape of the trapezoidal shaped fins enhances electron mobility, and forming vertical shaped fins on the substrate. A straight vertical shape of the vertical shaped fins enhances hole mobility, and the trapezoidal shaped fins have a larger base that the vertical shaped fins. An integrated circuit is formed by the trapezoidal shaped fins and the vertical shaped fins.

**[0008]** Embodiments include a semiconductor device. Trapezoidal shaped fins are formed on a substrate, where a trapezoidal shape of the trapezoidal shaped fins enhances electron mobility. Vertical shaped fins are formed on the substrate, where a straight vertical shape of the vertical shaped fins enhances hole mobility. The trapezoidal shaped fins have a larger base that the vertical shaped fins. The trapezoidal shaped fins and the vertical shaped fins are formed together as components in an integrated circuit.

**[0009]** Additional features and advantages are realized through the techniques described herein. Other embodiments and aspects are described in detail herein. For a better understanding, refer to the description and to the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** The present invention will now be described, by way of example only, with reference to preferred embodiments, as illustrated in the following figures:

FIG. 1 illustrates an example of a fin field effect transistor (FinFET) device, in accordance with the prior art, and in which a preferred embodiment of the present invention may be implemented;

FIG. 2 illustrates an example fin structure, in accordance with a preferred embodiment of the present invention;

FIGS. 3A though 3J together illustrate a process flow of fabricating a dual fin integration structure for electron and hole mobility enhancement, in accordance with a preferred embodiment of the present invention, in which:

FIG. 3A illustrates a layer of fin material layer deposited on substrate, and a fin hardmask deposited on the fin material, along with spacers and sacrificial layers deposited on the fin hardmask;

FIG. 3B illustrates removing the sacrificial layers to leave free standing spacers;

FIG. 3C illustrates that a mask is deposited over the area designated for the NFETs;

FIG. 3D illustrates etching to obtain vertical fin sidewalls, while the designated NFET area remains protected;

FIG. 3E illustrates removing the mask from the designated NFET area;

FIG. 3F illustrates depositing a mask over the area designated for PFETs;

FIG. 3G illustrates etching to obtain tapered fin sidewalls, while the designated PFET area remains protected;

FIG. 3H illustrates removing the mask from the designated PFET area;

FIG. 3I illustrates removing the fin hardmask from on top of the vertical fins and the tapered fins; and

FIG. 3J illustrates depositing a gate oxide and gate over both the vertical fins and tapered fins;

FIG. 4 illustrates further details of the tapered fin, in accordance with a preferred embodiment of the present invention;

FIGS. 5A and 5B illustrate a method of forming a semiconductor device with dual fin integration for electron and hole mobility enhancement, in accordance with a preferred embodiment of the present invention;

FIG. 6 illustrates a method of forming a semiconductor device with dual fin integration for electron and hole mobility enhancement, in accordance with a preferred embodiment of the present invention; and

FIG. 7 illustrates an example of a computer having capabilities, in accordance with the prior art, and in which a preferred embodiment of the present invention may be implemented.

**[0011]** In the accompanying figures and following detailed description of the disclosed embodiments, the various elements illustrated in the figures are provided with three or four digit reference numbers. The leftmost digit(s) of each reference number corresponds to the figure in which its element is first illustrated.

**DETAILED DESCRIPTION**

**[0012]** While the planar field effect transistor (FET) may appear to have reached the end of its scalable lifespan, the semiconductor industry has found an alternative approach with FinFETs. FinFET technology is viewed by many as the best choice for next generation advanced processes.

**[0013]** With advanced geometry planar FET technologies, such as 20 nanometer (nm), the source and the drain encroach into the channel, making it easier for leakage current to flow between them and making it very difficult to turn the transistor off completely. FinFETs are three-dimensional structures that rise above the substrate and resemble a fin, hence the name. FIG. 1 illustrates one example of a FinFET device 100. The fins 10 may be formed on the substrate 50. The fins 10 form the source 20 and drain 25 (on opposite ends), effectively

providing more volume than a planar transistor for the same area. The gate 30 wraps around the fin 10, providing better control of the channel and allowing very little current to leak through the body when the device is in the “off” state. This, in turn, enables the use of lower threshold voltages and results in better performance and power as compared to a planar transistor.

**[0014]** FIG. 2 illustrates an example fin structure 200. In FinFET, the height (z direction) of the fin (HFin) is a great knob (variable) for the increase of total effect current (Ieff) per inch because Weff = 2HFin + DFin. DFin is the width in the y direction. Weff is the effective channel width. For explanation purposes, it is assumed that the electrical current moves in the directions of arrows 205, 210, 215 (e.g., in the x direction), although electrons and holes (absence of electrons) may move in opposite directions. The electrical current flows along the outer surface of the fin 200.

**[0015]** Fin orientation is very germane because carrier mobilities are generally anisotropic (not the same in every direction). For example, electron mobility is highest in the (100) plane ((100) plane is equal to (001) plane). The (100) plane (i.e., x-y plane) has electrical current arrow 205 within the -x direction. The electron mobility (flow of electrical current) is highest in the (100) plane represented as flowing in the electrical current arrow 205, while hole mobility is lowest. The (100) plane (x-y plane) is the top surface with width “d” in the fin 200.

**[0016]** Conversely, hole mobility is largest in the (110) plane, while electron mobility is lowest. The (110) plane (i.e., x-z plane) has electrical current 210 in the -x direction. The hole mobility (flow of electrical current) is highest in the (110) plane represented as flowing in the electrical current arrow 210. The (110) plane (x-z plane) is the vertical sidewall with height “a” in the fin 200.

**[0017]** Also, the fin structure 200 has an angled foot at the base. The angled foot extends out at angle $\phi$. The angled foot creates a transition plane that shows electrical current arrow 215. In the transition plane of the angled foot, the electron mobility and hole mobility are neither the highest nor the lowest but in between.

**[0018]** In a silicon-on-insulator (SOI) FinFET, the (110) plane is usually used as the substrate to enhance the hole mobility as the electron mobility is intrinsically greater than hole mobility. Electrons are the majority carrier in a negative channel field effect transistor (NFET), while holes are the majority carrier in a positive channel field effect transistor (PFET). When determining the size of a fin, there is a trade-off between a fin with increased hole mobility versus increased electron mobility.

**[0019]** According to an embodiment, a novel dual fin profile integration is disclosed to make beneficial use of both electron and hole mobility favored planes. FIGS. 3A though 3J together illustrate a process flow of fabricating a dual fin integration structure for electron and hole mobility enhancement according to an embodiment. FIG. 3A illustrates a substrate 300 with a layer of fin material layer 302 deposited on the substrate 300. A fin hardmask 304 is deposited on the fin material 302.

**[0020]** In order to prepare to pattern the (future) fins and define the pitch of the fins, spacer lithography is performed. Spacer lithography may include sidewall image transfer (SIT). Blocks of sacrificial layers 306 (mandrel) are formed by layer deposition, pattering and etching, and spacers 308 (SIT spacers) are formed on sidewall surfaces of the mandrels 306. The spacer layer 308 may be formed, for example, by blanket deposition on the hardmask 304 and mandrels 306, followed by anisotropic (directional) etching to remove horizontally disposed surface of the spacer layer material.

**[0021]** The substrate 300 may be a material such as an insulator. The fin material 302 may be silicon, germanium, etc. The thickness of the fin material 302 determines the height of the fin (being fabricated). The fin hardmask 304 may be an oxide, such as silicon dioxide or germanium oxide. Also, the fin hardmask 304 may be a nitride. The spacer 308 can be a nitride when the fin hardmask 304 is an oxide, and the spacer 308 can be an oxide when the fin hardmask 304 is a nitride. The sacrificial layer 306 may be a polysilicon material. The width of the spacer 308 determines the width of the fin (being fabricated for vertical fins and the top width for tapered fins).

**[0022]** In FIG. 3B, the sacrificial layers 306 are removed to leave the free standing spacers 308. The area of the four free standing spacers 308 defines the fin regime. The two left spacers 308 are designated for building NFETs, and the two right spacers are designated for building PFETs. The location of the spacers 308 determines the position of the future fins. The spacers 308 are (simultaneously formed) for both the PFETs and NFETs. The dimensions (height and width) of the spacers 308 can be the same for both the fins of the PFETs and NFETs.

**[0023]** The spacer width 313 of each spacer 308 is substantially equal. The spacer width 313 may include a range of 6-10 nm. The pitch 311 between each of the spacers is substantially equal. The pitch 311 may be, e.g., 21 nm – 32 nm.

**[0024]** FIG. 3C illustrates that a mask 310 is deposited over the two left spacers 308 (designated for the NFETs) and deposited over a left portion of the fin hardmask 304 in order to protect the two left spacers 308 and the left portion of the fin hardmask 304. Moreover, the mask 310 protects the area designated for the NFETs before etching occurs to prepare fins for the PFETs.

**[0025]** FIG. 3D illustrates etching, such as reactive ion etching RIE, to remove both the fin hardmask 304 and fin material 302 that are not immediately under the two right spacers 308. The etching in the designated PFET area forms straight fin side walls (110) planes for PFETs, while the designated NFET area remains protected. The etching, which may be dry etching, and time are tuned to obtain two vertical profile fins 315. For example, after the etching reaches its end point (e.g. stop on substrate 300), over-etch time and angle can be tuned to obtain vertical fins.

**[0026]** In FIG. 3E, the mask 310 is removed, e.g., by dry etching. FIG. 3F illustrates that a mask 320 is deposited over the two right spacers 308 and over the hardmask 304 in the designated PFET area, in order to protect the two right spacers 308 and the right portion of the fin hardmask 304. In this case, the mask 320 protects the area designated for the PFETs before etching occurs to prepare fins for the NFETs. The masks 310 and 320 may be an oxide.

**[0027]** FIG. 3G illustrates etching (e.g., RIE) to obtain tapered fin sidewalls approaching (100) plane for two tapered fins 325. The etching (e.g., dry etching) and time are tuned to obtain the two tapered fins 325. The tapered fins 325 are formed in a trapezoidal shape, and the base at the bottom of the trapezoid is wider than the width at the top of the trapezoid. For example, after the etching reaches its end point (e.g., stop on substrate 300), reduction in over-etch time can be tuned to obtain tapered fins.

**[0028]** FIG. 3H illustrates that the mask 320 is removed from the designated PFET area. The fin hardmask 304 is removed from on top the tapered fins 325 and the vertical fins 315. The tapered fins 325 and vertical fins 315 can be formed in close proximity and still be respectively optimized for electron mobility (NFETs) and hole mobility (PFETs), during/sharing the same deposition process for the fin material 302 and fin hardmask 304. The spacing "s" between the tapered fin 325 and vertical fin 315 may be approximately 18-30 nm.

**[0029]** FIG. 3I illustrates that fin hardmask 304 is removed from on top of the vertical fins 315 and the tapered fins 325. In FIG. 3I, a dual fin structure 380 has both the tapered fins 325 fabricated with enhanced electron mobility for NFETs and the vertical fins 315 fabricated with enhanced hole mobility. The vertical fins 315 and the tapered fins 325 both have a height "h". The top of the tapered fins 325 have the same width "d" as the vertical fins 315. However, the base of the tapered fins 325 has the wider base width "bw". The top width "d" may be about 5 or 6 nanometers (nm). The base width "bw" may be about 11 or 12 nm. Further, the base width "bw" is designed to be about twice as much as the top width "d", such that the electron mobility is improved along the tapered plane (shown as tapered sidewall 420 in FIG. 4). The height "h" may be about 30-45 nm, or as desired for the intended application.

**[0030]** Even though the spacer width 313 may be equal (or nearly equal) for each spacer 308 and the spacer pitch 311 is equal (or nearly equal) between each spacer 308 (shown in FIG. 3B), the fabrication process is configured to optimize electron mobility in the tapered fins 325 and optimize hole mobility in the vertical fins 315 (both of which are on the same microprocessor).

**[0031]** FIG. 3J illustrates a gate stack including a gate oxide layer 340 and a gate electrode layer 350 deposited over both the vertical fins 315 and the tapered fins 325, thus forming the two NFETs 360 and the two PFETs 365. The gate electrode layer 350 and gate oxide layer 340 (underneath the gate electrode layer 350) are etched to form the structure 380 shown in FIG. 3J (using any technique known to one skilled in the art). The gate oxide layer 340 is wrapped around (the tops and sides) the tapered fins 325 and vertical profile fins 315, and the gate electrode layer 350 is on top of the gate oxide layer 340 as understood by one skilled in the art, such that the NFETs 360 and PFETs 365 are formed. The gate material of the gate electrode layer 350 may include silicon, germanium, metals, metal alloys, and a combination thereof, which are doped with dopants to conduct electricity. The gate oxide layer 340 may be a high-K dielectric, such as a thin layer of hafnium oxide, for example.

**[0032]** Although FIGS. 3A through 3J show building the vertical profile fins 315 for PFETs before forming the tapered (trapezoidal) fins 325 for NFETs, embodiments are not meant to be limited to this order. In one embodiment, the tapered (trapezoidal) fins 325 for NFETs can be formed before the vertical profile fins 315 for PFETs.

**[0033]** FIG. 4 illustrates further details of the tapered fin 325 according to an embodiment. As discussed in FIG. 2, the electron mobility is highest in the (100) plane (x-y plane), which corresponds to electrical current 205. The tapered fin 325 has a tapered sidewall 420 that has been optimized to increase electron mobility better that the vertical sidewall in the vertical fin 315 and better than the angled foot in FIG. 2. The flatter (i.e., more horizontal) the tapered sidewall 420, the better the electron mobility is in the electrical current 415. As the top width “d” and the height “h” remain constant, the base width “bw” can be increased to correspondingly increase the electron mobility (which decreases the angle $\phi$). Accordingly, the base width “bw” should be about twice the length of the top width “d”.

**[0034]** Referring back to FIGS. 3I and 3J, the dual fin structure 380 is optimized with tapered fins 325 for NFETs and vertical fins 315 for PFETs on the same structure (circuit). The dual fin structure 308 may be a microprocessor. In one example, the dual fin structure 308 can be static random-access memory (SRAM) which is a building block/circuit in a semiconductor microprocessor. The dual fin structure 308 may be utilized in the same circuit to form various

logic circuits, such as “AND” circuits, “OR” circuits, and “NOT” circuits. For example, the dual fin structure 308 may be utilized as an inverter circuit.

**[0035]** Now turning to FIGS. 5A and 5B, a method 500 of forming a semiconductor device (with dual fin integration for electron and hole mobility enhancement) is provided according to an embodiment. Reference can be made to FIGS. 1-4, 6, and 7 discussed herein.

**[0036]** At block 505, a plurality of sacrificial mandrels 306 are formed over the hardmask layer 304, where the hardmask layer 304 is disposed over a semiconductor layer 302, as shown in FIG. 3A.

**[0037]** At block 510, plurality of spacers 308 are formed on sidewalls of the sacrificial mandrels 306, as shown in FIG. 3A. At block 515, the sacrificial mandrels 306 are removed to leave the plurality of spacers 308 as shown in FIG. 3B.

**[0038]** At block 520, a masking process is performed to leave exposed a first set of the plurality of spacers 308 with a second set of the plurality of spacers 308 protected as shown in FIG. 3C. At block 525, a first fin etch process is performed to form a first set of fins (e.g., vertical profile fins 315) in the semiconductor layer 302 using the first set of spacers 308 (e.g., the right set of spacers 308), such that the first set of fins 315 has a vertical sidewall profile, as shown in FIGS. 3D and 3E.

**[0039]** At block 530, another masking process is performed to leave exposed the second set of spacers 308 (e.g., the left set of spacers 308) while protecting the first set of spacers 308 and the first set of fins 315, as shown in FIG. 3F. At block 535, a second fin etch process is performed to form a second set of fins (e.g., trapezoidal/tapered fins 325) in the semiconductor layer 302 using the second set of spacers 308, such that the second set of fins 325 has a trapezoidal sidewall profile as shown in FIG. 3G.

**[0040]** During the masking process a first mask 310 covers the second set of the plurality of spacers 308, and the first mask may be an oxide.

**[0041]** During the other masking process a second mask 320 covers the first set of the plurality of spacers 308, and the second mask may be an oxide.

**[0042]** The plurality of spacers 308 includes at least one of an oxide and a nitride. The semiconductor layer 302 comprises at least one of silicon and germanium. The first set of fins 315 comprises positive channel field effect transistors (PFET) devices, and the second set of fins 325 comprises negative channel field effect transistors (NFET) devices, as shown in FIG. 3J. A gate electrode 350 is formed over the first set of fins 315 and the second set of fins 325.

**[0043]** A base width ("bw") of the second set of fins 325 is at least twice a length of a top width of the second set of fins 325 (reference can be made to FIG. 4). A height ("h") of the second set of fins 325 is about equal to a height ("h") of the first set of fins 315. The trapezoidal shaped fins 325 have a larger base ("bw") than the base ("d") of the vertical shaped fins.

**[0044]** An integrated circuit includes the first set of fins 315 and the second set of fins 325. An individual microprocessor (e.g., structure 380) includes the integrated circuit having the first set of fins 315 and the second set of fins 325, such that the first set of fins comprises PFET devices 365 and the second set of fins comprises NFET devices 360.

**[0045]** By having both the trapezoidal shaped fins 325 and the vertical shaped fins 315 on the same microprocessor (e.g., the dual fin structure 380 is a semiconductor microprocessor (i.e., chip)) increases the speed of the microprocessor as compared to either only having the trapezoidal shaped fins or only having the vertical shaped fins. In the microprocessor dual fin structure 380, the electron current is optimized in the NFETs 360 because of the trapezoidal/tapered shaped fins 325, and concurrently, the hole current is optimized in the PFETs 365 because of the vertical shaped fins 315.

**[0046]** FIG. 6 illustrates a method 600 of forming a semiconductor device dual fin integration for electron and hole mobility enhancement according to an embodiment. Reference can be made to FIGS. 1-5, and 7.

**[0047]** At block 605, negative channel field effect transistors (NFETs) 360 are provided, in which the NFETs 360 have trapezoidal shaped fins 325 for a source and a drain. The source is on one side of the gate 350 while the drain is across the gate 350 on the opposite side of the trapezoidal shaped fin 325.

**[0048]** At block 610, positive channel field effect transistors (PFETs) are provided, in which the PFETs have vertical shaped fins 315.

**[0049]** At block 615, the trapezoidal shaped fins have a larger base (base width "bw") that the vertical shaped fins, and the trapezoidal shaped fins and the vertical shaped fins are together on the same substrate 300 in a microprocessor (e.g., in the dual fin structure 380).

**[0050]** The base width "bw" of the trapezoidal fins 325 is about twice the length of the top width "d" of the trapezoidal fins 325. The height "h" of the trapezoidal fins 325 is about equal to the height of the vertical shaped fins 315.

**[0051]** FIG. 7 illustrates an example of a computer 700 having capabilities, which may be included in exemplary embodiments. Various methods, procedures, modules, flow diagrams, tools, applications, circuits, elements, and techniques discussed herein may also incorporate and/or utilize the capabilities of the computer 700. Moreover, capabilities of the computer 700 may be utilized to implement features of exemplary embodiments discussed herein. One or more of the capabilities of the computer 700 may be utilized to implement, incorporate, to connect to, and/or to support any element discussed herein (as understood by one skilled in the art) in FIGS. 1-6.

**[0052]** Generally, in terms of hardware architecture, the computer 700 may include one or more processors 710, computer readable storage memory 720, and one or more input and/or output (I/O) devices 770 that are communicatively coupled via a local interface (not shown). The local interface can be, for example but not limited to, one or more buses or other wired or wireless connections, as is known in the art. The local interface may have additional elements, such as controllers, buffers (caches), drivers, repeaters, and receivers, to enable

communications. Further, the local interface may include address, control, and/or data connections to enable appropriate communications among the aforementioned components.

**[0053]** The processor 710 is a hardware device for executing software that can be stored in the memory 720. The processor 710 can be virtually any custom made or commercially available processor, a central processing unit (CPU), a data signal processor (DSP), or an auxiliary processor among several processors associated with the computer 700, and the processor 710 may be a semiconductor based microprocessor (in the form of a microchip) or a microprocessor. Note that the memory 720 can have a distributed architecture, where various components are situated remote from one another, but can be accessed by the processor 710.

**[0054]** The software in the computer readable memory 720 may include one or more separate programs, each of which comprises an ordered listing of executable instructions for implementing logical functions. The software in the memory 720 includes a suitable operating system (O/S) 750 and one or more applications 760 of the exemplary embodiments. As illustrated, the application 760 comprises numerous functional components for implementing the features, processes, methods, functions, and operations of the exemplary embodiments. The application 760 of the computer 700 may represent numerous applications, agents, software components, modules, interfaces, controllers, etc., as discussed herein but the application 760 is not meant to be a limitation.

**[0055]** The operating system 750 may control the execution of other computer programs, and provides scheduling, input-output control, file and data management, memory management, and communication control and related services.

**[0056]** The application 760 may be a source program, executable program (object code), script, or any other entity comprising a set of instructions to be performed. When a source program, then the program is usually translated via a compiler, assembler, interpreter, or the like, which may or may not be included within the memory 720, so as to operate properly in connection with the O/S 750. Furthermore, the application 760 can be written as (a) an object oriented programming language, which has classes of data and methods, or (b) a procedure programming language, which has routines, subroutines, and/or functions.

**[0057]** The I/O devices 770 may include input devices (or peripherals) such as, for example but not limited to, a mouse, keyboard, scanner, microphone, camera, etc. Furthermore, the I/O devices 770 may also include output devices (or peripherals), for example but not limited to, a printer, display, etc. Finally, the I/O devices 770 may further include devices that communicate both inputs and outputs, for instance but not limited to, a NIC or modulator/demodulator (for accessing remote devices, other files, devices, systems, or a network), a radio frequency (RF) or other transceiver, a telephonic interface, a bridge, a router, etc. The I/O devices 770 also include components for communicating over various networks, such as the Internet or an intranet. The I/O devices 770 may be connected to and/or communicate with the processor 710 utilizing Bluetooth connections and cables (via, e.g., Universal Serial Bus (USB) ports, serial ports, parallel ports, FireWire, HDMI (High-Definition Multimedia Interface), PCIe, InfiniBand®, or proprietary interfaces, etc.).

**[0058]** When the computer 700 is in operation, the processor 710 is configured to execute software stored within the memory 720, to communicate data to and from the memory 720, and to generally control operations of the computer 700 pursuant to the software. The application 760 and the O/S 750 are read, in whole or in part, by the processor 710, perhaps buffered within the processor 710, and then executed.

**[0059]** When the application 760 is implemented in software it should be noted that the application 760 can be stored on virtually any computer readable storage medium for use by or in connection with any computer related system or method.

**[0060]** The application 760 can be embodied in any computer-readable medium for use by or in connection with an instruction execution system, apparatus, server, or device, such as a computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

**[0061]** In exemplary embodiments, where the application 760 is implemented in hardware, the application 760 can be implemented with any one or a combination of the following technologies, which are each well known in the art: a discrete logic circuit(s) having logic gates

for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), etc.

**[0062]** It is understood that the computer 700 includes non-limiting examples of software and hardware components that may be included in various devices, servers, and systems discussed herein, and it is understood that additional software and hardware components may be included in the various devices and systems discussed in exemplary embodiments.

**[0063]** In some embodiments, various functions or acts may take place at a given location and/or in connection with the operation of one or more apparatuses or systems. In some embodiments, a portion of a given function or act may be performed at a first device or location, and the remainder of the function or act may be performed at one or more additional devices or locations.

**[0064]** The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, element components, and/or groups thereof.

**[0065]** The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The present disclosure has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the disclosure. The embodiments were chosen and described in order to best explain the principles of the disclosure and the practical application, and to enable others of ordinary skill

in the art to understand the disclosure for various embodiments with various modifications as are suited to the particular use contemplated.

**[0066]** The diagrams depicted herein are illustrative. There may be many variations to the diagram or the steps (or operations) described therein without departing from the spirit of the disclosure. For instance, the actions may be performed in a differing order or actions may be added, deleted or modified. Also, the term “coupled” describes having a signal path between two elements and does not imply a direct connection between the elements with no intervening elements/connections therebetween. All of these variations are considered a part of the disclosure.

**[0067]** It will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow.

## CLAIMS

1. A method of forming a semiconductor device, the method comprising:
forming a plurality of sacrificial mandrels over a hardmask layer, the hardmask layer disposed over a semiconductor layer;
forming a plurality of spacers on sidewalls of the plurality of sacrificial mandrels;
removing the plurality of sacrificial mandrels to leave the plurality of spacers;
performing a first masking process to leave exposed a first set of the plurality of spacers with a second set of the plurality of spacers protected;
in response to the masking process, performing a first fin etch process to form a first set of fins in the semiconductor layer using the first set of the plurality of spacers, wherein the first set of fins has a vertical sidewall profile;
performing a second masking process to leave exposed the second set of the plurality of spacers with the first set of the plurality of spacers and the first set of fins protected;
in response to the second masking process, performing a second fin etch process to form a second set of fins in the semiconductor layer using the second set of the plurality of spacers, wherein the second set of fins has a trapezoidal sidewall profile.

2. The method of claim 1, wherein during the first masking process a first mask covers the second set of the plurality of spacers.

3. The method of claim 2, wherein the first mask is an oxide.

4. The method of any of the preceding claims, wherein during the second masking process a second mask covers the first set of the plurality of spacers.

5. The method of claim 4, wherein the second mask is an oxide.

6. The method of any of the preceding claims, wherein the plurality of spacers include at least one of an oxide and a nitride.

7. The method of any of the preceding claims, wherein the semiconductor layer comprises at least one of silicon and germanium.

8. The method of any of the preceding claims, wherein the first set of fins comprises positive channel field effect transistors (PFET) devices.

9. The method of any of claims 1 to 7, wherein the second set of fins comprises negative channel field effect transistors (NFET) devices.

10. The method of any of the preceding claims, wherein a gate electrode is formed over the first set of fins and the second set of fins.

11. The method of any of the preceding claims, wherein a base width of the second set of fins is at least twice a length of a top width of the second set of fins.

12. The method of any of the preceding claims, wherein a height of the second set of fins is about equal to a height of the first set of fins.

13. The method of any of the preceding claims, wherein an integrated circuit includes the first set of fins and the second set of fins.

14. The method of claim 13, wherein an individual microprocessor includes the integrated circuit having the first set of fins and the second set of fins, such that the first set of fins comprises PFET devices and the second set of fins comprises NFET devices.

15. A method of forming a semiconductor device, the method comprising:

forming trapezoidal shaped fins on a substrate, wherein a trapezoidal shape of the trapezoidal shaped fins enhances electron mobility; and

forming vertical shaped fins on the substrate, wherein a straight vertical shape of the vertical shaped fins enhances hole mobility, and wherein the trapezoidal shaped fins have a larger base that the vertical shaped fins;

wherein an integrated circuit is formed by the trapezoidal shaped fins and the vertical shaped fins.

16. The method of claim 15, wherein the trapezoidal shaped fins comprise negative NFET devices; and

wherein the vertical shaped fins comprise PFET devices.

17. The method of claim 16, wherein the integrated circuit is a microprocessor.

18. The method of any of claims 15 to 17, further comprising forming a gate electrode over the trapezoidal shaped fins and the vertical shaped fins.

19. A semiconductor device comprising:

trapezoidal shaped fins formed on a substrate, wherein a trapezoidal shape of the trapezoidal shaped fins enhances electron mobility; and

vertical shaped fins formed on the substrate, wherein a straight vertical shape of the vertical shaped fins enhances hole mobility, wherein the trapezoidal shaped fins have a larger base that the vertical shaped fins;

wherein the trapezoidal shaped fins and the vertical shaped fins are formed together as components in an integrated circuit.

20. The semiconductor device of claim 19, wherein the integrated circuit having both the trapezoidal shaped fins and the vertical shaped fins is a microprocessor.

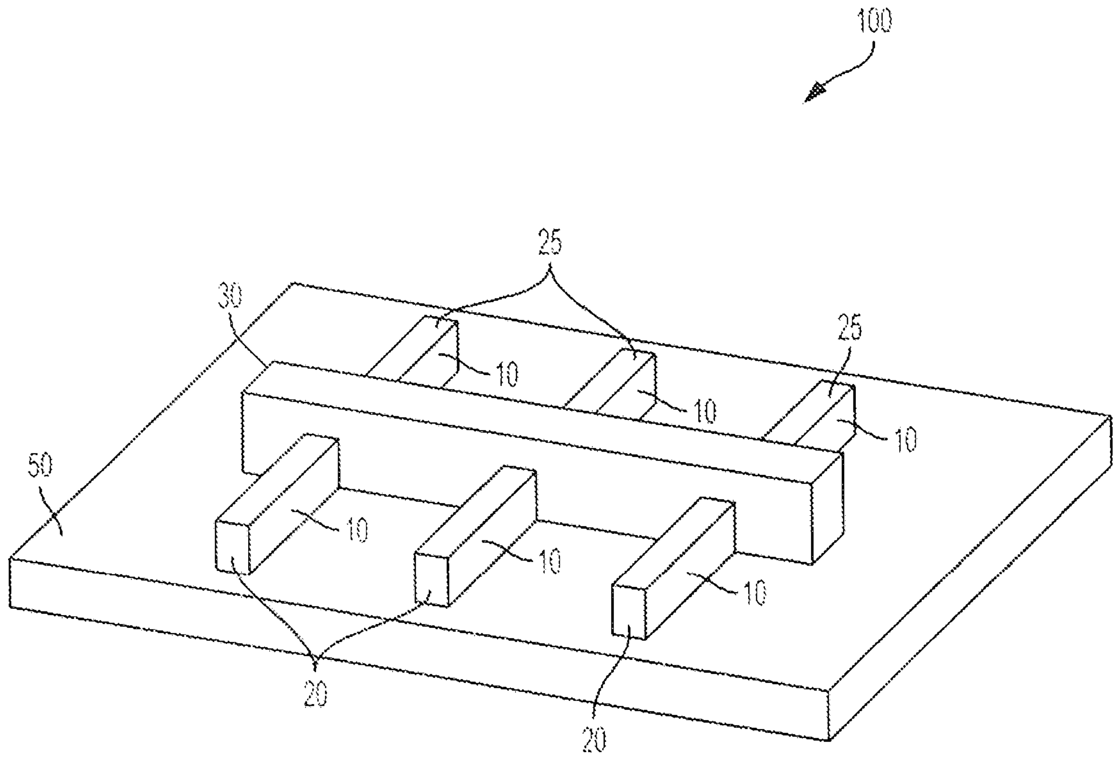


FIG. 1

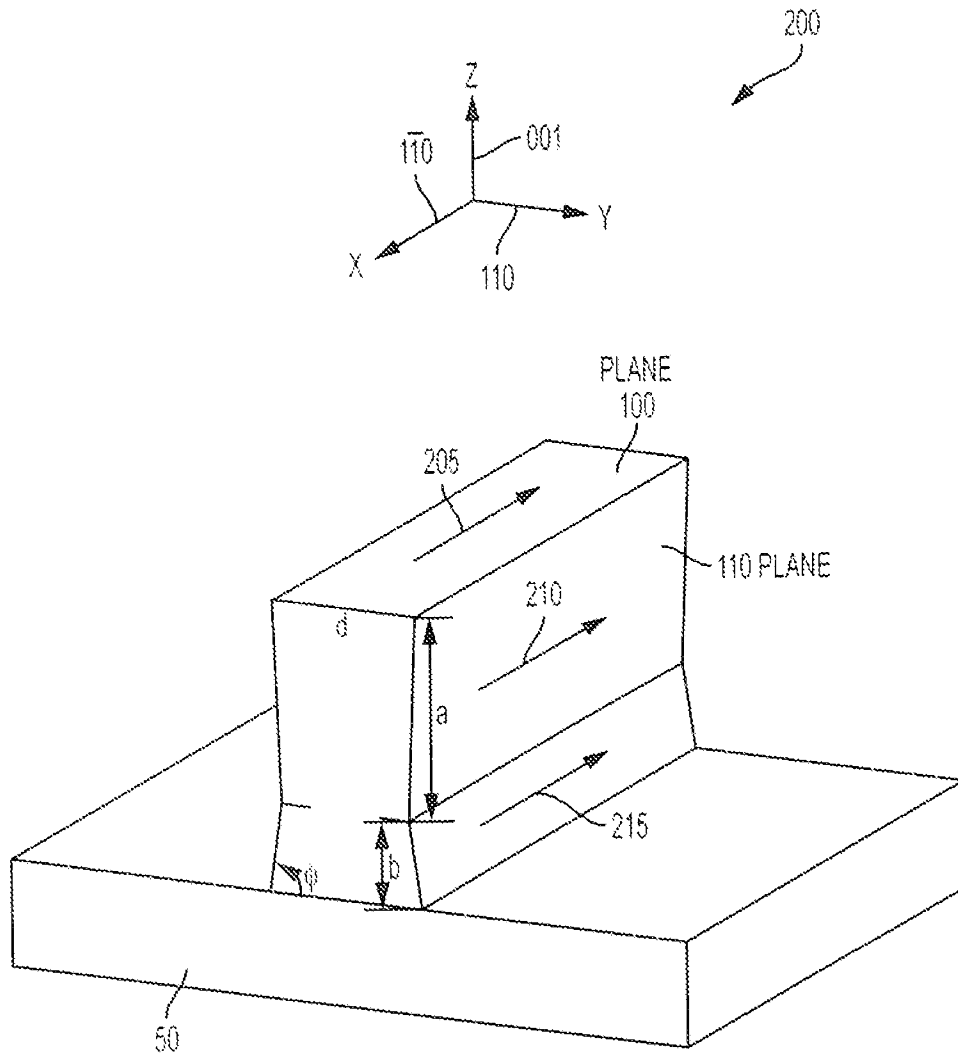


FIG. 2

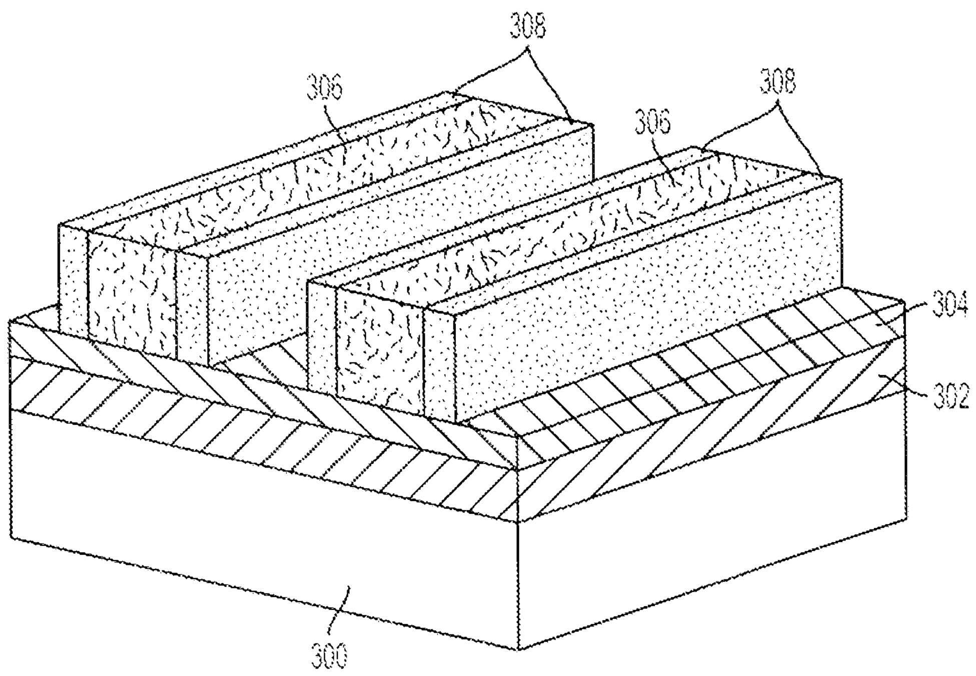


FIG. 3A

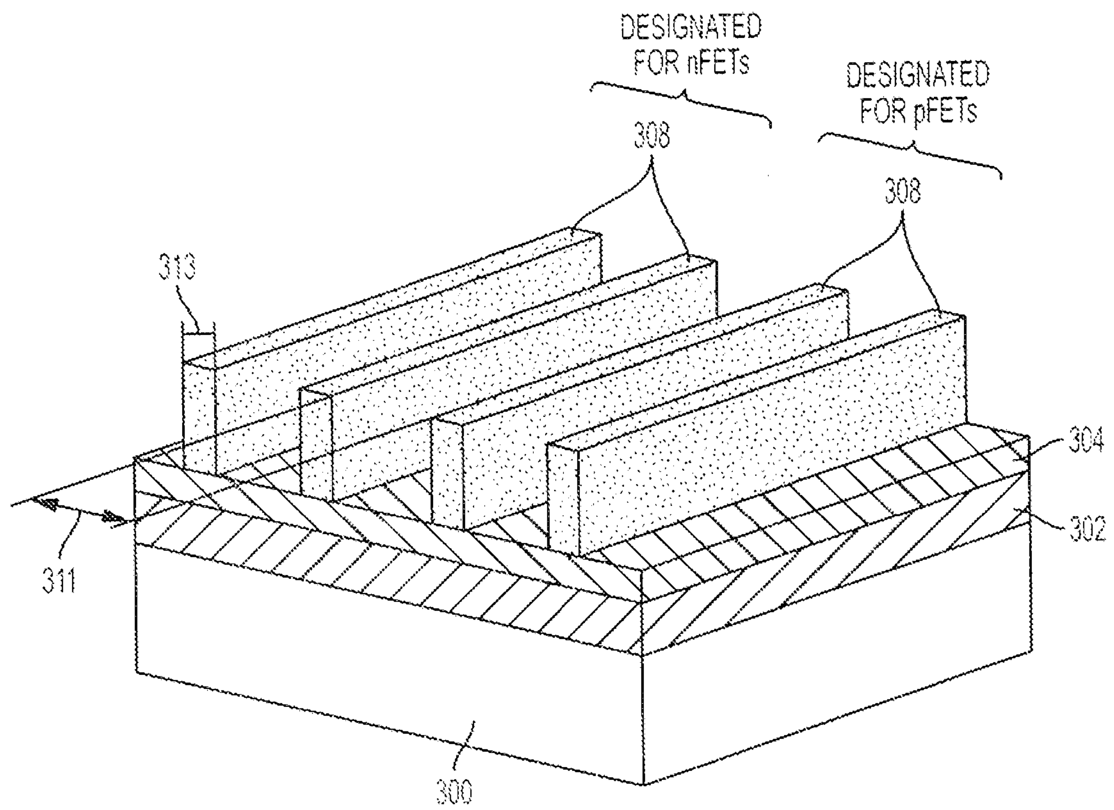


FIG. 3B

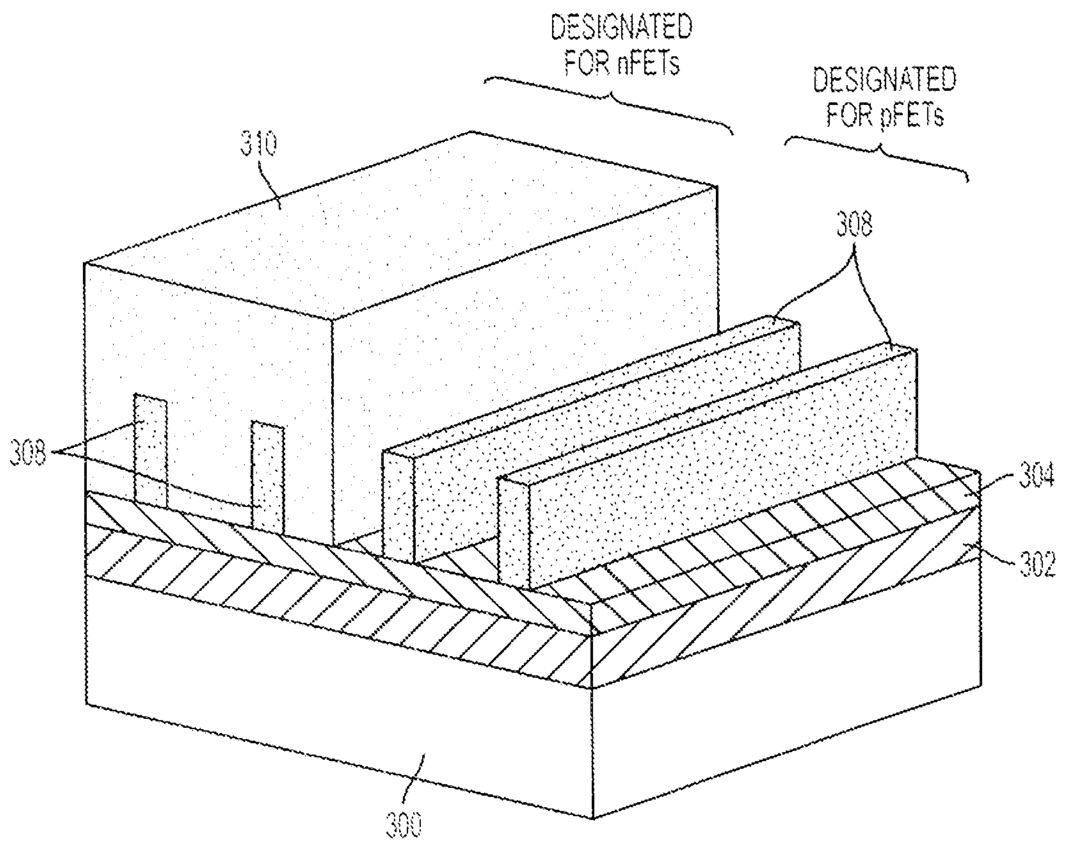


FIG. 3C

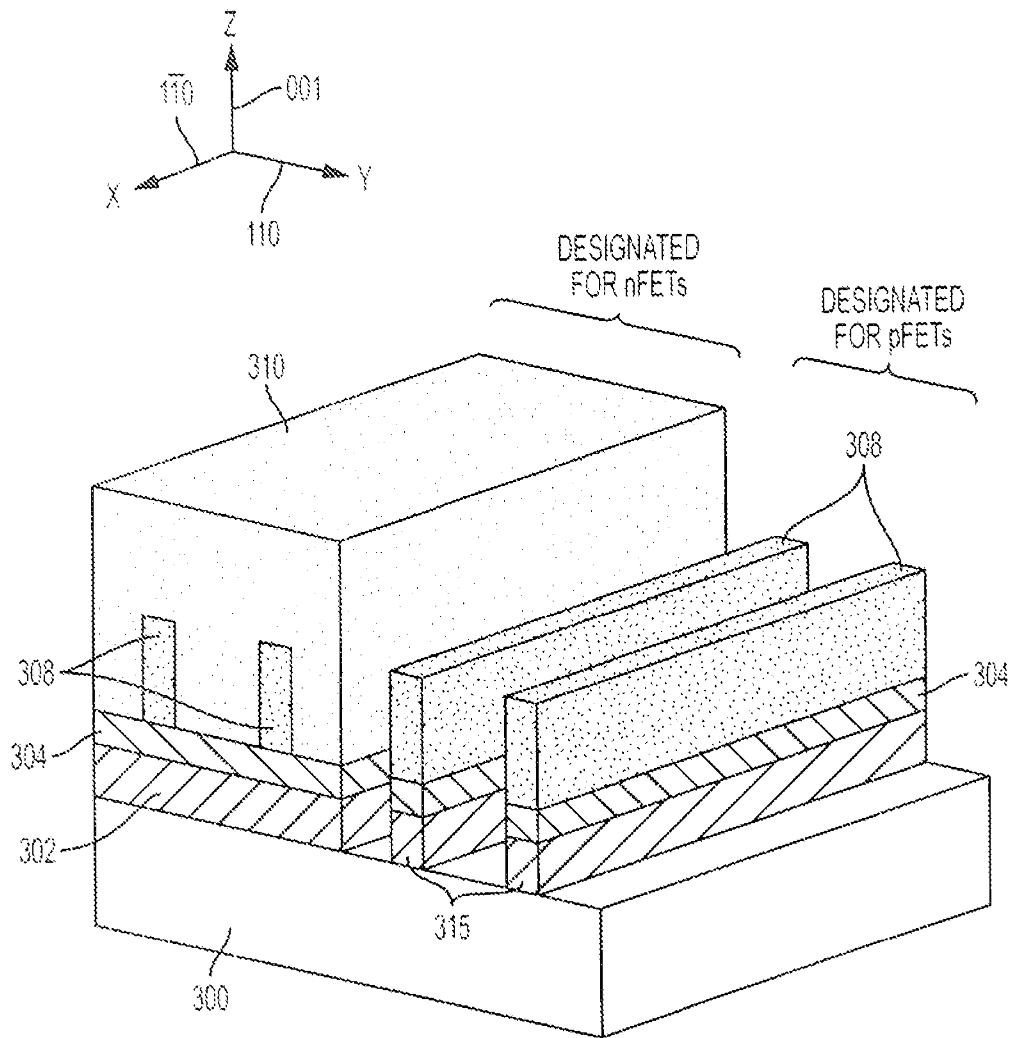


FIG. 3D

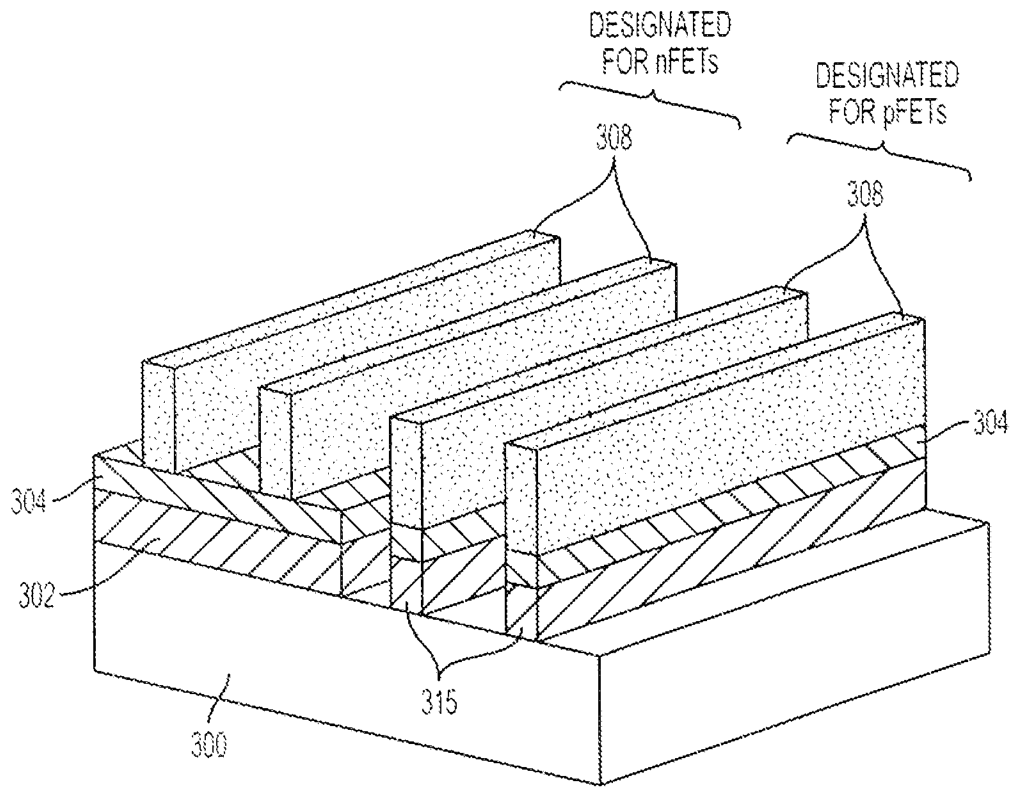


FIG. 3E

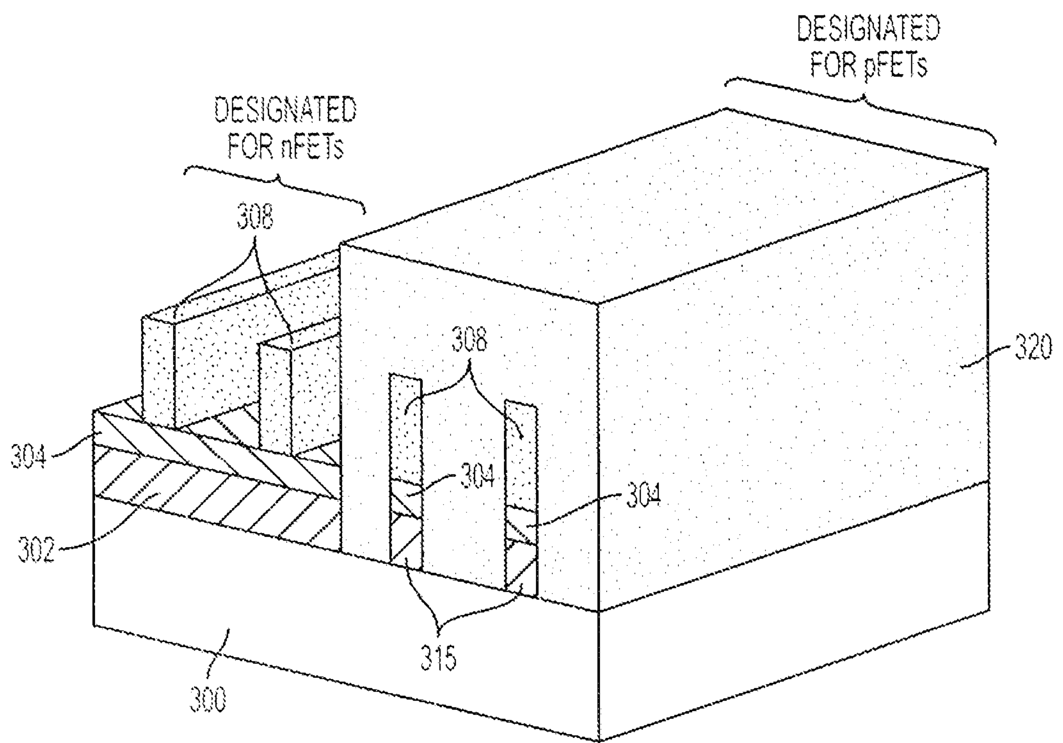


FIG. 3F

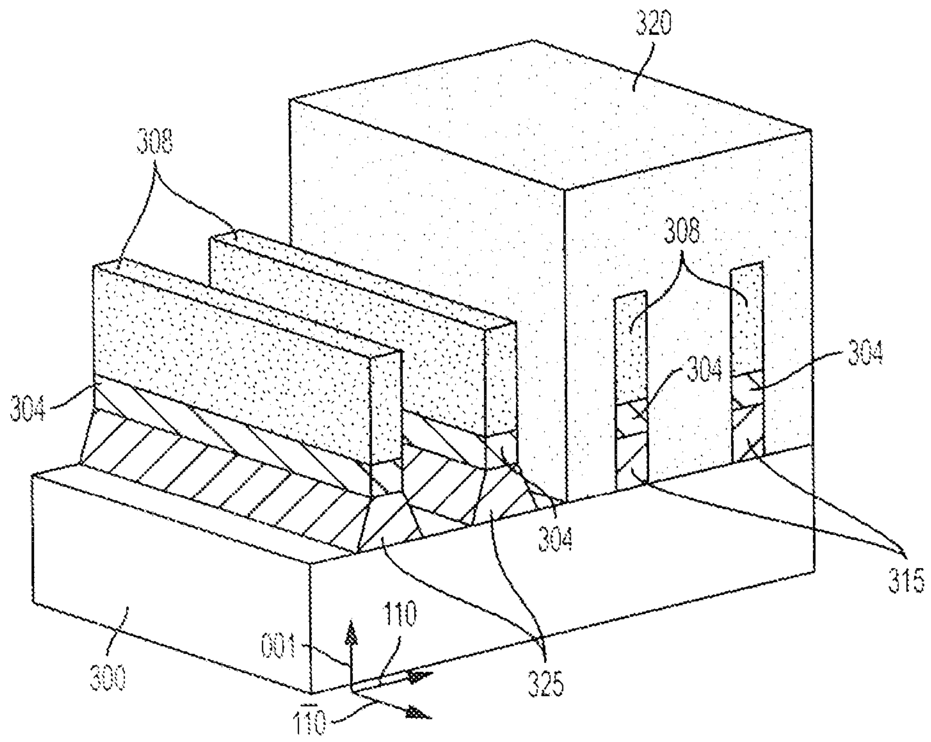


FIG. 3G

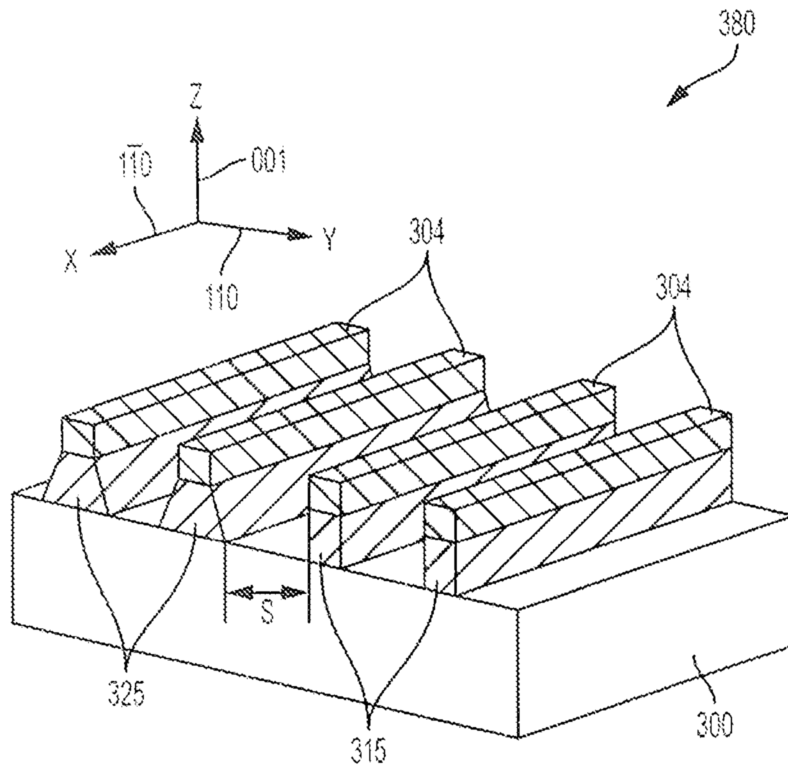


FIG. 3H

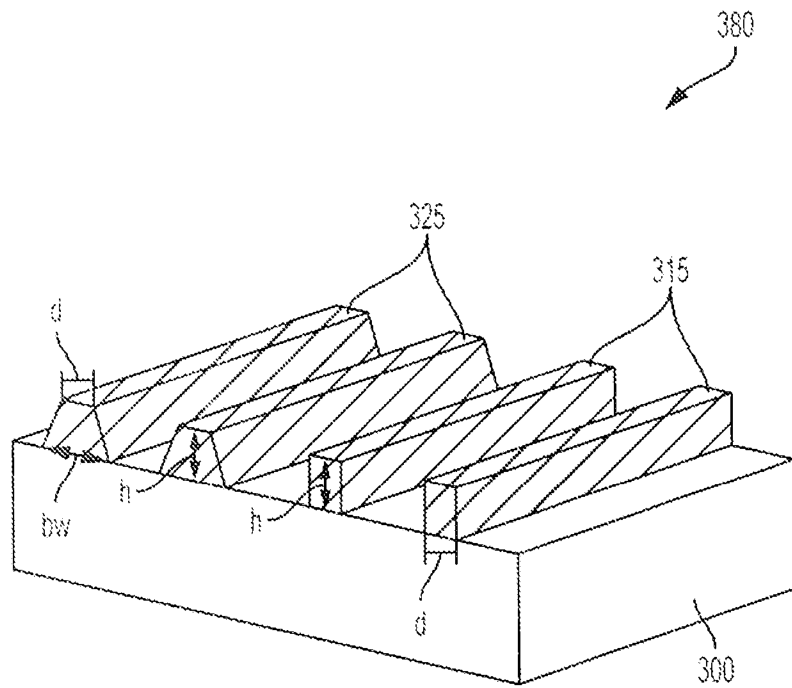


FIG. 3I

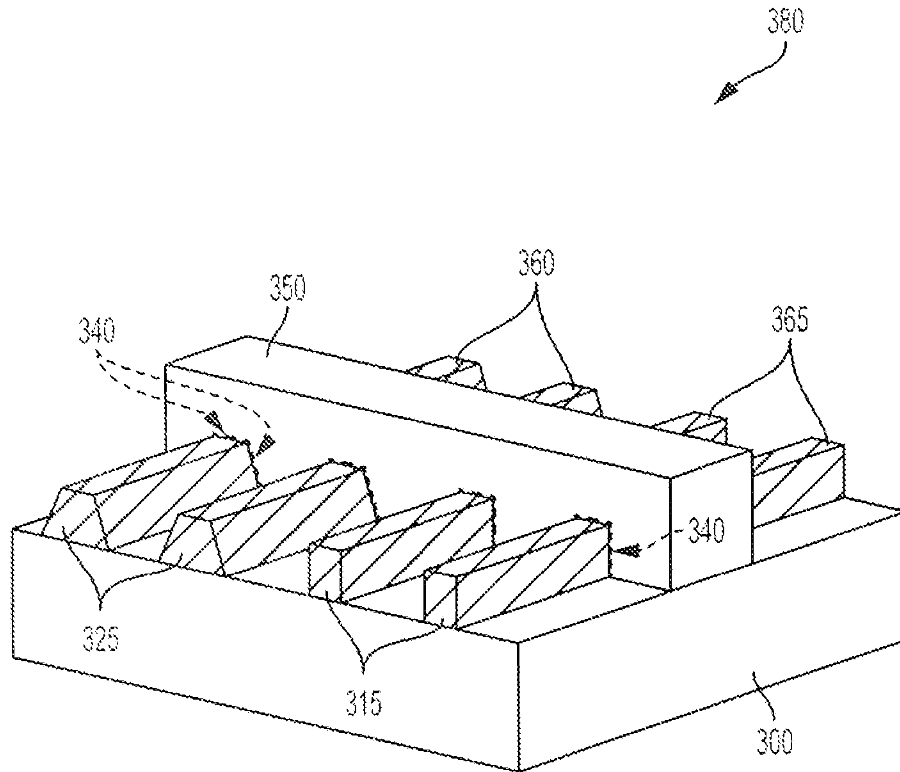


FIG. 3J

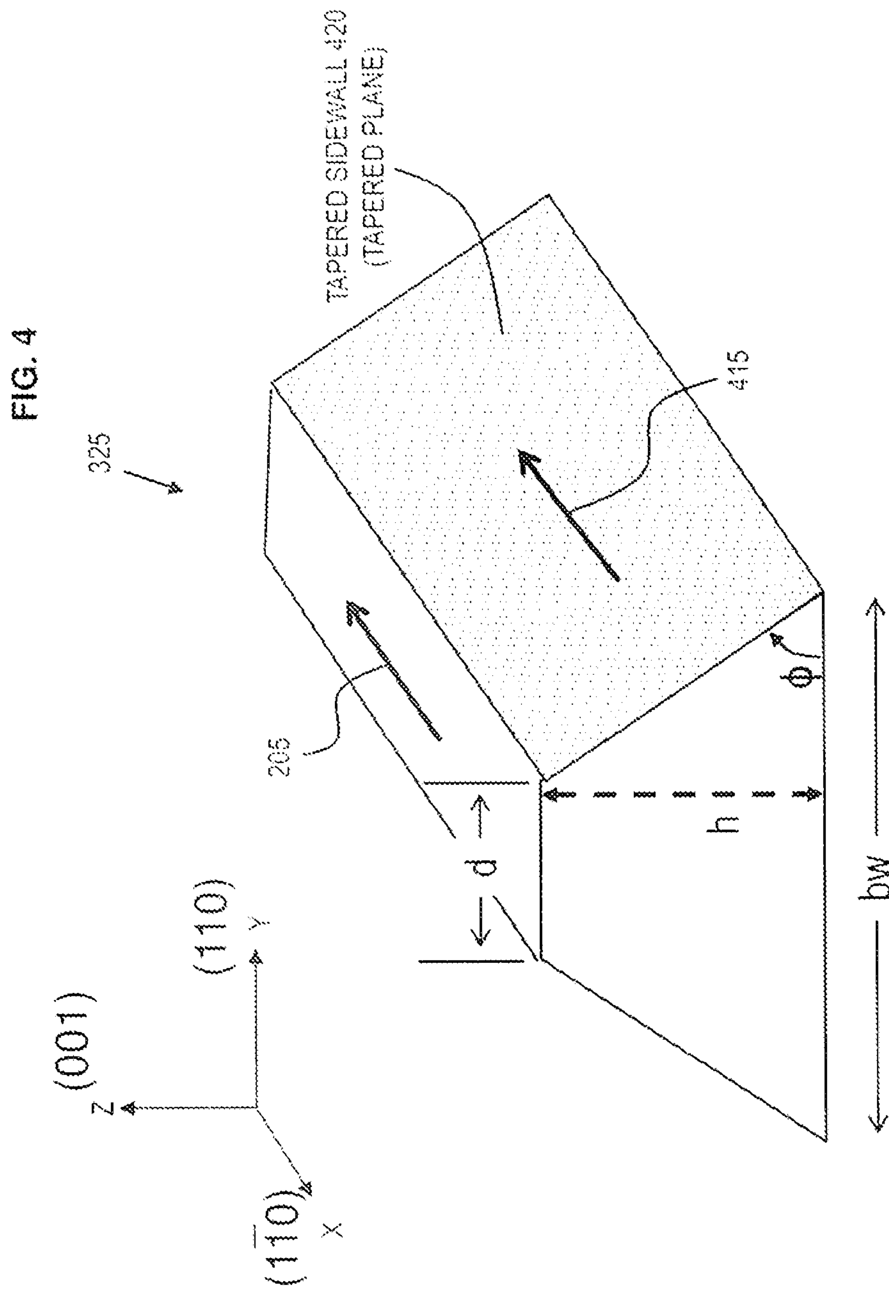


FIG. 4

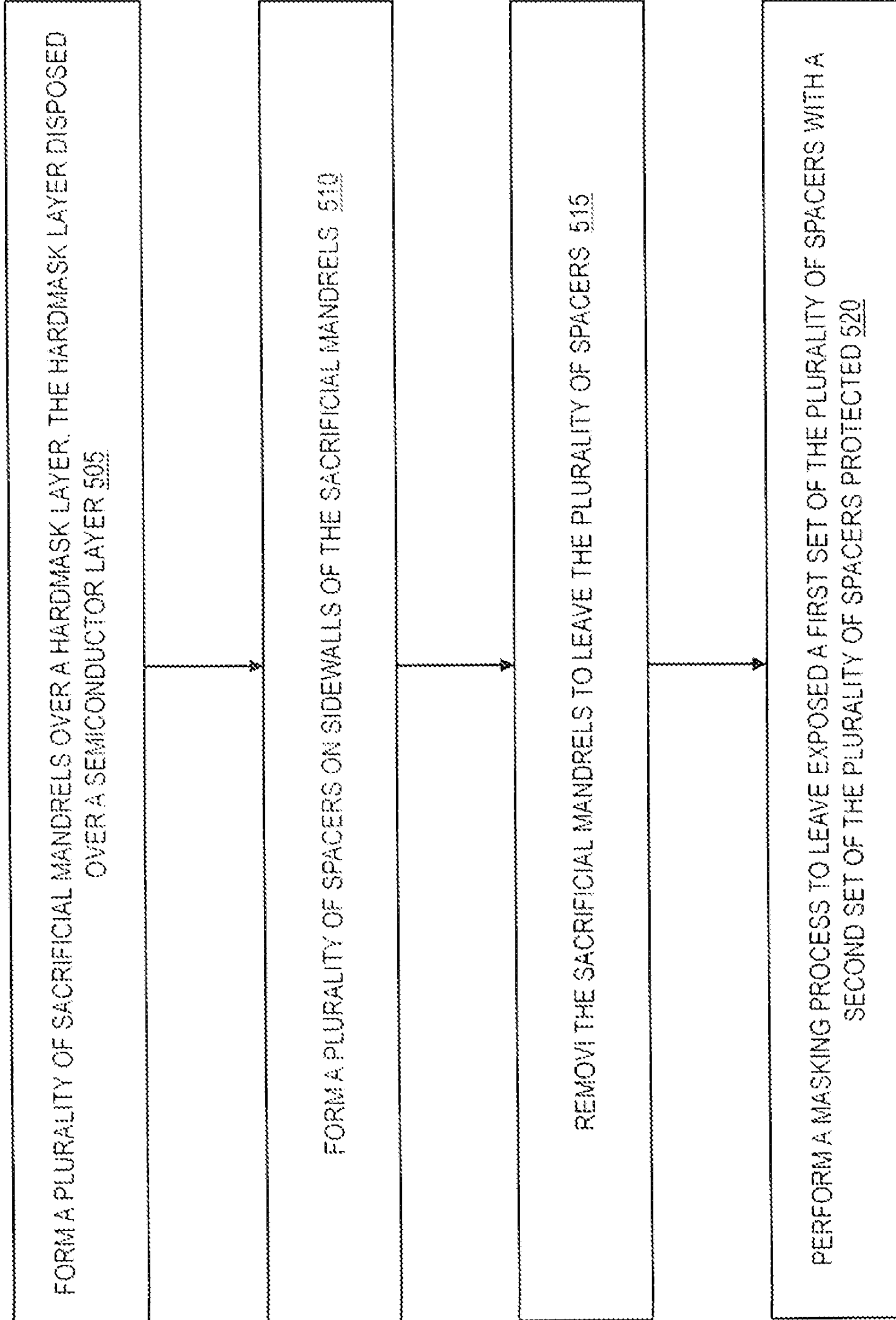


FIG. 5A

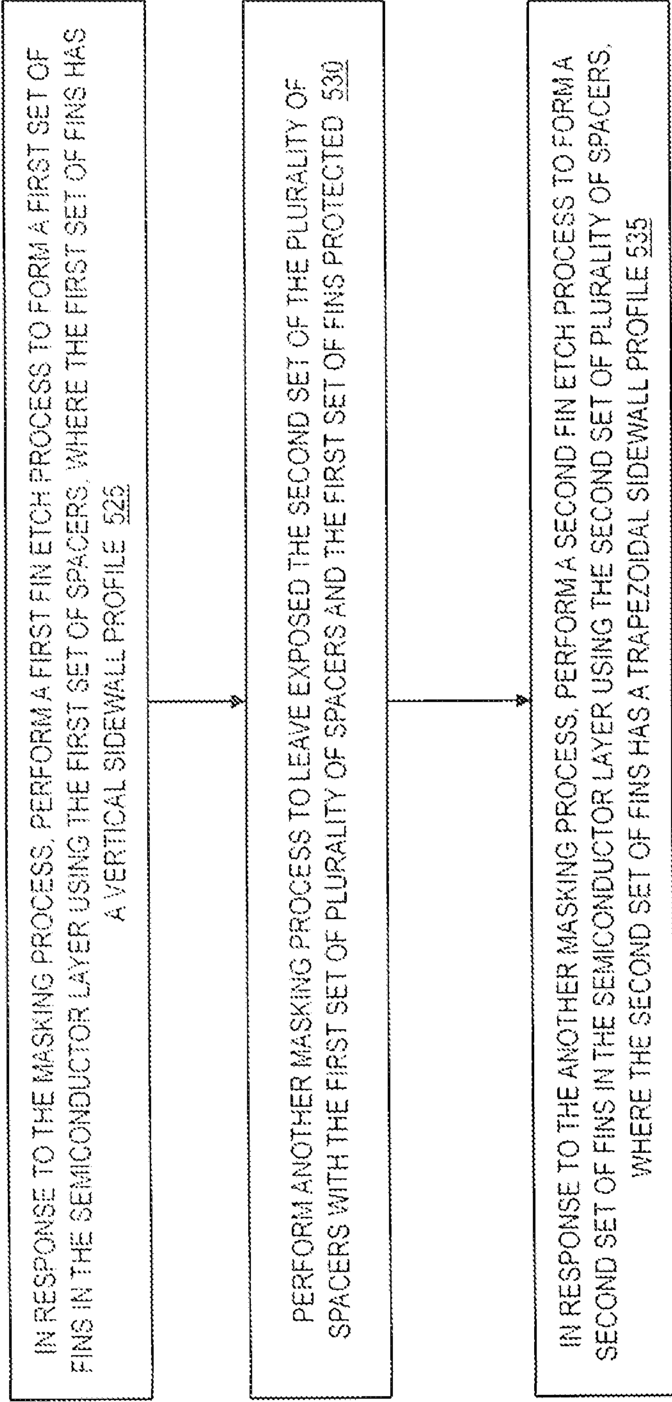


FIG. 5B

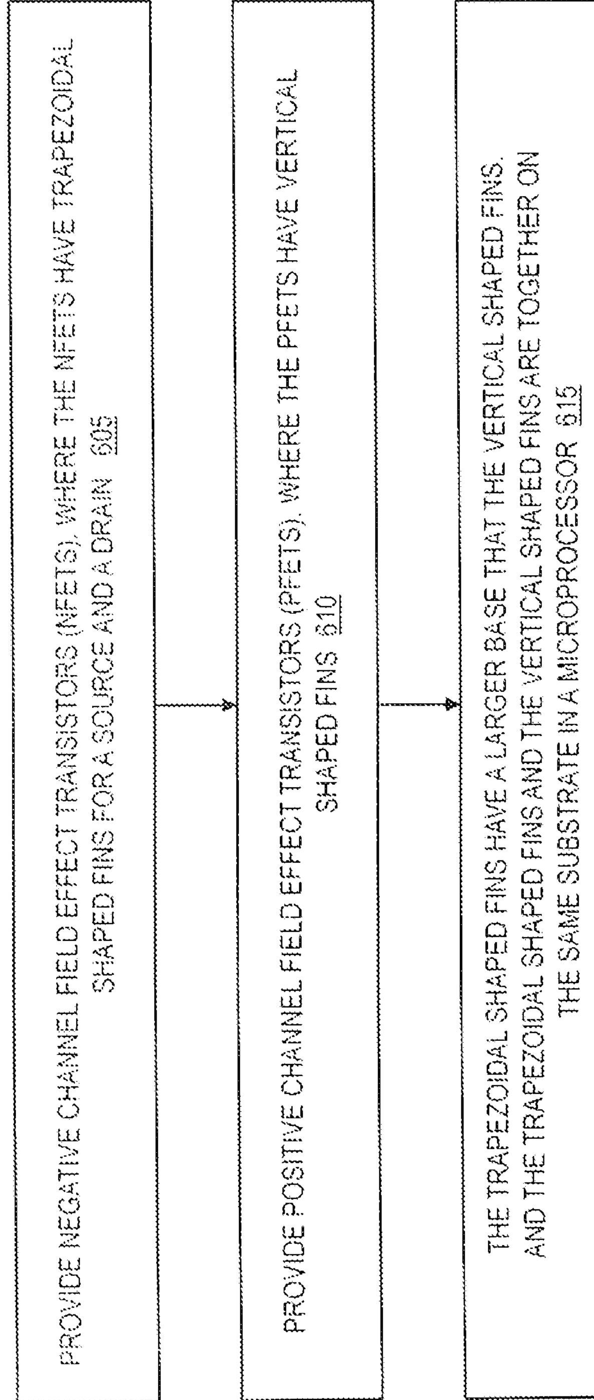
FIG. 6
600
PROVIDE NEGATIVE CHANNEL FIELD EFFECT TRANSISTORS (NFETS), WHERE THE NFETS HAVE TRAPEZOIDAL SHAPED FINS FOR A SOURCE AND A DRAIN 605
PROVIDE POSITIVE CHANNEL FIELD EFFECT TRANSISTORS (PFETS), WHERE THE PFETS HAVE VERTICAL SHAPED FINS 610
THE TRAPEZOIDAL SHAPED FINS HAVE A LARGER BASE THAT THE VERTICAL SHAPED FINS, AND THE TRAPEZOIDAL SHAPED FINS AND THE VERTICAL SHAPED FINS ARE TOGETHER ON THE SAME SUBSTRATE IN A MICROPROCESSOR 615

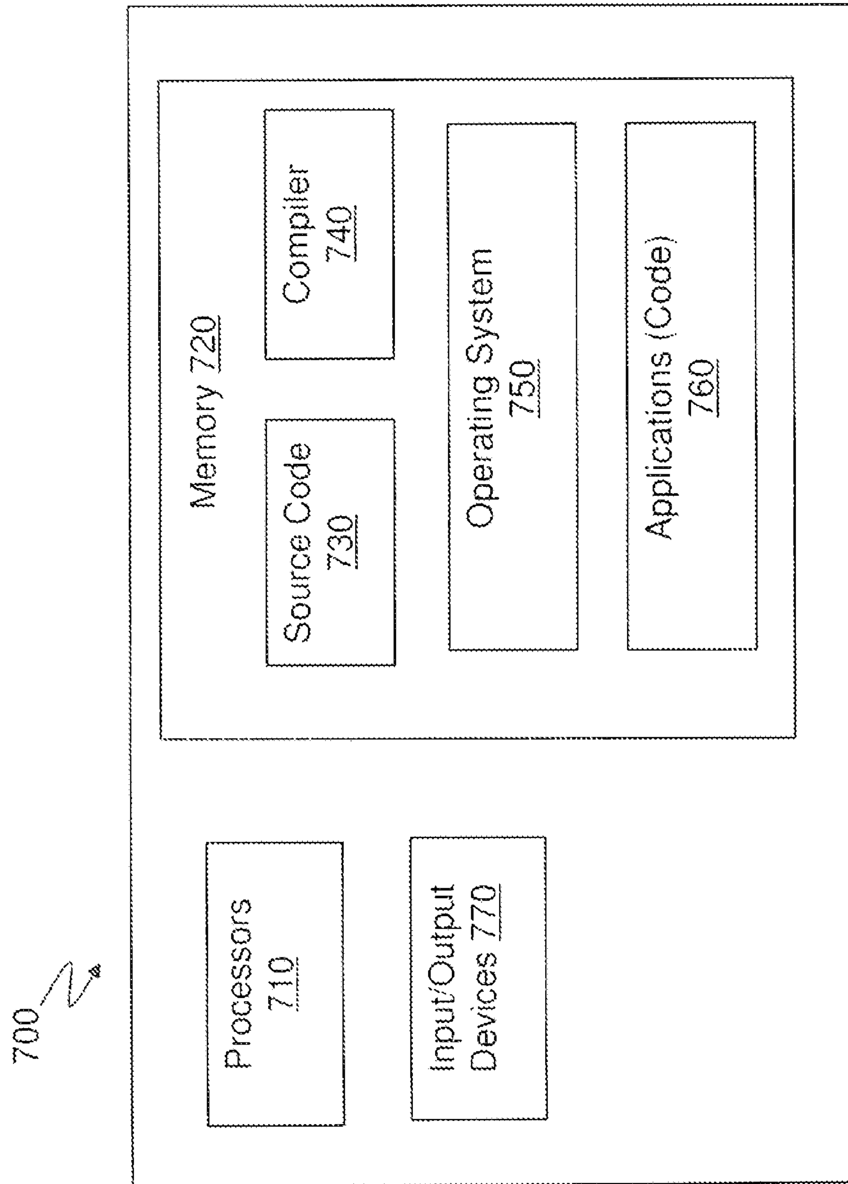


FIG. 7

# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/IB2016/050836**

**A. CLASSIFICATION OF SUBJECT MATTER**

H01L 21/336(2006.01)i; H01L 21/265(2006.01)i; H01L 27/092(2006.01)i; H01L 29/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNTXT;DWPI;VEN:hole, dual, substrate, semiconductor, fin, fins, angle, electron, hole, trapezoidal, mobility, vertical, device, perpendicular, slope, slant, incline, FINFET, first, second, mask, sidewall, spacer, source, drain, recess

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | CN 104078366 A (SHANGHAI INTEGRATED CIRCUIT RESEARCH & DEVELOPMENT CENTER) 01 October 2014 (2014-10-01)<br>description, paragraphs [0039] to [0056] and figures 2-3L | 1-14 |
| Y | CN 102194697 A (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED) 21 September 2011 (2011-09-21)<br>description, paragraphs [0032] to [0044] and figures 1-17 | 1-14 |
| A | EP 1993136 A1 (IMEC INTER UNI MICRO ELECTR) 19 November 2008 (2008-11-19)<br>the whole document | 1-20 |
| A | US 2005001273 A1 (IBM CORP) 06 January 2005 (2005-01-06)<br>the whole document | 1-20 |
| A | JP 2009054705 A (TOSHIBA CORP) 12 March 2009 (2009-03-12)<br>the whole document | 1-20 |

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| **06 June 2016** | **14 June 2016** |


| Name and mailing address of the ISA/CN | Authorized officer |
|---|---|
| **STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA**<br>**6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China** | **ZHANG,Hong** |
| Facsimile No. **(86-10)62019451** | Telephone No. **(86-10)62089915** |

**INTERNATIONAL SEARCH REPORT**
**Information on patent family members**

International application No.
**PCT/IB2016/050836**

| Patent document cited in search report | | | Publication date (day/month/year) | Patent family member(s) | | | Publication date (day/month/year) |
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| EP | 1993136 | A1 | 19 November 2008 | None | | | |
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| | | | | US | 2012009744 | A1 | 12 January 2012 |