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Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1.
NL-5621 BA Eindhoven(NL)

Inventor: Mac Kenna, Craig Alden
c/o INT. OCTROOIBUREAU B.V. Prof.
Holstlaan 6
NL-5656 AA Eindhoven(NL)
Inventor: Li, Jan-Kwei Jack
c/o INT. OCTROOIBUREAU B.V. Prof.
Holstlaan 6
NL-5656 AA Eindhoven(NL)

Representative: Strijland, Wilfred et al
INTERNATIONAAL OCTROOIBUREAU B.V.
Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

Logic circuit for expansion of monochrome display patterns to color form and video controller comprising such logic circuit.

A circuit which expands monochrome image-character patterns to color form for use in a raster scanned computer display system. Monochrome patterns are expanded from one bit per pixel to n bits per pixel. Foreground and background colors are programmable in a pattern generator which uses data from the expanded source patterns to select appropriate colors and characters for a destination pattern to be displayed. The expanded multicolor image is generated by hardware.

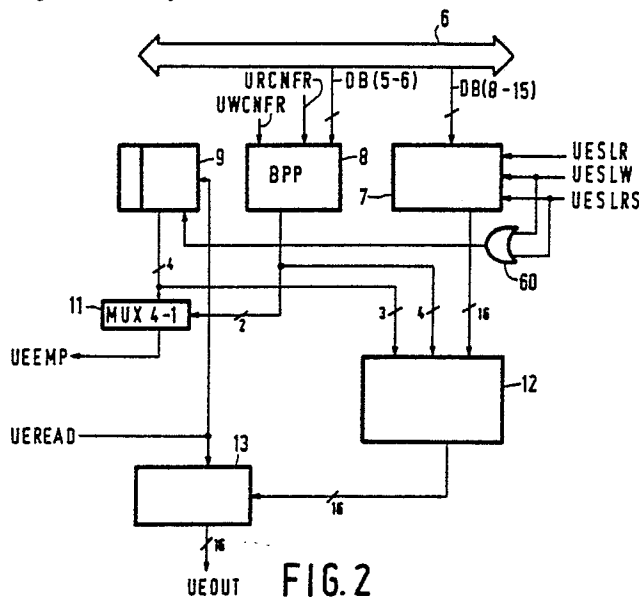


FIG. 2

Logic circuit for expansion of monochrome display patterns to color form and video controller comprising such logic circuit.

BACKGROUND TO THE INVENTION

This invention pertains to the general field of video display controllers or raster scan display controllers which are used in computer system. In particular it pertains to a logic circuit which is used to expand a monochrome image to a color image while minimizing memory storage requirements for a multicolor display.

Most presently available video display systems include a processor, a video controller, a display memory containing a single actual screen image, further system memory, and a raster scan video display. In normal or steady-state operation, the video controller continually reads out the contents of the display memory and transforms the information read into signals which control the raster scan beam during its active display time. The video controller also provides the horizontal and vertical retrace signals at appropriate intervals, and blanking of the raster scan beam during retrace.

The processor also has access to the display memory, so that it can change the actual screen image. This access may either be "through" the video controller or "around" it. The subject invention applies to the former type of system. In either case, use of the display memory typically involves careful control of updating accesses and display accesses to prevent image breakup while the video image is being changed.

20 SUMMARY OF THE INVENTION

An improved video controller incorporating the present invention is a logic circuit which has an address module and at least one data module. The controller is designed to work with an external processor which generates the necessary instructions. The major function of the address module is to generate both video addresses and update addresses, while the data modules are used to collect and integrate video data that have been read out from the display memory. The data output from the data module passes through high speed shift registers and a look-up table to a CRT display. The major parts of the address module are a synchronous signal generator, a window controller, an update controller and an interface controller. The address module also has the ability to update the contents of the display memory according to instructions passed from the host system. Thus, the host system itself does not have to access display memory to insert characters or graphic elements into display memory. It only passes the appropriate instructions and/or data to the controller. The present application pertains to a novel feature in the update controller.

In color CRT systems with two or more memory bits per pixel, many images/shapes/characters are shown in only one particular color. Such images can be defined by a pattern with one bit per pixel (1 = part of image, 0 = not part of image). When the display on a CRT screen is updated by a controller, the most typical operation is to display a shape/image/character on the screen in a single color. The shape is defined by a source monochrome pattern which is stored in display memory and has one bit per pixel. A -one-in the bit corresponding to a particular destination pixel indicates that the pixel is part of an image and should be displayed with a color code previously programmed in a foreground color latch. This invention expands such patterns into n-bit per pixel color form, with a programmable image color and an optional programmable background color. This minimizes memory requirements for storing patterns, and reduces the time needed to place the image on the screen.

The controller can be programmed to express a -zero-in the source pattern in either of two ways: a) by changing the corresponding pixel to the color code previously programmed into a background color latch, or b) by leaving the corresponding pixel unchanged. In the former mode of operation the entire region of the screen occupied by the image is changed to a new foreground/background image. In the latter mode, the image is drawn "over" a preexisting background. The operation is controlled by foreground color and background color registers, each of which has the number of bits needed to represent one pixel color code; the BPP register, which defines the number of bits per pixel; and a single bit register, write/overlay, which determines whether or not the background is to be changed.

Before active operation begins, all of these registers are loaded (e.g. by a microprocessor) with the desired values. Also, a counter in the expander is cleared to contain the value 0. A control unit begins active operation by fetching one word of the monochrome source pattern from the display memory and strobing it into a "Source Latch" in the expander. The function of the expander is to convert this source pattern into 1,

2, 4 or 8 words on its output. A programmed logic array in the expander performs this expansion by taking the word from the source latch, the contents of BPP (how much to expand), and the contents of register CT (which controls which word of a multi-word expansion is being done). A 4-to-1 multiplexer produces the "empty" output which tells the control unit when a new word must be fetched from the source pattern.

5 The control unit then fetches a word from the destination pattern and strobes it into the destination latch in the pattern generator. When both foreground and background are being changed, a smart control unit could omit this step, except for the first and last word of a scan line. A 2-to-1 multiplexer then selects between the destination data and the background latch, under control of a write/overlay register bit. For each bit, the corresponding output from the expander controls whether the display output is from the foreground latch or the 2-to-1 multiplexer. The resulting display is then colored and/or expanded according to the preprogrammed parameters.

10 Thus, in the present invention, the expansion of a monochrome image pattern to a multicolor form and/or the horizontal expansion of a character/image is programmable by the user and effected by a logical circuit. Furthermore, the same expansion circuitry is used for any level expansion. This feature adds flexibility to the system and widens its applicability. Although hereinafter, a CRT-display is described, other color display technologies would be applicable.

BRIEF DESCRIPTION OF THE DRAWINGS

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A preferred embodiment of the invention will be described with respect to the following Figures, wherein Figure 1 is a block diagram of an Update Controller subsystem of a raster scan video controller using the invention;

Figure 2 is a detail of the Expander block shown in Figure 1;

25 Figure 3 exemplifies the operation of the Expander for the particular case of four bits per pixel;

Figure 5 shows portions of the Pattern Generator block of Figure 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

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A bit-mapped raster scan video (CRT) controller has an address module and a data module. This controller provides hardware support for windows in a bit-mapped alphanumeric and graphic raster scan video (CRT) display system used in a computer system having one or more main processors and is particularly advantageous for use with multitasking operating systems. It typically includes logical circuits whereby a description of overlapping windows can be programmed.

35 The major parts of the address module are a synchronous signal generator, a window controller, an update controller and an interface controller. This application is directed primarily to the update controller of the address module. The major function of the address module is to generate both video addresses and update addresses, while the data modules are used to collect and integrate the display patterns that have been read out from the display memory. The data output by the data module(s) then goes through high speed shift register(s) and color look-up tables to the video display.

The address module also has the ability to update the contents of the display memory according to the instructions passed from the host system. Therefore, the host processor does not have to access the display memory when it wants to insert some characters or graphic elements into the display memory. Instead, it only needs to pass appropriate instructions to the address module.

45 After receiving the instructions passed from the host system, the address module executes them one by one like a special purpose microprocessor. Since the whole procedure is controlled by the internal hardware, updating can be done within a very short time. Typically the insertion speed is 5 to 50 times faster than a software procedure on the host processor.

50 Figure 1 shows the block structures of an Update Controller. It comprises an Expander 1, Pattern Shifter 2, Mask Generator 3, Pattern Generator 4, and Update Control Unit 5, and is connected to internal bus 6. The Update Control Unit 5 is used to update the display memory according to the instructions passed to it from the host system. The main update function provided by the Update Control Unit 5 is to insert characters and graphics elements into the display memory. A block move can be implemented as a special case of character insertion. In this mode, operation is similar to a monochrome character insertion operation. The expander may be used in a monochrome display mode to magnify the display patterns in the horizontal direction by a "zoom" factor of either 2, 4 or 8 times.

55 Details of the Expander 1 are shown in Figure 2. Under control of the Update Control Unit 5 and an

Interface Controller (not shown), "source words" are read from display memory (not shown) via Internal Data Bus 6 and placed in a Source Latch 7. Each source word has 16 bits and represents a part of an overall monochrome pattern that can either be expanded to a color form with 2, 4 or 8 bits per pixel or can be left in its incoming monochrome form with 1 bit per pixel.

5 The choice among these four alternative functions is determined by the preprogrammed contents of a BPP latch 8. This latch has 2 bits; its contents are encoded as follows:

TABLE 1

10	VALUE	FUNCTION
	00	Leave monochrome source word unchanged with 1 bit/pixel
	01	Expand monochrome source word to 2 bits/pixel
15	10	Expand monochrome source word to 4 bits/pixel
	11	Expand monochrome source word to 8 bits/pixel

The process of inserting a bit-mapped pattern into display memory may be divided into one or more major sections which correspond to successive scan lines on the screen. Each such major section is further divided into one or more successive 16-bit "destination words".

When expansion to 2, 4 or 8 bits/pixel is to be done, one source word contains information sufficient to update 2, 4 or 8 destination words (respectively) in display memory. Therefore in these cases, the Update Control Unit 5 must sequence memory accesses so that the appropriate number of destination words are accessed for each source word that is read from the monochrome pattern. A CT Counter 9 and 4-to-1 Multiplexer 11 function together to inform the Update Control Unit 5 when a new source word is needed by generating a signal named UEEMP which is fed back to the Update Control Unit 5. The CT Counter 9 is a 4-bit binary counter which is cleared whenever the Update Control Unit 5 loads a source word into Source Latch 7. The clear signal is produced by OR-gate 6 that combines the write and reset signals for Source Latch 7. The counter is incremented by 1 for each destination word that is processed and written back to memory. The 4-to-1 Multiplexer 11 has as its data inputs the four output bits of CT Counter 9 and the two outputs of the BPP Latch 8 as its control inputs. It functions as indicated in Table 2.

TABLE 2

35	IF THE BPP VALUE IS	THEN 4-1 MUX 11 PROPAGATES THE FOLLOWING BIT FROM CT COUNTER 9 TO LINE UEEMP	SO THAT LINE UEEMP BECOMES 1 AFTER THE FOLLOWING NUMBER OF DESTINATION WORDS ARE PROCESSED
	00	Least Significant	1
	01	2nd-Least Significant	2
45	10	2nd-Most Significant	4
	11	Most Significant	8

Thus, when UEEMP is 1, it is a signal to the Update Control Unit 5 that a new source word is needed.

50 Expansion Logic 12 takes as its inputs the 16 outputs of Source Latch 10, the 2 outputs of the BPP latch 8, and the three less-significant outputs of the CT counter 9. It uses these to divide the source word into 1, 2, 4 or 8 equal segments having 16, 8, 4 or 2 bits each respectively, depending on the BPP value. Each such segment corresponds to one destination word, and for each segment the Expansion Logic produces a 16-bit word at its outputs, having 1, 2, 4 or 8 consecutive bits (respectively) equal to the value of 1 bit of the segment. The operation of the Expansion Logic 12 is exemplified in Figure 3, for a BPP value of 10, that is, 4 bits/pixel.

55 The Expansion Logic can be a set of logic gates or a Programmable Logic Array (PLA). In either case, the Expansion Logic operates according to the logic equations in Tables 3a, 3b.

INPUTS: CT0 is the least-significant bit from the CT counter 8 thru CT3 is the most-significant bit from the CT counter 8

IO is the least-significant bit from the source latch 6 thru I15 is the most-significant bit from the source latch 6

5 BBP0 is the less-significant bit from the BPP latch 7

BBP1 is the more-significant bit from the BPP latch 7

NOTATION:

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* indicates and AND operation

/ indicates a NOT (inversion, negation) operation

+ indicates an OR operation

Table 3a, 3b show INTERMEDIATE LOGIC TERMS; table 3c shows output signals.

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The outputs of the Expansion Logic are stored in a 16-bit Latch 13, and are captured therein at the same time the CT Counter 9 is signalled to increment, that is, once for each destination word processed and written into memory. The outputs of Latch 13 constitute the output of the Expander 1 to the Pattern Shifter 2.

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The Pattern Shifter 2 aligns the output of the Expander 1 to correspond to "destination" data read from display memory. This function is not necessary to implement the present invention. For clarity of explanation, the Pattern Shifter is herein assumed to propagate the output from the Expander 1 to the Pattern Generator 4, without change.

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Since the pattern to be inserted into display memory can start and end at any pixel on the screen, and can be any number of pixels in width, it is typical for part of the first and last destination words of each major section to remain unchanged by the insertion process. The function of the Mask Generator 3 is to produce the bit patterns required for proper operation of the Pattern Generator 4, so that such parts of such first and last destination words remain unchanged. However, this function is also not necessary to implement the present invention. Herein it is assumed that the pattern to be inserted does indeed affect the entire first and last destination words of each major section, in which case the Mask Generator 3 outputs all zeroes to the Pattern Generator 4.

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The Pattern Generator 4 combines, for each destination word in each major section, some or all of the following information:

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1) the (optionally) expanded and shifted source information from the Pattern Shifter;

2) the previously-existing contents of said word in display memory;

3) the preprogrammed contents of a Foreground Color Register; and

4) the preprogrammed contents of a Background Color Register; to produce new contents for said word in display memory in accordance with other preprogrammed register contents.

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Figure 4 shows details of the Pattern Generator 4. Prior to the start of active operation, certain registers are preprogrammed (e.g., by a system microprocessor). Write/Overlay Register 55 is programmed to the "Write" state if pixels corresponding to zeroes in the monochrome are to be changed to the contents of the Background Color Register, or to the "Overlay" state if such pixels are to be left unchanged in display memory. Foreground Color Register 54 is programmed to contain the value to which pixels corresponding to -ones- in the monochrome pattern are to be changed. If Write/Overlay Register 55 is programmed to "Write", then Background Color Register 53 is programmed to contain the value to which pixels corresponding to zeroes in the monochrome pattern are to be changed.

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In the preferred embodiment both the Color Registers 53 and 54 are implemented as 8 bits wide. Because the major data paths of the Pattern Generator are 16 bits wide, the outputs of these registers are replicated twice into the inputs of Multiplexers 56 and 58 respectively. If the number of destination bits/pixel is 4, 2 or 1, then the Color Registers are typically programmed with the desired pixel value replicated 2, 4 or 8 times, respectively, but alternatively in this case, various graphic-pattern effects can be produced on the screen by programming the 2, 4 or 8 pixels in a Color Register to different values.

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The Update Control Unit 5, operating via the Interface Controller (not shown), reads one word from memory and places the data therefrom into the Source Latch 7, for each 8, 4, 2 or 1 destination words written into memory. For each such destination word, the Update Control Unit 5 may read the data from the word and place the data therefrom into the Destination Latch Register 52. The invention applies to both a simple embodiment of an Update Control Unit 5, which always reads each destination word from memory, and to a more complex and efficient embodiment which uses additional signals from the other blocks, so as

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to omit this step of reading a destination word if/when its contents are not needed to form the new contents for the word.

Two-to-one Multiplexer 56 selects between existent destination pixels from the Destination Latch 52, or the pixels from the Background Color Register 53, all 16 of its bits or stages being controlled by the common signal from the Write/Overlay Register 55. Thus the output of Multiplexer 56 may be characterized as the "effective background" that is used for pixels corresponding to zeroes in the monochrome pattern.

Multiplexer 57 propagates the "expanded and shifted" source data from the Pattern Shifter 2 to its outputs.

Two-to-one Multiplexer 58 selects between the "effective background" from Multiplexer 56, and the pixels from the Foreground Color Register 54, each of its bits or stages being individually controlled by the corresponding bit from Multiplexer 57. Thus the selection for each bit is, in effect, controlled by the Pattern Shifter 2, the Expander 1, and ultimately by one of the monochrome bits in the Source Latch 7. The output of Multiplexer 58 may be characterized as the integration of the foreground and background parts of the pattern.

Two-to-one Multiplexer 59 selects between the output of Multiplexer 58 and the output of Destination Latch 13, each of its bits of stages being individually controlled by the corresponding bit from the Mask Generator 3. This multiplexer handles the preservation of "unaffected" pixels in the first and last destination words for each scan line. For clarity in describing the invention, Multiplexer 59 can be assumed to propagate the data from Multiplexer 58 to its outputs.

The Drivers 60 are controlled by the Update Control Unit 5 so as to place the result from Multiplexer 59 on the internal bus 6, at the appropriate time so that it is propagated to the device's external data pins, and ultimately written to the destination word in display memory.

The Update Control Unit 5 controls the repetition of this process for each destination word in each scan line of the monochrome pattern, reading new source words from the monochrome pattern as needed.

The invention is generally applicable to any 3-way multiplexing scheme among existing destination data and two preprogrammed constant registers, said multiplexing controlled by a single write/overlay control bit and a plurality of foreground/background control bits that are derived from expanding a monochrome pattern by the method described herein.

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TABLE 3a

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NO = IO * /BPP1 * /BPPO
 N1 = I1 * /BPP1 * /BPPO
 N2 = I2 * /BPP1 * /BPPO
 N3 = I3 * /BPP1 * /BPPO
 N4 = I4 * /BPP1 * /BPPO
 N5 = I5 * /BPP1 * /BPPO
 N6 = I6 * /BPP1 * /BPPO
 N7 = I7 * /BPP1 * /BPPO
 N8 = I8 * /BPP1 * /BPPO
 N9 = I9 * /BPP1 * /BPPO
 N10 = I10 * /BPP1 * /BPPO
 N11 = I11 * /BPP1 * /BPPO
 N12 = I12 * /BPP1 * /BPPO
 N13 = I13 * /BPP1 * /BPPO
 N14 = I14 * /BPP1 * /BPPO
 N15 = I15 * /BPP1 * /BPPO
 N16 = IO * /BPP1 * /BPPO * CTO
 N17 = I1 * /BPP1 * /BPPO * CTO
 N18 = I2 * /BPP1 * /BPPO * CTO
 N19 = I3 * /BPP1 * /BPPO * CTO
 N20 = I4 * /BPP1 * /BPPO * CTO
 N21 = I5 * /BPP1 * /BPPO * CTO
 N22 = I6 * /BPP1 * /BPPO * CTO
 N23 = I7 * /BPP1 * /BPPO * CTO
 N24 = I8 * /BPP1 * /BPPO * /CTO
 N25 = I9 * /BPP1 * /BPPO * /CTO
 N26 = I10 * /BPP1 * /BPPO * /CTO
 N27 = I11 * /BPP1 * /BPPO * /CTO
 N28 = I12 * /BPP1 * /BPPO * /CTO
 N29 = I13 * /BPP1 * /BPPO * /CTO
 N30 = I14 * /BPP1 * /BPPO * /CTO
 N31 = I15 * /BPP1 * /BPPO * /CTO

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TABLE 3b

N32 = I0 * BPP1 * /BPPO * CT1 * CTO
 N33 = I1 * BPP1 * /BPPO * CT1 * CTO
 10 N34 = I2 * BPP1 * /BPPO * CT1 * CTO
 N35 = I3 * BPP1 * /BPPO * CT1 * CTO
 N36 = I4 * BPP1 * /BPPO * CT1 * /CTO
 15 N37 = I5 * BPP1 * /BPPO * CT1 * /CTO
 N38 = I6 * BPP1 * /BPPO * CT1 * /CTO
 N39 = I7 * BPP1 * /BPPO * CT1 * /CTO
 20 N40 = I8 * BPP1 * /BPPO * /CT1 * CTO
 N41 = I9 * BPP1 * /BPPO * /CT1 * CTO
 N42 = I10 * BPP1 * /BPPO * /CT1 * CTO
 N43 = I11 * BPP1 * /BPPO * /CT1 * CTO
 25 N44 = I12 * BPP1 * /BPPO * /CT1 * /CTO
 N45 = I13 * BPP1 * /BPPO * /CT1 * /CTO
 N46 = I14 * BPP1 * /BPPO * /CT1 * /CTO
 30 N47 = I15 * BPP1 * /BPPO * /CT1 * /CTO
 N48 = I0 * BPP1 * BPPO * CT2 * CT1 * CTO
 N49 = I1 * BPP1 * BPPO * CT2 * CT1 * CTO
 35 N50 = I2 * BPP1 * BPPO * CT2 * CT1 * /CTO
 N51 = I3 * BPP1 * BPPO * CT2 * CT1 * /CTO
 N52 = I4 * BPP1 * BPPO * CT2 * /CT1 * CTO
 N53 = I5 * BPP1 * BPPO * CT2 * /CT1 * CTO
 40 N54 = I6 * BPP1 * BPPO * CT2 * /CT1 * /CTO
 N55 = I7 * BPP1 * BPPO * CT2 * /CT1 * /CTO
 N56 = I8 * BPP1 * BPPO * /CT2 * CT1 * CTO
 45 N57 = I9 * BPP1 * BPPO * /CT2 * CT1 * CTO
 N58 = I10 * BPP1 * BPPO * /CT2 * CT1 * /CTO
 N59 = I11 * BPP1 * BPPO * /CT2 * CT1 * /CTO
 50 N60 = I12 * BPP1 * BPPO * /CT2 * /CT1 * CTO
 N61 = I13 * BPP1 * BPPO * /CT2 * /CT1 * CTO
 N62 = I14 * BPP1 * BPPO * /CT2 * /CT1 * /CTO
 N63 = I15 * BPP1 * BPPO * /CT2 * /CT1 * /CTO

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TABLE 3c

5	OUT0 =	N0+N16+N24+N32+N36+N40+N44+N48+N50+N52+N54+N56+N58+N60+N62
	OUT1 =	N1+N16+N24+N32+N36+N40+N44+N48+N50+N52+N54+N56+N58+N60+N62
	OUT2 =	N2+N17+N25+N32+N36+N40+N44+N48+N50+N52+N54+N56+N58+N60+N62
	OUT3 =	N3+N17+N25+N32+N36+N40+N44+N48+N50+N52+N54+N56+N58+N60+N62
10	OUT4 =	N4+N18+N26+N33+N37+N41+N45+N48+N50+N52+N54+N56+N58+N60+N62
	OUT5 =	N5+N18+N26+N33+N37+N41+N45+N48+N50+N52+N54+N56+N58+N60+N62
	OUT6 =	N6+N19+N27+N33+N37+N41+N45+N48+N50+N52+N54+N56+N58+N60+N62
15	OUT7 =	N7+N19+N27+N33+N37+N41+N45+N48+N50+N52+N54+N56+N58+N60+N62
	OUT8 =	N8+N20+N28+N34+N38+N42+N46+N49+N51+N53+N55+N57+N59+N62+N63
	OUT9 =	N9+N20+N28+N34+N38+N42+N46+N49+N51+N53+N55+N57+N59+N62+N63
20	OUT10 =	N10+N21+N29+N34+N38+N42+N46+N49+N51+N53+N55+N57+N59+N62+N63
	OUT11 =	N11+N21+N29+N34+N38+N42+N46+N49+N51+N53+N55+N57+N59+N62+N63
	OUT12 =	N12+N22+N30+N35+N39+N43+N47+N49+N51+N53+N55+N57+N59+N62+N63
	OUT13 =	N13+N22+N30+N35+N39+N43+N47+N49+N51+N53+N55+N57+N59+N62+N63
25	OUT14 =	N14+N23+N31+N35+N39+N43+N47+N49+N51+N53+N55+N57+N59+N62+N63
	OUT15 =	N15+N23+N31+N35+N39+N43+N47+N49+N51+N53+N55+N57+N59+N62+N63

30 **Claims**

1. A logic circuit for use in a color imaging system, for expanding a monochrome image having one bit per picture element to a color image having multiple bits per picture element, and for integration of that expanded image into an existing image in a memory, comprising:
- 35 an expander circuit including:
- a) a source latch for storing a part of said monochrome image;
 - b) extension latch means for defining an extension factor between one and an upper boundary that is greater than one;
 - c) source tracking means for determining successive currently-operating parts of said source latch,
 - 40 and signal a need to reload said source latch from memory;
 - d) expansion logic having inputs fed by outputs of said source latch, said extension latch means, and said source tracking means; and having as its outputs a signal representing one of an expanded and a non-expanded version of the contents of said source latch, wherein the number of consecutive bits indicated by the extension latch means correspond to one bit in the source latch;
 - 45 alignment means which shift the output of said expansion logic in said expander circuit, to correspond to the positioning of destination words in said memory;
 - clipping means which preserve parts of destination words in said memory, which are outside of said expanded image;
 - a pattern generator circuit comprising:
 - 50 a) a foreground register programmable with picture element value(s) which are to be substituted for ONES in said monochrome image;
 - b) a background register programmable with picture element value(s) that can optionally be substituted for ZEROS in said monochrome image;
 - c) a single-bit register programmable to alternately control picture elements corresponding to zeroes
 - 55 in said monochrome image 1) to be left unchanged, or 2) to be changed to the contents of said background register;
 - d) a destination latch, in which the contents of destination words in memory can be temporarily stored;

e) multiplexing logic which selects among the contents of said foreground register, said background register, and said destination latch, under control of the output of said single-bit register, said alignment means, and said clipping means; having as its output new contents for the current destination word; and control means which sequence the reading of memory data and its storage in said source and destination latches, and the writing of said new contents to memory.

2. The logic circuit as claimed in Claim 1, wherein said bits per pixel means are programmable for 1, 2, 4 or 8 bits/pixel.

3. A logic circuit as claimed in Claims 1 or 2, wherein said source tracking means comprises a counter capable of counting from zero through the number of bits per pixel minus 1, and a multiplexer having as its data inputs the outputs of said counter and having as its control inputs the outputs of said extension latch means; said multiplexer having as its output a signal indicating whether said source latch needs to be reloaded.

4. A logic circuit as claimed in Claims 1, 2 or 3, wherein said expansion logic is a logic array (PLA) structure.

5. In a video controller which receives bit mapped source pattern data from a display memory and converts said data into output signals for controlling a raster scan video display, the improvement comprising:

means which store color data which is associated with particular monochrome shape/image/character patterns in the display memory and

means which expand the data received from said display memory to selectively add color information to representations of said monochrome patterns in said output signal as claimed in any of Claims 1 through 4.

6. A logic circuit for expanding a monochrome image of a raster scan display to a color image while minimizing display memory storage requirements for use in a raster scan video controller of a computer display system, comprising:

a control unit to control operations of said circuit;

an expander circuit comprising:

a programmable bits per pixel register defining the number of bits per pixel for a colored/expander image;

a counter to control the output sequence of expanded, source patterns;

a source pattern latch which receives sequentially monochrome source patterns from display memory having one bit per pixel and defining shapes to be expanded and displayed;

a programmed logic array having as inputs the contents of said source pattern latch, said bits per pixel register, and said counter; the output of the PLA being a sequence of expanded source patterns;

a multiplexer connected to said counter and said bits per pixel register to produce a zero output indicating the completion of the expansion of one source pattern from said source pattern latch and a signal to said control unit to fetch the next source pattern, said signal being asserted when the output of said counter equals the value in said bits per pixel register;

a pattern generator having:

a foreground color latch programmable with a color code selected for a foreground image;

a background color latch programmable with a color code selected for the background of a displayed image;

a destination latch to receive sequentially destination patterns in display memory having one bit per pixel indicating which pixels are part of an image to be displayed;

a write/overlay register programmable to indicate whether the background of an image to be displayed should be filled;

a multiplexer to select between data in said destination latch and said background color latch under the control of said write/overlay register;

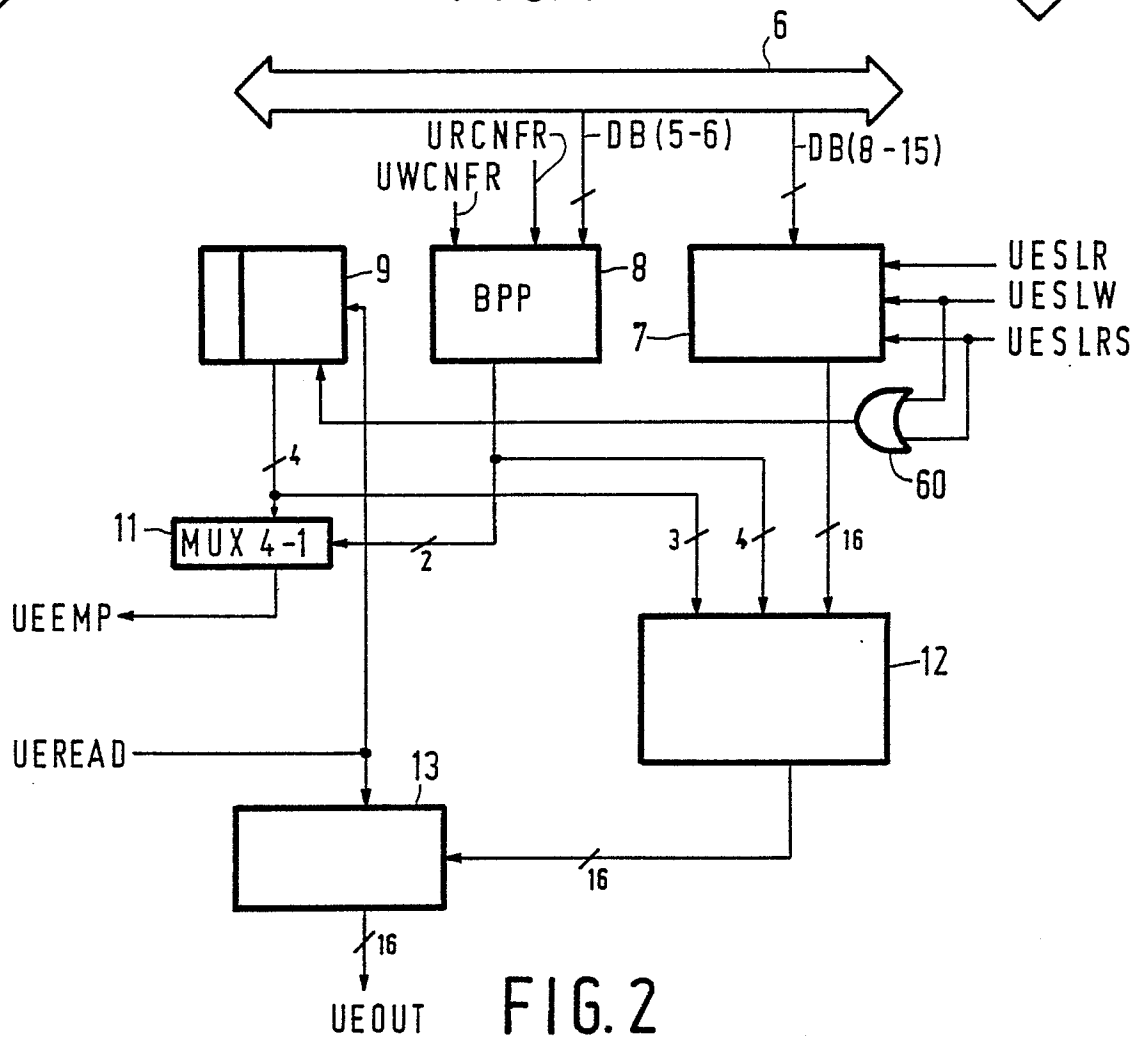
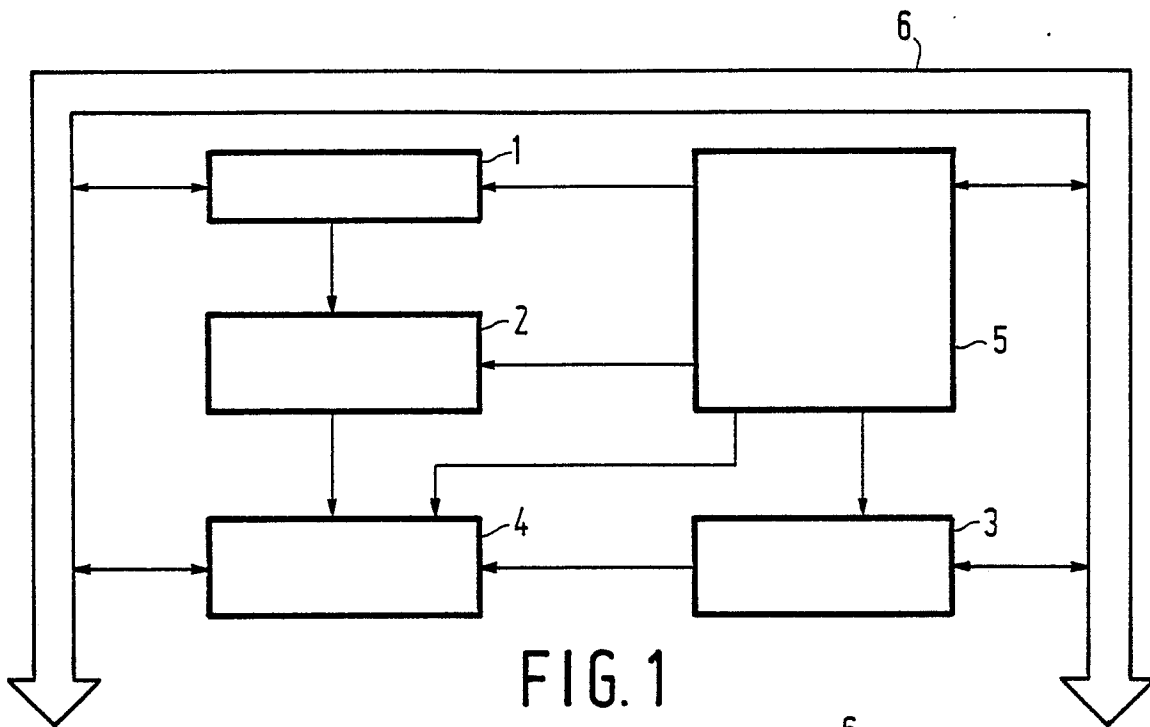
means under control of said expanded source pattern output from said expander to select between data in said foreground latch and from said multiplexer, said latter selected data being data for the colored and/or expanded image for said display.

7. The logic circuit of Claim 6 wherein said bits per pixel register may be programmed for one, two, four or eight bits per pixel.

8. The logic circuit of Claim 6 wherein a zero in a source pattern is expanded to a color code programmed into said background latch.

9. The logic circuit of Claim 6 wherein a zero in a source pattern is left unchanged.

11. The logic circuit of Claim 6 wherein said source pattern is a character font.



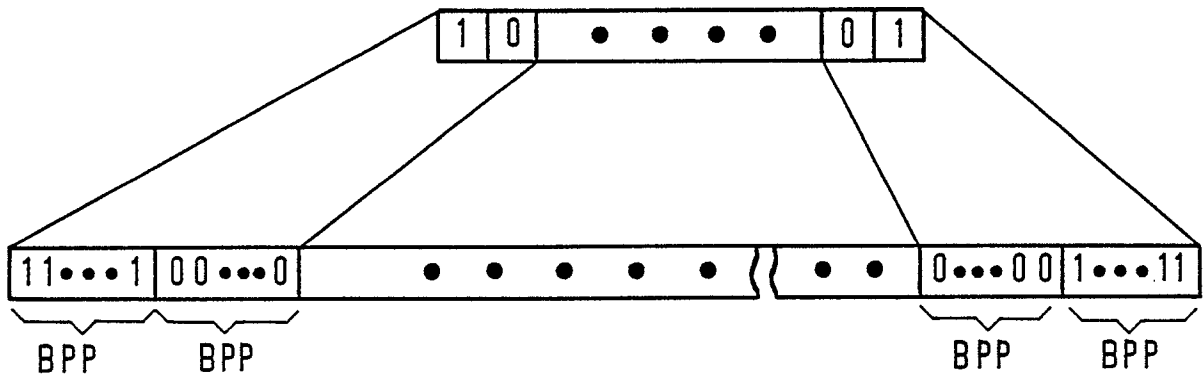


FIG. 3

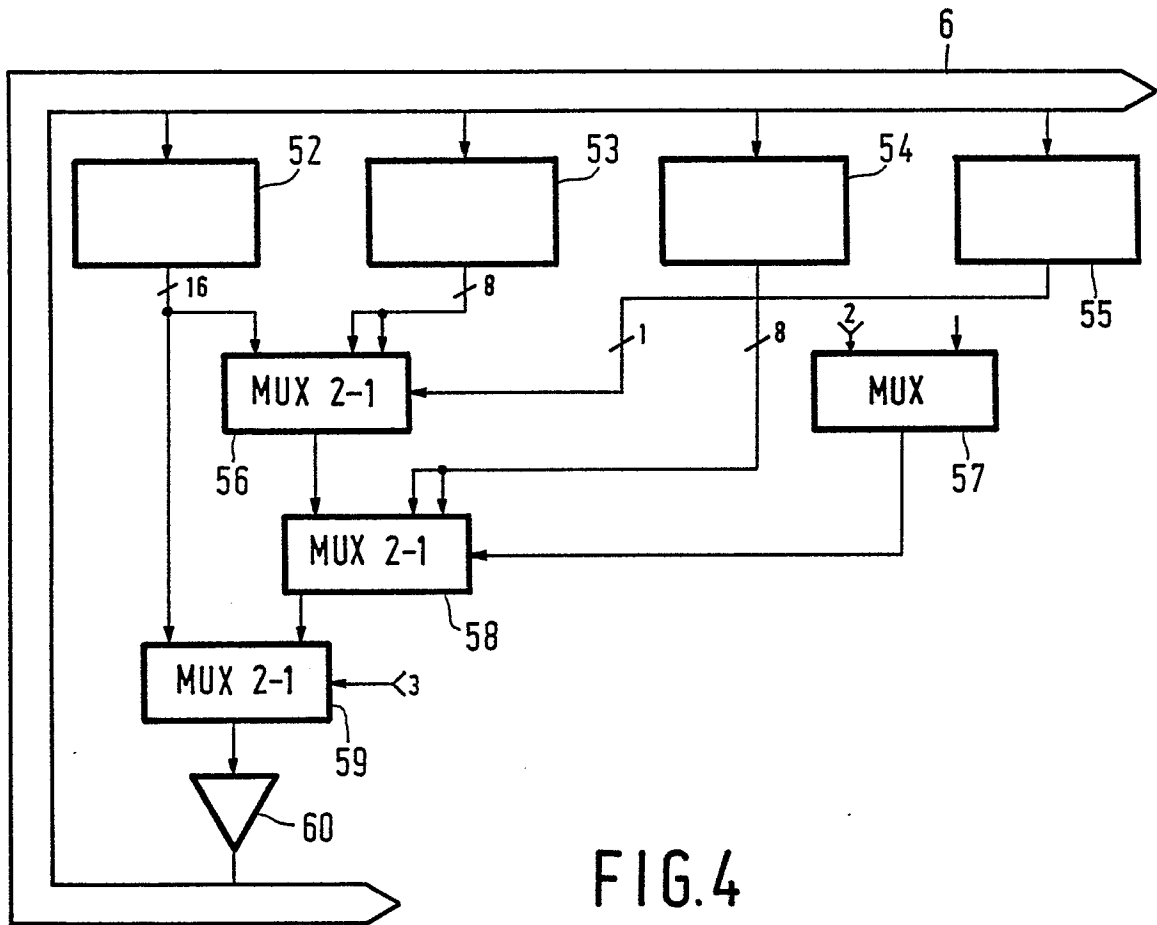


FIG. 4