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H4K
(71) Applicant
ITALTEL Societa Italiana
Telecomunicazioni SpA
Piazzale Zavattari 12
20149 Milan
Italy
(72) Inventors
Marcello Tommasi
Vincenzo Falzone
(74) Agents
Marks and Clerk
57/60 Lincoln's Inn
Fields
London WC2A 3LS

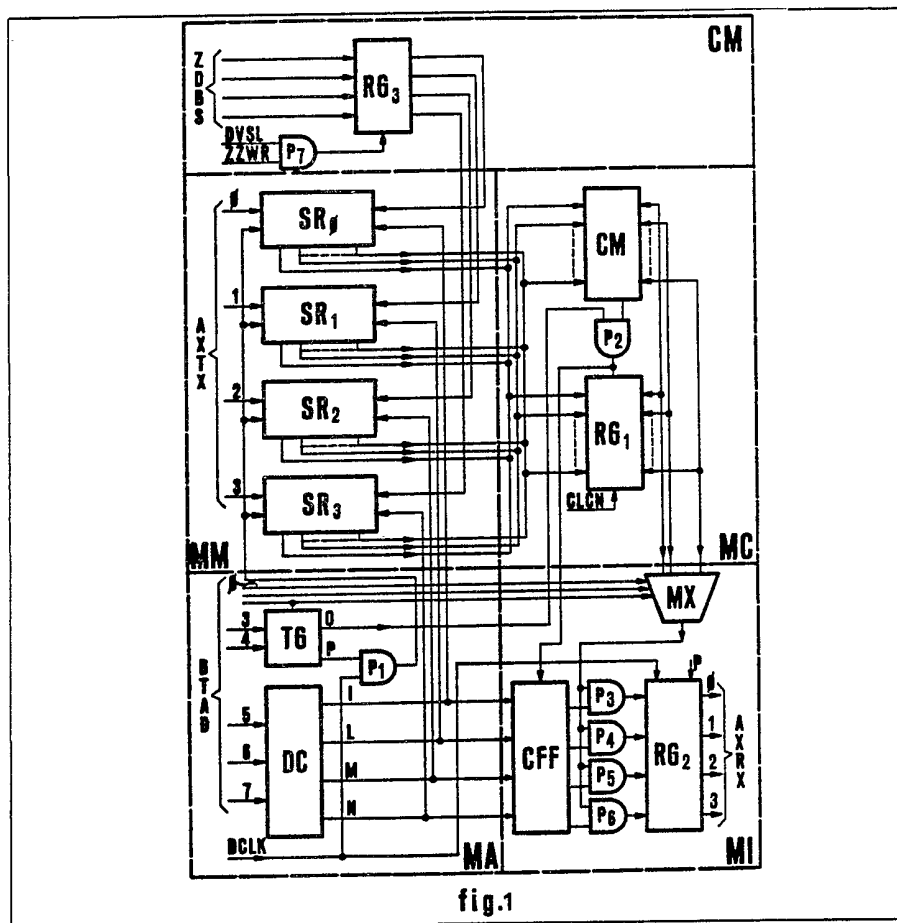
(54) TDM conference circuit

(57) Known T.D.M. conference circuits supply each participant with a signal which is the sum of the signals generated by the remaining users taking part in the conference. The signals are affected by a noise ratio which is a function of the number of users.

This invention provides a conference circuit which has a first means (MM) for storing the signals during a predetermined time slot of the frame according to which the PCM signals are arranged, second means (MC) for locating the highest level signal sample, third means (MI) for sending a null signal to the user generating the highest level signal sample and for sending the highest level signal sample to the other users, fourth means (MA) which enables the first, second and third

means (MM, MC, MI) by way of a digital word increasing at half the digit rate of the PCM signals and fifth means (CM) for enabling the first means (MM).

The noise ratio problem is mitigated as are other problems associated with the known circuits.



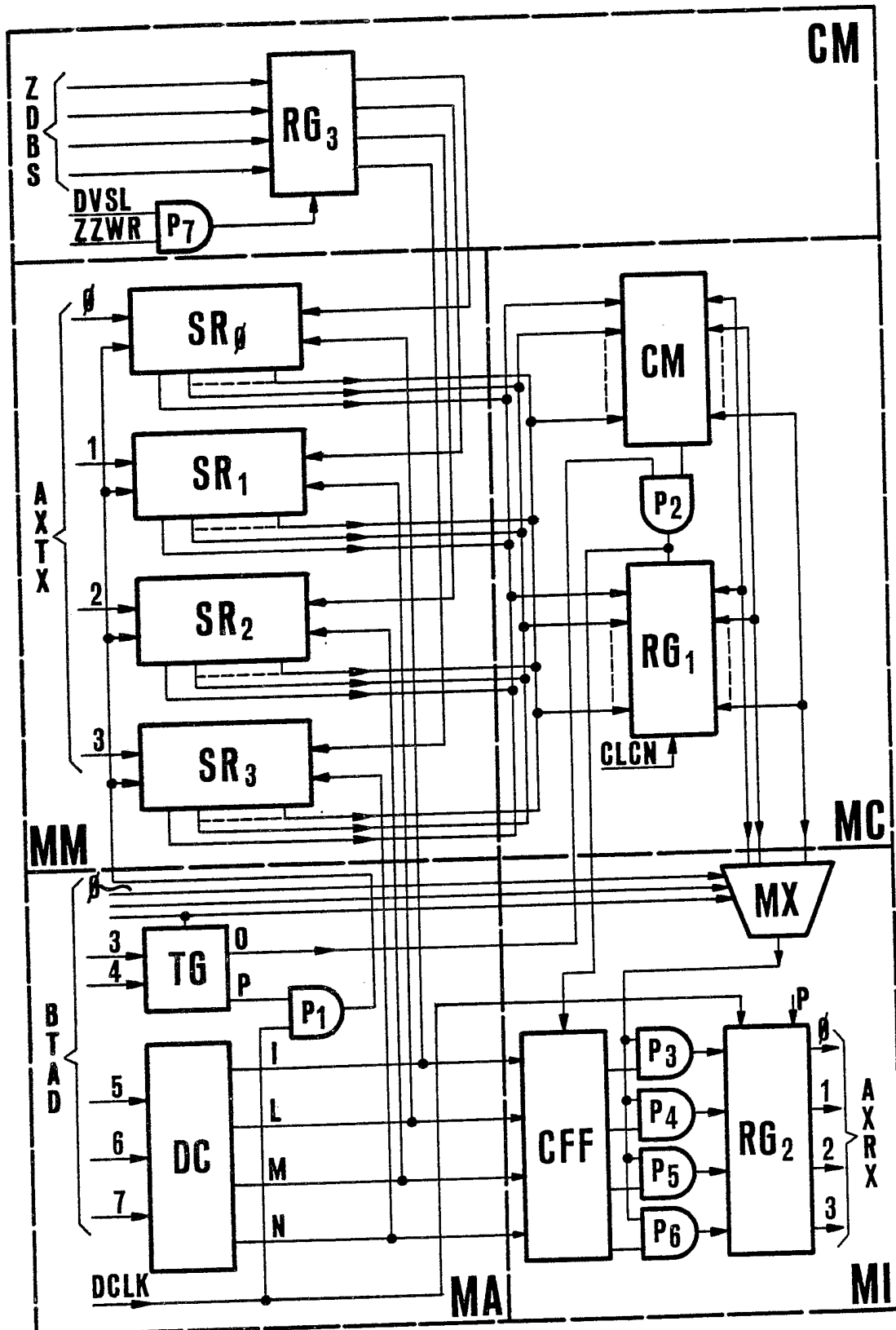


fig.1

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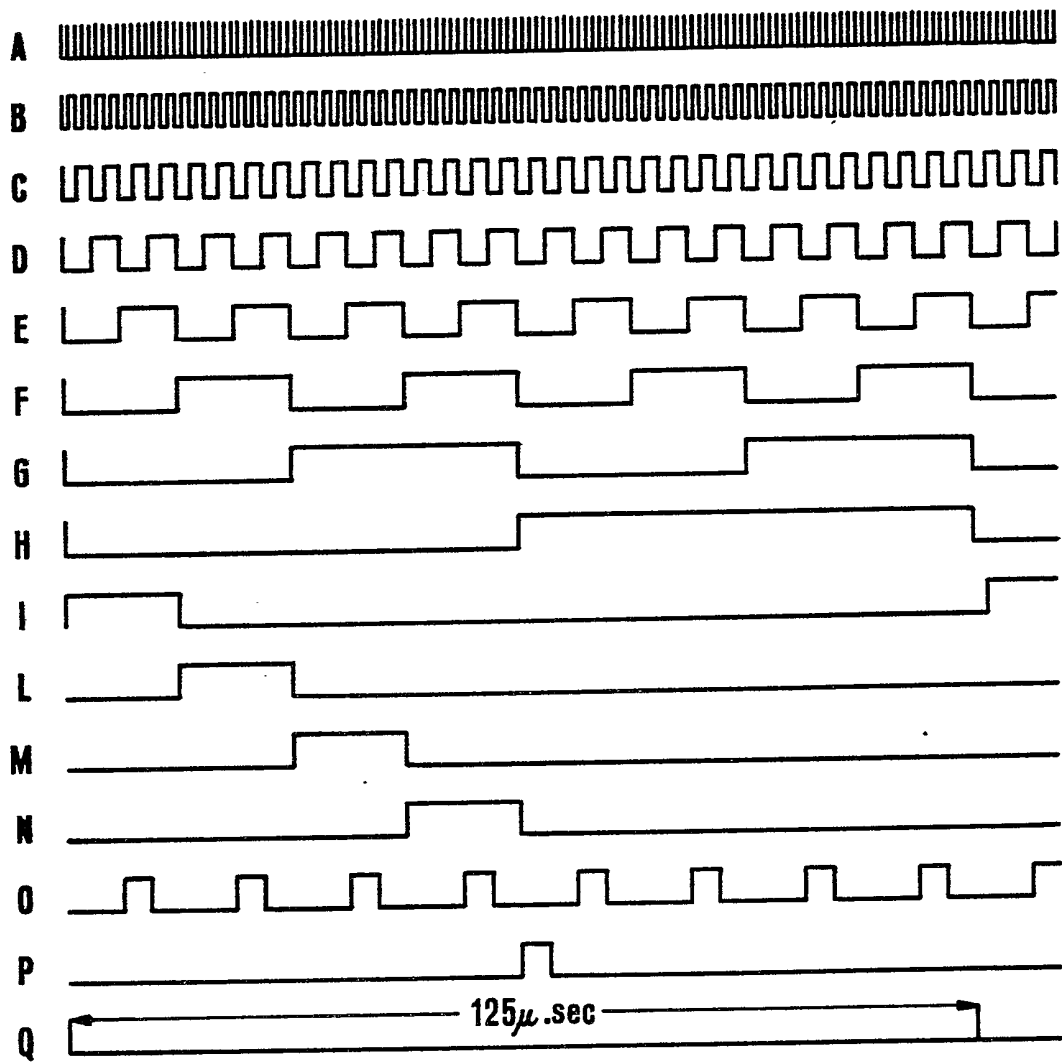


fig.2

SPECIFICATION

Conference circuit for switching numerical type telephone exchanges

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The present invention relates to a conference circuit for switching telephone exchanges of numerical type comprising at least a switching module formed by a matrix designed to perform switching of the signal samples allocated to a prefixed number of PCM bundles, on the basis of the messages supplied by a control circuit.

Prior art conference circuit for telephone exchanges utilize the algorithm of the sum.

The Italian patent number 1.040.208 discloses a conference circuit adapted to use the said algorithm and to supply each user with a signal which is the sum of the signals generated by the remaining users taking part in the conference.

Such a circuit has the drawback that the signal received by each user is affected by a noise ration which is a function of the number of users taking part in the conference.

In fact, let us assume that n users take part in the conference and that at a given instant only one of them generates a voice signal: a conference circuit utilizing the aforesaid algorithm adds the said signal to the noise present in the circuits of the $n - 1$ users; thus, the greater the number n , the less intelligible the voice signal.

Moreover, assuming that at a given instant there are three users taking part in a conference and that only the signal relative to one of them presents a high level, the use of the sum algorithm causes the signal generated by the other two subscribers to produce on the high level signal a result comparable with that caused by disturbance signals with the consequence that sometimes a non-intelligible signal is forwarded.

A further drawback of the aforesaid conference circuit is that the digital signals relative to the signal samples reach the conference circuit in compressed form (8 bits): granted that the sum of such digital words cannot be computed on compressed signals, the known conference circuits require the presence of means designed to expand such signals thus obtaining a word of 12 bits, as well as to compress them again, thus obtaining a word of 8 bits, after the summing operations have been performed, or alternatively, adapted to effect a local linearization as described in the aforementioned patent.

The object of the present invention is the realization of a conference circuit designed to mitigate the aforesaid drawbacks and to achieve this using circuit solutions which are particularly simple and economical.

To this aim, the conference circuit according to the invention uses an algorithm which performs a search for the highest level signal

sample among all those received at its input in a given moment, forwards a null signal to the subscriber who has emitted the highest level sample and forwards the said signal sample to the remaining users taking part in the conference.

Thus, the users receive a signal affected by a noise ratio which is only that of the subscriber who has generated the highest level sample. Moreover, the automatic elimination of the voice signals having a lower level than the highest one is achieved, thus preventing the users from receiving signals that are non-intelligible due to superimposition of more signals of low level.

Lastly, the expansion or linearization operations are eliminated, since the signal to be sent to the subscribers is obtained by the comparison of the compressed signals to one another.

According to the present invention there is provided a conference circuit for switching telephone exchanges of numerical type comprising at least a switching module formed by a matrix arranged to effect switching of the signal samples allocated to a prefixed number of PCM bundles, on the basis of information supplied by a control unit, characterised in that the said conference circuit comprises in combination the following characteristic elements:

- first means adapted to store the signal samples relative to n users taking part in the conference, during a prefixed time slot of the frame according to which the said PCM bundles are arranged;
- second means adapted to sequentially receive the signal samples stored in the first means and to search for the highest level signal sample;
- third means adapted to send a null signal to the user who has generated the highest level signal sample as well as to send the highest level signal sample to the remaining users taking part in the conference;
- fourth means adapted to supply enabling signals to the first, second and third means by way of a digital word increasing at a rate that is half the digit rate of the PCM bundles; and
- fifth means adapted to store a control word generated by the said control unit of the switching module and designated to enable the first means.

An embodiment of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1 shows a block diagram of a conference circuit; and

Figure 2 shows waveforms associated with the circuit of *Fig. 1*.

The conference circuit illustrated in *Fig. 1* is adapted to simultaneously receive in parallel the signal samples relative to the users taking part in the conference.

It is acknowledged that the signal samples may be allocated in any time slot of anyone of the PCM bundles connected to the switching matrix, this results in that they reach the

switching matrix in different time intervals and consequently, before being sent to the conference circuit, they must be handled in order to perform the aforesaid linearization.

According to the numerical telephone exchange disclosed in the Italian patent application 19414 A/81 of 30.1.1981 the linearization is achieved by performing a translation operation of the signal samples in the time slot 16 of a prefixed number of PCM bundles.

The switching matrix disclosed in the said patent application is in fact adapted to switch 256 input channels relative to eight 2Mbit/s PCM bundles on the same number of output channels and further provides a prefixed number (e.g. four) of auxiliary inputs-outputs, AXRX and AXTX respectively, towards the conference circuit. It is acknowledged that the time slot 16 of each PCM bundle is arranged to transmit the signalling information which is withdrawn when the bundle reaches the switching module, this results in that the time slot 16 of the 8 PCM bundles reaching the switching matrix result to be free and suitable to be used for performing the said translation operations.

In the assumption that the signal samples of the users taking part in the conference be allocated to the time slots 3, 8, 19 and 27 of the PCM bundles 2, 4, 6 and 7 respectively, the matrix switches:

—the sample allocated to the time slot of the PCM bundle 2 into the time slot 16 of the PCM bundle 0;

—the sample allocated to the time slot 8 of the PCM bundle 4 into the time slot 16 of the PCM bundle 1;

—the sample allocated to the time slot 19 of the PCM bundle 6 into the time slot 16 of the PCM bundle 2;

—the sample allocated in the time slot 27 of the PCM bundle 7 into the time slot 16 of the PCM bundle 3.

It successively determines the switching of the contents of the time slot 16 of bundles 0, ..., 3 on the said auxiliary outputs AXTX 0 ..., AXTX₃ that therefore receive at the same time, the four signal samples of the users taking part in the conference.

Fig. 1 shown that the said outputs AXTX₀ ..., AXTX₃ are connected to respective shift registers SR₀ ..., SR₃ forming part of the memory means MM.

The load of the digital words into registers SR is performed at a rate determined by a sequence of clock pulses DCLK whose frequency is equal to the digit frequency of the PCM bundles.

The impulses DCLK are available at the output of a gate P₁ forming part of the enabling means MA. Unit P₁ is enabled by the

signal available at output P of a timing unit TG operating during the time slot 16, as illustrated in diagram P of Fig. 2.

During time slot 16 the four signal samples are therefore each loaded into a respective shift register SR.

The inputs of the enabling means MA receive the clock signals PTAD₀ ..., BTAD₇ illustrated in detail in diagrams A ..., H of Fig. 2, which supply the number of the bit 0 ..., 256 presently available in the PCM bundles (in a frame of a 2Mbit/s PCM bundle there are allocated 32 time slots and in each slot there are allocated 8 bits, i.e. 256 bits in a frame). The output of memory means MM is connected to the comparison means MC which are designed to sequentially receive the four signal samples in order to search for the one presenting the highest level.

The comparison means MC comprise a register RG₁ which is set to zero at the beginning of the frame by an impulse CLCN illustrated in diagram Q.

The enabling means MA further comprise a decoding unit DC whose input receives signals BTAD_{5,6,7} and which, during the first half of each frame time interval, sequentially activates each of its four outputs for a time interval equal to the duration of the four time slots, as illustrated in diagrams, I, L, M and N.

The outputs of unit DC are designed to sequentially activate the outputs of the shift registers SR₀ ..., SR₃ so as to output their contents thereby causing the emission of the first signal sample by unit SR₀ during the time interval defined by the impulse illustrated in diagram I.

The said sample is applied to the input of register RG₁ and to the first input of a comparator CM adapted to energize its own output when the signal sample available at the input of register RG₁ is higher than the sample stored in the same register.

Taking into account that unit RG₁ had been set to zero, the output of unit CM is energized, the said unit activates a gate circuit P₂ whose second input receives a sequence of pulses, generated by unit TG and illustrated in diagram O. The impulse available at the output of gate P₂ causes register RG₁ to store the signal sample available at its input and previously stored in SR₀.

As impulse L becomes available at the second output of unit DC the contents of register SR₁ is read out, so that the second sample is applied to the input of unit CM and compared to the first sample.

Assuming that the level of the second sample is lower than that of the first sample, the impulse of sequence O cannot pass through P₂ because the output of unit CM is not activated, so that the first sample remains stored in register RG₁.

Upon activation of the third output of unit

DC, register SR_2 is enabled so as to be read out and the third sample is compared to the first one. Assuming that the third sample exceeds the first sample, the output of unit CM is activated, thus causing the passage of an impulse of sequence 0 through unit P_2 , so that register RG_1 stores the third sample. Assuming that the fourth sample is lower than the third one, the latter remains stored in register RG_1 at the end of the time slot 15, since this third sample is the highest level signal sample and is therefore destined to be forwarded to all the users taking part in the conference, except the one who has generated it.

The said operation is performed by sending units MI which comprise a number of bistable circuits CFF of D type whose data inputs receive a respective output of unit DC and whose clock input receives the impulses available at the output of a gate circuit P_2 .

Unit CFF is designed to store the highest signal sample among the four that have been applied to the input of register RG_1 , thus generating an output binary configuration at the end of the comparisons, the said binary configuration only presenting a zero at the bistable circuit associated with the highest level sample.

In view of the above described example, in which the highest level signal is assumed to be the third, the binary configuration available at the output CFF is 1101.

The said binary configuration is applied to the enabling input of each of a corresponding number of gates $P_3 \dots P_6$ whose second inputs receive the output of multiplexer MX. The data input of the multiplexer MX receives the sample stored in unit RG_1 whereas the address input receives impulses $BTAD_0 \dots BTAD_2$ which determine the scanning of the cells of unit RG_1 thus causing the serialization of their contents.

As the user having generated the highest level signal sample is destined to receive a null signal, while the remaining three users are destined to receive the highest level signal sample, unit CFF disables unit P_5 and enables units P_3 , P_4 and P_6 which send the signal available at the output of MX to the respective users via a register RG_2 . The input of register RG_2 receives clock pulses DCLK as well as the enabling signal illustrated in diagram P that is to be active during time slot 16.

The signals available at the output of unit RG_2 are sent to the auxiliary inputs AXRX of the switching matrix that provides for switching them in the time slots of the PCM bundles associated with the users taking part in the conference. The conference circuit further comprises control means CM by way of which the device checking the switching operations is designed for example to disable one of the shift registers when there are now at least four speakers taking part in the conference.

In fact, the said control means forwards a control word to a data bus ZDBS and generates signal DVSL and ZZWR thus activating the output of gate P_7 that determines the writing of said word into a register RG_3 . If there are three users taking part in the conference, such a word disables register SR_3 whose output will provide a sequence of zeros that cannot modify the results of the comparisons previously effected by unit CM.

CLAIMS

1. A conference circuit for switching telephone exchanges of numerical type comprising at least a switching module formed by a matrix arranged to effect switching of the signal samples allocated to a prefixed number of PCM bundles, on the basis of information supplied by a control unit, characterised in that the said conference circuit comprises in combination the following characteristic elements:

—first means adapted to store the signal samples relative to n users taking part in the conference, during a prefixed time slot of the frame according to which the said PCM bundles are arranged;

—second means adapted to sequentially receive the signal samples stored in the first means and to search for the highest level signal sample;

—third means adapted to send a null signal to the user who has generated the highest level signal sample as well as to send the highest level signal sample to the remaining users taking part in the conference;

—fourth means adapted to supply enabling signals to the first, second and third means by way of a digital word increasing at a rate that is half the digit rate of the PCM bundles; and

—fifth means adapted to store a control word generated by the said control unit of the switching module and designed to enable the first means.

2. A conference circuit as claimed in claim 1, characterised in that the said first means and the said third means are adapted to respectively receive and emit the signal samples relative to the users taking part in the conference during the time slot assigned to the signalling of the PCM bundles connected to the switching matrix and characterised in that the said switching matrix is adapted to perform a translation of the signal samples from the time slot allocated to the user into the time slot assigned to the signalling of a respective PCM bundle and viceversa.

3. A conference circuit as claimed in claims 1 and 2, characterised in that the said fourth means comprise in combination the following characteristic elements;

—a decoding unit with n outputs each of which is sequentially active during the first half of the frame of the PCM bundles;

—a first timing unit adapted to generate a

first signal providing an impulse at any activation of the outputs of the said decoding unit, as well as a second signal active during the time slot relative to the signalling of the PCM bundles;

—a first logic product unit whose first input is applied to a third signal whose frequency is equal to the digit frequency of the PCM bundles.

4. A conference circuit as claimed in claim 1, characterised in that the said first means comprise n shift registers adapted to store the signal samples when impulses become available at the output of the first logic product unit, further adapted to send in parallel their own contents when a respective output of the said decoding unit is active and further adapted to emit a sequence of zeros in response to prefixed state of a respective output of the said fifth means.

5. A conference circuit as claimed in claim 1, characterised in that the second means comprise:

—a first register whose reset input receives a fourth signal active at the beginning of each frame of PCM bundles, adapted to store the signal sample available at its input when it receives a loading control;

—a comparator whose output is arranged to emit an impulse when the level of the sample available at the input of the first register exceeds the level of the sample available at the output of the same register;

—a second gate whose first input is connected to the output of comparator, whose second input receives the said first signal generated by the timing unit and whose output is applied to the said loading control for the first register.

6. A conference circuit as claimed in claim 1, characterised in that the said third means comprise the combination of the following characteristic elements:

— n bistable circuits of the D type whose data input is connected to a respective output of the said decoding unit and whose clock inputs are connected to the output of the second logic product unit;

—a multiplexer adapted to serialize the binary configuration stored in the first register;

— n gate circuits an input of which is connected to the output of the multiplexer, while the other input is connected to a respective output of the bistable circuits;

—a second register having n memory cells, whose n outputs are adapted to emit the bits available at the output of a respective gate among the said gates at the rate defined by the said third signal when the second signal is active.

7. A conference circuit as claimed in claim 1, characterised in that the said fifth means comprise a third register having n memory cells, adapted to write the binary configuration available at its input when it activates the

output of a third gate whose input is applied to signals generated by the said control unit of the switching module.

8. A conference circuit substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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