



(51) International Patent Classification:

G01R 33/07 (2006.01) G01R 33/28 (2006.01)
G01R 15/20 (2006.01) H04R 3/04 (2006.01)

(21) International Application Number:

PCT/US2024/037921

(22) International Filing Date:

12 July 2024 (12.07.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/526,920 14 July 2023 (14.07.2023) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,

(54) Title: MAGNETIC FIELD SENSING AT DC AND HIGH FREQUENCIES SIMULTANEOUSLY

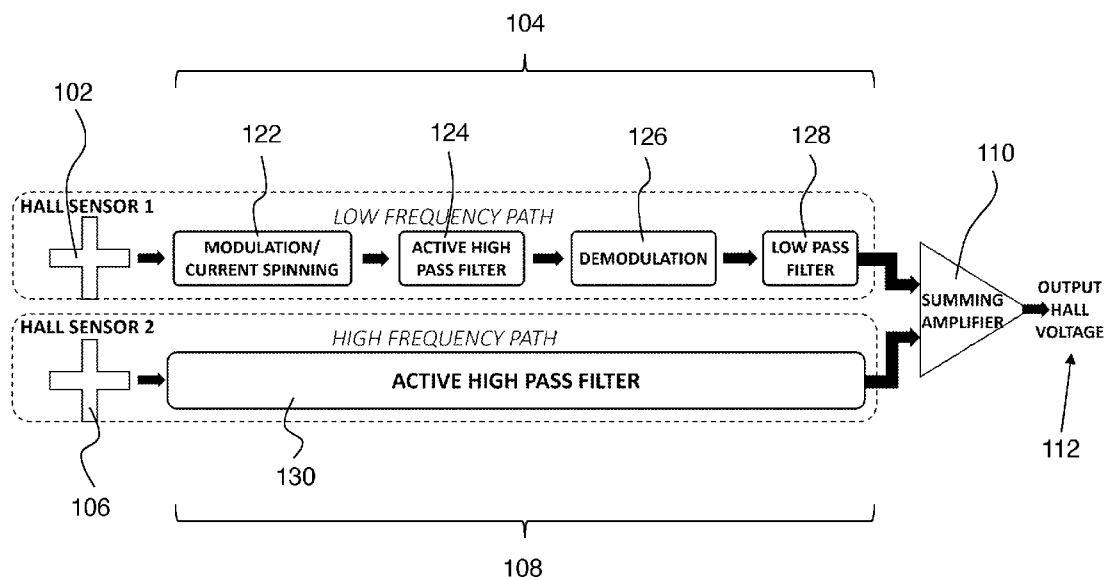


FIG. 1

(57) Abstract: A broadband readout interface for Hall-effect sensors is presented. This current sensing system includes two high-bandwidth Hall sensors and a fast readout interface having two signal paths, one being a high frequency path and the other being a DC/low frequency path. In one example, the readout interface (ROT) utilizes a 2-way current spinning technique in the DC/low frequency signal path to minimize offset at DC while using high pass filtering in the high frequency signal path to eliminate any offset at the high frequencies. The DC/low frequency signal path measures the Hall voltage from its Hall sensor, while the high frequency signal path can measure the inductive voltage (or an AC Hall voltage) from its Hall sensor.

MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

Magnetic field sensing at DC and high frequencies
simultaneously

FIELD OF THE INVENTION

5 This invention relates to magnetic field sensing.

BACKGROUND

Hall effect sensors are commonly used to measure magnetic fields. The sensor offset (i.e., the non-zero
10 Hall voltage at zero magnetic field) is a major sensor non-ideality whose mitigation typically dominates practical designs for Hall sensor readout circuits. Many approaches for offset mitigation have been considered in the literature, and most of these approaches undesirably limit
15 the system bandwidth to a value far less than the bandwidth of the Hall sensor itself. Accordingly, it would be an advance in the art to provide an improved broadband Hall-effect sensor readout architecture.

20 SUMMARY

A broadband readout interface design for Hall-effect sensors is presented. This current sensing system includes two high-bandwidth Hall sensors and a fast readout interface having two signal paths, one being a high
25 frequency path and the other being a DC/low frequency path. In one example, the readout interface (ROI) utilizes a 2-way current spinning technique in the DC/low frequency signal path to minimize offset at DC while using high pass filtering in the high frequency signal path to eliminate
30 any offset at the high frequencies. The DC/low frequency

signal path measures the Hall voltage from its Hall sensor, while the high frequency signal path can measure the inductive voltage from its Hall sensor.

The usage of two sensors and signal paths makes it possible to take advantage of the full bandwidth of the sensors. This system can detect fast changes in the magnetic field, resulting in a non-invasive fast current detection solution. In the detailed example considered below, the die area of the readout interface is approximately 2850 μm by 200 μm . When testing with a current trace at a distance of 1.5 mm from the sensor and using a ferrite-core magnetic field concentrator, the current sensitivity is observed to be 12.7 mV/A.

Significant advantages are provided. Previous work on improved Hall effect sensors did not provide the capability of simultaneously measuring low frequency (including DC) and high frequency magnetic fields. This work provides that new capability.

Although the example of Section B below shows operation from DC to 25 MHz, it is expected that the upper frequency range for this approach could be as high as 100-200 MHz.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the architecture of a readout interface circuit in accordance with an embodiment of the invention.

FIG. 2 shows an exemplary schematic of a designed readout interface.

FIG. 3 shows exemplary 2-way current spinning switches.

FIG. 4 shows an exemplary fully differential operational transconductance amplifier

FIG. 5 shows an exemplary single-ended operational transconductance amplifier

5 FIG. 6. shows the transfer function of the readout interface of section B.

FIG. 7 shows transient simulation results of the readout interface of section B.

10 FIG. 8 shows output waveforms of the readout interface of section B in standalone testing.

FIG. 9 shows a zoomed-in view of the output waveforms of FIG. 8 to show pulse edges.

FIG. 10 shows measurement waveforms from the Hall-effect sensor and the ROI of section B.

15 FIG. 11 shows measurement from the sensing system of section B to observe response times.

DETAILED DESCRIPTION

A) General principles

20 FIG. 1 is a block diagram of an exemplary embodiment of the invention. Here we have a first Hall-effect sensor element 102, a second Hall-effect sensor element 106, a first signal conditioning network 104 configured to receive a first sensor signal from the first Hall-effect sensor
25 element and provide a first signal having a high frequency cutoff frequency f_1 , a second signal conditioning network 108 configured to receive a second sensor signal from the second Hall-effect sensor element and provide a second signal having a low frequency cutoff frequency f_2 , a summing
30 amplifier 110 configured to receive the first signal and

the second signal and configured to provide a sum output 112 that is the first signal times a first gain plus the second signal times a second gain. Here the first gain and the second gain are selected such that a frequency response
5 of the sum output is substantially flat between zero frequency and a cutoff frequency f_s of the second Hall-effect sensor, as further described below in connection with FIG. 6.

Preferably, the frequency response of the sum output
10 is as flat as possible over the designed frequency range. More quantitatively, it is preferred that the frequency response of the sum output varies by no more than 10% over a frequency range between 0 and $0.9 f_s$. It is preferred for f_1 and f_2 as defined above to have equal values. More
15 quantitatively, it is preferred that $|f_1 - f_2| < 0.1 f_1$.

In some embodiments, the first signal conditioning network can include one or more optional features, such as a current spinning circuit 122 to mitigate a DC offset signal and/or a chopper stabilization circuit (combination
20 of high pass filter 124, demodulator 126 and low pass filter 128 on FIG. 1).

The second signal conditioning network 108 can include a high pass filter 130.

The first and second Hall-effect sensors preferably
25 have the same device configuration (i.e., the same device geometry in the same material system).

The first sensor signal is preferably a Hall-effect signal.

The second sensor signal can be an inductive signal.
30 Alternatively, the second sensor signal can be a frequency shifted Hall-effect signal. In this case, the frequency shifted Hall-effect signal can have a frequency shift

determined by a frequency of an applied current to the second Hall-effect sensor (i.e., an AC Hall-effect measurement). In cases where the second signal is a frequency shifted Hall-effect signal, the second signal conditioning network 108 can include a compensating frequency shift so that there is no net frequency shift between the second Hall sensor 106 and the summing amplifier 110.

10 B) Detailed example

B1) Introduction

Hall-effect sensors are magnetic field sensors. Corresponding to their biasing, they generate a voltage proportional to the magnetic field's strength. Their applications range from the automotive industry to primary consumers. Hall-effect sensors are the most prevalent magnet sensors with ~70% market share in 2017.

One of the most common uses of these sensors is current sensing. When current flows through a conductor, it creates a magnetic field around it. The Hall-effect sensor has a current flowing inside it when biased. When the sensor is placed close to the current line, the external magnetic field coincides with the Hall-effect sensor's internal current and Lorentz force generates a potential across the opposite terminals of the sensor. This is called the Hall-effect signal (or Hall-effect voltage).

The Hall-effect sensors have an inherent offset, which is the sensor's output when no external magnetic field is present. This output should be ideally zero, but practically the output voltage present in zero magnetic field when the sensor is biased, is called Hall-effect offset. Various studies have been conducted on multiple

shapes and sizes of these devices to mitigate this offset. However, the offset may be low for some devices and high for others, but it always exists. Hence it needs to be compensated in the readout interface (ROI).

5 The type of Hall-effect sensor ROI initially depends upon the output, whether it is current or voltage. It is categorized as either current-mode or voltage-mode. Another categorization is based on whether the output is digital, detecting certain current levels, requiring high
10 sensitivity and accuracy, while in many applications, the analog output is preferred. For each of these categories, no matter what final output is desired from the Hall-effect sensor, the most critical design step in the ROI is to nullify the Hall-effect offset. For this purpose,
15 initially, the Hall-effect offset voltage needs to be separated from the Hall-effect signal. A commonly used commercial technique for this purpose is the current spinning technique. This becomes the first stage of the ROI.

20 Following the current spinning stage, various dynamic offset cancellation techniques can be employed, including chopper stabilization, auto-zeroing, track-and-hold, and other techniques. Using these cancellation techniques, a variety of ROI designs can be seen in the literature. One
25 such ROI uses sample and hold circuitry for demodulation, which provides a highly sensitive signal but more complex circuitry than a chopper. Another design uses analog-to-digital converters (ADCs) with feedback loops to obtain low offset errors, forming a complex signal conditioning
30 system. One ROI uses an ADC, which takes input directly from current spinning, and requires internal offset compensation for the operational amplifiers and a very high-resolution ADC. Another simulated design offers a

solution for reducing residual offset, where four phases are used with correlated double sampling for further subtraction of offset. Of all these ROIs, the most effective is the chopper stabilization (CHS) in combination with current spinning. This can provide high sensitivity with sufficiently low flicker noise while effectively reducing inherent offsets of the operational amplifiers as well. However, the chopping adds switching noise in the signal, and one technique to reduce that is to eliminate demodulation choppers. This improves the signal-to-noise ratio (SNR) but provides a modulated AC Hall-effect signal as the output.

Dynamic offset cancellation schemes in ROIs limit the system's bandwidth, so other approaches have been used at higher frequencies. One high-frequency technique is a current spinning method followed by three ripple reduction loops instead of a low pass filter. This allows full system bandwidth, although it requires a complicated multiplex signal conditioning system, including data converters.

Another method that provides high bandwidth is by combining chopper stabilization with track and hold comparators. It uses sampling techniques to eliminate offset rather than filters. Another work considers an X-Hall-effect sensor that is orthogonally shaped and uses a differential-difference current feedback amplifier. This sensor avoids using current spinning, allowing full practical bandwidth of the system. However, it can only be used for orthogonal-shaped sensors with eight terminals, which requires rearchitected sensor and the entire circuitry along with it. One technique recently developed allowed the separation of the Hall-effect signal from offset without using current spinning but could only work for AC magnetic fields and cannot detect the DC signal. Other high-bandwidth sensing

options then explore various other sensors, such as coils and magnetoresistance transducers, instead of Hall-effect sensors.

Most of the ROIs mentioned above utilize current spinning to differentiate between the Hall-effect offset and the Hall-effect signal. Following that step, some techniques focus on improving sensitivity or linearity, while others focus on decreasing the residual offset. There is limited work for bandwidth improvement of ROIs for Hall-effect sensors. The ROI architecture of this work focuses on increasing the bandwidth performance of the circuit by using two signal paths. This ROI, when combined with any high-bandwidth Hall-effect sensors, results in a fast current detection system. This system can be designed using any wide-bandgap devices such as aluminum gallium nitride/gallium nitride (AlGaN/GaN) or aluminum gallium arsenide/gallium arsenide (AlGaAs/GaAs) Hall-effect devices.

Section B2 covers the architecture of the designed ROI, followed by the circuit schematic and its details in Section B3. The ROI simulation results are presented in Section B4. The measurement results of the designed and fabricated ROI application-specific integrated circuit (ASIC) and sensor testing are discussed in Section B5. This is followed by comparing the results with the state-of-the-art designs in Section B6.

B2) Readout interface architecture

Hall-effect sensors detect magnetic fields and generate a corresponding output voltage. Since a current-carrying conductor produces a magnetic field around it, these magnetic sensors can detect the current flowing

through that conductor. Conventional Hall-effect sensors provide high magnetic field sensitivity but limited bandwidth. The state-of-the-art AlGa_N/Ga_N Hall-effect sensors have a bandwidth of greater than 10 MHz. Such sensors can thus be used to detect fast magnetic field variations. Due to their miniature size, they can be used in integrated power applications to detect currents. Whenever there is an abrupt fluctuation in the current flowing through a conductor, these Hall-effect sensors can detect that rapid change and respond quickly because of their high bandwidth. Catastrophic failure in high-power devices caused by current fluctuations can thus be avoided. For such a scenario, the circuit reading the signal from the sensor must also have a high system bandwidth. Due to various design limitations, the commercially available readout interface (ROI) circuits do not provide high bandwidth. This gives rise to the need for an ROI circuit that can be used with such high-bandwidth Hall-effect sensors without limiting the system bandwidth.

FIG. 1 shows the block diagram of the architecture of the current sensing interface circuit designed in this work. The overall signal is divided into two signal paths. The low-frequency path makes use of the current spinning technique to separate the Hall-effect offset from the Hall-effect voltage. This is followed by a modified version of the chopper stabilization technique to process the modulated Hall-effect voltage and remove the Hall-effect offset. The second path of this design is the high-frequency path. This uses a high-pass filter to remove the Hall-effect offset and the low-frequency components of the Hall-effect voltage. Hence only the high-frequency components are processed and allowed to pass in this signal path. This way, both the signal paths are devoid of offset

and contain a certain frequency portion of the Hall-effect voltage. In the end, a summing amplifier is used to add these two signals to obtain the final Hall-effect voltage.

5 The division of the signal into two paths is done to be able to amplify the signal and efficiently remove the offset. Hall-effect offset is present in the signal generated by the Hall-effect devices, due to unavoidable structural mismatches. It varies from one device to another as well as with temperature. Hence signal conditioning
10 methods must be applied to the output generated by the sensor to remove this offset. Two methods are used to remove this offset. The current spinning technique is the method used in the low-frequency path. However, this technique limits the usable bandwidth and hence it cannot
15 be applied to high-frequency signals. Similarly, filtering is applied in the high-frequency path to remove the offset, but it also rejects the low-frequency components and hence cannot be used in the low-frequency path. This leads to the use of two signal paths with two different methods for
20 offset cancellation, to be able to process a wider frequency range.

The low-frequency path is a combination of two techniques, namely current spinning and chopper stabilization (CHS). CHS is a signal conditioning method
25 that works in the frequency domain. It first modulates the desired signal on a high-frequency carrier. Then during amplification, the operational amplifier offset gets added to the signal as well as any flicker noise. Although the offset is a low-frequency signal and does not interfere
30 with the desired modulated signal. The desired signal is then demodulated to its original form, whereas since the offset also passes through the demodulation switches, it gets modulated. Low-pass filtering then removes the

modulated offset as well as any noise. This way, CHS gets rid of the offset and flicker noise. Since CHS technique is implemented using fully-differential signal propagation, it facilitates the rejection of common-mode and environmental noise. The addition of current spinning to this technique is due to the Hall-effect sensor. The current spinning replaces the modulation block of CHS, as shown in FIG. 1. The current spinning partially works similarly to the modulation block, such that it modulates the desired Hall-effect voltage. Although in addition to that, it also separates the Hall-effect offset by leaving it unmodulated.

B3) Schematic of the readout interface

The circuit schematic of the ROI is shown in Fig. 2. The top branch is the low-frequency path, while the bottom branch is the high-frequency path. Hall-effect sensor#1 is connected to the top branch through the current spinning block, which is elaborated in FIG. 3.

There are two phases controlled by clock signals (CLK and $\overline{\text{CLK}}$). When CLK is high, during phase#1, terminals 1 and 3 of the Hall-effect sensor are connected to the bias current, while terminals 2 and 4 are connected to the output of this block. Next, when $\overline{\text{CLK}}$ is high, during phase#2, the connections of the terminals switch up such that the bias current is now provided to terminals 2 and 4, while the output is taken from terminals 1 and 3. Due to the switching from phase#1 to phase#2, the polarity of the measured Hall-effect voltage changes in the two phases. Since the offset is due to structural mismatches and is being measured between two terminals in both phases, it remains unaffected by the switching. As a result, a

modulated Hall-effect voltage is generated, whose frequency is the same as the clock frequency, and the Hall-effect offset remains a low-frequency discrete (DC) signal.

The rest of the circuit chain include operational
5 transconductance amplifiers (OTA) in fully differential (FIG. 4) or single-ended (FIG. 5) configurations. The first stage for both these OTA is designed using the folded-cascode configuration. This type of OTA uses cascode devices for high gain and high bandwidth. Compared to other
10 cascode configurations, folded-cascode provides a large swing without compromising on gain or bandwidth. This results in high output common-mode range (OCMR). The folded-cascode configuration also provides a high power supply rejection ratio (PSSR).

15 When designing a fully differential OTA (FIG. 4), it requires a common-mode feedback stage to support each gain stage, since it has differential outputs. The purpose of the common-mode feedback circuit is to establish an appropriate current in each branch while maintaining the
20 correct output common-mode voltage of both output nodes. This stage deduces the output common-mode voltage by averaging the two output nodes and then compares it with the reference common-mode voltage (VCM). As a result, it generates the required control voltage for the PMOS current
25 source of the folded-cascode stage. Thus, by controlling that bias current it keeps the output common-mode voltage close to VCM through this feedback loop.

The next stage of the fully differential OTA (FIG. 4) is the differential amplifier. This stage further increases
30 the gain of the OTA. Since this stage also needs to have differential outputs, a similar common-mode feedback stage is required for this gain stage as well.

The single-ended OTA (FIG. 5) also uses the folded-cascode as the first stage and a differential amplifier as the second stage. Since in this OTA, the output is single-ended, there is no need for a common-mode stage for the second stage. However, as can be seen in (FIG. 5), the first stage is designed to be fully differential. This helps in keeping the output common-mode voltage more accurate since the common-mode feedback circuit maintains it.

The Indirect Miller compensation scheme is used in both the amplifiers. Miller compensation uses a capacitor between the output and the input of the second stage, bypassing this stage for high frequencies. This causes pole splitting due to multiplication of capacitance and adds a dominant pole in the amplifier. For Indirect Miller compensation scheme, a series resistor is added with the capacitor to add a zero, which increases the bandwidth of the amplifiers, as compared to using only Miller scheme. The stability of the amplifiers is ensured by designing them with a phase margin of greater than 50 degrees.

From the schematic in FIG. 4, it can be seen that the input stage and the active high pass filter of both signal paths are fully differential. Hence these stages use the fully differential OTA. Any other stage that has an amplifier uses the single-ended OTA.

Considering the low-frequency path, the first block is the current spinning where the Hall-effect voltage gets modulated to the switching frequency (the frequency of the CLK signal), while the offset remains DC. This signal is then picked up by the fully differential input stage, which serves as a pre-amplifier stage, with high input resistance. Since the desired Hall-effect voltage is modulated to a high frequency, the next stage is an active

high pass filter which then rejects the DC Hall-effect offset and amplifies the Hall-effect voltage. Since amplifiers are used in this chain, a DC offset of the OTA gets added to the signal. After filtering, the Hall-effect voltage is demodulated using the same switching frequency (CLK) back to its original form. However, the amplifier offset gets modulated when passed through the demodulation switches. Then the signal is passed through a low pass filter to reject the modulated offset as well as the high-frequency switching noise. A passive low-pass filter is used. The final signal at this stage is only the amplified Hall-effect voltage in its original unmodulated form. However, this is a fully differential signal, so it is passed through an instrumentation amplifier to convert it into a single-ended output. The offset of the amplifiers of this stage does not have any significant effect on the signal since the Hall-effect voltage is already amplified. Additionally, common-centroid techniques are implemented to minimize it.

The high-frequency signal path is simpler than the low-frequency path since no current spinning is required here. The reason is that no DC voltage needs to be processed in this signal path, and current spinning is needed to separate the DC Hall-effect voltage from the DC Hall-effect offset. The input stage is a fully differential amplifier with very high input resistance so that it doesn't load the sensor. This is the pre-amplifier stage for this signal path providing a low gain but high input resistance and bandwidth. Then the active high-pass filter provides gain and filters the offset. The use of a fully differential amplifier helps reduce noise. At this point, the output is the high-frequency components of the amplified Hall-effect voltage without any offset. Since it

is a fully differential signal, an instrumentation amplifier converts it to single-ended output. The last stage in this path is the gain stage. Since this is a high-bandwidth signal path, the gain of the amplifiers is lower as compared to the low-frequency signal path. Hence a gain stage is used to amplify the high-frequency signal further.

The final stage of the system is a summing amplifier. This stage takes input from both signal paths and adds them with appropriate gain. An inverting weighted summing amplifier configuration is used. In this configuration, a different gain can be set for the two inputs by adjusting the input resistor values. Another feature added to this stage is gain variability for the high-frequency signal using three gain bits as shown in FIG. 2. The low-frequency signal path gain is fixed, while the high-frequency gain can be slightly adjusted to match it. This feature is added to cater to any mismatches between the two signal amplitudes.

To determine the transfer function for the system shown in FIG. 2, assume the low-frequency path as path#1 and the high-frequency path as path#2. The DC gain of each block is mentioned in FIG. 2. Let $V_i(s)$ and V_{os} represent the input signal and offset, respectively. The modulation block shifts the center frequency of the signal to a higher frequency called the carrier or switching frequency (ω_s). This block only modulates the input signal, while offset remains a DC signal, given by:

$$V_i(s + j\omega_s) + V_{os}$$

After it passes through the input stage (whose gain is represented by A_{I1}) and an active high pass filter, it becomes:

$$-A_{I1} \frac{R_2}{R_1} \left[\frac{sR_1C_1}{1+sR_1C_1} \right] [V_i(s+jw_s) + V_{Os}]$$

Since the input frequency is modulated at a higher frequency, the pole and zero of the high pass filter do not affect this signal ($w_s \gg \frac{1}{R_1C_1}$). The zero exists at the zero
 5 frequency and it eliminates V_{Os} which is the DC signal. The output after high pass filtering is given by:

$$-\frac{R_2}{R_1} V_i(s+jw_s) * A_{I1}$$

The demodulator shifts the input signal frequency back to its origin and the output is given by:

$$10 \quad -\frac{R_2}{R_1} V_i(s) * A_{I1}$$

Hence the transfer function before the low pass filter is given by:

$$-A_{F1} * A_{I1}$$

$$\text{where } A_{F1} = \frac{R_2}{R_1}$$

15 The complete transfer function for path#1 is given by:

$$TF_1 = -A_{F1} * A_{I1} \frac{1}{1+sRC} * A_{IA1}$$

Similarly, the transfer function for path#2 is given by:

$$TF_2 = A_{I2} * \left[-\frac{R_F}{R} \right] \frac{1}{1+\frac{1}{sRC}} * A_{IA2} * A_{G2}$$

The final transfer function of the summed output is:

$$20 \quad TF = -[A_{S1}(TF_1) + A_{S2}(TF_2)] * \frac{1}{1+\frac{s}{p_d}}$$

The 3-dB bandwidth is represented by the dominant pole of the summing amplifier, given by:

$$p_d = \frac{g_{m1}}{A_L C_c}$$

During this transfer function analysis, only the most dominant pole is shown for simplicity. The rest of the amplifiers have poles equal to or greater than this pole.

5 Solving for the final transfer function:

$$A_x = -[A_{S1} * A_{IA1} * A_{F1} * A_{I1} \left(\frac{1}{1 + sRC} \right) - A_{S2} * A_{G2} * A_{IA2} * A_{F2} * A_{I2} \left(\frac{sRC}{1 + sRC} \right)]$$

$$\text{where } A_{F2} = \frac{R_F}{R}$$

The total gain of both the paths is kept equal:

$$A_{S1} * A_{IA1} * A_{F1} * A_{I1} = A_{S2} * A_{G2} * A_{IA2} * A_{F2} * A_{I2} = A_v$$

$$10 \quad A_x = -A_v \left[\frac{1}{1 + sRC} + \frac{sRC}{1 + sRC} \right]$$

$$A_x = -A_v \left[\frac{1+sRC}{1+sRC} \right] = -A_v$$

The poles of the low and high-frequency paths cancel out, reducing the final transfer function to:

$$TF = \frac{A_v}{1 + \frac{s}{p_d}}$$

15 From the transfer function analysis, it can be determined that the bandwidth of the readout interface circuit is dependent on the operational amplifiers and is not limited by the filters. By keeping the RC (resistor and capacitor) value and in turn, the filters' cut-off frequency of both
20 the paths same, the effect of the poles and zeros of the filters cancel out in the final output. Then also matching the gain of both the paths results in a smooth crossover. The simplified transfer function equation of the final output shows that the gain remains constant throughout the
25 frequency range, having a smooth crossover, and the bandwidth is only limited by the dominant pole of the

operational amplifiers. The transfer function is graphically depicted in FIG. 6.

B4) Simulation results

5 The readout interface is implemented on 180 nm XFAB XH018 (modular mixed-signal sensor CMOS) technology. The circuit was designed using 3.3 V ultra-low noise transistors supporting an extended temperature range of -40 to 175 °C.

10 The fully differential OTA is designed with 83.51 dB DC gain and exhibits a 329.4 MHz unity gain bandwidth (for a load of 100 fF). It has a current consumption of 527.6 μ A. While the single-ended OTA has 80.82 dB DC gain and shows a unity gain bandwidth of 150.2 MHz (for a load of
15 100 fF), and 430.1 μ A current consumption. Both the OTAs have an input and output common-mode voltage of 1.65 V, and a phase margin of greater than 50 degrees.

 Using a supply voltage of 3.3 V, the common-mode voltage was kept at mid-rail (1.65 V). The circuit was
20 designed and simulated after parasitic extraction (PEX). The switching frequency is designed to be 250 kHz. For the simulation, input pulses of 10 kHz and 2 mV were provided to both signal paths. An external DC offset of 100 mV was also added to the input for the purpose of testing. With no
25 input, the output of the circuit is at the reference output common-mode voltage of 1.65 V. The transient simulation result for this test is shown in FIG. 7. The 3-dB frequency of the low-frequency path is determined by the low-pass filter in that chain, while the active high-pass filter
30 determines the 3-dB frequency in the high-frequency signal path. During design, both these frequencies were kept the same to achieve a constant final output. This frequency is

called the crossover frequency which is observed to be 11.6 kHz. The cross-over frequency is chosen to be approximately a decade less than the spinning frequency, so that the spinning frequency is efficiently rejected from the low-frequency path. Both filters are designed with the same resistor and capacitor values to match the frequencies and get a smooth crossover. To minimize the effect of filter components' tolerance on the cross-over frequency, the same resistor and capacitor type with similar values and filter order are used. The layout of the devices is also optimized to minimize the process variation. As shown in FIG. 7, the rise time of both signal paths is $\sim 30 \mu\text{s}$. The final output from the summing amplifier can be seen as a combination of both signals, giving a fast pulse response. Since an inverting configuration is used for the summing amplifier, it is inverse when compared to the signal from the two paths; however, it is in phase with the input.

Considering the gain, the high-frequency path has a gain of $\sim 126 \text{ V/V}$. While the low-frequency path has a gain of $\sim 280 \text{ V/V}$. Hence a gain of 2.2 V/V is provided through the weighted summing amplifier to the high-frequency signal, while the low-frequency signal is added with a gain of 1 V/V . This is where the 3-bit gain variability comes in. The high-frequency gain can be selected using 3-bits G_0 , G_1 , and G_2 , as shown in FIG. 2. These bits provide a respective gain of 2.85, 2.22, and 1.82 V/V . The default setting is G_1 . In case of a significant gain mismatch between the two signal paths, the bits G_0 or G_2 can be used depending upon whether it is required to decrease or increase the gain of the high-frequency path.

The AC analysis was performed on the ROI to plot the output gain by providing a fixed input voltage. Monte Carlo simulation was performed to test the circuit performance

across temperature and process corners. The achieved gain is ~49 dB. The standard deviation of the gain is 91.95 mdB. The resistors and the transistors all have an inherent temperature coefficient. The circuit design utilizes a PTAT (proportional to absolute temperature) and CTAT (complimentary to absolute temperature) combination of resistors in closed-loop amplifier configurations across the chain to maintain the gain constant. The consecutive positive and negative temperature coefficients cancel out each other's effect, keeping the gain variations minimum throughout the range. The readout interface is designed with multiple Hall-effect sensors in mind. Hence, the gain is initially kept constant over temperature, to demonstrate the frequency capability of the readout circuit as shown in FIG. 8. Since each sensor material will have different temperature dependent sensitivities, the PTAT and CTAT closed-loop resistors used for minimizing the change in gain over temperature would be modified to nullify the temperature effect of the particular sensor, once that dependence is measured or known.

B5) Measurement results

B5a) Readout interface testing

The ROI is tested by providing a square wave input of 1 kHz. A supply voltage of 3.3 V and VCM of 1.65 V is used. CLK and $\overline{\text{CLK}}$ are provided by a complimentary clock signal of 250 kHz. Three outputs are observed, the low-frequency signal (VLF), high-frequency signal (VHF), and final summed output (VOUT). The measured oscilloscope results are shown in FIG. 8. The results are normalized to the ground. The low-frequency path output is a square signal but with a slow rising edge, while the high-frequency path output

spikes at the edge, giving a much shorter rise time. The final output is then a fast-rising square wave. It is the amplified version of the input with a fast response. The noise in the signal is random noise from the environment since the amplifiers are high bandwidth, and there is no low-pass filtering in the high-frequency path to limit bandwidth.

To see the performance of both the paths and final output, one of the edges is zoomed in FIG. 9. Here, it can be seen that VHF rises quickly with a sharp pulse and then decays slowly. VLF, on the other hand, has a longer rise time. The fall-time of VHF and the rise-time of VLF were set the same by keeping the 3-dB frequencies of both filters equal to the crossover frequency. This rise-time of VLF and the fall-time for VHF are $\sim 30 \mu\text{s}$. The final summed output VOUT, in turn, shows the addition of the two signals, providing a fast response to the input pulse. The two signals, VLF and VHF, are inverted as compared to the input, which leads to the final output being in-phase with the input signal.

B5b) Readout interface testing with Hall-effect sensor

ROI testing verified the performance of the circuit. This ROI is designed with multiple Hall-effect sensors in mind, and hence it can be used for testing with any four terminal Hall-effect device. Preferably a high bandwidth sensor should be chosen to highlight the high bandwidth capability of this ROI. The sensors used for these tests were AlGaAs/GaAs Hall-effect sensors.

The Hall-effect sensors are wire-bonded on the PCB with the ROI. These are two sensors fabricated on the same die next to each other. They are connected to the ROI as

shown in FIG. 2 and FIG. 3. One sensor is connected to the current spinning of the low-frequency path, while the second sensor is connected to the high-frequency path. The second sensor does not need any current spinning since it is going to the high-frequency path, and this path does not process any DC signal (current spinning is only required for low-frequency DC signals). Hence its two alternating terminals (P1 and P3) are connected to the current bias, while the other two terminals (P2 and P4) are used for input to the ROI. A current trace is fabricated next to the sensors at a distance of 1.5 mm. A current pulse generator is used to drive the current trace on the PCB and provide high-current pulses for testing. A magnetic field concentrator is also used in this testing. It is a gapped ferrite core placed in such a way that the current trace passes from its middle, and the sensors sit inside the gap. It helps concentrate the magnetic field onto the sensors and improve sensitivity. The most common material used is ferrite, which has high permeability and low losses as needed for these magnetic field concentrators. Although the magnetic field concentrator is not a necessary part of the system and the system can be implemented without it, it helps increase sensitivity by focusing the field and reducing the noise captured by the sensor.

The Hall-effect sensors are biased with a current of 300 μ A. The testing conditions of the ROI are set up in the same manner as explained in the previous subsection. The current pulse generator produces short pulses of high current for the sensor to detect. This generates a step response of the combined setup of the sensor and the interface circuit. The normalized testing results are shown in FIG. 10. The current waveform peaks at ~17 A and then decays slightly for the pulse duration. The low-frequency

path signal slowly rises and then follows the current pulses. The high-frequency path signal gives a sharp peak during the rising edge of the current pulse, which speeds up the overall response of the system. As mentioned in the previous section, the high-frequency signal path is lower in amplitude and will be added with a higher gain using the weighted summing amplifier. From this figure, the sensitivity of the sensor can be calculated as $230\text{mV}/18\text{A} = 12.7\text{ mV/A}$.

The output signals of the sensing system in FIG. 10 include slight noise peaks at each current pulse edge. This is due to electromagnetic coupling between the sensing system and the current pulse generator. These noise peaks can be eliminated by using isolation in the sensor packaging. To calculate the residual offset, the sensor is connected to the ROI, but no magnetic field is generated by not providing any current pulses on the current trace. The change in the DC value of the low-frequency output of the ROI is noted. The input-referred residual offset is 1.525 mV. This offset is from the sensor due to using a 2-way current spinning technique. This can be minimized further by using a 4-way or 8-way spinning technique. For this work, the readout interface was tested with multiple sensor samples, and a 1.5 mV average offset was measured.

The normalized response of the sensor with the ROI to a single pulse is shown in FIG. 11. VLF and VHF are inverted with respect to the current pulse. The final summed output (VOUT) is the fast response to the current flowing through the current trace and is in phase with it. It is the combination of VLF, which follows the current pulse but with a longer rise time, and VHF, which has a sharp rising edge and hence makes the final output faster. From this figure, it can be seen that the low and high-

frequency paths, respectively, have a rise and fall time of ~30 μ s. Having similar response times is due to having the same filter frequencies in their design (as discussed previously). This ensures proper signal addition, resulting in VOUT. From FIG. 11, the rise time of the high-frequency signal can be noted as 40 ns. This rise time dictates the bandwidth of the current sensing system and how fast it can respond.

There are two methods for bandwidth calculation from rise time. One method utilized in filters is to use an approximation to calculate bandwidth, given as $0.35/\text{rise time}$. Another method is to invert the rise time of the step response to get the bandwidth. For accurate comparison with state-of-the-art, the second method is used. The calculated bandwidth for this work is 25 MHz.

B6) Comparison to state of the art

A comparison of the design with the state-of-the-art is shown in Table I. The relevant work using only Hall-effect sensors is included in the table. The focus of this work was to improve the bandwidth of the ROI and hence the overall current sensing system. As seen from the table, this work achieves the highest frequency compared to other Hall-effect sensor-based designs.

25

Table I: Comparison with state-of-the-art

	[15] 2012	[8] 2018	[12] 2015	[20] 2014	[21] 2019	This work
Process	0.35 μm	0.8 μm	0.8 μm	0.18 μm	0.35 μm	0.18 μm
Bandwidth	10 kHz	30 kHz	30 kHz	>100 kHz	1.7 MHz	25 MHz
Sensitivity	-	16 mV/mT	-	-	-	12.7 mV/A 95.25 mV/mT*
Temperature range	-40 to 150°C	-	-	-	-40 to 150°C	-40 to 175°C
Residual Offset	>3 μV >30 mT	5 mV 0.3 mT	0.2 mT	25 μT	85 μT	1.5 mV 15.75 μT **

* To convert from mV/A to mV/mT, the formula for magnetic

field created by current in a straight wire is used [$B = \frac{\mu_0 I}{2\pi R}$

5 where B = strength of magnetic field, μ_0 = permeability of free space, I = current flowing in the wire, and R = distance from the wire].

** To convert from T to mV, the reported sensitivity is used.

10

B7) Conclusions

The current sensing system of this work makes use of Hall-effect sensors and a readout interface ASIC. A high bandwidth ROI is designed for Hall-effect sensors, that

removes the offset and amplifies the signal without limiting bandwidth. AlGaAs/GaAs Hall-effect sensors are used for this testing; however, this ASIC can be used for any four terminal Hall-effect sensors. This system utilizes
5 only Hall-effect sensors which makes miniaturization much easier as compared to other devices. This is a non-invasive magnetic field detection system. It has a high bandwidth, providing a fast response to a current pulse, and hence can be used in power electronics applications, including
10 control and overshoot safety systems.

CLAIMS

1. An electrical circuit comprising:

a first Hall-effect sensor element;

a second Hall-effect sensor element;

5 a first signal conditioning network configured to receive a first sensor signal from the first Hall-effect sensor element and provide a first signal having a high frequency cutoff frequency f_1 ;

a second signal conditioning network configured to
10 receive a second sensor signal from the second Hall-effect sensor element and provide a second signal having a low frequency cutoff frequency f_2 ;

a summing amplifier configured to receive the first signal and the second signal and configured to provide a
15 sum output that is the first signal times a first gain plus the second signal times a second gain;

wherein the first gain and the second gain are selected such that a frequency response of the sum output is substantially flat between zero frequency and a cutoff
20 frequency f_s of the second Hall-effect sensor.

2. The electrical circuit of claim 1, wherein the frequency response of the sum output varies by no more than 10% over a frequency range between 0 and $0.9 f_s$.

25

3. The electrical circuit of claim 1, wherein
 $|f_1 - f_2| < 0.1 f_1$.

4. The electrical circuit of claim 1, wherein the first signal conditioning network includes a current spinning circuit to mitigate a DC offset signal.

5 5. The electrical circuit of claim 1, wherein the first signal conditioning network includes a chopper stabilization circuit to mitigate a DC offset signal.

6. The electrical circuit of claim 1, wherein the second
10 signal conditioning network includes a high pass filter.

7. The electrical circuit of claim 1, wherein the first and second Hall-effect sensors have the same device configuration.

15

8. The electrical circuit of claim 1, wherein the first sensor signal is a Hall-effect signal.

9. The electrical circuit of claim 1, wherein the second
20 sensor signal is an inductive signal.

10. The electrical circuit of claim 1, wherein the second sensor signal is a frequency shifted Hall-effect signal.

25 11. The electrical circuit of claim 10, wherein the frequency shifted Hall-effect signal has a frequency shift determined by a frequency of an applied current to the second Hall-effect sensor.

30

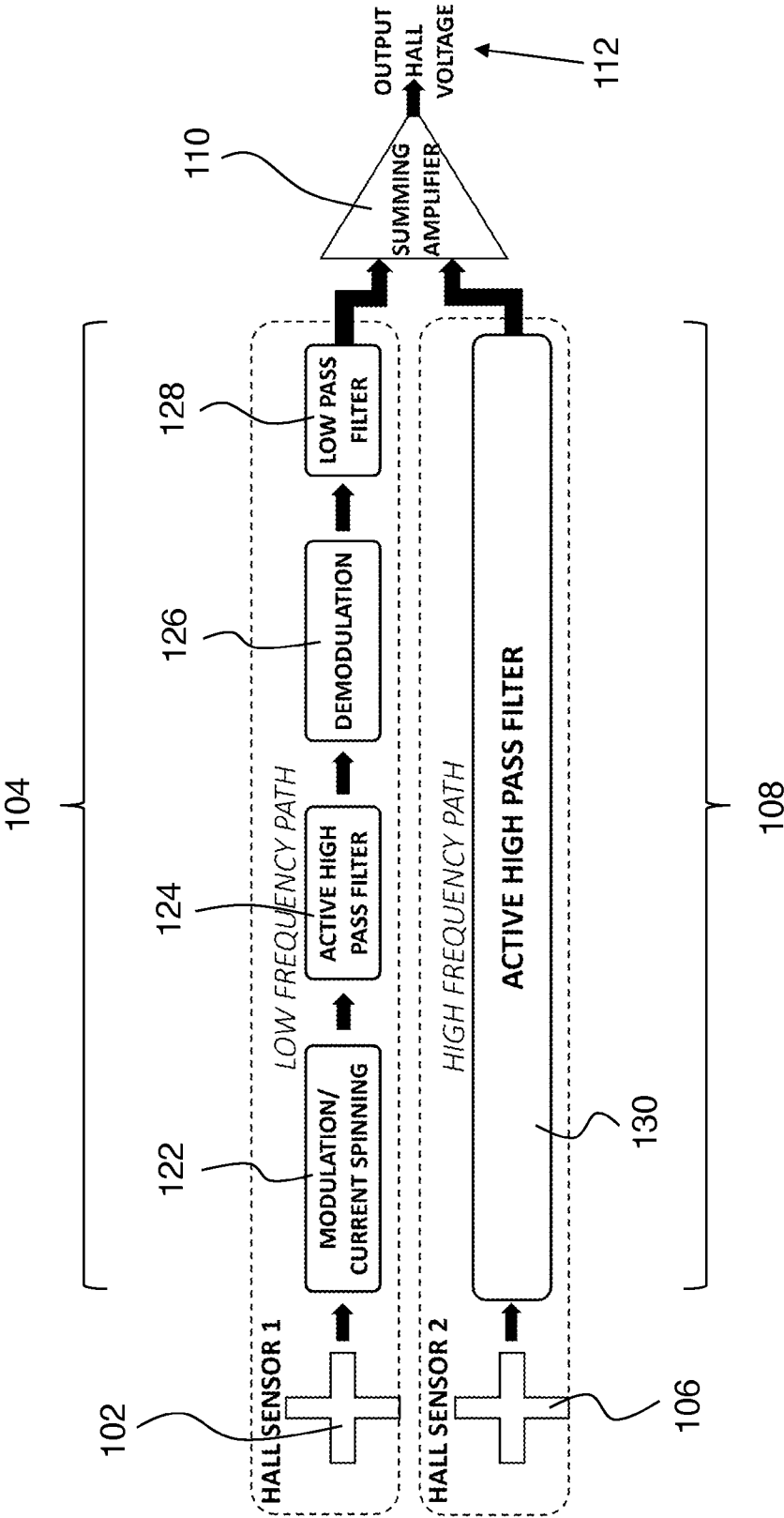


FIG. 1

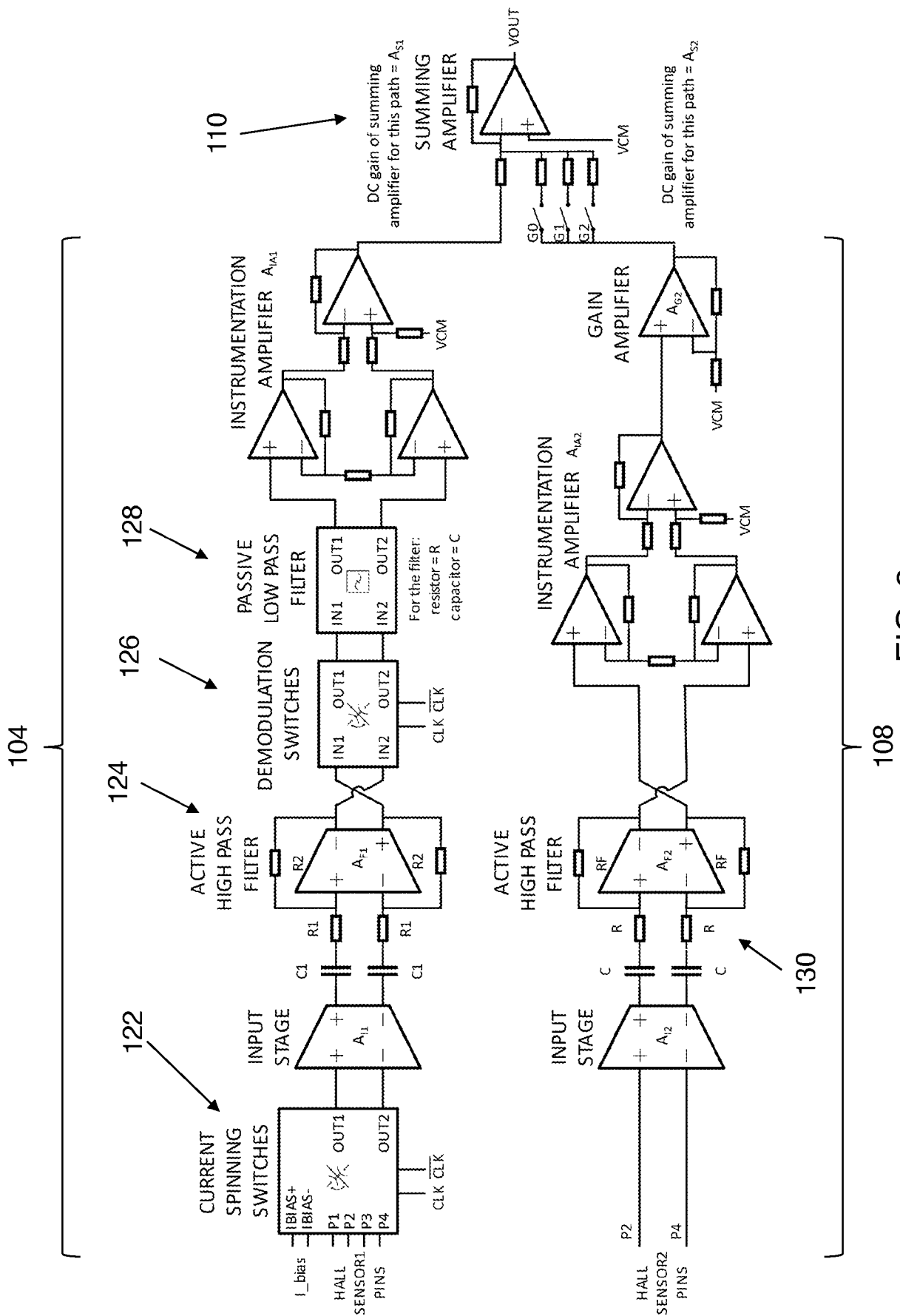


FIG. 2

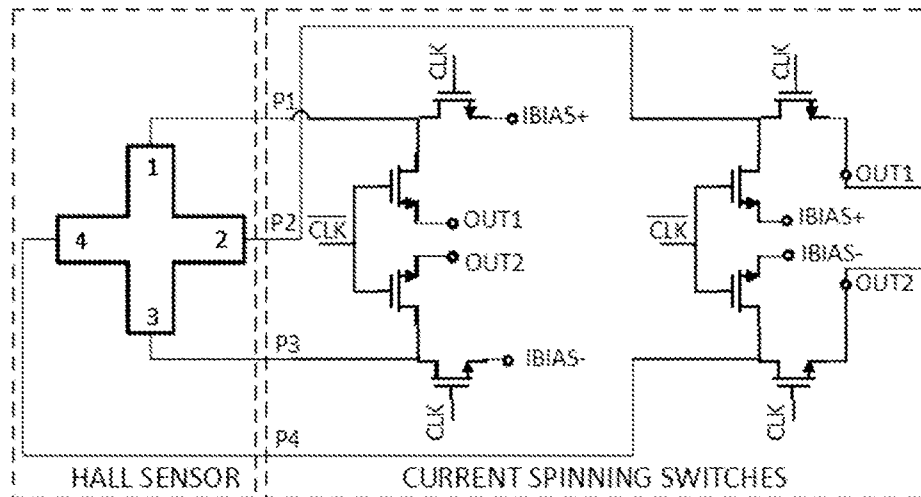


FIG. 3

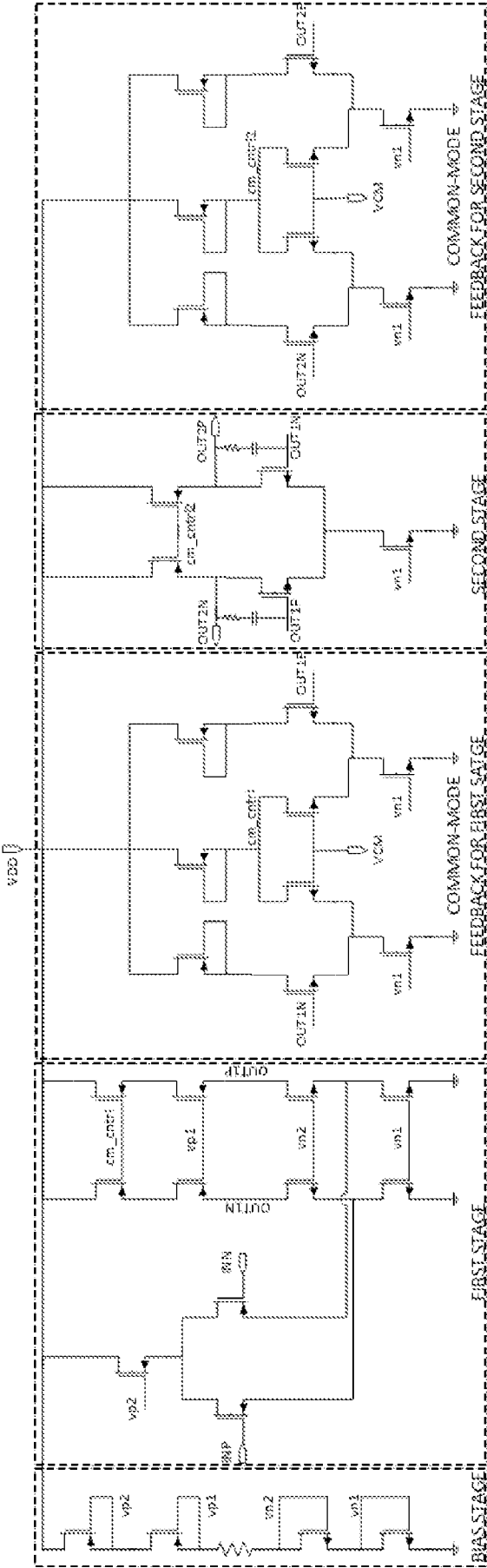


FIG. 4

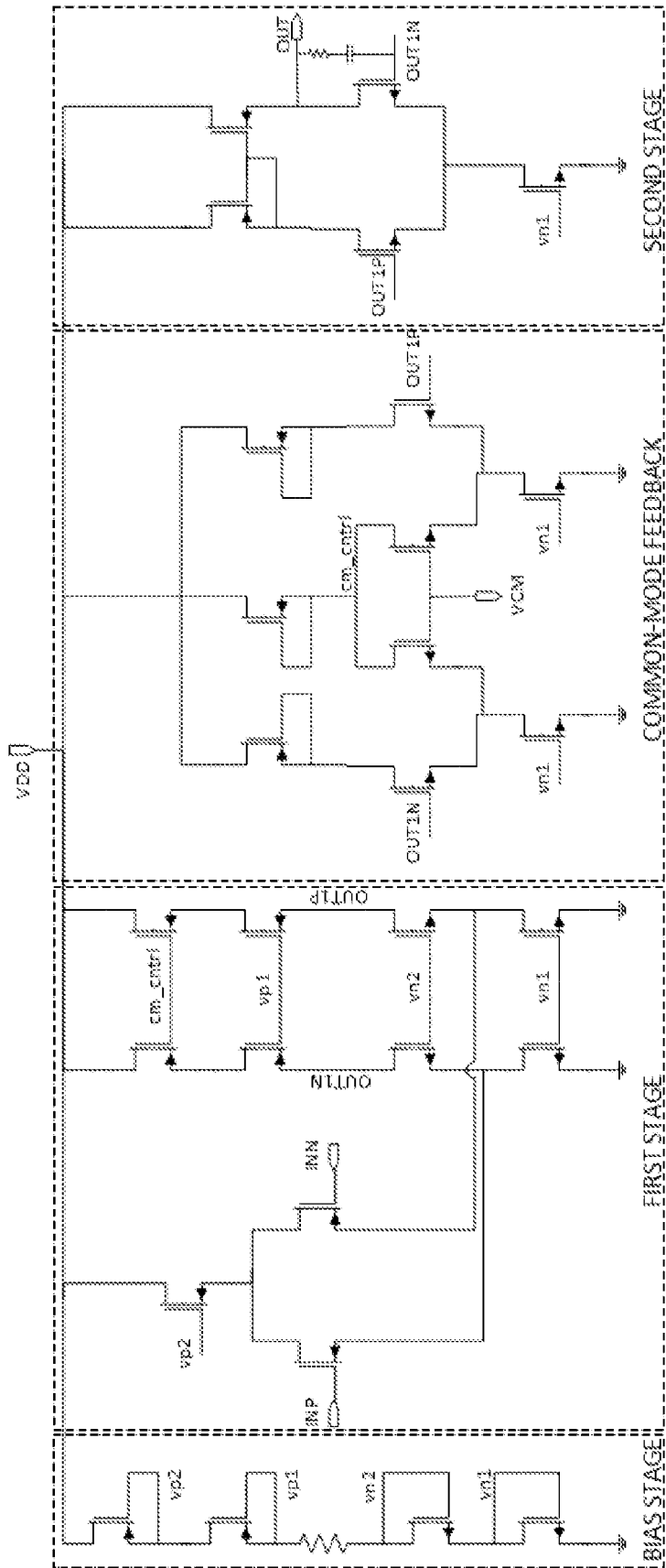


FIG. 5

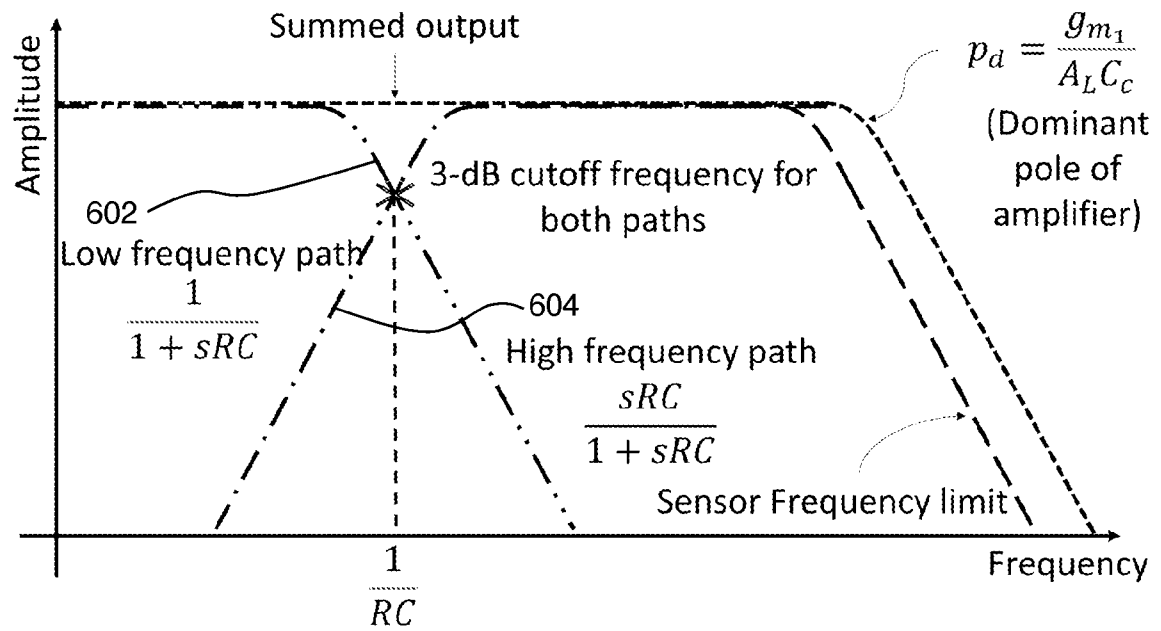


FIG. 6

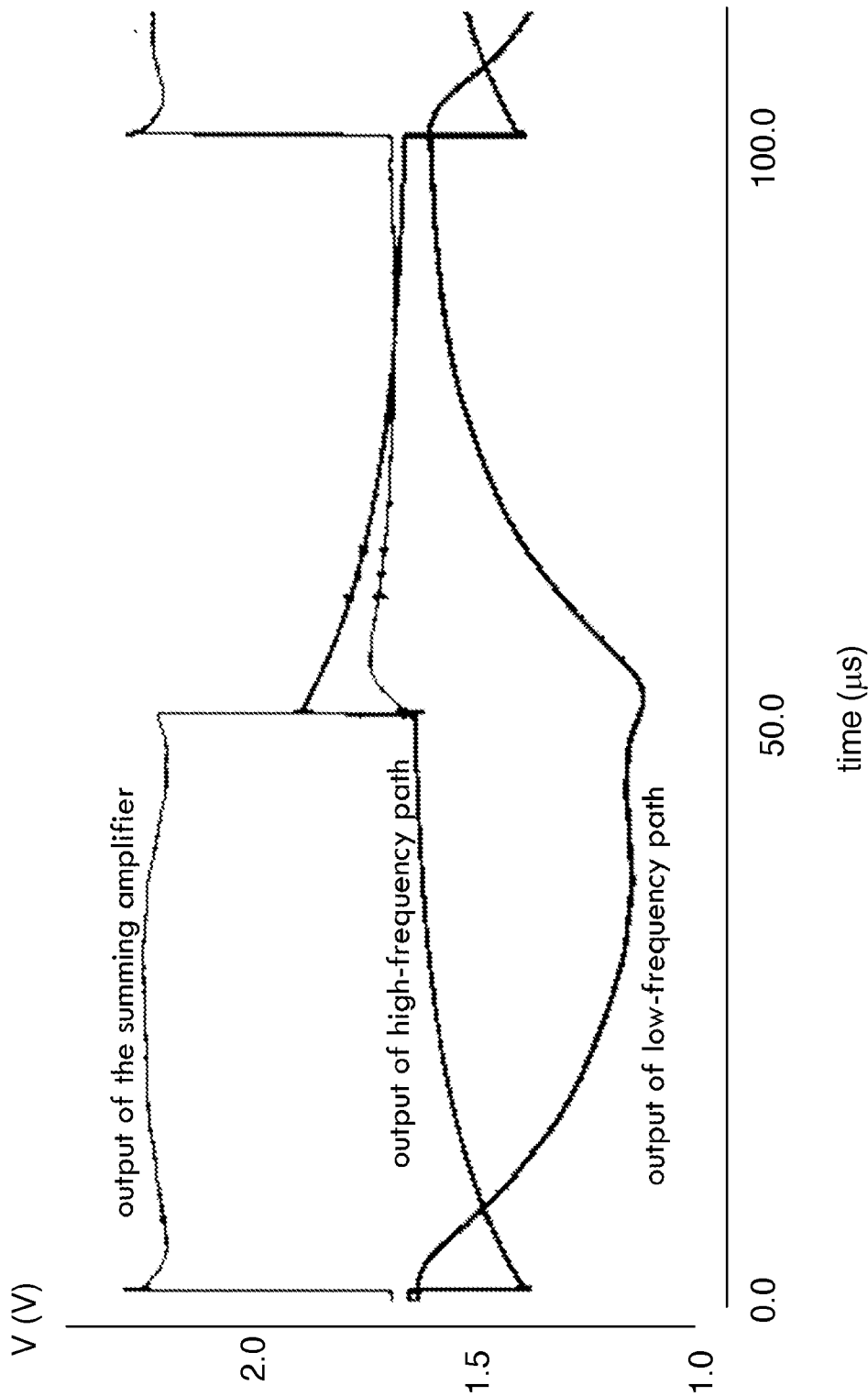


FIG. 7

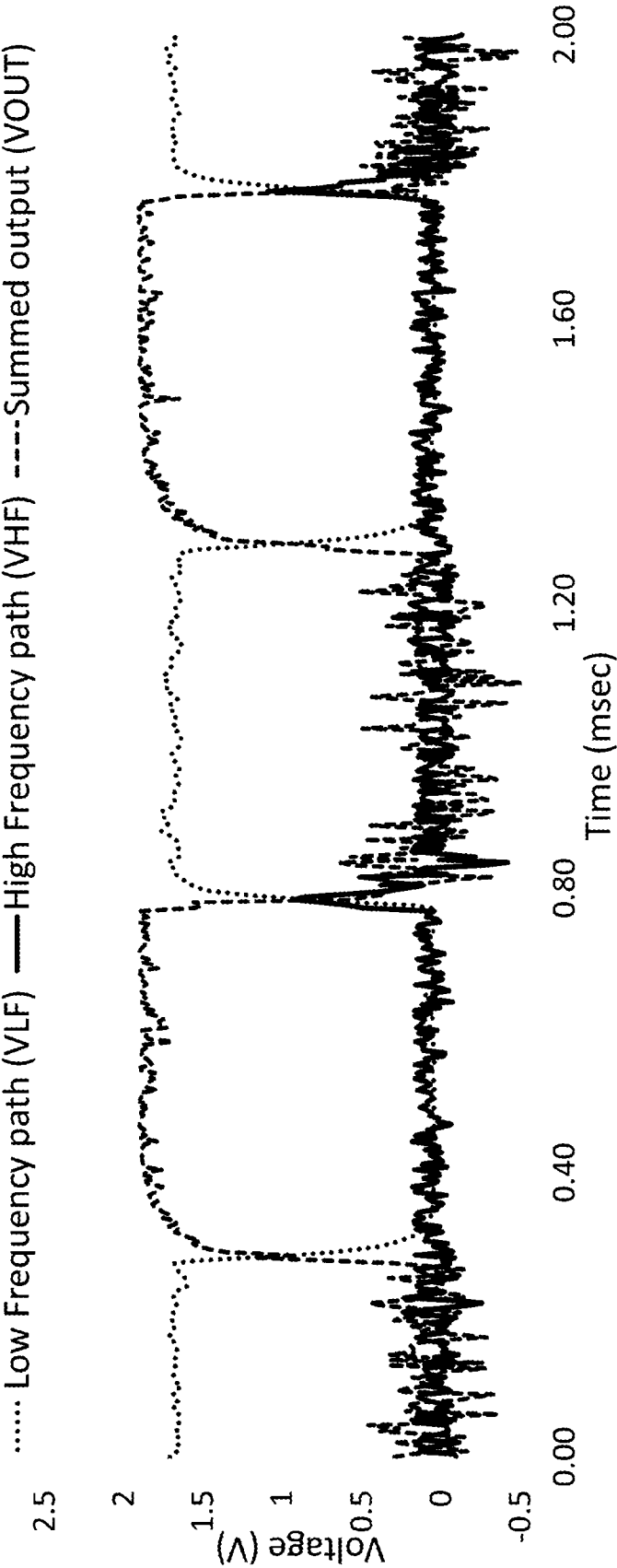


FIG. 8

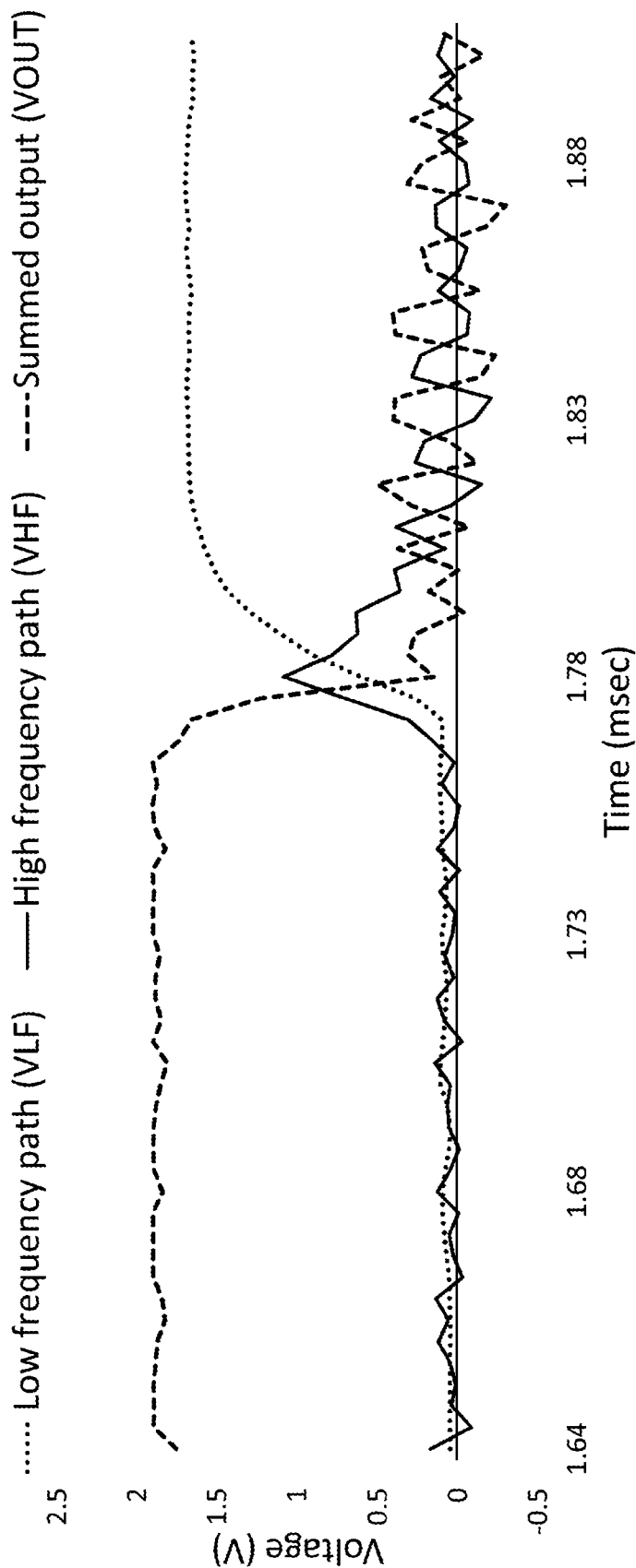


FIG. 9

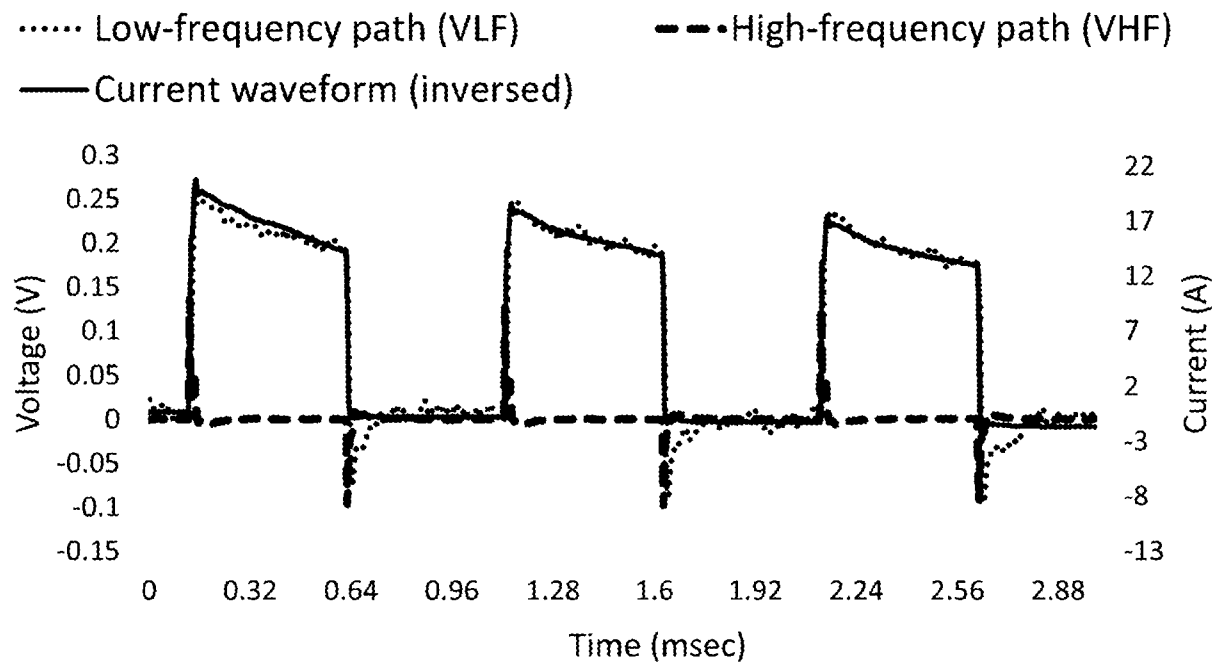


FIG. 10

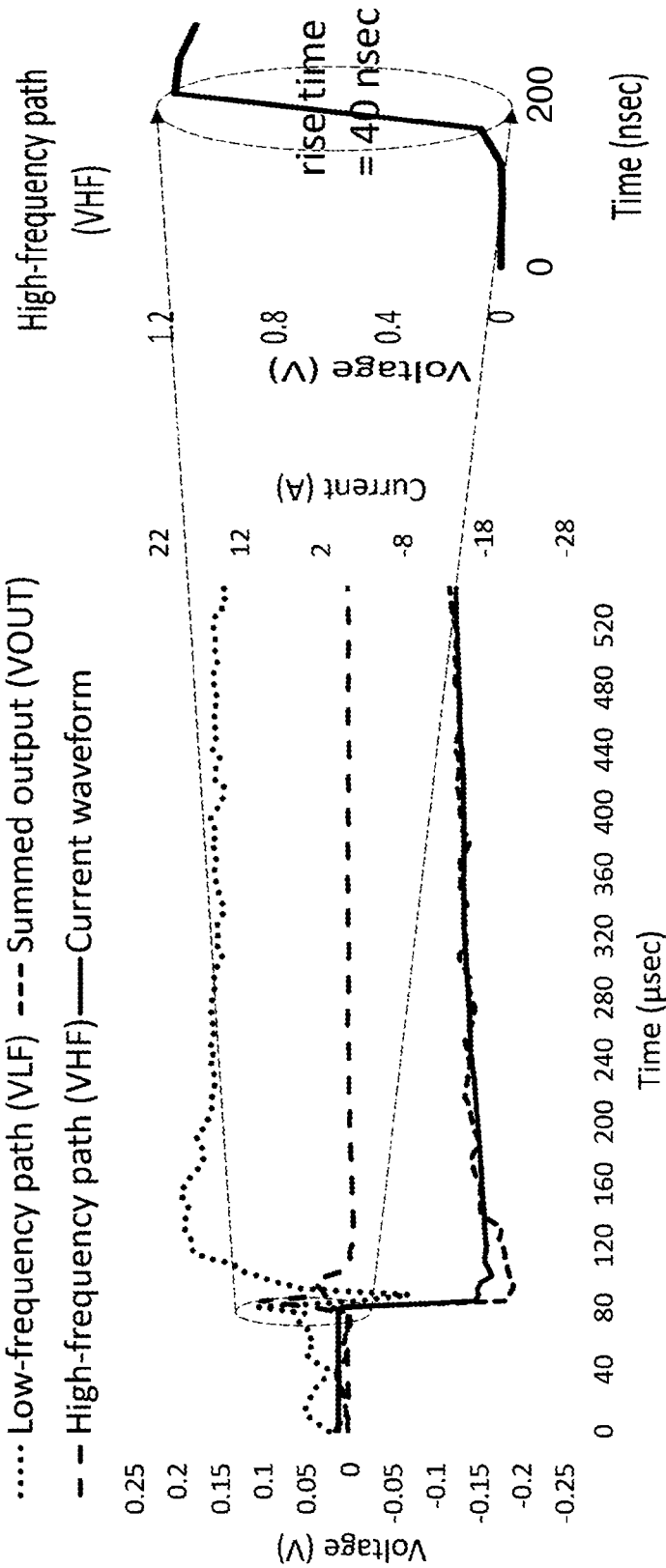


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/037921

A. CLASSIFICATION OF SUBJECT MATTERIPC: **G01R 33/07** (2023.01); **G01R 15/20** (2023.01); *G01R 33/28* (2023.01); *H04R 3/04* (2023.01)CPC: **G01R 33/07**; **G01R 15/202**; *G01R 33/28*; *H04R 3/04*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/0070008 A1 (INFINEON TECHNOLOGIES AG) 12 March 2015 (12.03.2015)	
Y	entire document	1-3, 5-8
Y	entire document	4, 9-11
Y	US 2015/0369881 A1 (INFINEON TECHNOLOGIES AG) 24 December 2015 (24.12.2015)	
Y	entire document	4
Y	US 2018/0364111 A1 (ROLLS-ROYCE CORPORATION et al.) 20 December 2018 (20.12.2018)	
Y	entire document	9
Y	US 2012/0025817 A1 (ROMERO et al.) 02 February 2012 (02.02.2012)	
Y	entire document	10, 11
A	US 2008/0094055 A1 (MONREAL et al.) 24 April 2008 (24.04.2008)	
A	entire document	1-11



Further documents are listed in the continuation of Box C.



See patent family annex.

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

26 August 2024 (26.08.2024)

Date of mailing of the international search report

04 September 2024 (04.09.2024)

Name and mailing address of the ISA/US

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