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(54) **Title:** PHOTOELECTRIC ELEMENT, IN PARTICULAR FOR USE IN STANDARD CMOS PROCESSES

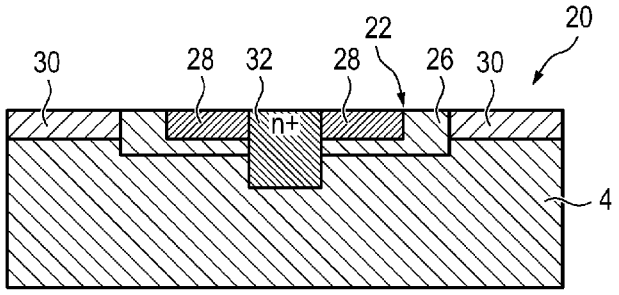

Fig. 2

(57) **Abstract:** The invention suggests a photoelectric element (20) that may be implemented on advanced CMOS technology very easily and offers superior technical properties regarding balancing of leakage currents and other parameters. According to the invention, the photoelectric element (20) comprises: - a substrate (4) of semiconductor material of a first type of electric conductivity, - a halo implant (26) in said substrate (4), said halo implant (26) having a second type of electric conductivity opposite to said first type of conductivity, and - an ldd implant (28) of said first type of electric conductivity, said ldd implant (28) being surrounded by said halo implant (26), wherein - a core set (22) formed by said ldd implant (28) and said halo implant (26) provides a pn-junction for a photodiode (24) for collecting light induced-charges.

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Photoelectric Element, in particular for use in Standard CMOS processes

DESCRIPTION

Technical background of the invention

The invention relates to a photoelectric element. The invention more particularly relates to a photoelectric element for use in standard CMOS processes. The invention furthermore relates to a photodetector device comprising a number of such photoelectric elements.

Background

Integrated photodetectors on standard CMOS technology are widely used for variety of applications. Depending on the respective application field and the requirements imposed thereby, typically the trade-off of photodetector characteristics regarding optical & electrical need to be considered for design and layout purposes. Leakage current, capacitance and spectral responsivity are parameters to be optimized for most of typical applications.

In order to modify the characteristics and optimize the parameters mentioned above for the respective individual purpose, the following typical approaches are considered in known systems:

A highly doped shallow layer (generally p-type, called surface passivation layer) at the surrounding region of the photodiode on top of the silicon may be introduced for suppressing the leakage current from the interface. In general, shallow p+ layer is used for this purpose.

Many distributed small-sized island photodiodes may be used to reduce the leakage current and capacitance basically by reducing the total area of the active photodiode. Small standard NWELL or nplus S/D implant layers may be used to

form the n-type island photodiode (IPD) region. However, it is rather difficult to achieve best trade-off between electrical and optical characteristics of the photodiode by using deep NWELL or any highly n-type implants existing on the standard CMOS process, and therefore this approach is only of limited value for applications in CMOS processes.

For further reducing the capacitance of pn-junction photodiode, a proper gap between IPD and surface-passivation region could be used, suppressing the perimeter junction capacitance of the photodiode.

With photodiodes designed in a conventional deep-junction NWELL concept, comparatively high leakage currents and high capacitances are observed because of the large depletion region by the deep-junction and lateral spreading of NWELL. Another approach is to use shallow junction nplus S/D-implant and nldd-implant, but doping concentration is too high for optimizing photodiode characteristics.

Consequently, in conventional approaches using conventional n-type wells existing on the standard CMOS process, it is difficult to optimize simultaneously the leakage current, junction capacitance, and spectral responsivity, because of the deep junction of the NWELL or very high doping concentration of the n-type S/D implants existing on the standard process. It needs dedicated implantation with additional alignment for further optimization of photodiode characteristics.

Summary

The object of the invention is therefore to provide an improved photoelectric element using pn-junction photodiodes that helps overcome the deficiencies identified above, and that may be implemented on advanced CMOS technology very easily, in particular targeting for an improved photodiode with low-leakage and low-capacitance characteristics. Further, an improved photo detector device should be provided.

With respect to the photoelectric element, this object is achieved with

- a substrate of semiconductor material of a first type of electric conductivity,
- a halo implant in said substrate, said halo having a second type of electric conductivity opposite to said first type of conductivity, and
- an ldd implant of said first type of electric conductivity, said ldd implant being surrounded by said halo implant,

wherein

- a core set formed by said ldd implant and said halo implant provides a pn-junction for a photodiode for collecting light induced-charges.

In particular, incoming light will generate light-indicued charge carriers in a region comprising the substrate, the pn-junction as such and its outside region. The carriers so generated will then be collected by the junction.

Preferred embodiments are subject of the dependent claims.

The invention is based on the consideration that for especially high compatibility with CMOS technology and superior properties of the photoelectric element, the concept of "partially buried pn-junction" should be considered, in particular in order to overcome the drawbacks arising from previous approaches as mentioned above. A partially buried pn-junction according to an aspect of the invention may be provided by using a halo-implant of a given type of electric conductivity, typically and preferably n-type, which is already existing and therefore readily available in advanced standard CMOS processes and CMOS technology. In particular, an n-type halo-implant is part of core-pldd implant set on almost all advanced standard CMOS technologies, which is used for the suppressing punch-through between source and drain of the low-voltage PMOS transistors, and therefore vastly and readily available.

According to an aspect of the inventions, such core-pldd implant set containing an n-type halo-implant may be specifically used to provide the pn-junction of the photodiode. Thereby, it is possible to introduce simultaneously both of buried n-type pn-junction and p-type surface passivation layer on top of the n-type photodiode layer without any additional mask. With a core-pldd layer (both of p-type ldd-implant and n-type halo-implant), either one of single large size photodiodes or distributed photodiodes with many small island-type photodiodes may be provided, depending on the desired trade-off and expected parameters among spectral responsitivity, leakage current, and CV specifications.

As a summary of one aspect of the invention, proper pn-junction photodiodes together with highly doped shallow p-type surface passivation on top of n-type photodiodes can be introduced. Trade-off among SR, leakage current and capacitance could be adjusted by changing photodiode size, shapes, and distribution pattern.

In a preferred embodiment, the photoelectric element further comprises a contact implant region in said substrate, said contact implant region having said second type of electric conductivity, wherein said halo implant laterally surrounds said contact implant region. In order to provide versatile contact points to the junction, in further preferred embodiment this contact implant region extends into the bulk of said substrate beyond said halo implant; in this embodiment, the contact implant region may be referred to as a body well. In other words, in this preferred aspect of the invention the active layer forming the pn junction is designed relatively shallow, thereby being restricted to a comparatively small and thin layer zone close to the surface, and with respect to depth into the substrate it extends less deeply than the contact implant region or body well.

In a preferred embodiment, the contact implant region is doped higher than said pldd and halo implant in order to provide safe and reliable contact function.

According to yet another aspect of the invention, the core set of said ldd implant and said halo implant has an overall layer thickness of 0.1 µm to 1 µm, preferably to 0.6 µm, at maximum.

In yet another preferred embodiment said ldd implant is doped higher than said substrate.

The substrate of the photoelectric element according to the invention may be a “conventional”, bulk substrate. In an alternative aspect of the invention, the substrate may as well be an epitaxial layer system. In the latter case, the thickness of the epitaxial layer preferably is between 2 µm to 60 µm, depending on electrical & optical characteristics and requirements.

Preferably and in view of the beneficial compatibility with standard CMOS technology, the first type of electric conductivity is a positive (p-type) conductivity, and the second type of conductivity is a negative (n-type) conductivity.

In order to further minimize leakage currents, in a preferred embodiment of the invention the halo implant is laterally surrounded by a surface passivation layer of said first type of conductivity, said surface passivation layer doped higher than said substrate.

In another aspect of the invention, the photoelectric element may comprise a multitude of island photodiode elements, wherein each island photodiode element comprises a core set formed by one of said ldd implants and one of said halo implants. Preferably, in this embodiment the lateral distance between any two of neighbouring island photodiode elements is at least 5 µm.

With respect to the photo detector device the invention suggests to provide a photoelectric element of any one of the embodiments mentioned above and an aperture metal mask cover-

ing, as seen in top view, an outer fringe of the surface of said photoelectric element. In a preferred embodiment, the outer fringe covered by the aperture metal mask has a width of about 1 mm maximum. In an aspect of the invention, the width of the metal or black-filter mask is chosen such that the outside of the photodiode region is covered sufficiently in order to safely protect from unnecessary incident light. In particular, and in one embodiment of the invention, the distribution pattern and additional number of islands underneath the metal/black-filter mask may be determined and chosen in view of the trade-off among leakage, capacitance, and spectral responsivity.

In accordance with an aspect of the invention considered independently inventive, the photo detector device comprises a number of island photodiode elements each of which is positioned underneath said aperture metal mask, wherein each island photodiode element comprises a core set formed by one of said ldd implants and one of said halo implants. In particular, and in one aspect of the invention, such island photodiode elements may be positioned underneath the metal or black-filter mask so as to efficiently collect photo-generated carriers in this area, too.

Main advantages of the present invention may be seen in that in order to overcome the problems mentioned above, the invention suggests partially buried photodiodes by using core-pldd implant set (p-type pldd and n-type halo implants) existing on the advanced CMOS process. An n-type halo implant well may be located between p-type ldd implant well on top and p-type substrate at the bottom, and a partially buried n-type well can be introduced without any additional alignment. A p-type ldd implant well on top of n-type halo implant well may also act as a p-type surface passivation layer, and it reduces further the leakage current by protecting leakage current contribution from the interface. Additionally, low periphery junction-capacitance can be achieved by the laterally diffused n-type halo-implant well at the outside of the p-type ldd implant well.

It is considered particularly beneficial that standard components of CMOS processes, namely existing core pldd-implant sets having an n-type halo implant, may be used to provide the pn-junction for a photodiode, thereby providing particularly efficient manufacturing as well as high compatibility with standard CMOS technology. In particular, and as a significant advantage of the invention, such a core set in production may be introduced with one mask only. Energy and tilt-angle of a halo implant are higher and steeper than those of ldd implant, respectively.

Brief Description of the Preferred Embodiments

Preferred embodiments and aspects of the invention are described further in connection with a drawing. In this drawing,

FIG. 1 shows embodiments of photoelectric elements comprising photodiodes of prior art systems in cross section;

FIG. 2 a photoelectric element in accordance with the invention in cross section;

FIG. 3 shows embodiments of photoelectric elements in accordance with the invention in top view;

FIG. 4 shows the photoelectric element with various photodiode patterns in top view;

FIG. 5 shows another embodiment of a photoelectric element both in top view (FIG. 5a) and in cross section (FIG. 5b);

FIG. 6 shows a photo detector device in top view; and

FIG. 7 shows various graphs representing the results of comparative measurements of the suggested design.

Identical parts are labelled by the same reference numerals.

Detailed Description of the Preferred Embodiments

FIG. 1 shows two embodiments of prior art photoelectric elements 1, 1´, each providing pn-junction photodiodes 2, 2´. In both embodiments shown in FIG. 1, the photoelectric element 1, 1´ comprises a substrate 4 of semiconductor material, which may especially be silicon, for instance. A contact implant region 6 is formed in the substrate 4. A plurality of body contacts 8, both cathode contacts 8a and anode contacts 8b, are provided on the contact implant region 6 or directly on the substrate 4, respectively.

In the embodiments shown, the substrate 4 is a bulk substrate of said semiconductor material, in particular silicon. Alternatively, the substrate 4 may be an epitaxial layer system.

The substrate 4 of the photoelectric elements 1, 1´ as well as that of the embodiments in accordance with the present invention as described below is made of a semiconductor material of a first type of electric conductivity. In the embodiments shown, this first type of electric conductivity is chosen to be p-type. Accordingly, in the embodiments shown, a second type of electric conductivity is meant to mean “n-type”. In general, however, this association might be reversed, and n-type as being said “first type” and p-type as being said “second type” might also be possible. In the following, with respect to the embodiments shown, p-type shall be understood as meaning “a first type of an electric conductivity” and n-type shall be understood as meaning “a second type of an electric conductivity”.

The contact implant region 6 of the photoelectric elements 1, 1´ is an n-type contact implant region 6. Therefore, as shown in FIG. 1, the prior art uses existing n-type implants 8 (NWELL, n+ or nldd) to form the pn-junction photodiode 2, 2´. Depending on the selected trade-off among leakage current, capacitance, and spectral responsivity, it can be a single large size photodiode 2 (FIG. 1a) or a distributed islands

photodiode 2´ (FIG. 1b). As further shown in FIG. 1b, a surface passivation layer 10 in form of a highly doped shallow p-type region can be introduced on the top silicon surface at the surrounding region of the active pn-photodiode 2´ for further suppressing leakage current. It mainly acts as to protect leakage current generated near the Si and oxide interface in this area.

In view of a desired compatibility with standard CMOS processes, in such conventional approaches using conventional n-type wells existing on the standard CMOS process, it has turned out to be difficult to optimize simultaneously the leakage current, junction capacitance, and spectral responsivity, in particular because of the deep junction of the NWELL or very high doping concentration of the n-type S/D implants existing on the standard process. In order to overcome these deficiencies, and to provide a photoelectric element 20 that is particularly suitable for integration into standard CMOS technology and CMOS processes, the present invention suggests to use an existing core pldd-implant set 22 to provide the pn-junction photodiode 24.

Therefore, in a photoelectric element 20 according to the present invention, as shown in cross section in FIG. 2, a halo n-type implant 26 and an pldd implant 28 surrounded by the halo implant 26 are provided in the substrate 4, the halo n-type implant 26 together with the pldd implant 28 constituting the core pldd-implant set 22. This core set 22 formed by the pldd implant 28 and the halo implant 26 provides the pn-junction for the photodiode 24 for generating light induced-charges.

Depending on the selected trade-off among leakage current, spectral response, and capacitance, photodiode size, shape, and layouts can be properly adjusted and adequately chosen. Proper island types and distribution patterns may be used for the pn-junction photodiode 24 structure. In a preferred embodiment, the halo implant 26 further may be laterally surrounded by a surface passivation layer 30 of said first type

of conductivity, said surface passivation layer 30 doped higher than the substrate 4 (in the embodiment shown p+).

In other words, as may be seen in FIG. 2, the photoelectric element 20 in the embodiment of the invention shown here provides a partially buried photodiode 24 by using the core-pldd implant set 22 (p-type pldd implant 28 and n-type halo implant 26) existing on the advanced CMOS process. The n-type halo implant well 26 is located between the p-type ldd implant well 28 on top and p-type substrate 4 at the bottom, and therefore the partially buried n-type well 26 can be introduced without any additional mask alignment. The p-type ldd implant well 28 on top of the n-type halo implant well 26 acts also as a p-type surface passivation layer, and it reduces further the leakage current by protecting against leakage current contribution from the interface. Additionally, low periphery junction-capacitance can be achieved by the laterally diffused n-type halo-implant well 26 at the outside of the p-type ldd implant well 28.

For contacting purposes, the photoelectric element 20 further comprises a contact implant region 32 in said substrate, said contact implant region 32 having said second type of electric conductivity (n-type). The contact implant region 32 is doped higher the halo implant 26, and therefore in the embodiment shown is n+. The halo implant 26 laterally surrounds this contact implant region 32. In the case of a highly doped contact region, due to higher doping and in case of deeper junction-depth than said core pldd set, the contact implant region 32 may also be referred to as a body well. The contact implant region 32 in the embodiment shown, and comparably to a body well, extends into the bulk of the substrate 4 way beyond the depth of the halo implant 26. Further, the core set 22 of the pldd implant 28 and the halo implant 26 has an overall layer thickness of about 0.6 µm at maximum.

The lateral structure of the photoelectric element 20 may be chosen in accordance to specific requirements of the respective application; relatively high flexibility is possible.

FIG. 3 shows top views of various structures of the photoelectric element 20, namely a circular type in FIG. 3a, and a rectangular type in FIG. 3b. The cathode contact region 34 or the contact implant region 32 is located in the middle of the structure (n+ S/D implant). The p+ region at the outside of the cathode contact is provided by the pldd implant 28, and the n- region is provided by the n-type halo implant 26. Advanced CMOS technology offers these two implants 26, 28 as a set 22 of core-pldd implant. As may be seen clearly in this top view, the shallow p+ passivation layer 30 is provided at the outside of the n- region given by the halo implant 26, completely surrounding it for further reducing the leakage current. The schematic view along the Cut line A is shown in FIG. 2.

In an aspect of the invention, a multitude of island photodiode elements 24 of the type described above may be provided for the photoelectric element 20. In this embodiment of the invention, preferably each island photodiode element 24 comprises a core set 22 formed by one of the pldd implants 28 and an associated one of the halo implants 26. In a preferred embodiment, the lateral distance D between any two of neighbouring island photodiode elements 24 is at least 5 µm. In FIG. 4, various photodiode patterns are shown for the photoelectric element 20 of this kind. The suggested photodiodes 24 could be either single large and small photodiodes 24 or any distributed photodiodes 24 as shown in the figure. Any shape of island or stripe patterns may be conceived, depending on applications. Island diameter, stripe dimension (width and length) and distance D between two photodiodes 24 should be properly adjusted so as to fulfil the electrical and optical requirements of the respective applications. In particular, the diameter of the respective island photodiodes 24 could be from 0.5 µm up to 10 µm. Stripe width and length could be from 0.5 µm up to 10 µm. The distance between neighbour islands could be from 5 µm up to 50 µm, depending on the electrical and optical characteristics and requirements.

In an aspect considered independently inventive, as shown in FIG. 5a in top view and in FIG. 5b in cross section, the photoelectric element 20 may be provided with a single and large rectangle photodiode 24. The contact implant region 32 providing the n+ cathode contact in this embodiment is formed, as seen in top view, as a closed rectangular structure completely surrounding in inner areas of the pldd implant 28. In this embodiment it is introduced at the surrounding photodiode region. This large single rectangle photodiode 24 could be in the range of 10 µm x 10 µm and 1000 µm x 1000 µm.

In yet another aspect of the invention, a photo detector device 40 comprising a photoelectric element 20 of type described above is provided. As can be seen in the top view in FIG. 6, the photo detector device 40 further comprises an aperture metal layer mask covering 42, providing an aperture for the photoelectric element 20 and covering an outer fringe 44 of the surface of the photoelectric element 20. The outer fringe 44 covered by the aperture metal mask 42 in a preferred embodiment has a width chosen appropriately in view of a desired trade-off between leakage, capacitance, and spectral responsivity.

In yet another independently inventive aspect of the invention, in the photo detector device 40 a number of island photodiode elements 24 is positioned underneath this metal or black-filter mask 42, wherein each island photodiode element 24 comprises a core set 22 formed by one of the pldd implants 28 and one of the halo implants 26. In this setup the island photodiode elements 24 positioned underneath the mask 42 may be used to efficiently collect the laterally spreading photo carriers generated at the main photodiode region.

Functionality of the suggested inventive design concepts has been verified in various comparative measurements, the results of which are shown in various graphs in FIG. 7. FIG. 7a shows the spectral responsivity SR as a function of wavelength λ in a comparison of distributed photodiodes 24 be-

tween previous and now suggested approaches. Evidently, the two lines of results more or less overlap, showing that by proper design of photodiode dimensions (mainly diameter and distance between distributed photodiodes), similar spectral responsivity between two approaches may be achieved. In FIG. 7b, the leakage current IL as a function of cathode Voltage Vc of distributed photodiodes is compared between previous and suggested approaches. The approach suggested now in accordance with the invention shows lower leakage current while keeping similar spectral responsivity as shown in FIG. 7a. Further, in FIG. 7c the capacitance C as a function of cathode Voltage Vc of distributed photodiodes is compared between previous and suggested approaches. The approach suggested now in accordance with the invention shows lower junction capacitance while keeping similar spectral responsivity as shown in FIG. 7.

LIST OF REFERENCE NUMERALS

1, 1´	photoelectric element (prior art)
2, 2´	pn-junction photodiode
4	substrate
6	contact implant region
8	implant
10	surface passivation layer
20	photoelectric element
22	core pldd-implant set
24	photodiode
26	halo implant
28	pldd implant
30	passivation layer
32	contact implant region
34	contact region
36	line
40	photo detector device
42	aperture metal mask covering
44	outer fringe
D	Distance between photodiodes
λ	Wavelength
SR	Spectral responsitivity
IL	Leakage current
cV	Cathode Voltage
C	Capacitance

CLAIMS

1. A photoelectric element (20), comprising:
- a substrate (4) of semiconductor material of a first type of electric conductivity,
- a halo implant (26) in said substrate (4), said halo implant (26) having a second type of electric conductivity opposite to said first type of conductivity, and
- an ldd implant (28) of said first type of electric conductivity, said ldd implant (28) being surrounded by said halo implant (26), wherein
- a core set (22) formed by said ldd implant (28) and said halo implant (26) provides a pn-junction for a photodiode (24) for collecting light induced-charges.

2. The photoelectric element (20) of claim 1, further comprising a contact implant region (32) in said substrate (4), said contact implant region (4) having said second type of electric conductivity, wherein said halo implant (26) laterally surrounds said contact implant region (32).

3. The photoelectric element (20) of claim 2, wherein said contact implant region (32) extends into the bulk of said substrate (4) beyond said halo implant (26).

4. The photoelectric element (20) of claim 2 or 3, wherein said contact implant region (32) is doped higher than said halo implant (26).

5. The photoelectric element (20) of any one of claims 1 to 4, wherein said core set (22) of said ldd implant (28) and said halo implant (26) has an overall layer thickness of 0.1 µm and 1 µm, preferably between 0.1 µm and 0.6 µm, at maximum.

6. The photoelectric element (20) of any one of the preceding claims, wherein said ldd implant (28) is doped higher than said substrate (4).

7. The photoelectric element (20) of any one of the preceding claims, wherein said substrate (4) is an epitaxial layer system.

8. The photoelectric element (20) of any one of the preceding claims, wherein said first type of electric conductivity is a positive (p-type) conductivity, and said second type of conductivity is a negative (n-type) conductivity.

9. The photoelectric element (20) of any one of the preceding claims, wherein said halo implant (26) is laterally surrounded by a surface passivation layer (30) of said first type of conductivity, said surface passivation layer (30) doped higher than said substrate.

10. The photoelectric element (20) of any one of the preceding claims, comprising a multitude of island photodiode elements (24), wherein each island photodiode element (24) comprises a core set (22) formed by one of said ldd implants (28) and one of said halo implants (26).

11. The photoelectric element (20) of claim 10, wherein the lateral distance (D) between any two of neighbouring island photodiode elements (24) is at least 5 µm.

12. A photo detector device (40) comprising a photoelectric element (20) of any one of the preceding claims and an aperture metal or black-filter mask (42) covering, as seen in top view, an outer fringe (44) of the surface of said photoelectric element (20).

13. The photo detector device (40) of claim 12, wherein the outer fringe (44) covered by the aperture metal mask (42) has a width of 5 mm maximum.

14. The photo detector device (40) of claim 12 or 13, wherein a number of island photodiode elements (24) is positioned underneath said aperture metal mask (42), wherein each island

photodiode element (24) comprises a core set (22) formed by one of said ldd implants (28) and one of said halo implants (26).

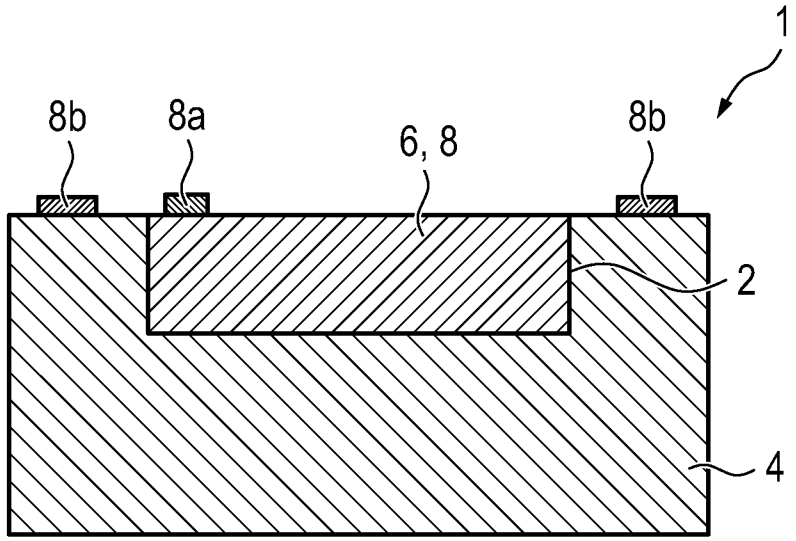

Fig. 1a
(PRIOR ART)

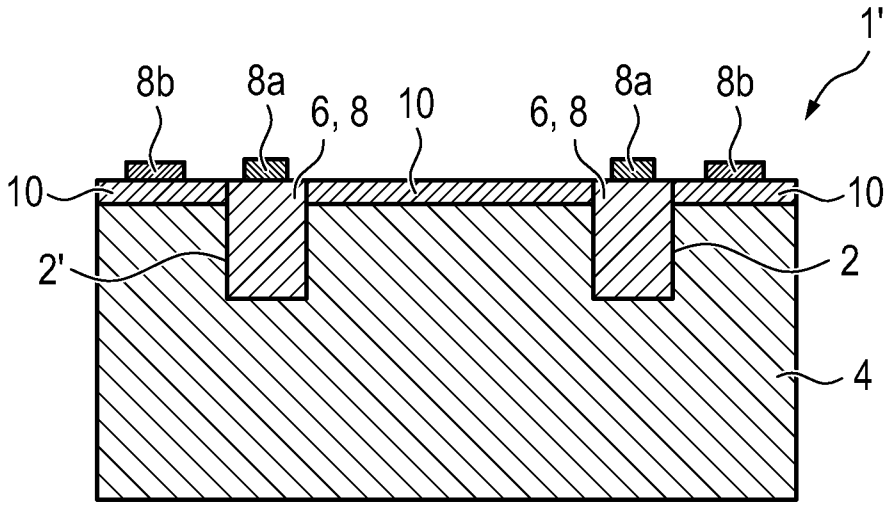

Fig. 1b
(PRIOR ART)

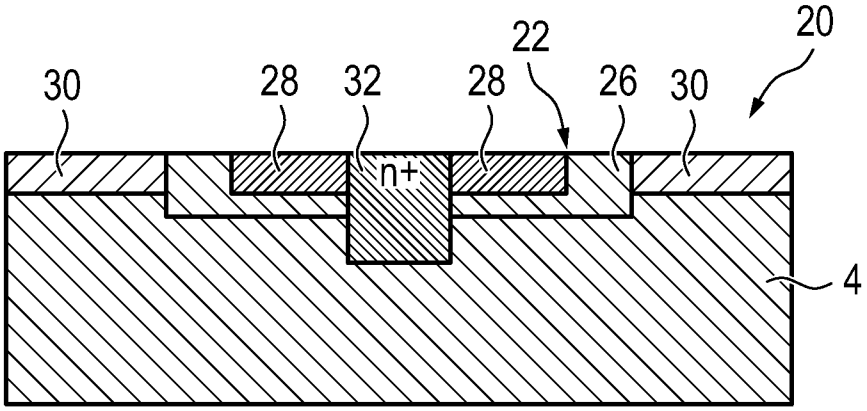

Fig. 2

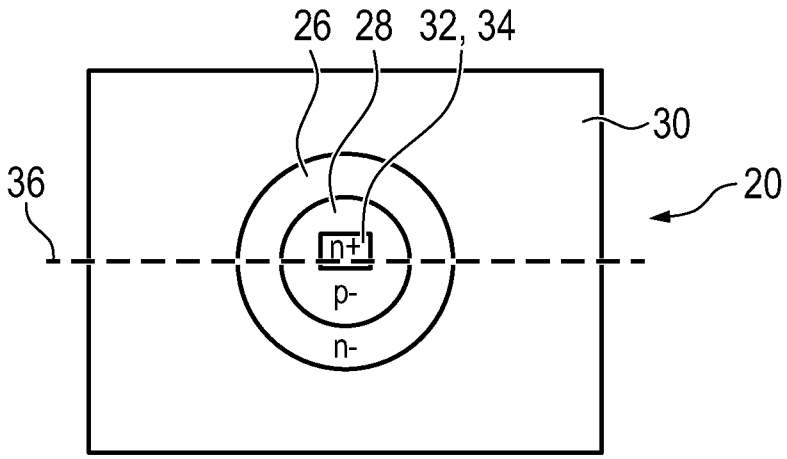

Fig. 3a

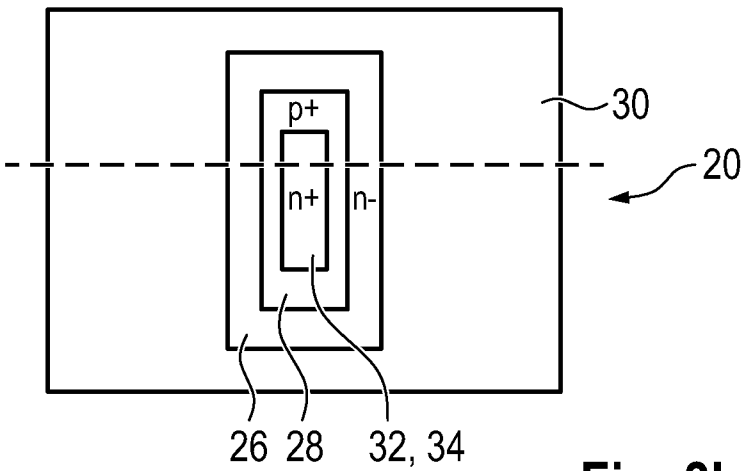

Fig. 3b

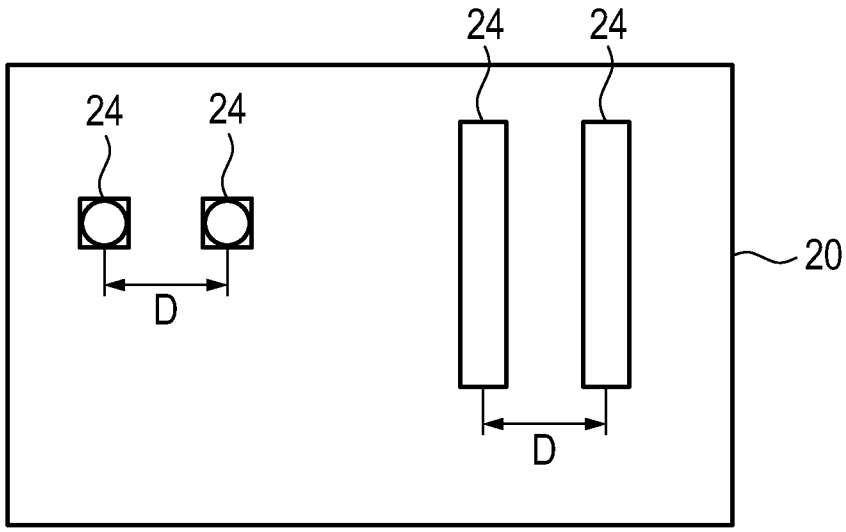

Fig. 4

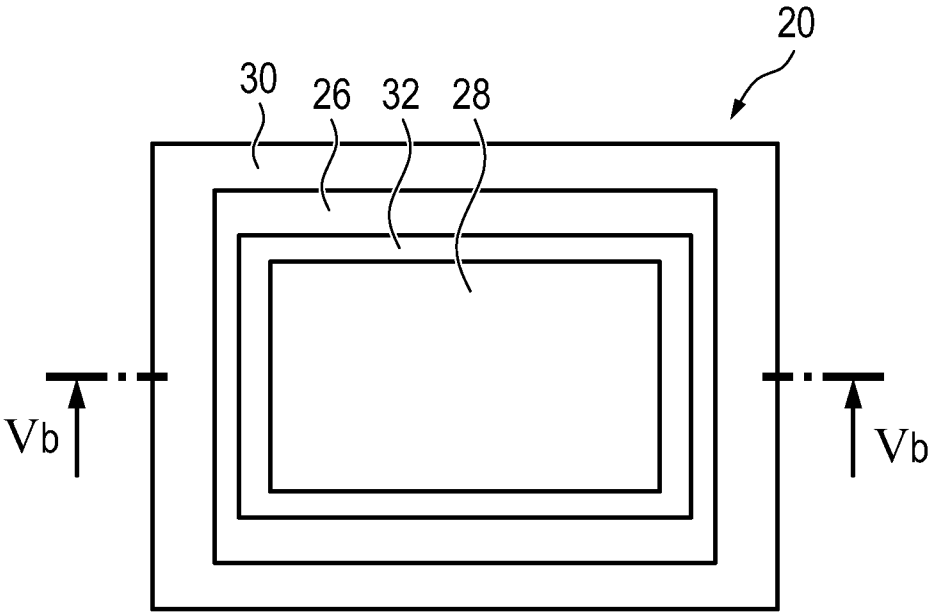

Fig. 5a

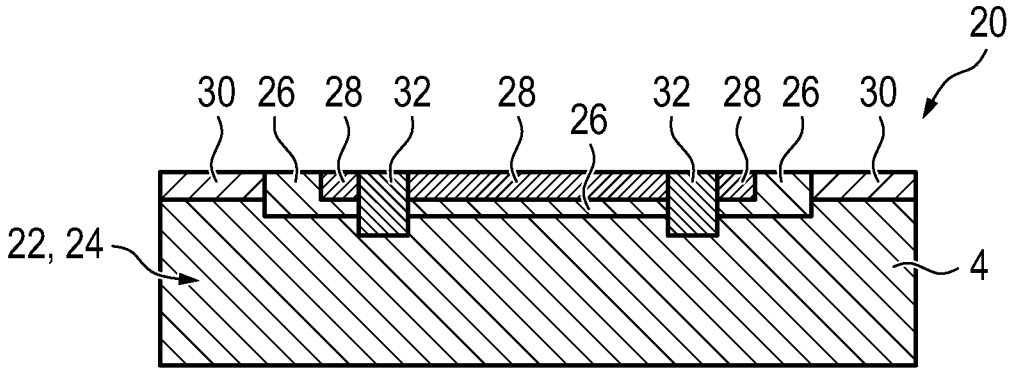

Fig. 5b

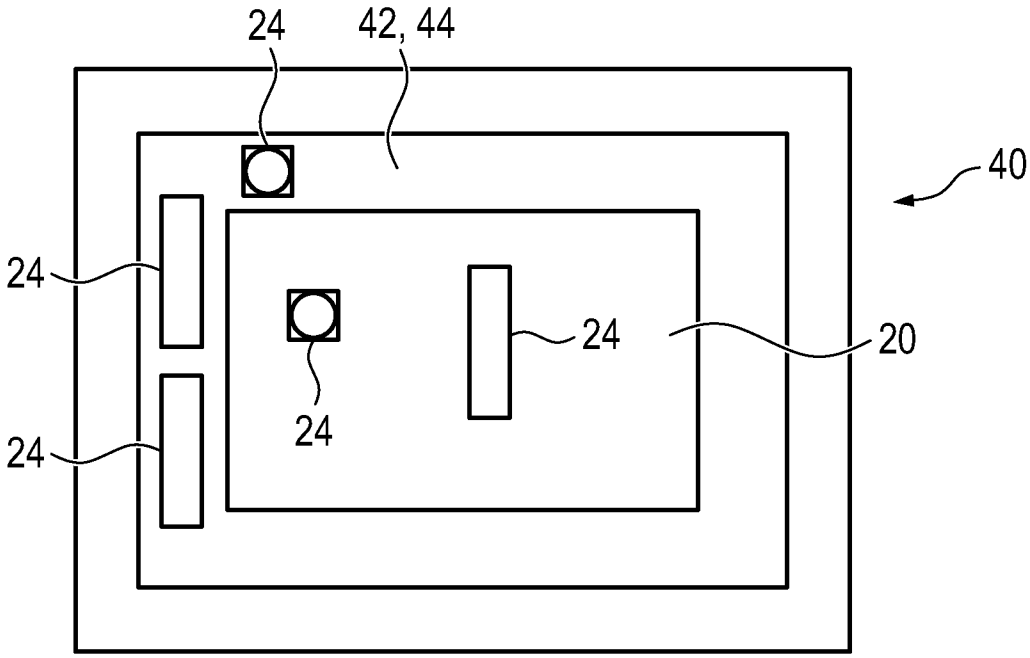

Fig. 6

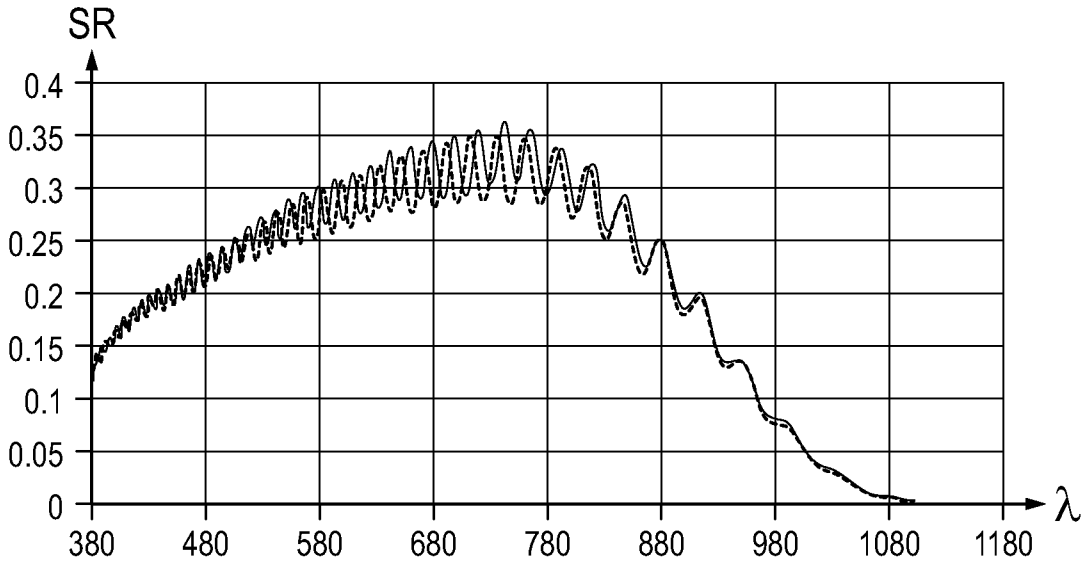
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Fig. 7a

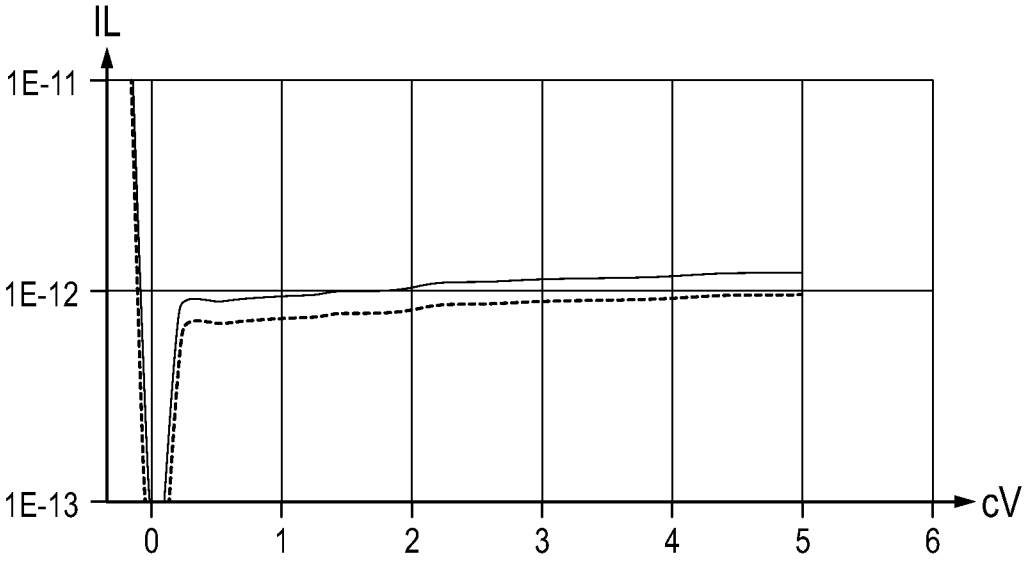
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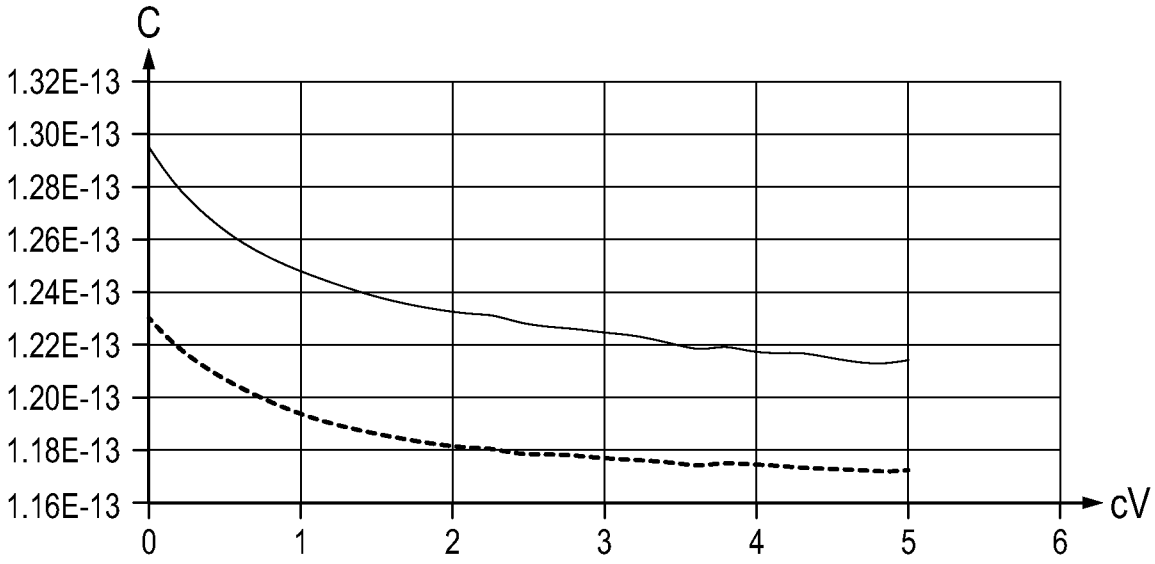
Fig. 7b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cV

Fig. 7c

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/058082

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/103 H01L27/144
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/038296 A1 (MERRILL RICHARD B [US]) 27 February 2003 (2003-02-27)	1,5-8, 10-14
A	abstract paragraph [0026] figure 1	2-4,9

X	US 5 994 162 A (BURGHARTZ JOACHIM NORBERT [US] ET AL) 30 November 1999 (1999-11-30) abstract column 3, lines 19-37 column 4, line 1 - column 5, line 43 figures 1-3	1-14

A	US 2003/148574 A1 (THOMAS DANIELLE A [US] ET AL) 7 August 2003 (2003-08-07) paragraphs [0016] - [0023] figures 1b,1c	1-14

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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 June 2024	10/07/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ekoué, Adamah

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/058082

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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