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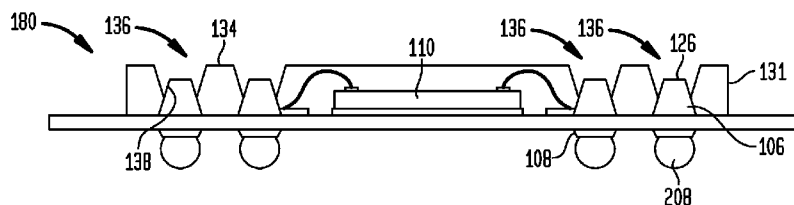
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(54) Title: STACKABLE MOLDED MICROELECTRONIC PACKAGES

FIG. 5



(57) Abstract: A microelectronic package has a microelectronic element 110 overlying or mounted to a first surface 102 of a substrate 100 and substantially rigid conductive posts 106 projecting above the first surface or projecting above a second surface 104 of the substrate remote therefrom. Conductive elements 108 exposed at a surface of the substrate opposite the surface above which the conductive posts project are electrically interconnected with the microelectronic element. An encapsulant 130 overlies at least a portion of the microelectronic element 110 and the surface 102 of the substrate 100 above which the conductive posts 106 project, the encapsulant having a recess 336 or one or more openings 136, 236 each permitting at least one electrical connection to be made to at least one conductive post. At least some conductive posts 106 are electrically insulated from one another and adapted to simultaneously carry different electric potentials. In particular embodiments, the openings 136, 140, 146, 236 in the encapsulant 130 at least partially expose conductive masses 144 joined to posts, fully expose top surfaces 126 of posts 106 and partially expose edge surfaces 138 of posts, or may only partially expose top surfaces 126 of posts.

STACKABLE MOLDED MICROELECTRONIC PACKAGES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the filing date of U.S. Patent Application Serial No. 12/838,974 filed July 19, 2010, the disclosure of which is hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to microelectronic packages and to methods of making or testing microelectronic packages.

BACKGROUND OF THE INVENTION

[0003] Microelectronic devices such as semiconductor chips typically require many input and output connections to other electronic components. The input and output contacts of a semiconductor chip or other comparable device are generally disposed in grid-like patterns that substantially cover a surface of the device (commonly referred to as an "area array") or in elongated rows which may extend parallel to and adjacent each edge of the device's front surface, or in the center of the front surface. Typically, devices such as chips must be physically mounted on a substrate such as a printed circuit board, and the contacts of the device must be electrically connected to electrically conductive features of the circuit board.

[0004] Semiconductor chips are commonly provided in packages that facilitate handling of the chip during manufacture and during mounting of the chip on an external substrate such as a circuit board or other circuit panel. For example, many semiconductor chips are provided in packages suitable for surface mounting. Numerous packages of this general type have been proposed for various applications. Most commonly, such packages include a dielectric element, commonly referred to as a "chip carrier" with terminals formed as plated or etched metallic structures on the dielectric. These

terminals typically are connected to the contacts of the chip itself by features such as thin traces extending along the chip carrier itself and by fine leads or wires extending between the contacts of the chip and the terminals or traces. In a surface mounting operation, the package is placed onto a circuit board so that each terminal on the package is aligned with a corresponding contact pad on the circuit board. Solder or other bonding material is provided between the terminals and the contact pads. The package can be permanently bonded in place by heating the assembly so as to melt or "reflow" the solder or otherwise activate the bonding material.

[0005] Many packages include solder masses in the form of solder balls, typically about 0.1 mm and about 0.8 mm (5 and 30 mils) in diameter, attached to the terminals of the package. A package having an array of solder balls projecting from its bottom surface is commonly referred to as a ball grid array or "BGA" package. Other packages, referred to as land grid array or "LGA" packages are secured to the substrate by thin layers or lands formed from solder. Packages of this type can be quite compact. Certain packages, commonly referred to as "chip scale packages," occupy an area of the circuit board equal to, or only slightly larger than, the area of the device incorporated in the package. This is advantageous in that it reduces the overall size of the assembly and permits the use of short interconnections between various devices on the substrate, which in turn limits signal propagation time between devices and thus facilitates operation of the assembly at high speeds.

[0006] Assemblies including packages can suffer from stresses imposed by differential thermal expansion and contraction of the device and the substrate. During operation, as well as during manufacture, a semiconductor chip tends to expand and

contract by an amount different from the amount of expansion and contraction of a circuit board. Where the terminals of the package are fixed relative to the chip or other device, such as by using solder, these effects tend to cause the terminals to move relative to the contact pads on the circuit board. This can impose stresses in the solder that connects the terminals to the contact pads on the circuit board. As disclosed in certain preferred embodiments of U.S. Patents 5,679,977; 5,148,266; 5,148,265; 5,455,390; and 5,518,964, the disclosures of which are incorporated by reference herein, semiconductor chip packages can have terminals that are movable with respect to the chip or other device incorporated in the package. Such movement can compensate to an appreciable degree for differential expansion and contraction.

[0007] Testing of packaged devices poses another formidable problem. In some manufacturing processes, it is necessary to make temporary connections between the terminals of the packaged device and a test fixture, and operate the device through these connections to assure that the device is fully functional. Ordinarily, these temporary connections must be made without bonding the terminals of the package to the test fixture. It is important to assure that all of the terminals are reliably connected to the conductive elements of the test fixture. However, it is difficult to make connections by pressing the package against a simple test fixture such as an ordinary circuit board having planar contact pads. If the terminals of the package are not coplanar, or if the conductive elements of the test fixture are not coplanar, some of the terminals will not contact their respective contact pads on the test fixture. For example, in a BGA package, differences in the diameter of the solder balls attached to the terminals, and non-planarity of the chip

carrier, may cause some of the solder balls to lie at different heights.

[0008] These problems can be alleviated through the use of specially constructed test fixtures having features arranged to compensate for non-planarity. However, such features add to the cost of the test fixture and, in some cases, introduce some unreliability into the test fixture itself. This is particularly undesirable because the test fixture, and the engagement of the device with the test fixture, should be more reliable than the packaged devices themselves in order to provide a meaningful test. Moreover, devices used for high-frequency operation are typically tested by applying high frequency signals. This requirement imposes constraints on the electrical characteristics of the signal paths in the test fixture, which further complicates construction of the test fixture.

[0009] Additionally, when testing packaged devices having solder balls connected with terminals, solder tends to accumulate on those parts of the test fixture that engage the solder balls. This accumulation of solder residue can shorten the life of the test fixture and impair its reliability.

[0010] A variety of solutions have been put forth to deal with the aforementioned problems. Certain packages disclosed in the aforementioned patents have terminals that can move with respect to the microelectronic device. Such movement can compensate to some degree for non-planarity of the terminals during testing.

[0011] U.S. Patents 5,196,726 and 5,214,308, both issued to *Nishiguchi et al.*, disclose a BGA-type approach in which bump leads on the face of the chip are received in cup-like sockets on the substrate and bonded therein by a low-melting point material. U.S. Patent 4,975,079 issued to *Beaman et al.* discloses a test socket for chips in which dome-shaped

contacts on the test substrate are disposed within conical guides. The chip is forced against the substrate so that the solder balls enter the conical guides and engage the dome-shaped pins on the substrate. Sufficient force is applied so that the dome-shaped pins actually deform the solder balls of the chip.

[0012] A further example of a BGA socket may be found in commonly assigned U.S. Patent 5,802,699, issued September 8, 1998, the disclosure of which is hereby incorporated by reference herein. The '699 patent discloses a sheet-like connector having a plurality of holes. Each hole is provided with at least one resilient laminar contact extending inwardly over a hole. The bump leads of a BGA device can be advanced into the holes so that the bump leads are engaged with the contacts. The assembly can be tested, and if found acceptable, the bump leads can be permanently bonded to the contacts.

[0013] Commonly assigned U.S. Patent 6,202,297, issued March 20, 2001, the disclosure of which is hereby incorporated by reference herein, discloses a connector for microelectronic devices having bump leads and methods for fabricating and using the connector. In one embodiment of the '297 patent, a dielectric substrate has a plurality of posts extending upwardly from a front surface. The posts may be arranged in an array of post groups, with each post group defining a gap therebetween. A generally laminar contact extends from the top of each post. In order to test a device, the bump leads of the device are each inserted within a respective gap thereby engaging the contacts which wipe against the bump lead as it continues to be inserted. Typically, distal portions of the contacts deflect downwardly toward the substrate and outwardly away from the center of the gap as the bump lead is inserted into a gap.

[0014] Commonly assigned U.S. Patent 6,177,636, the disclosure of which is hereby incorporated by reference herein, discloses a method and apparatus for providing interconnections between a microelectronic device and a supporting substrate. In one preferred embodiment of the '636 patent, a method of fabricating an interconnection component for a microelectronic device includes providing a flexible chip carrier having first and second surfaces and coupling a conductive sheet to the first surface of the chip carrier. The conductive sheet is then selectively etched to produce a plurality of substantially rigid posts. A compliant layer can be provided on the second surface of the support structure and a microelectronic device such as a semiconductor chip is engaged with the compliant layer so that the compliant layer lies between the microelectronic device and the chip carrier, and leaving the posts projecting from the exposed surface of the chip carrier. The posts are electrically connected to the microelectronic device. The posts form projecting package terminals that can be engaged in a socket or solder-bonded to features of a substrate as, for example, a circuit panel. Because the posts can be movable with respect to the microelectronic device, such a package can substantially accommodate thermal coefficient of expansion mismatches between the device and a supporting substrate when the device is in use. Moreover, the tips of the posts can be coplanar or nearly coplanar.

[0015] Despite all of the above-described advances in the art, still further improvements in making or testing microelectronic packages would be desirable.

SUMMARY OF THE INVENTION

[0016] A microelectronic package has a microelectronic element overlying or mounted to a first surface of a substrate and substantially rigid conductive posts projecting above the first surface or projecting above a second surface

of the substrate remote therefrom. Conductive elements exposed at a surface of the substrate opposite the surface above which the conductive posts project are electrically interconnected with the microelectronic element. An encapsulant overlies at least a portion of the microelectronic element and the surface of the substrate above which the conductive posts project, the encapsulant having a recess or a plurality of openings each permitting at least one electrical connection to be made to at least one conductive post. At least some conductive posts are electrically insulated from one another and adapted to simultaneously carry different electric potentials. In particular embodiments, the openings in the encapsulant at least partially expose conductive masses joined to posts, fully expose top surfaces of posts and partially expose edge surfaces of posts, or may only partially expose top surfaces of posts.

[0017] In one embodiment, the conductive posts project to a first height above at least one of the first or second surfaces, the encapsulant contacts the conductive posts and has a major surface at a second height above the same surface of the substrate above which the conductive posts project, the second height being greater than the first height, and the openings in the encapsulant being openings in the major surface.

[0018] In a particular embodiment, the conductive posts can project above the first surface and the conductive elements can be exposed at the second surface.

[0019] In one embodiment, the first surface can have a first region and a second region extending from the first region. The microelectronic element may overlie the first region, and the posts can be aligned with the second region.

[0020] In a particular embodiment, the conductive posts can project above the second surface and the conductive elements can be exposed at the first surface.

[0021] The major surface of the encapsulant can be a substantially planar surface. The encapsulant can further have a second surface overlying the microelectronic element at a third height above the first surface, the third height being different from the second height, for example, being greater than the second height.

[0022] In one embodiment, the major surface of the encapsulant can be a substantially planar surface which overlies the first and second regions of the first surface at an at least substantially uniform second height therefrom and overlying the microelectronic element.

[0023] In one variation, at least one conductive post can include a tip region remote from the microelectronic element and a second region disposed below the tip region and closer to the substrate. The second region and tip region can have respective concave circumferential surfaces. The at least one post can consist essentially of metal and have a horizontal dimension which is a first function of vertical location in the tip region and which is a second function of vertical location in the second region.

[0024] In one embodiment, the conductive elements include at least one of conductive posts or masses of conductive bonding material, and a portion of the encapsulant overlies the second surface. Such portion can have a major surface at a height above the second surface and at least one of a recess or one or more openings in the major surface. The recess or the one or more openings can at least partially expose at least one of the conductive elements for electrical connection thereto. At least some of the conductive elements can be electrically insulated from one another and adapted to simultaneously carry different electric potentials.

[0025] In one or more embodiments, surfaces of at least two of the conductive posts or surfaces of at least two conductive masses are at least partially exposed within a single one of the openings.

[0026] A method of making a microelectronic package is provided in accordance with one embodiment. Such method can include providing a microelectronic assembly including a substrate, a microelectronic element mounted to the substrate and substantially rigid conductive posts having top surfaces remote from the substrate. First and second ones of the conductive posts can be electrically connected by conductive features of the substrate to the microelectronic element for carrying a first signal electric potential on the first conductive post and for simultaneously carrying a second electric potential on the second conductive post, the second electric potential being different from the first signal electric potential. An encapsulant layer can then be formed overlying at least a portion of the microelectronic element and covering the top surfaces of the conductive posts. At least one of a recess or one or more openings can then be formed in the encapsulant layer. Each recess or opening can be aligned with at least one of the conductive posts and each recess or opening permitting an electrical connection to be made with at least one of the conductive posts.

[0027] In one embodiment, the encapsulant layer can contact the conductive posts and each recess or opening can at least partially expose at least one of the conductive posts.

[0028] In one embodiment, at least one individual opening can at least partially expose two or more of the conductive posts.

[0029] The microelectronic assembly may further include conductive masses joined with respective ones of the conductive posts. Each recess or opening formed in the encapsulant layer can at least partially expose at least one

of the conductive masses. In a particular embodiment, at least one individual opening may at least partially expose two or more of the conductive masses.

[0030] The encapsulant layer may be formed to have a substantially planar surface, and the recess or opening can extend from or be formed in the substantially planar surface.

[0031] In one embodiment, the conductive posts can have edge surfaces extending away from the top surfaces, and the edge surface of at least one conductive post can be at least partially exposed within at least one of the openings.

[0032] In a particular embodiment, at least first and second microelectronic packages can be made, and then the second microelectronic package can be stacked atop the first microelectronic package and the first and second microelectronic packages be electrically interconnected together using the conductive posts of at least one of the first and second microelectronic packages.

[0033] In a further example, the step of forming the encapsulant layer can include forming first and second substantially planar surfaces of the encapsulant layer above a surface of the substrate. The first surface can overlie at least a portion of the substrate aligned with the microelectronic element and the second surface can overlie another portion of the substrate beyond an edge of the microelectronic element. The first and second surfaces can have different heights from the surface of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1A is a sectional view illustrating a microelectronic assembly through lines 1A-1A of Fig. 1B.

[0035] Fig. 1B is a top plan view illustrating the microelectronic assembly shown in Fig. 1A.

[0036] Fig. 1C is a partial sectional view illustrating a conductive post formed in accordance with an embodiment of the invention.

[0037] Fig. 1D is a partial sectional view illustrating a post according to a variation of the post shown in Fig. 1C.

[0038] Fig. 1E is a partial sectional view illustrating a method of forming a post as shown in Fig. 1D.

[0039] Figs. 1F, 1G, 1H, and 1I are partial sectional views illustrating stages in a fabrication method relating to the forming of posts.

[0040] Fig. 2 is a partial fragmentary sectional view further illustrating a post as shown in Fig. 1I.

[0041] Fig. 3 is a sectional view illustrating a molding stage in a method of fabricating a microelectronic package in accordance with an embodiment of the invention.

[0042] Fig. 4 is a sectional view illustrating a stage of a fabrication method subsequent to the stage shown in Fig. 3.

[0043] Fig. 5 is a sectional view illustrating a microelectronic package in accordance with an embodiment of the invention.

[0044] Fig. 5A is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment of the invention shown in Fig. 5.

[0045] Fig. 5B is a sectional view illustrating a microelectronic package in accordance with a further variation of the embodiment of the invention shown in Fig. 5.

[0046] Fig. 6 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 5.

[0047] Fig. 7 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 5.

[0048] Fig. 8 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 5.

[0049] Fig. 9 is a sectional view illustrating a molding stage in a method of fabricating a microelectronic package in

accordance with a variation of the embodiment shown in Fig. 3.

[0050] Fig. 10 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 6.

[0051] Fig. 11 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 7.

[0052] Fig. 12 is a sectional view illustrating a stacked microelectronic assembly in accordance with an embodiment of the invention.

[0053] Fig. 13 is a sectional view illustrating a microelectronic package in accordance with a variation of the embodiment illustrated in Fig. 8.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0054] Referring to FIG. 1A, in accordance with an embodiment of the present invention, a microelectronic package includes a substrate 100 having a first or top surface 102 adjacent a face 114 of a microelectronic element 110 and a second or bottom surface 104 opposite therefrom. The microelectronic element 110 can be a first semiconductor chip having a front face 113 facing in an upward direction toward the top of the drawing in Fig. 1A and a rear face 114 facing in the opposite, rearward direction. Rear face 114 is generally parallel to front face 113. The directions parallel to front face 113 are referred to herein as "horizontal" or "lateral" directions; whereas the directions perpendicular to the front face are referred to herein as upward or downward directions and are also referred to herein as the "vertical" directions. The directions referred to herein are in the frame of reference of the structures referred to. Thus, these directions may lie at any orientation to the normal or gravitational frame of reference. A statement that one feature is disposed at a greater height "above a surface"

than another feature means that the one feature is at a greater distance in the same orthogonal direction away from the surface than the other feature. Conversely, a statement that one feature is disposed at a lesser height "above a surface" than another feature means that the one feature is at a smaller distance in the same orthogonal direction away from the surface than the other feature.

[0055] The microelectronic element 110 includes active circuit elements which are disposed in a relatively thin layer adjacent the front face 113. The active circuit elements may include devices such as transistors, diodes and other elements, and circuits incorporating the same. Typically, the active circuit elements have dimensions on the order of a few microns or less.

[0056] The substrate 100 includes first conductive posts 106 exposed at a top surface 102 and conductive elements 108 exposed at the second surface 104 of the substrate 100. As used in this disclosure, a conductive element "exposed at" a surface of a dielectric element may be flush with such surface; recessed relative to such surface; or protruding from such surface, so long as the conductive element is accessible for contact by a theoretical point moving towards the surface in a direction perpendicular to the surface.

[0057] In the example shown in Fig. 1A, the conductive elements 108 are conductive pads. The substrate 100 may be flexible, and in one embodiment may be made of a dielectric material such as polyimide. The substrate typically has conductive may also have conductive traces (not shown) that extend over the top surface 102, the bottom surface 104 and/or between the top and bottom surfaces. A microelectronic element 110 such as a semiconductor chip is attached to the first surface 102 of a substrate 100. As seen in Figs. 1A-B, contacts 117 of the microelectronic element can be electrically interconnected with one or more

conductive pads 105 using conductive elements 112 such as wire bonds. In turn, the conductive pads 105 can be connected with conductive posts 106. At least some of the conductive posts are electrically insulated from one another and are adapted to carry different electric potentials, for example, different signals, or different voltages, e.g., power, ground, or a combination thereof. An adhesive 115 can be used for attaching to the substrate 100 a rear face 114 of the microelectronic element 110 opposite the front, i.e., contact-bearing face to the substrate 100.

[0058] When viewed from above the top surface 102 of the substrate, the base 107 of each conductive post can have an area in contact with the bond layer which can be larger than the top surface 126 of the post. The base 107 may have circular, elliptical, oblong or other rectangular or polygonal shape, for example. The top surface 126 may define a tip or apex of the post. The top surface or tip, which is disposed above the top surface 102 of the substrate, can have a smaller area than the base. Typically, the tip has the same shape as the base when viewed from above the top surface 102. The shape of the post is rather arbitrary and may be not only frusto-conical, i.e., a truncated cone which is a part of a cone whose apex is cut off along a face parallel or generally parallel to its bottom face, as shown in the drawings. Alternatively, the conductive posts can have cylindrical, conical, or any other similar shape, such as, for example, a cone with round top or a plateau shape. Furthermore, in addition to or rather than the three dimensional (3D) shape having a circular cross-section, which is called a "solid of revolution", such as the truncated cone, the post 130 may have an arbitrary shape such as any three dimensional shape having a polygonal horizontal cross-section. Typically, the shape can be adjusted by changing the resist pattern, etching conditions or the thickness of

the original layer or metal foil from which the post is formed. Although the dimensions of the post 106 are also arbitrary and are not limited to any particular ranges, often, it may be formed to project from an exposed surface of the substrate 100 by 50 to 300 micrometers, and if the post has the circular cross-section, the diameter may be set in a range of a few tens of microns and greater. In a particular embodiment the diameter of the post can range between 0.1 mm and 10 mm. In a particular embodiment, the material of the post 106 can be copper or copper alloy. The copper alloy can include an alloy of copper with any other metal or metals. The structure and details of fabricating posts and substrates having posts can be as described in United States Patent Publication 2007-0148822.

[0059] Typically, the posts can be formed by etching a layer of metal, e.g., a foil laminated to a substrate, isotropically, with a mask 14 (FIG. 1C) disposed on or above the metal foil such that etching proceeds downwardly from the surface of the metal foil in contact with the mask 14 in a direction of a thickness 10 of the metal foil, i.e., towards the top surface 102 of the substrate below. Etching can proceed until top surface 102 of the substrate 100 is fully exposed between posts such that the top surface 126 (Fig. 1A) of each post has the same height from the top surface 102 of the substrate and the top surfaces 126 are co-planar. The width 12 of the mask 14 typically is greater than a width of the conductive post 106 at the surface in contact with the mask.

[0060] The width 135 (Fig. 2) of the tip can be the same or different in the lateral directions 111, 113 in which the substrate extends. When the width is the same in the two directions, the width can represent a diameter of the tip. Likewise, the width 137 of the base can be the same or different in lateral directions 111, 113 of the metal foil,

and when it is the same, the width 137 can represent a diameter of the base. In one embodiment, the tip can have a first diameter, and the base can have a second diameter, wherein a difference between the first and second diameters can be greater than 25% of the height of the post extending between the tip and base of the post.

[0061] FIG. 1C illustrates a substrate after forming a conductive post 106 by etching completely through a metal foil to expose the underlying substrate 100. In a particular example, the conductive posts can have a height from a few tens of microns and lateral dimensions, e.g., diameter from a few tens of microns. In a particular example, the height and diameter can each be less than 100 microns. The diameter of the posts is less than the lateral dimensions of the conductive pads. The height of each post can be less than or greater than the post's diameter.

[0062] FIG. 1D illustrates an alternative embodiment in which the post 40 is formed with a base having a width 47 which can be narrower in relation to a height 46 of the post than the width 137 (Fig. 1B) of the base when the post is formed as discussed with reference to FIG. 1C. Thus, a post 40 having a greater height to width aspect ratio may be obtained than the post formed as discussed above. In a particular embodiment, the post 40 can be formed by etching portions of a layered structure (FIG. 1E) using a masking layer 48, where the layered structure including a first metal foil 50, a second metal foil 52 and an etch barrier layer 54 disposed between, e.g., sandwiched between the first metal foil and the second metal foil. The resulting post 40 can have an upper post portion 42 and a lower post portion 44 and can have an etch barrier layer 45 disposed between the upper and lower post portions. In one example, the metal foil consists essentially of copper and the etch barrier 45 consists essentially of a metal such as nickel that is not attacked by

an etchant that attacks copper. Alternatively, the etch barrier 45 can consist essentially of a metal or metal alloy that can be etched by the etchant used to pattern the metal foil, except that the etch barrier 45 is etched more slowly than the metal foil. In such manner, the etch barrier protects the second metal foil 52 from attack when the first metal foil is being etched in accordance with masking layer 48 to define an upper post portion 42. Then, portions of the etch barrier 45 exposed beyond an edge 43 of the upper post portion 42 are removed, after which the second metal foil 52 is etched, using the upper post portion as a mask.

[0063] The resulting post 40 can include a first etched portion having a first edge, wherein the first edge has a first radius of curvature $R1$. The post 40 also has at least one second etched portion between the first etched portion and the top surface of the substrate, wherein the second etched portion has a second edge having a second radius of curvature $R2$ that is different from the first radius of curvature. Another way that the post 40 can be described is that each conductive post includes a tip region, remote from the substrate and a second region disposed below the tip region closer to the substrate, the second region and tip region having respective concave circumferential surfaces, and each solid metal post has a horizontal dimension which is a first function of vertical location in the tip region and which is a second function of vertical location in the second region.

[0064] In one embodiment, the upper post portion 42 may be partially or fully protected from further attack when etching the second metal foil to form the lower post portion. For example, to protect the upper post portion, an etch-resistant material can be applied to an edge or edges 43 of the upper post portion prior to etching the second metal foil. Further description and methods of forming etched metal posts similar

to the posts 40 shown in FIG. 1D are described in commonly owned United States Application 11/717,587 filed March 13, 2007 (Tessera 3.0-358 CIP CIP), the disclosure of which is incorporated herein by reference.

[0065] In one example, the starting structure need not include an etch barrier layer sandwiched between first and second metal foils. Instead, the upper post portion can be formed by incompletely etching, e.g., "half-etching" a metal foil, such that projecting portions 32 (Fig. 1F) of the metal foil are defined as well as recesses 33 between the projecting portions where the metal foil has been exposed to the etchant. After exposure and development of a photoresist as a masking layer 56, the foil 58 can be etched as shown in Fig. 1F. Once a certain depth of etching is reached, the etching process is interrupted. For example, the etching process can be terminated after a predetermined time. The etching process leaves first post portions 32 projecting upwardly away from the substrate 100 with recesses 33 defined between the first portions. As the etchant attacks the foil 58, it removes material beneath the edges of masking layer 56, allowing the masking layer to project laterally from the top of the first post portions 32, denoted as overhang 30. The first masking layer 56 remains at particular locations as shown.

[0066] Once the foil 58 has been etched to a desired depth, a second layer of photoresist 34 (Fig. 1G) is deposited onto an exposed surface of the foil 58. In this instance, the second photoresist 34 can be deposited onto the recesses 33 within the foil 58, i.e., at locations where the foil has been previously etched. Thus, the second photoresist 34 also covers the first post portions 32. In one example, an electrophoretic deposition process can be used to selectively form the second layer of photoresist on the exposed surface of the foil 58. In such case, the second photoresist 34 can

be deposited onto the foil without covering the first photoresist masking layer 56.

[0067] At the next step, the substrate with the first and second photoresists 56 and 34 is exposed to radiation and then the second photoresist is developed. As shown in Fig. 1H, the first photoresist 56 can project laterally over portions of the foil 58, denoted by overhang 30. This overhang 30 prevents the second photoresist 34 from being exposed to radiation and thus prevents it from being developed and removed, causing portions of the second photoresist 34 to adhere to the first post portions 32. Thus, the first photoresist 56 acts as a mask to the second photoresist 34. The second photoresist 34 is developed by washing so as to remove the radiation exposed second photoresist 34. This leaves the unexposed portions of second photoresist 34 on the first post portions 32.

[0068] Once portions of the second photoresist 34 have been exposed and developed, a second etching process is performed, removing additional portions of the foil 56, thereby forming second post portions 36 below the first post portions 32 as shown in Fig. 1I. During this step, the second photoresist 34, still adhered to first post portions 32, protects the first post portions 32 from being etched again. Thereafter, the first and second photoresist masks 56, 34 can be removed, leaving posts 60 projecting from a major surface of the substrate 100.

[0069] These steps may be repeated as many times as desired to create the preferred aspect ratio and pitch forming third, fourth or nth post portions. The process may be stopped when the substrate 100 is reached, such layer which can act as an etch-stop or etch-resistance layer. As a final step, the first and second photoresists 58 and 34, respectively, may be stripped entirely.

[0070] In such manner, posts 60 (Fig. 1I) having a shape similar to the shape of posts 40 (Fig. 1D) can be formed, but without requiring an internal etch barrier 45 to be provided between upper and lower post portions as seen in Fig. 1D. Using such method, posts having a variety of shapes can be fabricated, in which the upper post portions and lower post portions can have similar diameters, or the diameter of the upper post portion can be larger or smaller than that of a lower post portion. In a particular embodiment, the diameter of the post can become progressively smaller from tip to base or can become progressively larger from tip to base, by successively forming portions of the posts from the tips to the bases thereof using the above-described techniques.

[0071] The posts 60 formed by the above-described process (Figs. 1F-1I) can be as shown in FIG. 2. Each post 60 can have a first portion 32 at or adjacent to a tip region and a second portion 36 underlying the first portion and closer to the substrate surface. A circumferential surface 22 of the first portion 32 and the circumferential surface 24 of the second portion 36 are concave surfaces, and each has a slope or dx/dz which changes at most gradually with position in the Z direction (direction of height above the substrate surface). With respect to each of the circumferential surfaces of the posts described herein (e.g., surface 22, or surface 24, "concave" means that at every height between the boundaries of the circumferential surfaces (e.g., at every height 29 between an upper boundary 19 of the circumferential surface 22 and a lower boundary 21 of that circumferential surface 22, the circumferential surface encloses a smaller diameter 25 than the diameter, at the same height 29, enclosed by a theoretical conical surface defined by a series of straight lines extending between the boundaries. For example, every point on circumferential surface 22 between boundaries 19, 21 lies inward from the theoretical conical

surface 26 defined by a series of straight lines extending through the boundaries 19, 21.

[0072] Instead of forming posts by etching, as in the above-described processes, it is also possible to form posts by a plating process in which a sacrificial layer such as a photoresist layer is deposited on the top surface of the substrate, after which openings are formed therein by photolithography. The openings define the locations at which a metal can be plated to form the posts. Typically the posts formed by this method have uniform cross-section from base to tip, and can be cylindrical in shape, for example.

[0073] Referring to FIG. 3, once the posts are formed, the substrate 100 may be placed between top and bottom plates 116, 120 of a mold. The top plate 120 is positioned over the bottom plate 116 for capturing the substrate 100 therebetween. Specifically, the top plate 120 of the mold can be placed in contact with the first surface 102 of the substrate and the bottom plate 116 of the mold can be in contact with the second surface 104 of the substrate 100. The mold top plate 120 can include an inlet 122 that enables a flowable material to be introduced into a cavity 124 defined by the mold bottom plate 116 and the mold top plate 120.

[0074] The top plate 120 of the mold can be pressed against a top surface 102 of the substrate to define an interior cavity 124 having a volume. An interior surface 128 of the top plate 120 can be juxtaposed with and spaced apart from top surfaces 126 of the conductive posts 106. The bottom plate 116 can provide counter-force against the substrate 110 during the molding process. Then, a curable, flowable material such as a curable encapsulant can be introduced into the cavity 124 of the mold through the inlet 122. The curable encapsulant may be clear, opaque or have optical properties anywhere along the scale between clear and opaque. For example, the

encapsulant may be clear when the microelectronic element 110 includes active devices which emit or receive visible wavelength spectra. The curable material is preferably cured to form a cured encapsulant layer, which preferably provides stability to the package and protects the microelectronic element 110, the conductive wire bonds 112 and the conductive posts 106.

[0075] Referring to FIG. 4, the top surfaces 126 of the conductive posts 106 extend to a first height H_1 from the top surface 102 of the substrate 100. After molding, the encapsulant 130 can have a major surface 134 at a height H_2 that is sufficient to cover the semiconductor chip 110, the wire bonds 112 and the conductive posts 106. In the particular embodiment shown in FIG. 4, the major surface 134 can be at a uniform height from a first region of the surface 102 to which the microelectronic element is mounted as well as a second region of the surface 102 above which the conductive posts 126 project. The height H_1 of the conductive posts 106 above the top surface 102 of the substrate 100 is less than the height H_2 of the encapsulant major surface, such that top surfaces 126 of the conductive posts are buried below the major surface 134.

[0076] FIG. 5 illustrates a subsequent step of fabrication of microelectronic package 180 in which openings 136 are formed in the encapsulant major surface 134 which at least partially expose conductive posts 106. In one embodiment, the openings 136 can be formed after the encapsulant has been cured. Alternatively, in a variation the openings 136 can be formed after the package is removed from the mold at which time the encapsulant may only be partially cured. In such variation, full curing of the encapsulant can occur after the openings 136 are made therein. As particularly shown in Fig. 5, the openings 136 can be formed so as to at least partially expose the top surface 126 but also at least partially expose edge

surfaces 138 of individual conductive posts. For this purpose, a laser can be used to ablate the encapsulant material above top surfaces of conductive posts 106 so as to form openings 136. Mechanical drilling or etching are other possible ways of forming openings in the encapsulant.

[0077] The openings may be formed so as to fully or partially expose one or more of the conductive posts. In a particular example, at least one of the openings can only partially expose a single conductive post. In this way, the opening can provide a conduit in the encapsulant layer insulating an electrical connection between the conductive post and a corresponding conductive element of a circuit panel or other element, e.g., another microelectronic package, to which the conductive post can be connected.

[0078] In a particular case, an opening may expose more than one conductive post. In one such example, an entire row of posts or a portion of such row can be exposed or partially exposed in one opening of the encapsulant. In another example, a plurality of rows of posts or portions of a plurality of rows of posts can be exposed or partially exposed in one opening in the major surface of the encapsulant. In a particular example, a plurality of conductive posts which are exposed or partially exposed together in a single opening or in respective openings can be connected to one or more conductive elements at the same electric potential, such as for making ground or power connections. However, in one embodiment, a single opening can at least partially expose a plurality of posts which carry different signals so that, for example, a combination of at least two of power, ground or a signal at can be carried simultaneously by at least two posts which are at least partially exposed together within a single opening in the encapsulant. Fig. 5 further illustrates conductive masses, e.g., solder balls 208 being joined with the

conductive pads 108 of the substrate. The solder balls 208 can be aligned with the conductive posts for joining thereto, as will be further described below. The joining of the solder balls with conductive elements, e.g., pads, etc., of a substrate is implicit in the embodiments shown below, unless otherwise noted.

[0079] In a particular embodiment (FIG. 5A) in which at least two posts 106 are at least partially exposed within a single opening 236, a saw can be used to form the opening 236 extending in one or more horizontal directions across the substrate surface 102. In such case, top surfaces 126' of the conductive posts can be exposed within the opening. In particular embodiments, the top surfaces 126' of the conductive posts can be disposed above the surface 238 of the encapsulant layer within the opening, below the surface 238 or can be flush with the surface 238. In the particular embodiment shown in FIG. 5A, opening 236 does not extend horizontally to a peripheral edge of the encapsulant layer, i.e., to peripheral edge 131 of the encapsulant layer as shown in FIG. 5. In one variation as seen in FIG. 5B, a saw or other means can be used to form a recess 336 in the encapsulant layer which does extend to the peripheral edge 131 of the encapsulant layer and which at least partially exposes one or a plurality of the conductive posts 106. In particular embodiments, the top surfaces 126' of the conductive posts 106 can be disposed above the recessed surface 338 of the encapsulant layer, below the recessed surface 338 or which can be flush with the recessed surface 338.

[0080] Fig. 6 shows a variation of the embodiment shown in Fig. 5. In this embodiment, openings 140 are formed in such manner that the top surfaces 126 of the conductive posts 106 are only partially exposed within each opening 140. As seen in Fig. 6, portions 142 of the top surfaces 126 of the posts

lie between the openings 140 and the edge surfaces 138. These portions 142 of the top surfaces of the conductive posts remain buried within the cured encapsulant layer 130 after forming the openings. Moreover, the edge surfaces 138 of the conductive posts are buried within the encapsulant in the embodiment illustrated in Fig. 6.

[0081] Fig. 7 illustrates yet another variation in which conductive masses 144, e.g., a bonding metal such as tin, solder or other bond material, contacts top and edge surfaces 126, 138 of the conductive posts. Openings 146 formed in the cured encapsulant material 130 at least partially expose the conductive masses 144, and may also expose portions of the posts 106.

[0082] Fig. 8 illustrates a microelectronic package 200 according to a variation of the microelectronic package shown in Fig. 5. In this case, the encapsulant 130 is formed to have a plurality of regions which have major surfaces at different heights from the top surface 102 of the substrate 100. As seen in Fig. 8, the encapsulant 130 includes a central region 147 which has a major surface 148 at a height 150 that is sufficient to cover the semiconductor chip 110 and the wire bonds 112. As particularly shown in Fig. 8, the package may include a plurality of microelectronic elements 110, e.g., semiconductor chips which are stacked and electrically connected with conductive elements, e.g., conductive pads of the substrate 100. Alternatively, similar to the embodiment shown in Fig. 5, the microelectronic package may include a single microelectronic element 110.

[0083] The encapsulant 130 also includes a peripheral region 151 that extends from the central region 147 towards peripheral edges 156 of the substrate 100. The major surface 152 of the encapsulant in the peripheral region 151 has a height 154 that is less than height 150 of the encapsulant in

the central region. Typically, the heights of the major surfaces of the encapsulant in the central and peripheral regions 147, 151 are determined by the shape of the top plate 120A of a mold used to form the encapsulant, in a method similar to that shown in Fig. 3. Referring to Fig. 9, to form the central and peripheral regions of the encapsulant material having different heights, the inner surface 128A of the top plate 120A of the mold lies at a greater height from the substrate top surface 102 at locations above the microelectronic element 110 and the wire bonds 112 than inner surface 128B of the top plate 120A lies from the substrate top surface 102 above the conductive posts 106.

[0084] Alternatively, in one variation, the encapsulant layer can be formed with a major surface at a uniform height 150 in both the central and peripheral regions 147, 151, and then a saw or other means can be used to reduce the height of the encapsulant layer in the peripheral region to the lower height 154.

[0085] Fig. 10 illustrates a variation of the microelectronic package shown in Fig. 8, in which the top surfaces of the conductive posts 106 are only partially exposed within openings 140 in the encapsulant material, similar to the embodiment described above with respect to Fig. 6.

[0086] Fig. 11 illustrates a variation of the microelectronic package shown in Fig. 8, in which surfaces of conductive masses 144 joined to conductive posts 106 are at least partially exposed within openings 146 in the encapsulant material, similar to the embodiment described above with respect to Fig. 7.

[0087] FIG. 12 shows the microelectronic package of FIG. 8 stacked on top of other microelectronic packages. Specifically, a first microelectronic package 200A is stacked atop a second microelectronic package 200B, which in turn is stacked atop a third microelectronic package 200C. The third

microelectronic package, in turn, is stacked atop a fourth microelectronic package 200D. The four microelectronic packages are preferably electrically interconnected with one another. Conductive masses 208A, e.g., solder balls, of the first microelectronic package 200A are in contact with the conductive posts 106B of the second microelectronic package 200B. During assembly, the conductive masses 208A can be elevated in temperature so as to at least partially transform into a molten state so that the conductive posts 106B can be at least partially inserted therein and are joined to one another thereby. The temperature of the conductive masses 208A then may be lowered so that the conductive masses re-solidify for permanently connecting the substrate 200A with the substrate 200B through the conductive posts 106B and the conductive masses 208A. The electrical connections between the second microelectronic package 200B and the third microelectronic package 200C are made in a similar fashion, as are the electrical interconnections between the third microelectronic package 200C and the fourth microelectronic package 200D. Typically, joining of the microelectronic packages to form the electrical connections in the assembly is done simultaneously as to all packages therein. However, it can be done as to only a subset of the packages, and then further joining processes then applied to join additional packages or one or more subsets of packages thereto. Although FIG. 12 shows an assembly including four microelectronic packages stacked one atop the other, the present invention contemplates that any size assembly of two or more microelectronic packages may be manufactured. For example, in one embodiment, a stack of five or more microelectronic packages may be possible. The uppermost or lowermost package in the stack may be electrically connected to an external element such as a circuit board or a test board, i.e., through solder balls, other conductive masses or posts, etc.

Optionally, as seen in FIG. 12, the uppermost microelectronic package 200A in the assembly can be made without conductive elements such as conductive posts, conductive masses, etc. being exposed at a top surface 152A of such package 200A. Before the individual microelectronic packages are assembled together in a stack, each package can be individually tested.

[0088] FIG. 13 shows a microelectronic package in accordance with a variation of the embodiment shown in Fig. 8. In this case, conductive masses, e.g., solder balls 218 are exposed at a top surface 102 of the package. An encapsulant layer 130 overlies a face of a microelectronic element or plurality of microelectronic elements 110A, 110B.

[0089] An additional encapsulant layer 230 overlies a bottom surface 104 of the substrate 100, having openings 240 which expose top surfaces 226 of conductive posts 108 which project away from the bottom surface 104 of the substrate 100. Similar to the openings 136 in the encapsulant layer 130 of the above-described embodiment (Fig. 5), the openings 240 can expose the top surfaces 226 of the conductive posts and partially expose the edge surfaces 238 of the conductive posts. Optionally, conductive masses e.g., solder masses, tin, conductive paste, among others, can be joined with surfaces of the conductive posts 108. The microelectronic package 300 illustrated in Fig. 13 can be stacked and joined with one or more other microelectronic packages in a manner similar to that described above with respect to Fig. 12.

[0090] In a variation of the embodiment illustrated in Fig. 13, the conductive masses 218 can be replaced by conductive posts, such as described above. In another variation, the top surfaces 226 of the conductive posts 108 can be only partially exposed within the openings 240, similar to the arrangement of the conductive posts 106 and openings 140 shown and described above with respect to Fig. 6. In yet another variation, surfaces including top surfaces 226 and

edge surfaces 238 of the second conductive posts 108 can be joined with conductive masses prior to placing the assembly into the mold, similar to the arrangement shown and described above with respect to Fig. 7. In such case, the openings 240 at least partially expose the conductive masses joined with the second conductive posts, similar to the arrangement shown in Fig. 8 in which conductive masses 144 are partially exposed within openings 146. Each of these variations can be combined with features shown and described above with respect to any of the foregoing figures. Although the present invention is not limited by any particular theory of operation, it is believed that the planarization of the conductive masses will enable the mass production on a plurality of microelectronic packages, each package having a standard height. The structure shown in any of FIGS 5, 5A, 5B, 6, 7, 8, 10, 11, and 13 may be stacked atop other microelectronic packages to form a stacked assembly, similar to the stacked assembly shown in FIG. 12.

[0091] In another variation of the embodiments described above, a contact-bearing face 113 (Fig. 1A) of the microelectronic element 110 can be placed adjacent the top surface 102 of the substrate 100, and contacts 117 can be juxtaposed in a flip-chip manner with substrate contacts exposed at the top surface 102 of the substrate in alignment therewith, the contacts 117 of the microelectronic element being conductively bonded with contacts exposed at the top surface of the substrate. Such arrangement can be combined with any of the embodiments and variations thereof described in the foregoing. Moreover, in the embodiments shown and described above (Figs. 5, 5A, 5B, 6, 7, 8, 10, 11, and 12), instead of conductive masses 108 projecting away from the substrate bottom surface, the microelectronic package can instead have conductive posts such as described above, or posts which can be combined with conductive masses thereon,

e.g., masses of conductive bonding material such as tin, solder, conductive paste, etc., in their place. Further details of microelectronic packages to which the foregoing described embodiments can be applied include United States Application 11/318,404 filed December 23, 2005 (Tessera 3.0-484), the disclosure of which is incorporated by reference herein.

[0092] The foregoing descriptions of the preferred embodiments are intended to illustrate rather than to limit the present invention. Particular methods of fabricating microelectronic packages and structures therein can be as further described in commonly owned United States Application No. 12/839,038 of Belgacem Haba titled "STACKABLE MOLDED MICROELECTRONIC PACKAGES WITH AREA ARRAY UNIT CONNECTORS" filed July 19, 2010, the disclosure of which is incorporated by reference herein.

[0093] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

1. A microelectronic package comprising:

a substrate having a first surface and a second surface remote from the first surface;

a microelectronic element overlying the first surface;

substantially rigid conductive posts projecting above at least one of the first or second surfaces, the conductive posts having top surfaces remote from the substrate and edge surfaces extending away from the top surfaces;

conductive elements exposed at a surface of the substrate opposite the surface above which the conductive posts project, the conductive elements being electrically interconnected with the microelectronic element; and

an encapsulant overlying at least a portion of the microelectronic element and the surface of the substrate above which the conductive posts project, the encapsulant having a plurality of openings each exposing the top surface and partially exposing the edge surface of at least one of the conductive posts, wherein at least some of the conductive posts are electrically insulated from one another and adapted to simultaneously carry different electric potentials.

2. A microelectronic package comprising:

a substrate having a first surface and a second surface remote from the first surface;

a microelectronic element overlying the first surface;

substantially rigid conductive posts projecting above at least one of the first or second surfaces, the conductive posts having top surfaces remote from the substrate and edge surfaces extending away from the top surfaces;

conductive elements exposed at a surface of the substrate opposite the surface above which the conductive posts project, the conductive elements being electrically interconnected with the microelectronic element; and

an encapsulant overlying at least a portion of the microelectronic element and the surface of the substrate

above which the conductive posts project, the encapsulant having a plurality of openings each partially exposing the top surface of at least one of the conductive posts, wherein at least some of the conductive posts are electrically insulated from one another and adapted to simultaneously carry different electric potentials.

3. A microelectronic package comprising:

a substrate having a first surface and a second surface remote from the first surface;

a microelectronic element overlying the first surface;

substantially rigid conductive posts projecting above at least one of the first or second surfaces, the conductive posts having top surfaces remote from the substrate and edge surfaces extending away from the top surfaces;

conductive masses joined to the conductive posts;

conductive elements exposed at a surface of the substrate opposite the surface above which the conductive posts project, the conductive elements being electrically interconnected with the microelectronic element; and

an encapsulant overlying at least a portion of the microelectronic element and the surface of the substrate above which the conductive posts project, the encapsulant having a plurality of openings each partially exposing at least one of the conductive masses joined to the conductive posts, wherein at least some of the conductive masses are electrically insulated from one another and adapted to simultaneously carry different electric potentials.

4. The microelectronic package as claimed in claim 1, wherein the conductive posts project to a first height above at least one of the first or second surfaces, the encapsulant contacts the conductive posts and has a major surface at a second height above the same surface of the substrate above which the conductive posts project, the second height being

greater than the first height, wherein the openings in the encapsulant are openings in the major surface.

5. The microelectronic package as claimed in claim 2, wherein the conductive posts project to a first height above at least one of the first or second surfaces, the encapsulant contacts the conductive posts and has a major surface at a second height above the same surface of the substrate above which the conductive posts project, the second height being greater than the first height, wherein the openings in the encapsulant are openings in the major surface.

6. The microelectronic package as claimed in claim 3, wherein the conductive masses project to a first height above at least one of the first or second surfaces, the encapsulant contacts the conductive masses and has a major surface at a second height above the same surface of the substrate above which the conductive masses project, the second height being greater than the first height, wherein the openings in the encapsulant are openings in the major surface.

7. The microelectronic package as claimed in claims 4, 5 or 6, wherein the conductive posts project above the first surface and the conductive elements are exposed at the second surface.

8. The microelectronic package as claimed in claim 7, wherein the first surface has a first region and a second region extending from the first region, the microelectronic element overlies the first region, and the posts are aligned with the second region.

9. The microelectronic package as claimed in claims 4, 5 or 6, wherein the conductive posts project above the second surface and the conductive elements are exposed at the first surface.

10. The microelectronic package as claimed in claim 8, wherein the major surface of the encapsulant is a substantially planar surface, the encapsulant further having

a second surface overlying the microelectronic element at a third height above the first surface, the third height being different from the second height.

11. The microelectronic package as claimed in claim 10, wherein the third height is greater than the second height.

12. The microelectronic package as claimed in claim 8, wherein the major surface of the encapsulant is a substantially planar surface overlying the first and second regions of the first surface at an at least substantially uniform second height therefrom and overlying the microelectronic element.

13. The microelectronic package as claimed in claims 4, 5, or 6, wherein at least one conductive post includes a tip region remote from the microelectronic element and a second region disposed below the tip region and closer to the substrate, the second region and tip region having respective concave circumferential surfaces, and the at least one post consisting essentially of metal and having a horizontal dimension which is a first function of vertical location in the tip region and which is a second function of vertical location in the second region.

14. The microelectronic package as claimed in claim 7, wherein the conductive elements include at least one of conductive posts or masses of conductive bonding material, and a portion of the encapsulant overlies the second surface and further has a plurality of second openings, each partially exposing at least one of the conductive elements, wherein at least some of the conductive elements are electrically insulated from one another and adapted to simultaneously carry different electric potentials.

15. The microelectronic package as claimed in claims 4 or 5 wherein surfaces of at least two of the conductive posts are at least partially exposed within a single one of the openings.

16. The microelectronic package as claimed in claim 6, wherein surfaces of at least two of the conductive masses are at least partially exposed within a single one of the openings.

17. A method of making a microelectronic package comprising:

providing a microelectronic assembly including a substrate, a microelectronic element mounted to the substrate and substantially rigid conductive posts having top surfaces remote from the substrate, wherein first and second ones of the conductive posts are electrically connected by conductive features of the substrate to the microelectronic element for carrying a first signal electric potential on the first conductive post and for simultaneously carrying a second electric potential on the second conductive post, the second electric potential being different from the first signal electric potential;

then forming an encapsulant layer overlying at least a portion of the microelectronic element and covering the top surfaces of the conductive posts; and

then forming openings in the encapsulant layer, each opening aligned with at least one of the conductive posts, each opening permitting an electrical connection to be made with at least one of the conductive posts.

18. The method as claimed in claim 17, wherein the encapsulant layer contacts the conductive posts and each opening at least partially exposes at least one of the conductive posts.

19. The method as claimed in claim 18, wherein at least one individual opening at least partially exposes two or more of the conductive posts.

20. The method as claimed in claim 17, wherein the microelectronic assembly further includes conductive masses joined with respective ones of the conductive posts, and each

of the openings formed in the encapsulant layer at least partially exposes at least one of the conductive masses.

21. The method as claimed in claim 20, wherein at least one individual opening at least partially exposes two or more of the conductive masses.

22. The method as claimed in claim 17, wherein the encapsulant layer is formed to have a substantially planar surface, and the openings are formed in the substantially planar surface.

23. The method as claimed in claim 17, wherein the conductive posts have edge surfaces extending away from the top surfaces, and the edge surface of at least one conductive post is at least partially exposed within at least one of the openings.

24. The method as claimed in claim 17, in which at least first and second microelectronic packages are made, further comprising stacking the second microelectronic package atop the first microelectronic package, the first and second microelectronic packages being electrically interconnected together using the conductive posts of at least one of the first and second microelectronic packages.

25. The method as claimed in claim 17, wherein the step of forming the encapsulant layer includes forming first and second substantially planar surfaces of the encapsulant layer above a surface of the substrate, the first surface overlying at least a portion of the substrate aligned with the microelectronic element and the second surface overlying another portion of the substrate beyond an edge of the microelectronic element, the first and second surfaces having different heights from the surface of the substrate.

26. A method of making a microelectronic package comprising:

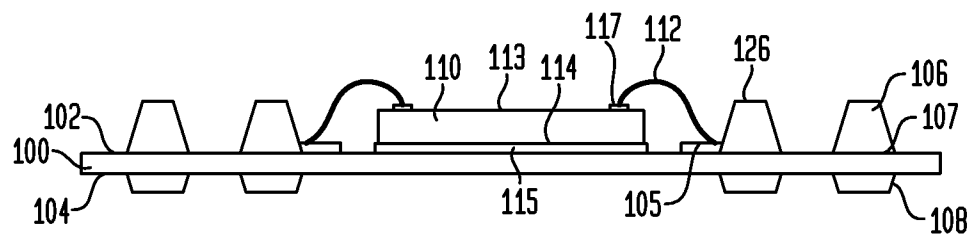
providing a microelectronic assembly including a substrate, a microelectronic element overlying the substrate

and substantially rigid conductive posts having top surfaces remote from the substrate, wherein first and second ones of the conductive posts are electrically connected through the substrate to the microelectronic element for carrying a first signal electric potential on the first conductive post and for simultaneously carrying a second electric potential on the second conductive post, the second electric potential being different from the first signal electric potential;

then forming an encapsulant layer overlying at least a portion of the microelectronic element and covering the top surfaces of the conductive posts; and

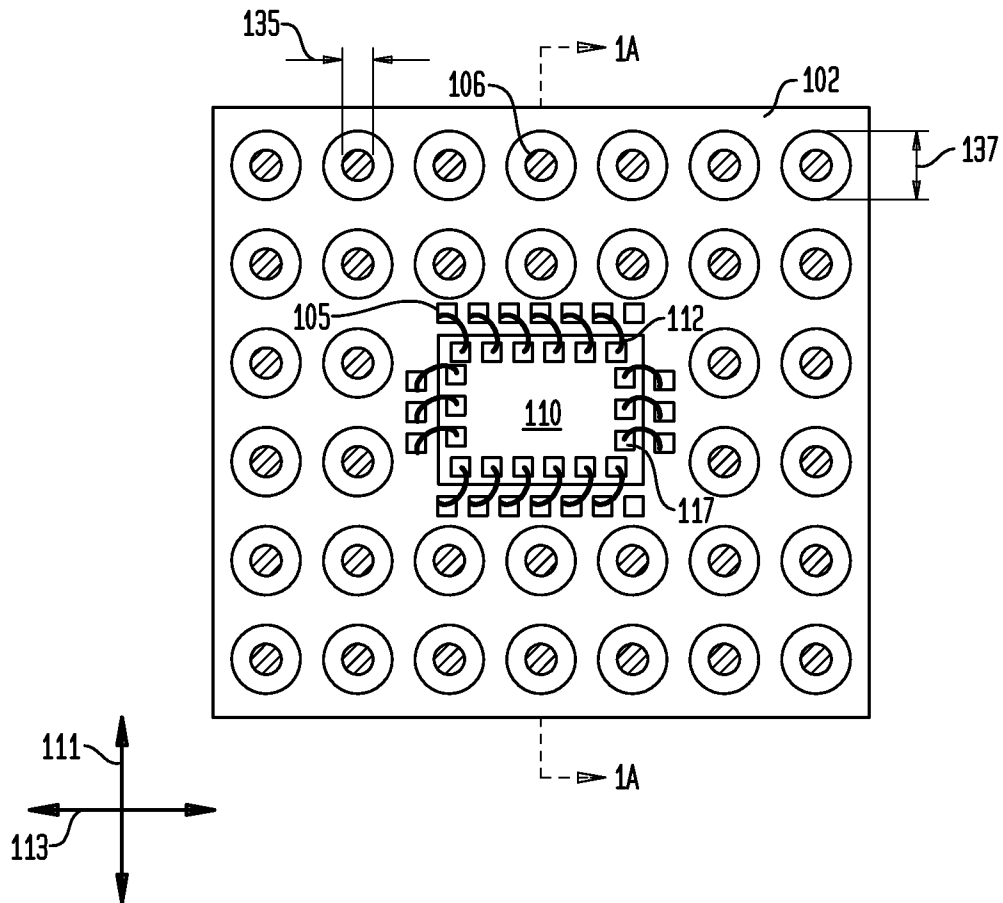
then forming a recess in the encapsulant layer aligned with at least one of the conductive posts, the recess permitting an electrical connection to be made with the at least one conductive post.

FIG. 1A



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FIG. 1B



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FIG. 1C

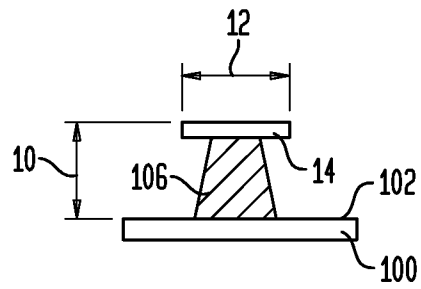


FIG. 1D

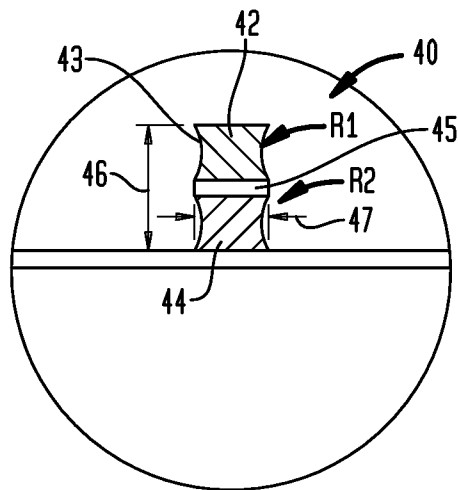
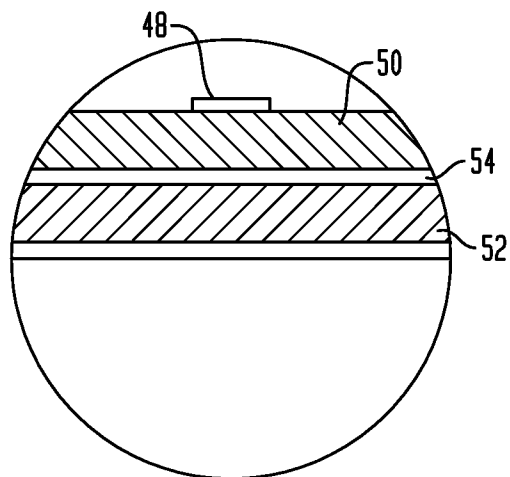


FIG. 1E



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FIG. 1F

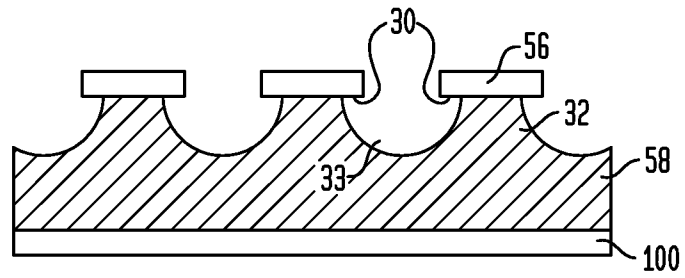


FIG. 1G

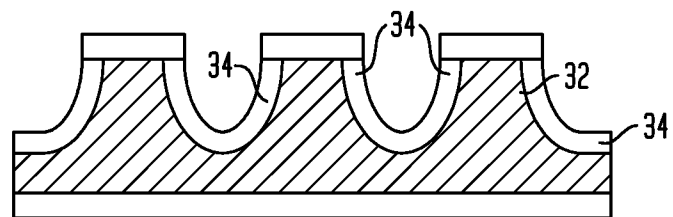


FIG. 1H

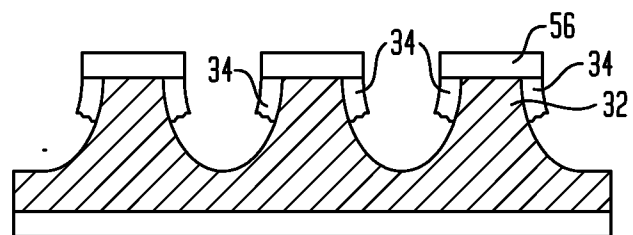


FIG. 1I

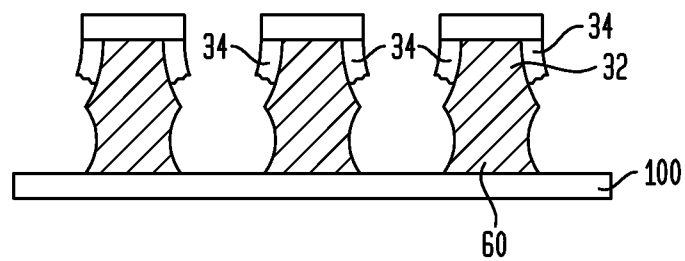


FIG. 2

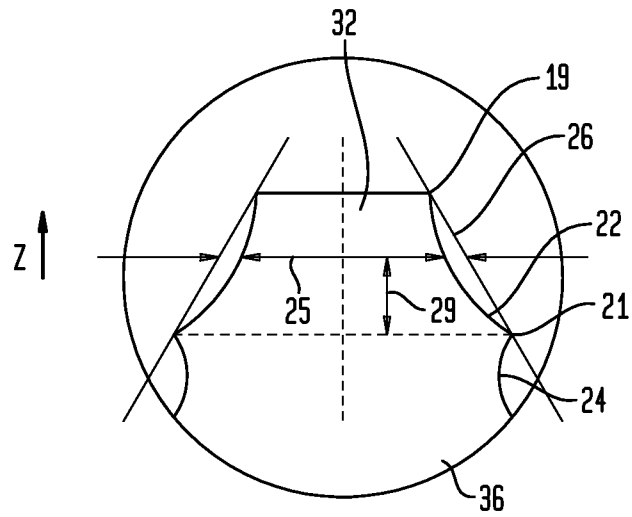
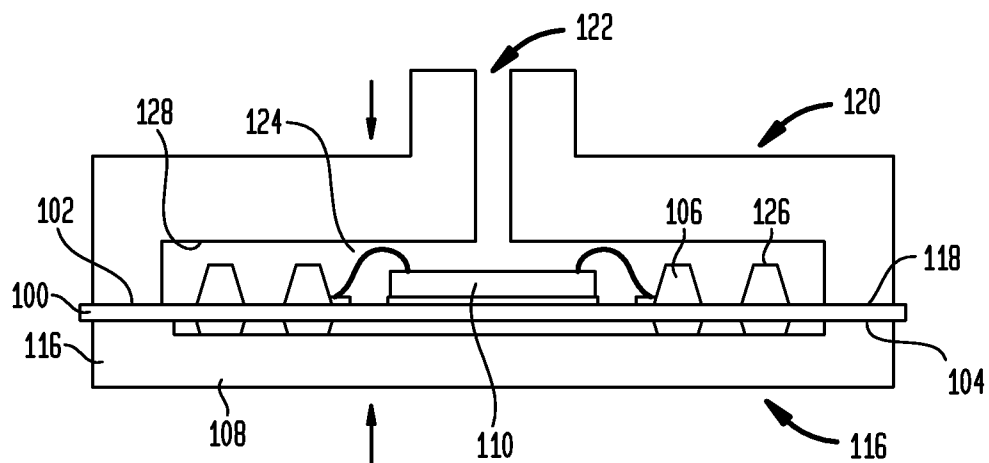


FIG. 3



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FIG. 4

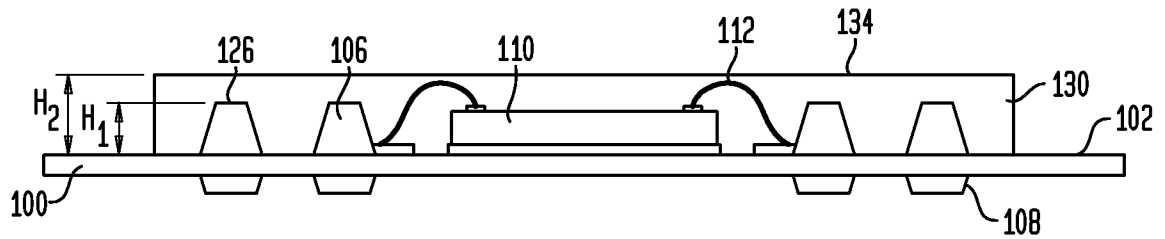


FIG. 5

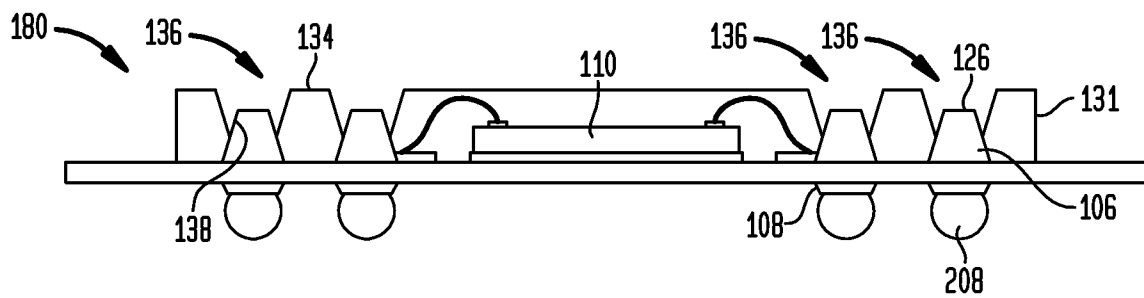


FIG. 5A

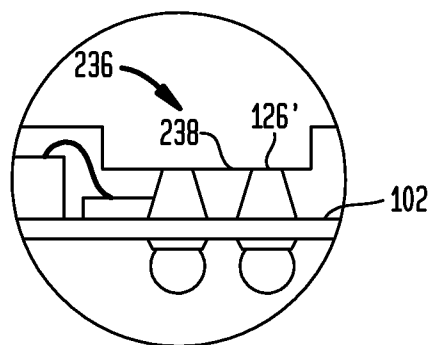


FIG. 5B

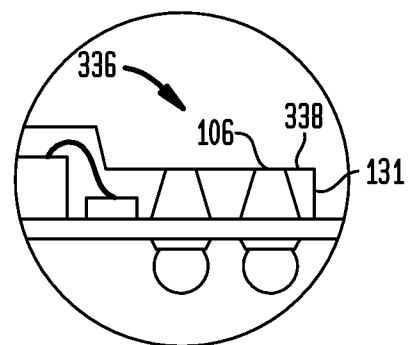
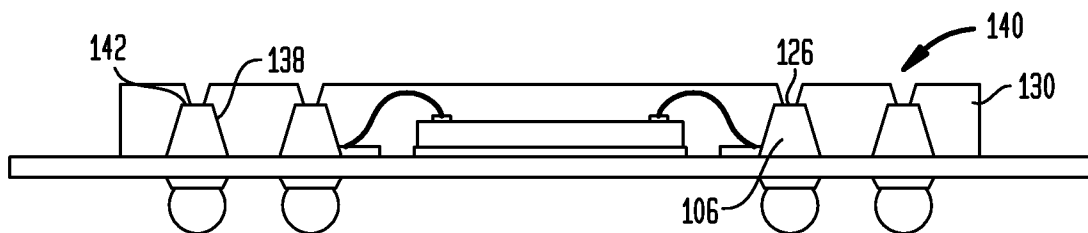


FIG. 6



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FIG. 7

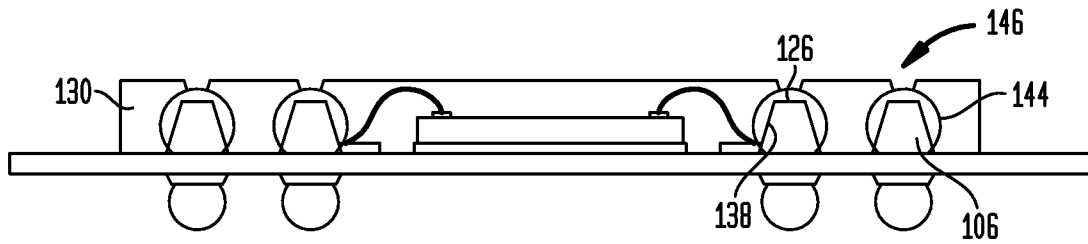


FIG. 8

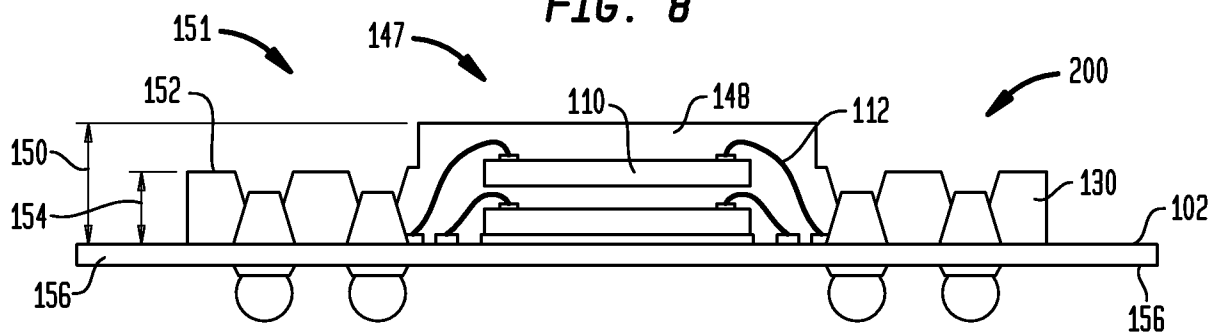


FIG. 9

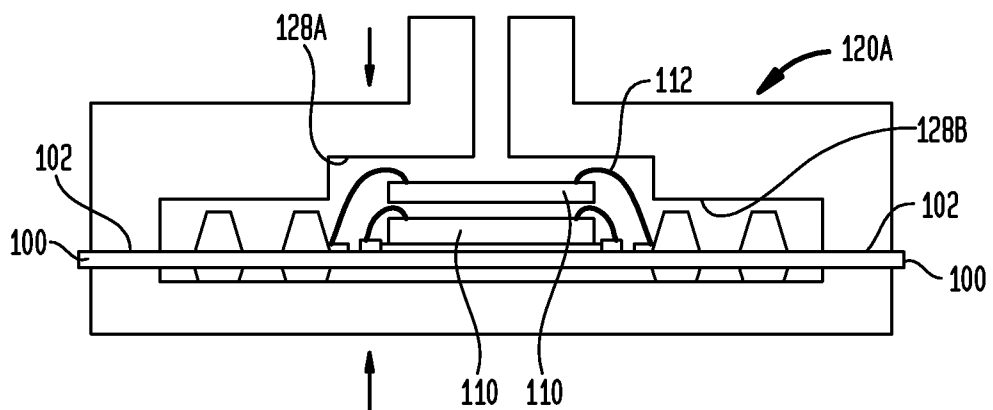


FIG. 10

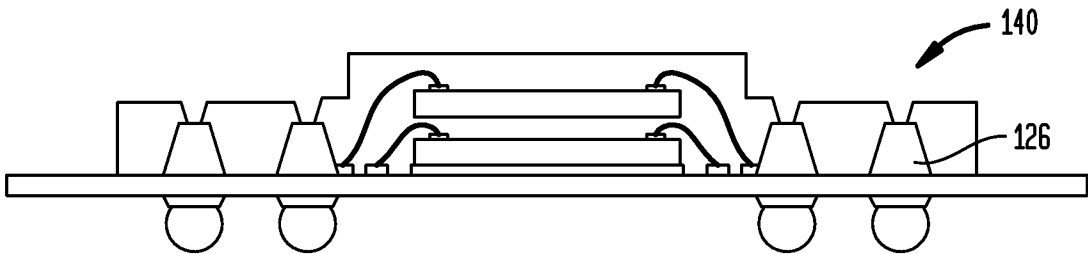
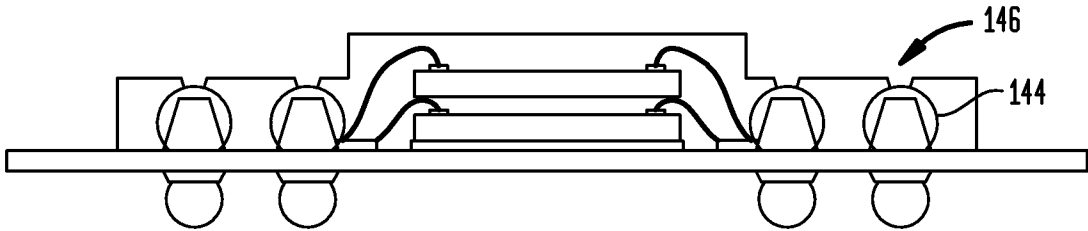


FIG. 11



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FIG. 12

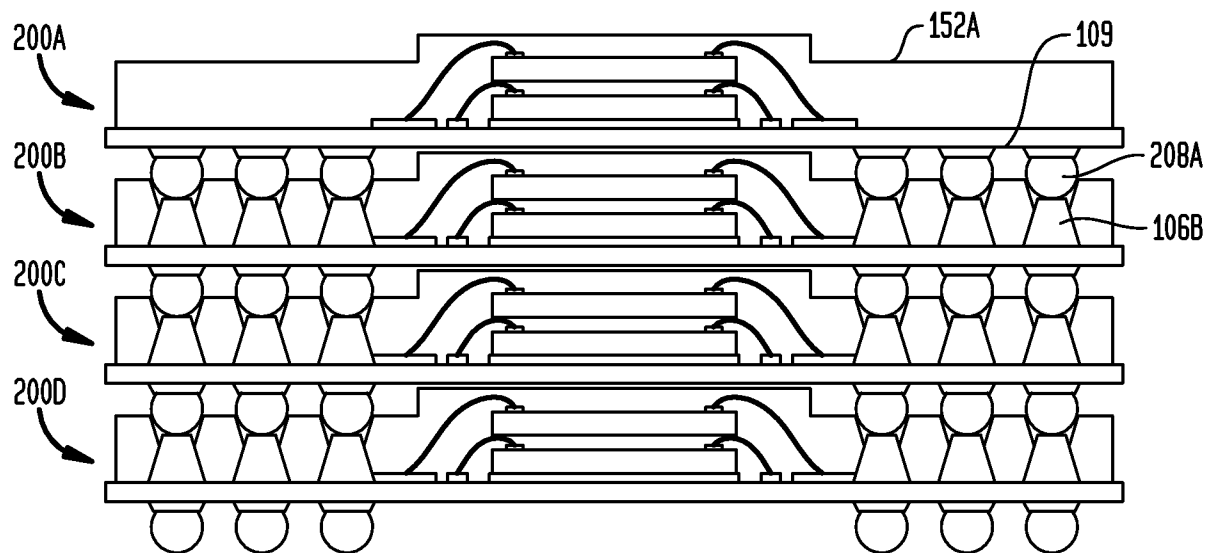


FIG. 13

