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Manber

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[54] **DISPLAY SYSTEM FOR SEVERAL FONTS OF CHARACTERS**

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[52] **U.S. Cl.** ..... **340/324 AD,** 315/22

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** ..... 340/324 AD; 315/19, 22, 315/30

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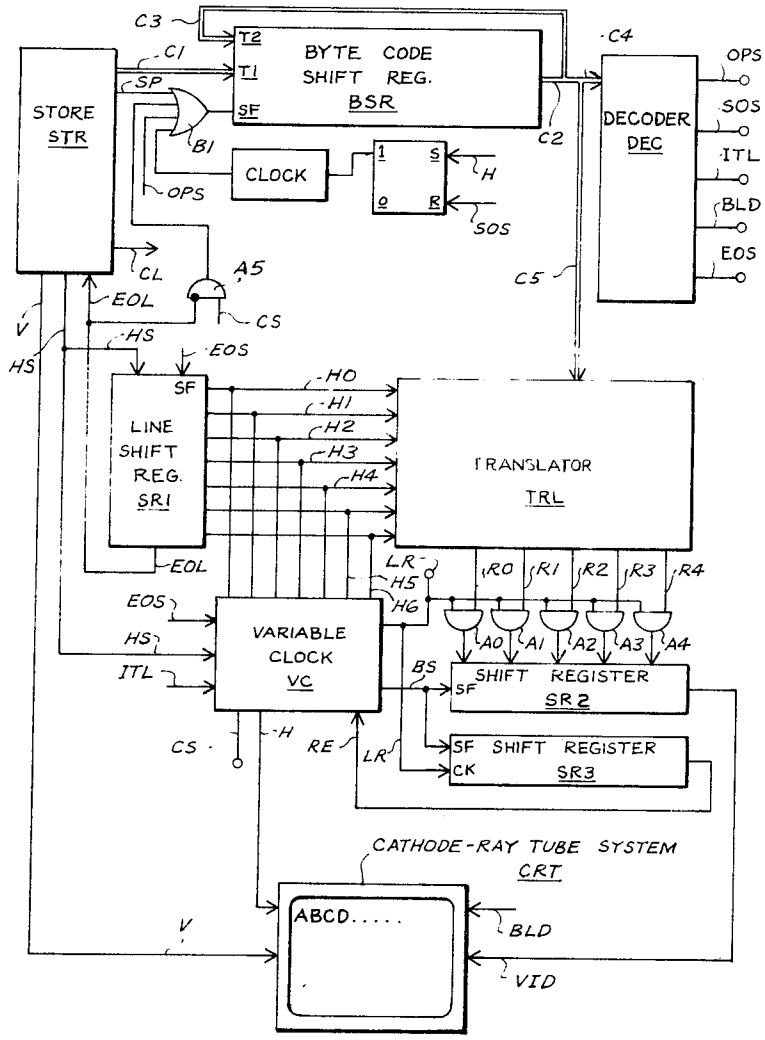
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[57] **ABSTRACT**

In a line raster type display device, characters are produced by generating rows of dots in response to signals. If italics characters are desired then the signals for producing each row of dots are delayed with respect to each other and if bold characters are desired the size of the dots is increased.

10 Claims, 3 Drawing Figures



DISPLAY APPARATUS

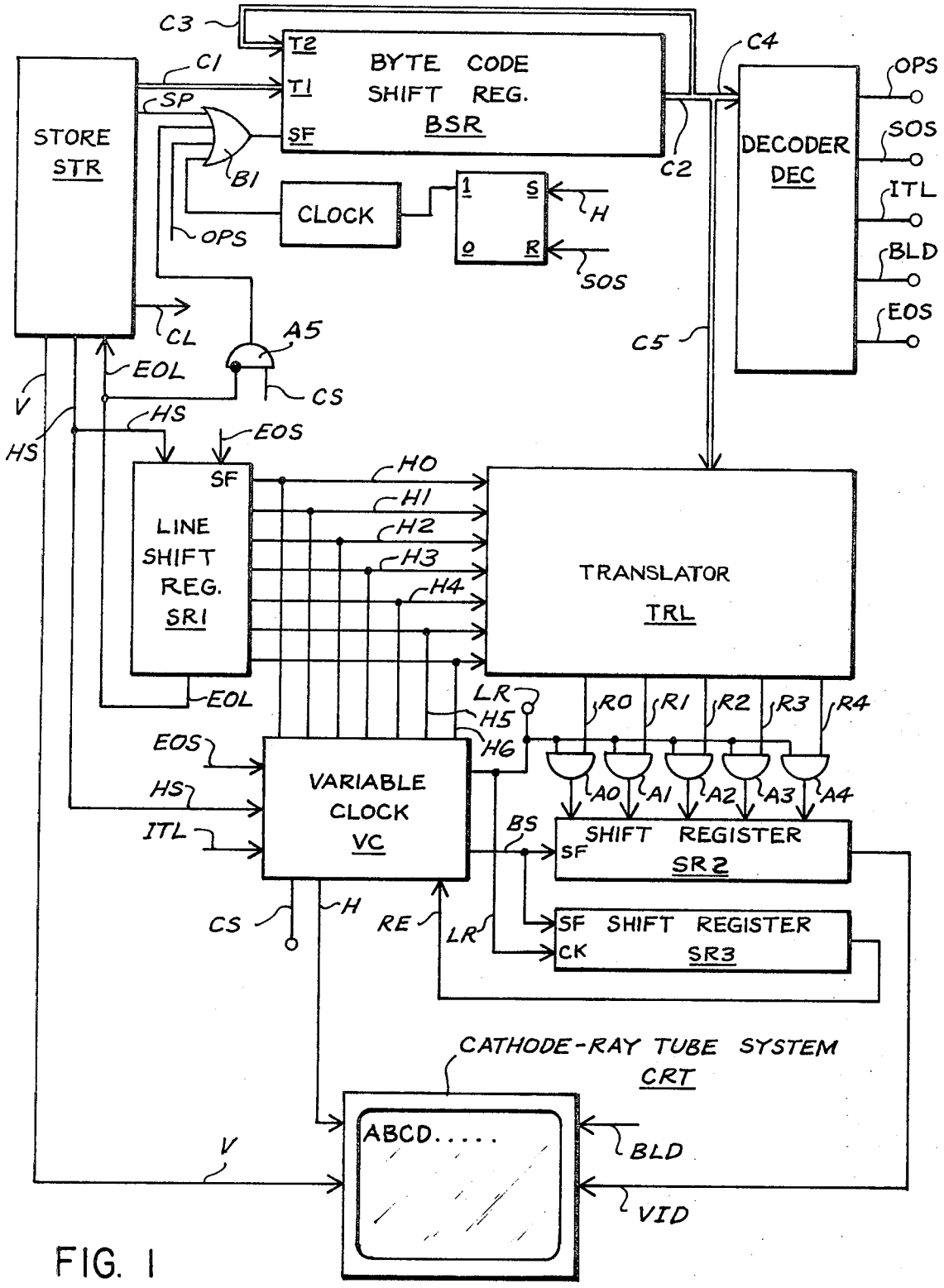
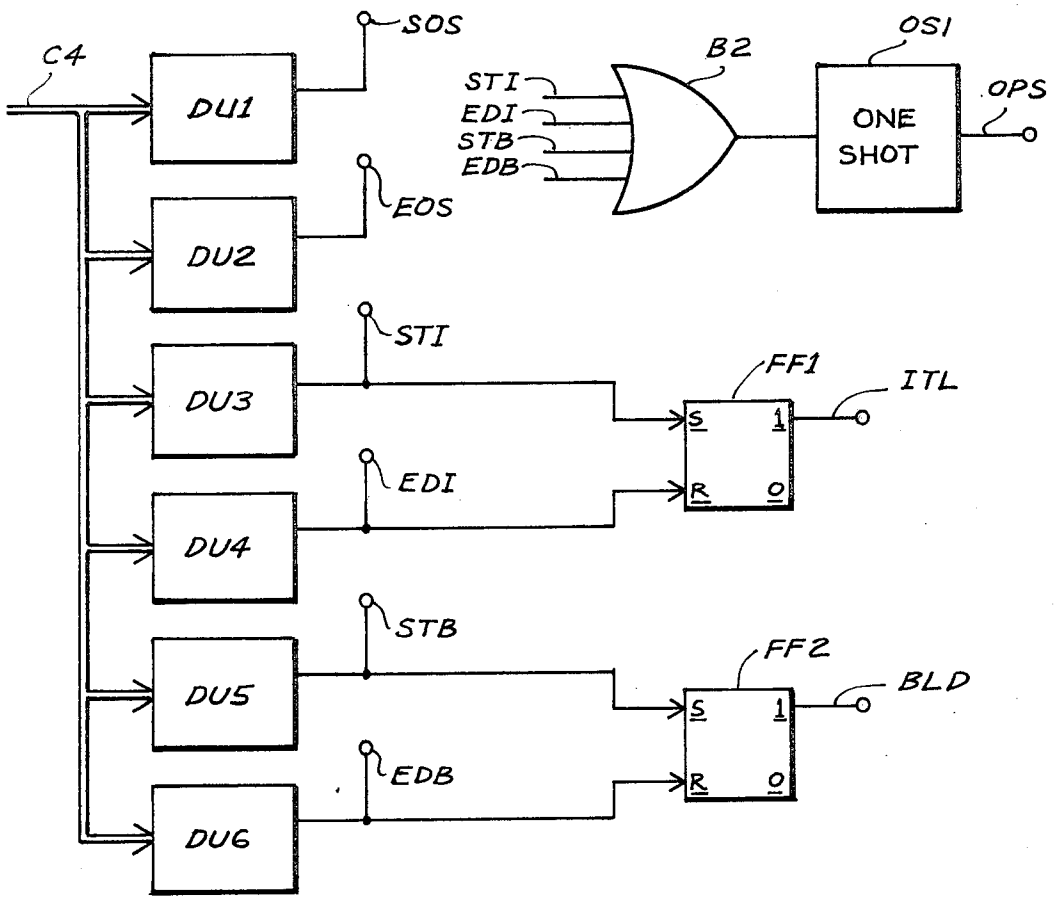


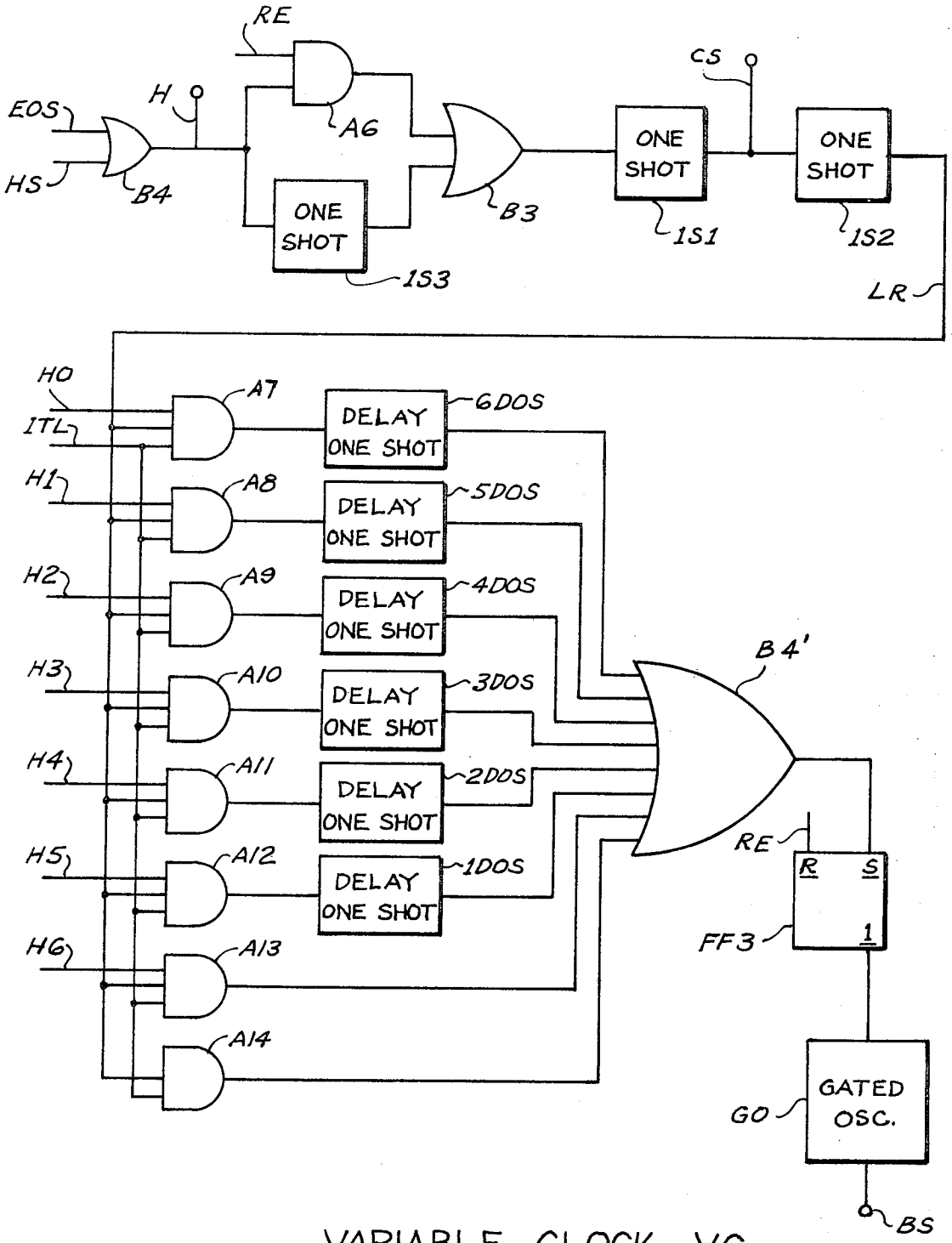
FIG. 1

DISPLAY APPARATUS



DECODER DEC

FIG. 2



VARIABLE CLOCK VC

FIG. 3

DISPLAY SYSTEM FOR SEVERAL FONTS OF CHARACTERS

This invention pertains to character display systems and more particularly to such systems utilizing line raster type scanning techniques.

A very common method of displaying symbols utilizes a cathode-ray tube system wherein the electron beam sweeps out a raster of horizontal lines which are uniformly displaced from each other in a vertical direction on the screen. In such a raster the horizontal lines are scanned at a uniform rate of speed. During the scan of each horizontal line, the beam is turned on and then off at particular points to "paint" dots on the screen. By choosing the points where the beam is turned on, one can construct characters. In fact, this technique it so common that for the set of alphanumeric characters, particular matrices of dots have become standardized. One of the most common is the 5×7 matrix, since it has been found that combinations of these 35 dots arranged in five columns and seven rows can legibly represent at least all 26 alphabetic characters and the 10 numerals. Although other matrices can be used, the following discussion will assume the 5×7 matrix. However, it should be realized the invention also contemplates the other matrices.

Generally, within the system there is provided storage for storing a representation of each dot matrix of the font, the set of alphanumeric symbols or characters to be displayed. If the system is to display another font there must also be provided storage for storing a representation of the dot matrices of this second font. Now, a very common second font is the italics characters. Therefore, if, in a display, one wishes to display both "standard" characters and the italics version of these characters it is necessary to store the fonts of each set. Hence the matrix storage capacity must be doubled. Another type style would be bold characters which would also require storage of its font.

It is a general object of the invention to provide a method and apparatus for displaying several of characters derived from a single stored font.

It is another object of the invention to display a standard character, the italicized version of that character or the bold version of that character using the same representation of the dot matrix of the character.

Other objects, the features and advantages of the invention will be apparent from the following detailed description when read with the accompanying drawing which shows by way of example and not limitation apparatus for implementing the invention while invention is defined in the appended claims.

In the drawing:

FIG. 1 is a block diagram of a display system according to the invention;

FIG. 2 is a logic diagram of the decoder of the system of FIG. 1; and

FIG. 3 is a logic diagram of the variable clock of FIG. 1.

Before describing the display apparatus, the assumed display format will be discussed. The displayed material will be horizontal lines of text on the screen of a cathode-ray tube which is driven in a conventional line -raster scan. Each line of text will start at the same left hand margin, except for controlled indentations or tabulations. Each line will have no more than a fixed number of alphanumerics. Each alphanumeric will be

represented by a 5×7 matrix of dots with a space allotment to one side of the alphanumeric. The possible five dots of any given row of the matrix for each alphanumeric of a line to be displayed, will be written during the same horizontal scan. Seven contiguous sequential scans will be required to write all seven rows of the matrix while the equivalent of about the next two possible horizontal scans of the raster will be blank to provide the space between lines of text. While a cathode-ray tube system is being assumed it should be realized that other raster type display systems such as electrostatic ink jet systems or laser systems could be used.

Generally, the bytes representing the alphanumerics of a line of text will be transmitted from a store to an end-around shift register. When the shift register has been loaded, a horizontal sync pulse is generated to start the first horizontal scan for that line of text. An indication associated with this first horizontal scan and the byte of the first alphanumeric at the output of the shift register are used by a translator to select and generate the dot signals of the top row of this alphanumeric which are loaded in parallel into a five-bit shift register.

A variable clock then generates five shift pulses at the appropriate time to feed the dot signals of the row to the intensity or "video" input of the cathode-ray tube system. The end-around shift register is then shifted one place to present the next alphanumeric for translation. This process continues until the last alphanumeric has been translated for the first time. At this point, the top row of dots of each alphanumeric has been displayed. Another horizontal sync pulse is generated and the process repeated for the second row. This time the translator receives the bytes and an indication associated with the second horizontal scan. This process continues for seven such horizontal scans so that all seven rows of the dot signals for all the alphanumerics of the first line of text are displayed. Then there is a pause to provide a vertical space before the next line of text is displayed. During this pause the bytes of this next line of text are transferred to the end-around shift register. This second line of text is displayed in the same manner as the first but vertically downward displaced therefrom.

Embedded in the character bytes stored in the shift register can be control bytes. For example when a character or a string of characters is to be italicized the character or characters is bracketed by a start italics control byte and an end italics control byte. When the start italics control byte is at the output of the shift register it is sensed by a decoder which sends an italics control signal to the variable clock to delay the generation of the five shift pulses by an increment of time which is a function of the row of matrice being generated. For example, the top row has associated with it a delay of six increments of time, the next lower row five increments, the next lower four increments, etc. In this way an italics character can be generated utilizing the same dot matrix as a standard character. Whenever, an end italics control byte is sensed, the italics control signal is terminated.

There can also be embedded in the character bytes start bold and end bold control bytes. If a character or string of characters are to be displayed in bold face they are bracketed by these control bytes. When the start bold control byte is sensed by the decoder it starts generating a bold control signal which is fed to the

cathode-ray tube where it either increases the intensity of the beam and/or defocuses it so that larger sized dots can be generated. When the end bold control byte is sensed the bold control signal terminates. There are also used start of line and end of line control bytes to indicate the start and end of the line or characters.

FIG. 1 shows a system utilizing positive logic for performing these operations. The system includes a store STR which can be a miniprocessor and memory which stores all the bytes representing the text to be displayed as well as the above-mentioned control bytes. Assume the bytes to be coded combinations of 7 bits. Store STR transmits these 7 bits in parallel to 7 line cable **C1.** In addition, store STR when transmitting a byte will emit a shift pulse on line SP to an input of OR-circuit **B1.** Furthermore, at the start of each "page" of text to be displayed store STR emits a vertical sync pulse onto line V, and at the start of each line of text to be displayed it emits a pulse onto line HS and a clear pulse on line CL. Finally, store STR can receive pulses from line EOL indicating that a line of text has been displayed so that it can initiate the transfer of the information for the next line.

The bytes from store STR are received by byte code shift register BSR which can be seven parallel end-around shift registers, say, 70 bits long, i.e., the maximum number of alphanumerics that can be displayed on a line. The bytes from store STR are received at inputs T1 and transmitted from outputs EX onto seven-line cable C2 as 7 bits in parallel. Seven-line cable C3 feeds the bytes back to inputs T2 to provide the end-around shifting facility. Pulses received at shift input SF from the output of OR-circuit B1 cause the shifting of the bytes.

Decoder DEC, hereinafter more fully described, when detecting the start-of-line control byte emits a pulse on line SOS and when detecting the end-of-line control byte emits a pulse of line EOS. In addition, when decoder DEC detects a start italics control byte its starts transmitting a signal on line ITL until an end italics control byte is sensed. Similarly it starts transmitting a signal on line BLD when a start bold control byte is sensed until an end bold control byte is sensed. The inputs of decoder DEC are connected via seven-line cables C4 and C2 to outputs EX of end-around shift register EASR.

The count of the number of horizontal scans per line of text is performed by row shift register **SR1,** a seven-bit long shift register which is cleared to a bit only in its first stage upon receipt of a pulse on line HS and is shifted one position each time it receives a pulse at shift input SF from line EOS. During such shifting, shift register SR1 successively transmits signals on lines **H0, H1, H2, ... H6,** and EOL. The pulses on lines H0 to H6, connected to translator TRL, are used to select the seven rows of dot signals and to variable clock VC to control the times of shifting. The signal on line EOL, connected to store STR, is used to indicate the entire line has been displayed. Note, that although a shift register has been used to count and record the number of horizontal scans associated with a line of text, one could equally use a modulo-7 counter.

Translator TRL can comprise a read only memory. Each register of the memory can comprise five bits of storage, related to a particular row of the matrix of a particular character. A register is selected by means of the byte received from the outputs EX of byte code shift register BSR via seven-line cables C2 and C5 (associated with the alphanumeric to be displayed) and a signal on one of the lines H0 to H6 (associated with the particular row of dots then to be displayed), whenever the translator TRL cannot select a register its outputs are low. The contents of the selected register are read in parallel, via lines R0 to R4 and AND-circuits A0 to A4, respectively, into shift register SR2.

Shift register SR2 can be a conventional 5-bit shift register wherein the five stages are loaded in parallel from AND-circuits A0 to A4 while shift pulses received at shift input SF connected to line BS sequentially shift the contents out onto line VID. In order to count the number of shifts and to indicate when five shifts has occurred, there is provided 5-bit shift register SR3 whose shift pulse input SF is connected to line BS and whose output is connected to line RE. A pre-setting input is connected to line LR such that upon receipt of a pulse therefrom, the first stage is set to "1" and the four remaining stages set to "0." In this way, after the register has been pre-set and five shift pulses occur, a pulse will be emitted onto line RE. Of course, shift register SR3 can be replaced by a modulo-5 counter which is cleared by a pulse on line LR and emits a pulse onto line RE after counting five pulses from line BS.

The shift pulses on line BS are generated by variable clock VC, hereinafter, more fully described in detail. For the present, one needs to know that variable clock VC controllably emits bursts of five shift pulses generally in response to pulses on line RE, i.e., a pulse on line RE results in a burst of five shift pulses on line BS preceded by pulse on line LR which is preceded by a pulse on line CS. The starting time for the burst of five pulses is controlled by signals on lines ITL and H0 to H6. If the ITL signal is absent indicating a standard (unitalicized character) the burst for each line starts at the same time after the signal on line LR. If the ITL signal is present indicating the character is to be italicized, then the burst for each line starts at a different time as will hereinafter become apparent. Whenever the end of a horizontal scan is reached, variable clock VC receives a signal on line EOS for decoder DEC to delay the generation of the pulses on lines CS, LR and BS until the horizontal scan is retraced in response to a signal on line H effectively caused by the signal on line EOS.

Cathode-ray tube system CRT can be a conventional CRT display having horizontal and vertical circuits connected respectively, to lines H and V for generating the horizontal and vertical deflection signals, to control the sweep of the electron beam, video circuits connected to line VID for intensity modulating the electron beam, and intensity for focusing circuits connected to line BLD.

The operation of the system of FIG. 1 will now be described. After the store STR transmits signals on line CL to initialize all registers and flip-flops it transmits a pulse of line V to cathode-ray tube system CRT as a vertical sync pulse; it transmits the bytes of the first line of text to be displayed to byte shift register BSR: and then transmits a pulse on line HS to variable clock VC and to the pre-set input of shift register SR1. The bytes of each line of text are prefixed by a start-of-line control byte and suffixed by an end-of-line control byte. Shift register SR1 is set to its first stage and starts generating a signal on line H0 associated with the first row of the dot matrices. Variable clock VC immediately

transmits a pulse on line H which is received by cathode-ray tube system CRT as a horizontal sync pulse, and which is received at the set input S of flip-flop F1. The setting of flip-flop F1 activates clock CK (a voltage controlled oscillator) to emit shift pulses via OR-circuit B1 to the shift pulse input of shift register BSR which starts shifting until the start-of-line control byte is at its outputs EX. This byte is sensed by decoder DEC which transmits a signal on line SOS to the reset input R of flip-flop F1 which resets and shunts off clock CK. In this way, variable length lines of text can start at the same left margin since the shifting occurs during the horizontal retrace time. Thereafter, variable clock VC transmits a pulse via line CS, AND-circuit A5 and OR-circuit B1 to the shift pulse input SF of shift register BSR causing the first alphanumeric byte to be transmitted from its output to translator TRL. This byte cooperates with the signal on line H0 in translator TRL to select the dot signals for the first (top row) of the dot matrix for the alphanumeric associated with this byte. The dot signals are fed in parallel via lines R0 to R4 to inputs of AND-circuits A0 to A4, respectively. Then, variable clock VC emits a pulse on line LR which gates the dot signals (bits) into shift register SR2 and sets a "1" into the first stage of shift register SR3. Thereafter, variable clock VC transmits five shift pulses to both shift registers. The dot signals are shifted onto line VID and into the cathode-ray tube system CRT to generate the dots for the first row of the matrix for the first symbol of the line. Following the fifth shift pulse, shift registers SR2 and SR3 are empty with the bit in register SR3 fed via line RE to variable clock VC. After a delay, variable clock VC transmits another pulse on line CS resulting in a shift in shift register BSR and the second byte is presented for translation in the same manner as the first byte. The dot signals for the first row of the second byte are gated into the shift register SR2 by another pulse on line LR which also loads thhe "1" bit into the first stage of shift register SR3. Another five shift pulses are generated and the dots of the first row of the second alphanumeric symbol are displayed. This process continues until decoder DEC detects the end-of-line control bit and transmits a signal on line EOS. Note translator TRL cannot translate this byte hence, it will transmit no dot signals. The signal on line EOS steps shift register SR1 which starts transmitting a signal on line H1 associated with the second row of the dot matrices. The signal on line EOS is received by variable clock VC which responds to it in the same manner as the receipt of a signal on line HS, i.e., by generating the signal on line H. The alignment shifting in end-around shift register EASR is performed and thereafter, the second rows of the dot signals are transmitted to cathode-ray tube system CRT in the same manner as the first rows, as described above. The third, fourth, fifth, sixth and seventh rows are similarly generated. After the seventh row has been displayed, shift register SR1 transmits a signal on line EOL which is fed to store STR to indicate that the whole line of text has been displayed. In addition, the signal on line EOL blocks AND-gate A5 to prevent any shifting in shift register BSR.

In order to display the second line of text, store STR must load the new line into shift register EASR and transmit a pulse on line HS. Thereafter, the system operates as described above except that because the vertical deflection is still operating and no new vertical sync pulse is generated, the second line is displayed below the first line.

Now, if, during the display of the characters italicization is called for, a start italics control byte is at the outputs EX of byte code shift register BSR. Decoder DEC senses this byte and starts transmitting a signal, via line ITL, to variable clock VC and transmits a signal via line OPS and OR-circuit B1 to the shift input SF of shift register BSR to present the next byte for translation by translator TRL. The dot code associated with the appropriate line, determined by one of the H0 to H6 signals, of this next byte is loaded into shift register SR2 in the usual manner. Now, if it is the top line of the character the signal on line H0 cooperates with the ITL signal in variable clock so that the five pulses on line BS start six increments of a given time unit after they would normally start. If the second row of dots is being displayed, indicated by a signal on line H1, then the H1 and ITL signals cooperate to cause the pulses on line BS to start five increments of such given time unit after they would normally start. For the third row the delay is four increments. Etc.

The termination of italicizing is indicated by an end italic control byte of the outputs EX of byte code shift register BSR. At that time decoder DEC senses the control byte, terminates the signal on line ITL, and generates a pulse on line OPS which passes through OR-circuit B1 to shift the bytes in shift register BSR.

If bold characters are to be displayed, they are preceeded by a start bold control byte which when at the outputs EX of shift register BSR is decoded by DEC. In response thereto decoder DEC transmits a BLD signal to cathode-ray tube system CRT which increases the possible intensity of the electron beam and can also defocus the beam so that larger diameter dots can be displayed. In addition decoder DEC transmits a pulse onto line OPS to shift the next byte to the output of byte code shift register BSR. When bold characters are to terminate an end bold control byte is shifted to the outputs EX. Decoder DEC senses this byte, terminates the BLD signal causing the electron beam to assume its normal state, and generates a pulse of line OPS which results in a shift of the next byte to the outputs EX of the byte code shift register.

The decoder DEC of FIG. 2 will now be described. The decoder DEC includes six decoding units DU1 to DU6 connected in parallel to the seven lines of cable C4. Each decoding unit is a logic circuit which emits an output when a particular combination of bits is present at its input. It can be a seven input AND-circuit wherein some of the inputs are inverting inputs depending on the bit combination to be decoded. Decoding unit DU1 indicates the start of line control byte by transmitting a pulse signal on line SOS. Decoding unit DU2 indicates the end of line control byte by transmitting a pulse signal on line EOS. Decoding unit DU3 indicates the start of italics control byte by transmitting a pulse signal on line ST1. Decoding unit DU4 indicates the end of italics control byte by transmitting a pulse signal on line EDI. Decoding unit DU5 indicates the start of bold control byte by transmitting a pulse signal on line STB. And decoding unit DU6 indicates the end of bold control byte by transmitting a pulse signal on line EDB.

The italics signal on line ITL is generated by the "1" output of set-reset flip-flop FF1. The set input of flip-flop FF1 is connected to line SI, and the reset input R

of flip-flop FF1 is connected to line EDI. The bold control signal is generated on line BLD connected to the "1" output of set-reset flip-flop FF2. The set S and reset R inputs of flip-flop FF2 are connected to lines STB and EDB, respectively.

The pulse signal for creating shifts when a control byte is sensed is generated on line OPS connected to the output of "one shot" circuits OS1 whose input is connected to the output of OR-circuit B2. The inputs of OR-circuit B2 are connected to lines STI, EDI, STB and EDB so that whenever a signal is on any one of these lines a pulse signal is immediately transmitted onto line OPS.

The variable clock of FIG. 3 will now be described. Basically, the variable clock VC generates the shift pulses for byte code shift register BSR and the loading pulses for shift registers SR2 and SR3 as well as their shift pulses. The clock is best described by starting at the output of OR-circuit B3 which is connected to the trigger input of trailing-edge-triggered one-shot circuits 1S1 whose output is connected to CS and to the trigger input of trailing-edge-triggered one-shot circuit 1S2. Thus, when OR-circuit B3 emits a pulse its trailing edge triggers one-shot IS1 which transmits a shift pulse on line CS. In addition, the trailing-edge of this pulse triggers one-shot 1S2 whose output is connected to line LR. One-shot 1S2 emits a pulse on line LR which samples AND-circuits A0 to A4 (FIG. 1) to load the dot signals into shift register SR2 and to pre-set shift register SR3. In addition, the output of one-shot 1S2 is connected to an input of each of the AND-circuits A7 to A14. AND-circuits A7 to A13 are three-input and circuits whose second inputs are connected to line ITL and whose third inputs are connected respectively, to lines H0 to H6, respectively. 44 The outputs of AND-circuits A7 to A13 are connected respectively, to delay one-shots 6DOS to 1DOS, respectively. Each delay one-shot can be single-shot multivibrator which emits a negative going pulse when triggered. The time constant of delay one shot 1DOS is chosen so that its pulse width is, say, a fraction of the normal dot recording time. This pulse width is the basic increment of delay. Each succeeding delay one shot then has a pulse width which is a multiple of the pulse width of delay one shot 1DOS. The multiple is indicated by the numeric of the reference character, i.e., delay one shot 4DOS generates a pulse having a width 4 times the width of the pulse generated by delay one shot 1DOS.

AND-circuit A14 is a two input AND-circuit whose second input is an inverting input connected to line ITL. The eight inputs of OR-circuit B4 are connected, respectively, to the outputs of delay one shots 6DOS to 1DOS, and AND-circuits A13 and A14. The output of OR-circuit B4 is connected to the set input S of set-reset flip-flop FF3 whose reset input is connected to line RE. The "1" output of flip-flop FF3 is connected to the input of gated oscillator GO whose output is connected to line BS. Oscillator Go can be a pulse generator which is free-running when its input is high and is cut-off when its input is low (a gated multivibrator).

In general, the pulse of line LR, eventually passes through OR-circuit B4' to set flip-flop FF3 (hereinafter described) turning one gated oscillator GO to provide the shift pulses on line BS for shift pulses for shift registers SR2 and SR3 (FIG. 1). After five such pulses a signal is present in line RE connected to the reset input of flip-flop FF3 which resets, terminating the shift pulses.

Generally, the pulse on line RE also passes through AND-circuit A6 to an input of OR-circuit B3 to repeat the cycle. However, at the end of each horizontal scan, there must be a time delay so that no dots are displayed while the beam is driven to the left margin. This is accomplished by connecting the output of OR-circuit B5 to the second (and inverting input) of AND-circuit A6 and via one-shot 1S3 to the second input of OR-circuit B3. One-shot 1S3 when triggered, emits a negative going pulse for a period of time sufficient to permit a horizontal retrace to occur.

The inputs of OR-circuit B5 are connected to lines EOS and HS. Thus, whenever a signal is present on either one of these lines, a pulse is transmitted to line H, one-shot 1S3 is triggered and AND-circuit A6 is blocked causing the generation of a new horizontal scan which is initiated by a retrace and thereafter, the shift pulse cycle can occur.

Now, the passage of the pulse on line LR to the output of OR-circuit B4 is determined by whether an italics character or a standard character is to be displayed.

For a standard character, the signal on line ITL is absent opening AND-circuit A14 and blocking AND-circuits A7 to A13. Thus the pulse of line LR passes undelayed to the set input of flip-flop FF3 and the shift pulses are immediately generated. If an italics character is to be displayed the signal on line ITL is high blocking AND-circuit A14 and permitting AND-circuits A7 to A13. Which of the circuits that will pass the pulse signal on line LR will be determined by which row of dots of the character is being written as determined by which of the lines H0 to H6 is carrying a signal. For example, if the third row from the top is being written, then line H2 is "high" and the pulse signal on line LR passes through AND-circuit A9 to trigger delay one shot 4DOS which generates a negative going pulse whose trailing edge occurs four time increments after being triggered. This trailing edge is positive going signal which passes through OR-circuit B4 to set flip-flop FF3 resulting in the generation of five shift pulses on line BS as described above. A similar analysis holds for the paths through AND-circuits A7 to A12. Note the LR pulse signal passes directly through AND-circuit A13 to flip-flop FF3 without delay during the occurence of the signal on line H6 associated withe the bottom row of dots. Hence this row assumes its normal position while all other rows are successively displaced to the right.

There will now be obvious to those skilled in the art, many modifications and variations satisfying many or all of the objects of the invention but which do not depart from the spirit thereof as defined by the appended claims.

What is claimed is:

1. A system for displaying characters as matrices of dots comprising: a record medium, a source of a beam which when impinging on said record medium changes the visual state of said record medium at the point of impingement, means for generating a line-scanning raster whereby the beam repetitively sweeps across said record medium at a uniform speed, means for storing a different plurality of dot signal representations for each of the characters to be displayed, means for intensity modulating the beam in accordance with received

dot signals to display sets of dots, transmitting means connected to said storing means for transmitting dot signals to said intensity modulating means, and control means for modifying the sets of displayed dots whereby each possible character whose representation is stored as one plurality of dot signal representations can be displayed in different styles, said control means including delay means for relatively delaying the transmission of the dot signals associated with rows of the matrices whereby italics type characters are displayed.

2. The system of claim **1** wherein said control means includes menas for increasing the diameter of the dots being displayed whereby bold style characters are displayed.

3. The system of claim **1** wherein said record medium is the screen of a cathode-ray tube display, said source of the beam is the electrode gun and associated circuits of said cathode-ray tube display, said means for generating the scanning raster is the display, and said control means includes means for changing the focus of the electron gun or the intensity of the beam.

4. The system of claim **1** wherein said control means includes means for counting line scans and said delay means introduces a delay in the transmission of the dot signals which is a function of a line scan count.

5. The system of claim **1** further comprising a first means for sequentially generating groups of coded combinations of bits wherein each coded combination of bits is associated with a character or a character style to be displayed, addressed memory means for storing indicia representing all possible symbols which can be displayed, selection means receiving the groups of coded combination of bits associated with the characters to be displayed for selecting from said addressed memory means in the indicia representing the character associated with the received group and converting the indicia into a parallel array of dot signals, a shift register for receiving in parallel the array of dot signals and transmitting the dot signals serially to said intensity modulating means, shift pulse generating means for generating a plurality of shift pulses for shifting the dot signals through said shift register, and control means responsive to the coded combinations of bits associated with a character style to be displayed for modifying the sets of displayed dots whereby each possible character can be displayed in different styles.

6. The system of claim **5** wherein said control further includes means for increasing the diameter of the dots being displayed whereby bold style characters are displayed.

7. The system of claim **5** wherein said record medium is the screen of a cathode-ray tube display, said source of the beam is the electrode gun and associated circuits of said cathode-ray tube display, said means for generating the scanning raster is the horizontal and vertical deflection circuits of said cathode-ray tube display, and said control means includes means for changing the focus of electron gun or the intensity of the beam.

8. The system of claim **5** wherein said delay means includes means for selectively delaying the operation of said shift pulse generating means.

9. The system of claim **8** wherein said control means includes means for counting line scans and said delay means delays the operations of said shift pulse generating means as a function of a line scan count.

10. A method for displaying an italics character as rows of dots on a raster-line-scanned record medium wherein each dot is generated in response to a pulse signal, comprising the steps of serially generating the group of pulse signals associated with each row and sequentially transmitting each of said groups to a dot generating means such that each row of dots is on a different line of the record medium, the transmission of each of said groups being delayed a different increment of time from a common relative reference time for all of said groups so that the rows of dots are longitudinally displaced from each other on the record medium.

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