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(54) **Method for manufacturing semiconductor device capacitor**

(57) A method of manufacturing a semiconductor device comprises the steps of forming an α-type silicon carbide layer (12) on a first conductive layer (10), serving as a first electrode of a capacitor, and forming a second conductive layer (20), serving as a second electrode of the capacitor, on the α-type silicon carbide layer (12).

FIG. 1

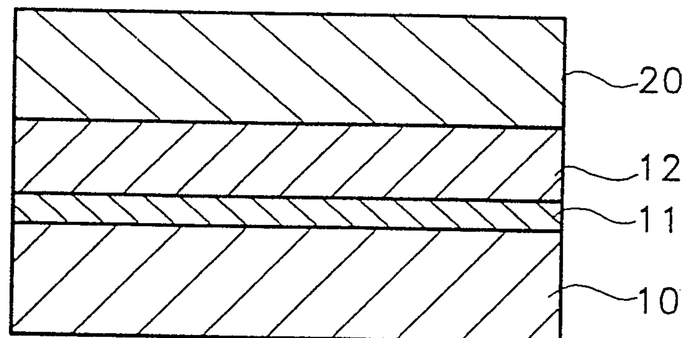

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FIG. 1

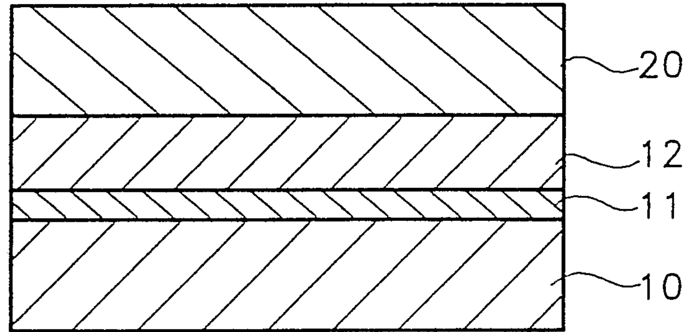
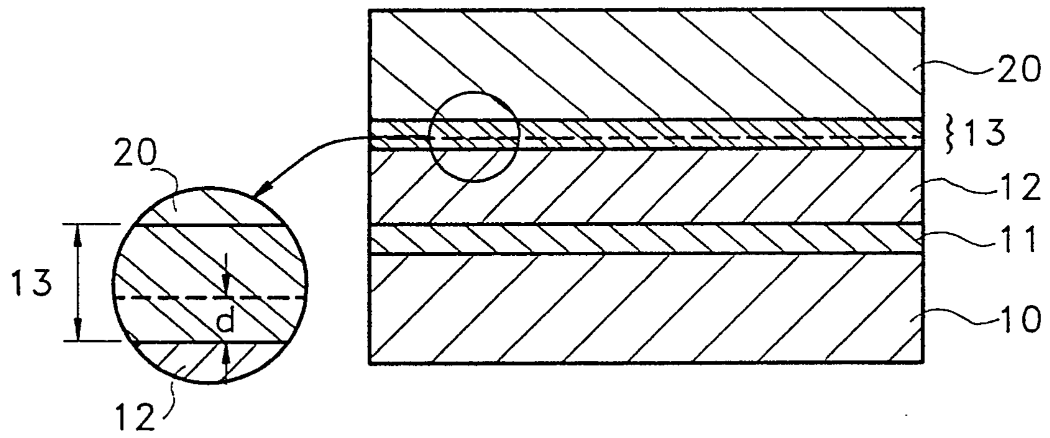


FIG. 2



METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

The present invention relates to a method for manufacturing a semiconductor device, and especially to a method which increases the capacitance of a memory device.

Recently, the development of large capacity memory devices has been progressed along with the development of semiconductor manufacturing methods and extension of the applicable field of memory devices. There has been particularly significant progress in dynamic random access memory (DRAM) devices in which one memory cell consists of one capacitor and one transistor, creating an integration advantage by enabling four times the integration in just three years. Presently, progress in the respective integration density categories is such that the 4Mb DRAM is actively manufactured and the 16Mb is under rapid development for active manufacture, while the 64Mb and 256Mb devices are actively being investigated for development.

Any such semiconductor memory device should possess large capacitance in order reliably to read out and store information. However, when integration density increases by four times, the size of the chip increases by only 1.4, so that relative memory cell size will decrease to one third. Therefore, existing capacitor structures cannot possess the necessary cell capacitance in a limited area. This demands investigation into methods for obtaining larger capacitances

for a given area.

These methods can be divided into three basic techniques: making dielectric layers thinner; increasing the effective area of the capacitor; and the use of materials having large dielectric constants. With reference to the first technique, where the thickness of the dielectric layer is below 100Å, use is limited by the Fowler-Nordheim current, and there are serious problems with reliability, which results in difficulties when applying this technique to a large capacitance memory device.

The second case, i.e., increasing of the capacitor's effective area, shows the greatest development and is classified into stack-type capacitor cells and trench-type capacitor cells according to the integration density, both of which are converted into a three dimensional structure from the conventional planar capacitor cell structure. However, while effective in 4Mb DRAM devices, these methods experience limitations when applied to 16Mb DRAMs. In addition to this, the stack-type capacitor cell has a severe problem with step, because the capacitor is stacked over the transistor. Similarly, the trench type capacitor cell suffers from current leakage between the trenches due to its scaled-down size. Both techniques exhibit problems when applied to 64Mb DRAMs.

Therefore, new capacitor structures such as stack-trench type capacitors, fin-structured capacitors, box-

structured capacitors spread-stack capacitors etc.. are proposed to solve problems in manufacturing large capacity DRAMs. However, due to design rule limitations and complicated processes, these attempts to increase capacitance by improving the structure of the storage electrode are inadequate to achieve the next generation devices which require higher integration density. Therefore, even newer capacitor structures are required.

To meet the requirement, a method is proposed, wherein increased capacitance is attained using the characteristics of the storage electrode material itself and does not depend on improvements of the storage electrode's structure. This method can be understood through "A New Stacked Capacitor Structure Using Hemi-Spherical Grain (HSG) Poly-Silicon Electrodes" (H. Watanabe, N. Aoto, S. Adachi, T. Ishijima, E. Ikawa and K. Terada, SSDM, 1990, pp. 873-876) as reported by NEC Co. and "Fabrication of Storage Capacitance-Enhanced Capacitors with a Rough Electrode" (Yoshio Hayashide, Hiroshi Miyatake, Junichi Mitsuhashi, Makoto Hirayama, Takashi Higaki and Haruhiko Abe, SSDM, 1990, pp. 869-872) as reported by Mitsbishi Co. These two reports teach that to increase cell capacitance, surface area of the storage electrode has to be increased, which can be achieved by enlarging the morphology of the polycrystalline silicon used as the storage electrode. In other words, the above investigators noticed that when polycrystalline silicon constituting the storage electrode is deposited using low-

pressure chemical vapor deposition (LPCVD), the surface morphology of the deposited polysilicon exhibits the greatest increase at the phase transition temperature where the amorphous silicon changes to polycrystalline silicon. In this case, however, in addition to the deposition temperature and pressure of the polysilicon, its thickness also plays a major role in changing surface morphology, and so certain applications of this technique to various capacitor structures are impeded. Also, electrostatic concentrations appear, at an inflection point between the HSG grains resulting from the unevenness in the storage electrode's surface, which downgrades the electrical characteristics of the dielectric layer and its reliability.

Therefore, the object of this invention is to provide a method of manufacturing a capacitor which can increase capacitance using a high-dielectric material to solve the problems of conventional techniques as above.

According to the present invention there is provided a method of manufacturing a capacitor of comprising a step of forming an α-type silicon carbide (SiC) layer on a first conductive layer serving as the first electrode, and a step of forming a second conductive layer serving as the capacitor's second electrode, on the α-type SiC layer.

Embodiments of the present invention are described below, by way of example referring to attached drawings, in which:

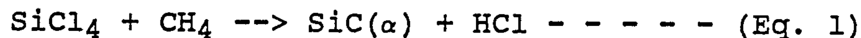
Fig. 1 is a cross-sectional view of a capacitor employing an O/SiC(α)-structured dielectric layer according

to an embodiment of the present invention.

Fig. 2 is a cross-sectional view of a capacitor that employs an O/SiC(α)/SiCxOy-structured dielectric layer according to an embodiment of the present invention.

The dielectric constant of α-type silicon carbide (hereinafter referred to as SiC(α)) is 10.2, superior to an oxide layer by 2.6 times and to a nitride layer by 1.36 times. That is, for a given thickness of the dielectric layer using SiC(α), capacitance will increase 2.6 times as compared with the oxide layer, and 1.36 times over the nitride layer.

The method of manufacturing an SiC(α) layer can be obtained by the reaction equation 1 below.



$$SiCl_4 + CH_4 \rightarrow SiC(\alpha) + HCl \text{ - - - - - - (Eq. 1)}$$

Two methods use an SiC(α) layer obtained through equation 1 as the dielectric layer of the capacitor as shown in Figs. 1 and 2. One method uses only the SiC(α) layer as illustrated in Fig. 1. Fig. 2 shows the other method which uses a SiC(α) layer plus a SiCxOy layer which is obtained by forcibly oxidizing the surface of the SiC(α) layer of Fig. 1.

Referring to Fig. 1, a natural oxide layer 11 about 15Å thick is formed on a first conductive layer 10, such as, for example, an impurity-doped, polycrystalline silicon layer, which is used as the first electrode of a capacitor, followed by a SiC(α) layer 12 of about 70Å which is obtained through

equation 1. On this structure, a second conductive layer 20, for example, another impurity-doped polycrystalline silicon used as the second electrode of the capacitor, is formed.

Referring to Fig. 2 wherein a method using both SiC(α) layer and SiCxOy layer is illustrated, after forming the first conductive layer 10, the natural oxide layer 11 and the SiC(α) layer 12 of approximately 70Å depth as shown in Fig. 1 are formed in cited order and then the SiC(α) layer is forcibly oxidised, creating an SiCxOy layer 13 of approximately 12Å. Subsequently, the second conductive layer 20 is formed on the resultant structure. In Fig. 2, "d" represent the thickness of the SiC(α) layer which was consumed when it was forcibly oxidized.

Table 1, compares the capacitances achieved when the dielectric layer is formed with the SiC(α) layer according to embodiments of the present invention with those obtained via conventional methods wherein the dielectric layer is formed with an oxide nitride oxide (ONO) layer structure, which are generally used for large capacity memory devices. Here, the data is arranged in terms of measured values and expected values, each of which is applied to the stack structure and single stack wrapped (SSW) structure of 16Mb DRAM cell capacitors.

<Table 1>

Method	Capacitor structure	T(dielectric layer) [A]	cell capacitance [fF]
conventional ONO structure (measured values)	stack structure T(N)=70Å	59.5	19.0
	SSW structure T(N)=80Å	68.94	23.8
O/SiC(α) structure (expected values)	stack structure T(Sic(α))=70Å	41.76	30.7
	SSW structure T(Sic(α))=80Å	45.58	36.81
O/SiC(α)/SiCxOy structure (expected values)	stack structure T(Sic(α))=70Å	52.11	24.65
	SSW structure T(Sic(α))=80Å	53.26	31.5

In Table 1, T(N) represents the thickness of the nitride layer, T(SiC(α)) the thickness of the SiC(α) layer and T(dielectric layer) the thickness of the dielectric layer which is interposed between the first and second electrodes of the capacitor. In addition, the O/SiC(α) structure represents the structure composed of the natural oxide layer and the SiC(α) layer as illustrated in FIG.1, while the O/Si(α)/SiCxOy structure represents the structure composed of the natural oxide layer, the SiC(α) layer and the SiCxOy layer as shown in FIG. 2.

It is noted from Table 1 that further improved capacitances can be obtained by using SiC(α) of the present

method as compared with using ONO structure of the conventional method.

Here, the dielectric layer thicknesses of the conventional ONO structure as well as their capacitance are electrically measured values. Expected values of the SiC(α) layer structure of the present invention can be obtained by the following calculations:

$$C = \epsilon \frac{A}{T\ (\text{dielectric layer})}$$

where, C = capacitance,

ϵ = dielectric constant ($\epsilon o \times \epsilon r$)

A = electrode surface area, and

T (dielectric layer) = the thickness of dielectric layer

Since A x ($\epsilon o \times \epsilon r$) is constant for a determined capacitor structure and dielectric layer, capacitance can be obtained for a given thickness of the dielectric layer. For example,

1) For an O/SiC(α) structure and stack structure,

T(SiC(α)) = 70Å

$$\begin{aligned} T(\text{dielectric layer}) &= T(\text{natural oxide layer}) + T(SiC(\alpha)) \\ &= 15Å + \frac{3.9}{10.2}\ 70Å \\ &= 41.76Å \end{aligned}$$

then,

C = 30.7 fF/cell

2) For an O/SiC(α) SiCxOy structure (when the forcibly oxidized layer is formed to about a 12Å thickness) and stack structure.

T(SiC(α)) = 70Å

T(dielectric layer) = T(natural oxide layer) + T(SiC(α))
+ T(SiCxOy)

$$= 15Å + \frac{3.9}{10.2}(70Å - 4.32Å) + 12Å$$

= 52.11Å

then,

C = 24.65 fF/cell

Here, the figure 4.32Å approximates the consumed thickness of the SiC(α) layer when forced to oxidize.

In the above example, the capacitor's second electrode is a polycrystalline layer doped with impurities after polycrystal silicon layer was deposited followed by a process of ion implantation. However, when impurities are ion-implanted, they can infiltrate the dielectric layer, and lower the electrical characteristics of the dielectric layer. To prevent this, an insitu-doped polycrystalline silicon layer may be used.

As described above, the method of manufacturing a capacitor in accordance with the present invention is to use a high-dielectric material SiC(α) as the capacitor's dielectric layer to increase memory cell capacitance. In addition, a margin of error is obtained for the process, because a very thin dielectric layer is not required

when materials of a low dielectric constant are used as the dielectric layer, which enables an increased yield as compared with the conventional method.

CLAIMS:

1. A method of manufacturing a semiconductor device comprising the steps of:

forming an α-type silicon carbide layer on a first conductive layer, said first conductive layer serving as a first electrode of a capacitor; and

forming a second conductive layer serving as a second electrode of said capacitor, on said α-type silicon carbide layer.

2. A method of manufacturing a semiconductor device as claimed in claim 1, further comprising forming a forcibly oxidized silicon carbide layer by forcibly oxidizing the upper portion of said α-type silicon carbide layer.

3. A method of manufacturing a semiconductor device as claimed in claim 1 or 2, wherein said α-type silicon carbide layer is obtained by reacting silicon tetrachloride with methane.

4. A method of manufacturing semiconductor device as claimed in any preceding claim, wherein said second conductive layer comprises an in situ-doped polycrystalline silicon layer.

5. A method of manufacturing a semiconductor device substantially as hereinbefore described with reference to Figures 1 and/or 2 of the accompanying drawings.

6. A semiconductor device comprising an α-type silicon carbide layer formed on a first conductive layer, said first conductive layer serving as a first electrode of a capacitor; and a semiconductive layer,

serving as a second electrode of said capacitor formed on said α-type silicon carbide layer.

7. A semiconductor device substantially as hereinbefore described with reference to Figure 1 and/or Figure 2 of the accompanying drawings.

Amendments to the claims have been filed as follows

6. A semiconductor device comprising an α-type silicon carbide layer formed on a first conductive layer, said first conductive layer serving as a first electrode of a capacitor; and

a second conductive layer, serving as a second electrode of said capacitor formed on said α-type silicon carbide layer.

7. A semiconductor device substantially as hereinbefore described with reference to Figure 1 and/or Figure 2 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) H1K (KFL, KGAM)

(ii) Int Cl (Edition 5) H01L

Search Examiner: W A MORRIS

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI

Date of Search: 16 JANUARY 1992]

Documents considered relevant following a search in respect of claims 1-7

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 4897710 (SHARP) see Figure 4	1

SF2(p)

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Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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