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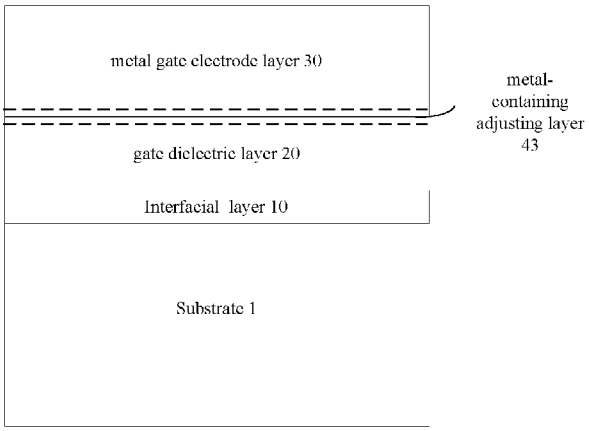



Fig. 3

(57) **Abstract**: A semiconductor structure is provided. The semiconductor structure comprises: a substrate (1); a gate dielectric layer (20) formed on the substrate; a metal gate electrode layer (30) formed on the gate dielectric layer (20); and at least one metal-containing adjusting layer (43) for adjusting a work function of the semiconductor structure, in which an interfacial layer (10) is formed between the substrate (1) and the gate dielectric layer (20), and an energy of bond between a metal atom in the metal-containing adjusting layer (43) and an oxygen atom is larger than that between an atom of materials forming the gate dielectric layer (20) or the interfacial layer (10) and an oxygen atom. Further, a method for forming the semiconductor structure is also provided.

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# SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

## FIELD

The present disclosure relates to a semiconductor manufacturing and design field, and more particularly to a semiconductor structure and a method for forming the same.

## BACKGROUND

In a conventional CMOS process, in order to improve a performance of a device, high k (dielectric constant) gate dielectric materials and metal gate materials are commonly used. Researches show that high k dielectric materials instead of silicon oxide as a gate dielectric of a CMOS device have a dielectric constant higher than that of silicon oxide, so that a gate capacitance may be increased without decreasing a physical thickness of the CMOS device. Therefore, an equivalent oxide thickness (EOT) may be decreased without increasing leakage, thus improving the performance of the device.

However, some problems need to be improved in a process of using high k gate dielectric materials and metal gate materials. For example, an interface state is high, the EOT needs to be further decreased, and a work function needs to be adjusted. However, a dielectric constant of an interfacial layer formed during annealing is low, and a thickness of the interfacial layer is about 1nm, thus preventing the EOT from being further decreased and preventing the performance of the device from being further improved. As for the work function, a use of $TiN/HfO_2$ may meet a requirement of PMOS (the work function being about 5.2eV). However, there is no suitable technology for adjusting the work function of the semiconductor structure without introducing a capping layer to meet a requirement of NMOS (the work function being about 4.2eV). In addition, a thermal stability of high k dielectrics is always a focus. Hafnium based gate dielectric has become a useful dielectric material. However, hafnium oxide may be easily crystallized at about 500°C, thus increasing a device leakage and deteriorating the performance of the device.

## SUMMARY

The present disclosure is aimed to solve at least one of the above mentioned technical problems.

According to an aspect of the present disclosure, a semiconductor structure is provided, comprising: a substrate; a gate dielectric layer formed on the substrate; a metal gate electrode layer formed on the gate dielectric layer; and at least one metal-containing adjusting layer for adjusting a work function of the semiconductor structure, in which an interfacial layer is formed between the substrate and the gate dielectric layer, and an energy of bond between a metal atom in the metal-containing adjusting layer and an oxygen atom is larger than that between an atom in the gate dielectric layer or in the interfacial layer and an oxygen atom.

In one embodiment, the metal-containing adjusting layer is formed in a lower part of the metal gate electrode layer; the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer; one part of the metal-containing adjusting layer is formed in the gate dielectric layer, and the other part of the metal-containing adjusting layer is formed in the metal gate electrode layer; or the gate dielectric layer comprises a first gate dielectric layer and a second gate dielectric layer, and the metal-containing adjusting layer is formed between the first gate dielectric layer and the second gate dielectric layer.

In one embodiment, a metal in the metal-containing adjusting layer is at least one metal selected from a group consisting of Er, Y, Gd, and Al.

In one embodiment, a work function of the metal in the metal-containing adjusting layer for a NMOS semiconductor structure is lower than that of a metal in the metal electrode layer; and a work function of the metal in the metal-containing adjusting layer for a PMOS semiconductor structure is higher than that of the metal in the metal electrode layer.

In one embodiment, the metal-containing adjusting layer is formed by implanting a metal ion, or the metal-containing adjusting layer is formed by atomic layer deposition (ALD) or plasma enhanced chemical vapor deposition (PECVD) process.

In one embodiment, an implanting depth of the metal-containing adjusting layer in a transversal direction of the semiconductor structure is same, here the transversal direction is parallel to a channel of the semiconductor structure; an implanting depth of the

metal-containing adjusting layer in a part of the semiconductor structure near a source region or near a drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in a middle part of the semiconductor structure in the transversal direction thereof; the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source region or near the drain region in the transversal direction of the semiconductor structure is smaller than that of the metal-containing adjusting layer in the middle part of the semiconductor structure in the transversal direction thereof; the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof; or the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof.

In one embodiment, the metal-containing adjusting layer is formed near a source region in a transversal direction of the semiconductor structure; the metal-containing adjusting layer is formed near the source region and in a middle part of the semiconductor structure in the transversal direction thereof; the metal-containing adjusting layer is formed near the source region and a drain region in the transversal direction of the semiconductor structure; or the metal-containing adjusting layer is formed in the middle part of the semiconductor structure in the transversal direction thereof.

According to another embodiment of the present disclosure, a method for forming a semiconductor structure is provided, comprising steps of: providing a substrate; forming a gate dielectric layer by depositing high k dielectric materials on the substrate; forming a metal gate electrode layer by depositing metal gate materials on the gate dielectric layer; forming a metal-containing adjusting layer for adjusting a work function of the

semiconductor structure in the gate dielectric layer and/or the metal gate electrode layer; and annealing the semiconductor structure, in which an interfacial layer is formed between the substrate and the gate dielectric layer, and an energy of bond between a metal atom in the metal-containing adjusting layer and an oxygen atom is larger than that between an atom in the gate dielectric layer or in the interfacial layer and an oxygen atom.

In one embodiment, the metal-containing adjusting layer is formed in a lower part of the metal gate electrode layer; the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer; one part of the metal-containing adjusting layer is formed in the gate dielectric layer, and the other part of the metal-containing adjusting layer is formed in the metal gate electrode layer; or the gate dielectric layer comprises a first gate dielectric layer and a second gate dielectric layer, and the metal-containing adjusting layer is formed between the first gate dielectric layer and the second gate dielectric layer.

In one embodiment, a metal in the metal-containing adjusting layer is at least one metal selected from a group consisting of Er, Y, Gd, and Al.

In one embodiment, a work function of the metal in the metal-containing adjusting layer for a NMOS semiconductor structure is lower than that of a metal in the metal electrode layer; and a work function of the metal in the metal-containing adjusting layer for a PMOS semiconductor structure is higher than that of the metal in the metal electrode layer.

In one embodiment, the metal-containing adjusting layer is formed by implanting a metal ion, or the metal-containing adjusting layer is formed by ALD or PECVD.

In one embodiment, an implanting depth of the metal-containing adjusting layer in a transversal direction of the semiconductor structure is same; an implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near a source region and a drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in a middle part of the semiconductor structure in the transversal direction thereof; the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source

region and the drain region in the transversal direction of the semiconductor structure is smaller than that of the metal-containing adjusting layer in the middle part of the semiconductor structure in the transversal direction thereof; the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof; or the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof.

In one embodiment, the metal-containing adjusting layer is formed near a source region in a transversal direction of the semiconductor structure; the metal-containing adjusting layer is formed near the source region and in a middle part of the semiconductor structure in the transversal direction thereof; the metal-containing adjusting layer is formed near the source region and a drain region in the transversal direction of the semiconductor structure; or the metal-containing adjusting layer is formed in the middle part of the semiconductor structure in the transversal direction thereof.

According to an embodiment of the present disclosure, the work function of the semiconductor structure may be adjusted by implanting metal ions into the semiconductor structure. Meanwhile, the oxygen atoms in the interfacial layer may also be absorbed in the metal-containing adjusting layer, thus thinning the interface layer, increasing the crystallization temperature of the gate dielectric, decreasing EOT (equivalent oxide thickness), and improving the performance of the semiconductor device.

Additional aspects and advantages of the embodiments of the present disclosure will be given in part in the following descriptions, become apparent in part from the following descriptions, or be learned from the practice of the embodiments of the present disclosure.

## BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of the disclosure will become apparent and more readily appreciated from the following descriptions taken in conjunction with the drawings in which:

Fig. 1 is a cross-sectional view of a semiconductor structure according to a first embodiment of the present disclosure;

Fig. 2 is a cross-sectional view of a semiconductor structure according to a second embodiment of the present disclosure;

Fig. 3 is a cross-sectional view of a semiconductor structure according to a third embodiment of the present disclosure;

Fig. 4 is a cross-sectional view of a semiconductor structure according to a fourth embodiment of the present disclosure;

Figs. 5-8 are diagrams showing different implanting depth of a metal ion in a transversal direction of a semiconductor structure according to an embodiment of the present disclosure;

Figs. 9-12 are cross-sectional views of different semiconductor structures with a metal-containing adjusting layer formed in different parts;

Fig. 13 is a flow chart showing a method for forming a semiconductor structure according to an embodiment of the present disclosure;

Fig. 14 is an atom distribution diagram in a semiconductor structure showing a state after an Er ion is implanted and then annealed;

Fig. 15 is a capacitance-voltage curve of a semiconductor structure with and without an Er ion implantation;

Fig. 16 is a schematic showing that an oxygen atom is adsorbed by a metal-containing adjusting layer when a semiconductor structure is annealed;

Fig. 17a is a cross-sectional transmission electron microscopy image of an annealed semiconductor structure with an Er ion implantation;

Fig. 17b is a cross-sectional transmission electron microscopy image of an annealed semiconductor structure without an Er ion implantation; and

Fig. 18 is a flow chart showing a method for forming a semiconductor structure according to another embodiment of the present disclosure.

## DETAILED DESCRIPTION

Embodiments of the present disclosure will be described in detail in the following descriptions, examples of which are shown in the accompanying drawings, in which the same or similar elements and elements having same or similar functions are denoted by like reference numerals throughout the descriptions. The embodiments described herein with reference to the accompanying drawings are explanatory and illustrative, which are used to generally understand the present disclosure. The embodiments shall not be construed to limit the present disclosure.

Various embodiments and examples are provided in the following description to implement different structures of the present disclosure. In order to simplify the present disclosure, certain elements and settings will be described. However, these elements and settings are only examples and are not intended to limit the present disclosure. In addition, reference numerals may be repeated in different examples in the disclosure. This repeating is for the purpose of simplification and clarity and does not refer to relations between different embodiments and/or settings. Furthermore, examples of different processes and materials are provided in the present disclosure. However, it would be appreciated by those skilled in the art that other processes and/or materials may be also applied. Moreover, a structure in which a first feature is “on” a second feature may include an embodiment in which the first feature directly contacts the second feature and may include an embodiment in which an additional feature is prepared between the first feature and the second feature so that the first feature does not directly contact the second feature.

Embodiment 1

Fig. 1 is a cross-sectional view of a semiconductor structure according to a first embodiment of the present disclosure. The semiconductor structure comprises: a substrate 1; an interfacial layer 10 formed on the substrate 1; a gate dielectric layer 20 formed on the interfacial layer 10; a metal gate electrode layer 30 formed on the gate

dielectric layer 20; and a metal-containing adjusting layer 41 formed in a lower part of the metal gate electrode layer 30 for adjusting a work function of the semiconductor structure. In one embodiment, the gate dielectric layer 20 or the metal gate electrode layer 30 may be formed by a conventional technique such as atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD). As used herein, the term "a lower part of the metal gate electrode layer 30" refers to a part of the metal gate electrode layer 30 near the gate dielectric layer 20. In other words, the metal-containing adjusting layer 41 is completely formed in the metal gate electrode layer 30 and connected with the gate dielectric layer 20. An energy of bond between a metal atom in the metal-containing adjusting layer 41 and an oxygen atom is larger than that between an atom of materials forming the gate dielectric layer 20 or the interfacial layer 10 and an oxygen atom. For example, the metal atom may be Er, Y, Gd, or Al. In this way, because the energy of bond between the metal atom in the metal-containing adjusting layer 41 and the oxygen atom is larger than that between the atom of materials forming the gate dielectric layer 20 and the oxygen atom and the energy of bond between the atom of materials forming the gate dielectric layer 20 and the oxygen atom is larger than that between the atom of materials forming the interfacial layer 10, the oxygen atoms may be transferred from the interfacial layer 10 to the gate dielectric layer 20, and the oxygen atoms in the gate dielectric layer 20 may be transferred to the metal-containing adjusting layer 41 to form an oxide with an implanted ion, thus thinning the interfacial layer 10 and decreasing an EOT (equivalent oxide thickness).

In one embodiment, the gate dielectric layer 20 or the metal gate electrode layer 30 may be formed by a conventional technique such as atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD), and the metal-containing adjusting layer 41 may be formed by a technique similar to that for forming the gate dielectric layer 20 or the metal gate electrode layer 30 or the metal-containing adjusting layer 41 may be formed by ion implanting. An accurate control on a transversal position and a thickness of the metal-containing adjusting layer may be

achieved by disposing an ion implantation mask, oblique implantation, and photolithography, thus adjusting the thickness and the position of the metal-containing adjusting layer according to a requirement of the semiconductor structure. The detailed description thereof is omitted here for brevity.

It should be noted that, the thickness of the metal-containing adjusting layer 41 may be set that the oxygen atoms in the interfacial layer may be adsorbed in the metal gate electrode layer partially or completely. Moreover, after the oxygen atoms are absorbed, dielectric constants of metal oxides and/or metal oxygen nitrides corresponding to metals (such as Er, Y, or Gd) and/or metal nitrides (such as AlN) are greater than that of the materials forming the interface layer.

In the following embodiments, the present disclosure will be described by taking ion implantation as an example; however, it would be appreciated by those skilled in the art that the metal-containing adjusting layer 41 is preferably formed by ALD.

In this embodiment, metal ions may be implanted into the metal gate electrode layer 30 by the cathode vacuum arc ion implantation process.

It would be appreciated that at least one metal ion selected from a group consisting of Er, Y, Gd, and Al may be implanted into the metal gate electrode layer 30 so as to form at least one metal-containing adjusting layer 41.

In addition, because the requirements of NMOS and PMOS for the work function are different, the work function of the metal ion implanted into a NMOS semiconductor structure may be different from that of the metal ion implanted into a PMOS semiconductor structure. Particularly, in this embodiment, the metal ion implanted into the NMOS semiconductor structure may be a metal with low work function, such as at least one metal selected from lanthanide metals, thus meeting the requirement of NMOS for the work function.

Embodiment 2

Fig. 2 is a cross-sectional view of a semiconductor structure according to a second embodiment of the present disclosure. The semiconductor structure comprises: a

substrate 1; an interfacial layer 10 formed on the substrate 1; a gate dielectric layer 20 formed on the interfacial layer 10; a metal gate electrode layer 30 formed on the gate dielectric layer 20; and a metal-containing adjusting layer 42. In this embodiment, the metal-containing adjusting layer 42 is similar to the metal-containing adjusting layer 41 in Embodiment 1, except that the metal-containing adjusting layer 42 is formed in an upper part of the gate dielectric layer 20. As used herein, the term “an upper part of the gate dielectric layer 20” refers to a part of the gate dielectric layer 20 near the metal gate electrode layer 30. In other words, the metal-containing adjusting layer 42 is completely formed in the gate dielectric layer 20 and connected with the metal gate electrode layer 30.

Embodiment 3

Fig. 3 is a cross-sectional view of a semiconductor structure according to a third embodiment of the present disclosure. The semiconductor structure comprises: a substrate 1; an interfacial layer 10 formed on the substrate 1; a gate dielectric layer 20 formed on the interfacial layer 10; a metal gate electrode layer 30 formed on the gate dielectric layer 20; and a metal-containing adjusting layer 43. In this embodiment, the metal-containing adjusting layer 43 is similar to the metal-containing adjusting layer 41 in Embodiment 1, except that one part of the metal-containing adjusting layer 43 is formed in the metal gate electrode layer 30 and the other part of the metal-containing adjusting layer 43 is formed in the gate dielectric layer 20.

Embodiment 4

Fig. 4 is a cross-sectional view of a semiconductor structure according to a fourth embodiment of the present disclosure. The semiconductor structure comprises: a substrate 1; an interfacial layer 10 formed on the substrate 1; a gate dielectric layer formed on the interfacial layer 10, in which the gate dielectric layer comprises a first gate dielectric layer 21 and a second gate dielectric layer 22, and a metal-containing adjusting layer 44 is formed between the first gate dielectric layer 21 and the second gate dielectric layer 22; a metal gate electrode layer 30 formed on the second gate dielectric layer 22.

It should be noted that, an implantation depth of the metal ions in a transversal direction of the semiconductor structure may be same or different. The equivalent oxide thickness may be changed by changing the implantation depth, thus modifying a control ability of the semiconductor structure to a channel region of a MOSFET device.

Figs. 5-8 are diagrams showing different implantation depths of a metal ion in a transversal direction of a semiconductor structure according to an embodiment of the present disclosure. It should be noted that in Figs. 5-8, the metal-containing adjusting layer may be formed in at least one layer selected from a group consisting of the interfacial layer 10, the gate dielectric layer 20, and the metal gate electrode layer 30.

As shown in Fig. 5, an implantation depth of a metal-containing adjusting layer 44 in two ends of the semiconductor structure in a transversal direction A (a direction shown by an arrow in Fig. 5) thereof is larger than that of the metal-containing adjusting layer 44 in a middle part of the semiconductor structure in the transversal direction thereof. In this way, a middle part of the interfacial layer 10 is thicker than two ends thereof, thus changing a transversal gate capacitance. Particularly, in this embodiment, a control ability of the semiconductor structure to a channel region may be weakened due to the relative small EOT near the source and drain region, and an influence of the gate on the source and the drain may be reduced, thus alleviating a drain induced barrier lowering (DIBL) effect and reducing leakage.

As shown in Fig. 6, an implantation depth of a metal-containing adjusting layer 45 in a middle part of the semiconductor structure in a transversal direction A (a direction shown by an arrow in Fig. 6) thereof is larger than that of the metal-containing adjusting layer 45 in two ends of the semiconductor structure in the transversal direction thereof. In this way, the middle part of the interfacial layer 10 is thinner than two ends thereof, thus changing a transversal gate capacitance.

The implantation depth of the ions in the middle part of the semiconductor structure in the transversal direction is larger than that of the metal-containing adjusting layer 45 in two ends of the semiconductor structure near a source region and a drain region in the

transversal direction thereof. Therefore, a control ability of the semiconductor structure to a channel region may be strengthened. When a gate voltage is applied, carrier injection or tunneling may be easily achieved in the part of the gate structure near the source region and the drain region, which may be used as a method for achieving multi-bit storage in memory device applications.

As shown in Fig. 7, an implantation depth of a metal-containing adjusting layer 46 in a part of the semiconductor device near a source in a transversal direction A (direction shown by an arrow in Fig. 7) thereof is larger than that of the metal-containing adjusting layer 46 in other parts of the semiconductor structure in the transversal direction thereof. In this way, a part of the interfacial layer 10 near the source is thinned down more, thus changing a transversal gate capacitance. In this embodiment, a control ability of the semiconductor structure to a channel may be strengthened. For a tunneling field effect transistor, a tunneling probability of a carrier in a channel near the source region may be increased, thus increasing a drive current.

As shown in Fig. 8, an implantation depth of a metal-containing adjusting layer 47 in a part of the semiconductor structure near a drain region in a transversal direction A (a direction shown by an arrow in Fig. 8) thereof is smaller than that of the metal-containing adjusting layer 47 in other parts of the semiconductor structure in the transversal direction thereof. In this way, a control ability of the semiconductor structure near the drain region to a channel may be weakened, thus alleviating a drain induced barrier lowering (DIBL) effect and reducing leakage.

Fig. 9 is a cross-sectional view of a semiconductor structure with a metal-containing adjusting layer formed in a part of a second gate dielectric layer 22 near a source region or a drain region. As shown in Fig. 9, a metal-containing adjusting layer is formed in a part of the semiconductor structure near a source region in a transversal direction of the semiconductor structure. Certainly, in other embodiments, the metal-containing adjusting layer may be only formed in a part of the semiconductor structure near a drain region in the transversal direction, or the metal-containing adjusting layer may also be formed in a

middle part and a part of the semiconductor structure near a source, but may not be formed in a part of the semiconductor structure near the drain, as shown in Fig. 10. As shown in Fig. 11, the metal-containing adjusting layer is formed in a part of the semiconductor structure near a source region and a drain region in a transversal direction of the semiconductor structure. As shown in Fig. 12, the metal-containing adjusting layer 44 is formed in a middle part of the semiconductor structure in a transversal direction of the semiconductor structure but is not formed in a part of the semiconductor structure near a source region and a drain region in the transversal direction.

It would be appreciated that the above embodiments shown in Figs. 1-12 are merely illustrative but are not intended to limit the scope of the present disclosure. The implantation depth of metal ions may be adjusted according to practical requirements, which should fall within the scope of the present disclosure.

In order to achieve the above embodiments, a method for forming a semiconductor structure may also be provided. Fig. 13 is a flow chart showing a method for forming a semiconductor structure according to an embodiment of the present disclosure. The method comprises the following steps.

Step S1301, a substrate is provided.

Step S1302, a gate dielectric layer is formed by depositing high k dielectric materials on the substrate. An interfacial layer is formed between the substrate and the gate dielectric layer.

Step S1303, a metal gate electrode layer is formed by depositing metal gate materials on the gate dielectric layer.

Steps S1301 to S1303 may be achieved through conventional technologies. The detailed description thereof is omitted here for brevity.

Step S1304, a metal-containing adjusting layer is formed by implanting metal ions into the metal gate electrode layer. Certainly, in other embodiments, the metal-containing adjusting layer may be also formed by ALD.

Particularly, metal ions may be implanted into the metal gate electrode layer by the cathode vacuum arc ion implantation to form the metal-containing adjusting layer.

An energy of bond between a metal atom in the metal-containing adjusting layer and an oxygen atom is larger than that between an atom of materials forming the gate dielectric layer or the interfacial layer and an oxygen atom. For example, the metal atom may be Er, Y, Gd, or Al. In addition, at least one metal ion may be implanted to form at least one metal-containing adjusting layer in the semiconductor structure.

Step S 1305, the semiconductor structure is annealed.

Moreover, it would be appreciated that, if a position of the implanted metal ions is different, the work function and the equivalent oxide thickness (EOT) will be different. For example, in one embodiment, the metal-containing adjusting layer is formed in a lower part of the metal gate electrode layer. In another embodiment, the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer. In yet another embodiment, one part of the metal-containing adjusting layer is formed in the metal gate electrode layer, and the other part of the metal-containing adjusting layer is formed in the gate dielectric layer.

Fig. 14 is an atom distribution diagram in a semiconductor structure showing a state after an Er ion is implanted and then annealed. As shown in Fig. 14, the Er ions have been implanted into the gate dielectric layer.

Fig. 15 is a capacitance-voltage curve of a semiconductor structure with and without an Er ion atom implanting.. As shown in Fig. 15, the capacitance of the semiconductor structure with Er ion implantation is larger than that of the reference semiconductor structure without Er ion implantation. This suggests that the EOT is decreased for the semiconductor structure with Er ion implantation. In addition, the flat band voltage of the semiconductor structure is shifted to negative direction, which is useful to adjust the work function of the semiconductor structure to meet a requirement of NMOS.

Moreover, for different devices, the implanted ions may be different. For example, for NMOS and PMOS, implanted ions with different work functions may be selected.

Generally, a work function of the metal ion in the metal-containing adjusting layer for a NMOS semiconductor structure is lower than that of a metal ion in the metal electrode layer; and a work function of the metal ion in the metal-containing adjusting layer for a PMOS semiconductor structure is higher than that of the metal ion in the metal electrode layer. Particularly, in one embodiment, lanthanide metal ions are implanted into the NMOS semiconductor structure.

In addition, an implantation depth of metal ions in the transversal direction of the semiconductor structure may also be different, as shown in Figs. 5-8. In one embodiment, different implantation depths may be achieved by oblique implantation or using an implantation hard mask with different thicknesses. The detailed description thereof is omitted here for brevity.

Fig. 16 is a schematic showing that an oxygen atom is adsorbed remotely during a semiconductor structure is annealed. Because the energy of bond between the metal atom in the metal-containing adjusting layer and the oxygen atom is larger than that between the atom of materials forming the gate dielectric layer and the oxygen atom and the energy of bond between the atom of materials forming the gate dielectric layer and the oxygen atom is larger than that between the atom of materials forming the interfacial layer and the oxygen atom, the oxygen atoms may be transferred from the interfacial layer to the gate dielectric layer, and the oxygen atoms in the gate dielectric layer may be transferred to the metal-containing adjusting layer to form an oxide of an implanted ion, thus thinning down the $SiO_x$ interfacial layer significantly. In one embodiment, the semiconductor structure comprises a 34nm-thick TiN/5nm-thick $HfO_2$/1nm-thick $SiO_x$ interfacial layer /Si substrate, the Er atom is implanted into the TiN layer and then annealed at 1000ºC for 30 seconds in $N_2$ atmosphere. After these processing, the thickness of $SiO_x$ interfacial layer is reduced to about 0.6nm. If the same semiconductor structure without Er atom implantation experiences the same annealing, the thickness of $SiO_x$ interfacial layer is increased to about 2.2nm. In order to explain the thickness of the $SiO_x$ layer reduction, the Gibbs free energy change may be introduced. The Gibbs free

energy change ($^{\Delta G^0_{1000}}$) at 1000K has a large positive value when the reaction given by: $Si + MO_x = M + SiO_x$ is satisfied.

In this situation, the material M represents the Hf and Er atom. The $^{\Delta G^0_{1000}}$ (0<47.468(Hf) <122.030(Er)) represents the ability that the material atomic bonding with the oxygen atom is strong or weak. The $^{\Delta G^0_{1000}}$ of Er atom is much larger than that of Hf atom. Therefore, during thermal annealing, the oxygen atoms move from the $SiO_x$ layer to the $HfO_2$ layer and then migrate to the upper region of the $HfO_2$ layer and bottom region of TiN layer containing implanted Er atoms where they react with the Er atoms. The oxidation of Er atom may be a driving force of the reaction, and the oxygen vacancies (Vo) in $HfO_2$ act as media for a cascade reaction of oxygen transfer from the $SiO_x$ layer to the Er atoms.

The metal-containing adjusting layer may not only adjust the work function of the semiconductor structure and decrease EOT, but also may increase the crystallization temperature of a gate dielectric, as shown in Fig. 17a and Fig. 17b. Fig. 17a is a cross-sectional transmission electron microscopy image of an annealed semiconductor structure with an Er ion atom implantation. Fig. 17b is a cross-sectional transmission electron microscopy image of an annealed semiconductor structure without an Er ion atom implantation. As shown in Fig. 17a and Fig. 17b, after the semiconductor structure is annealed at 1000°C, the dielectric layer with Er ion implanting still remains amorphous, and the dielectric layer without Er ion implanting becomes crystalline, so that the crystallization temperature of the dielectric layer may be increased after Er ion implantation. Moreover, it may be seen from Fig. 17a and Fig. 17b that the interfacial layer is significantly reduced.

In order to achieve the above embodiments, another method for forming a semiconductor structure is also provided. Fig. 18 is a flow chart showing a method for forming a semiconductor structure according to another embodiment of the present disclosure. The method comprises the following steps.

Step S1801, a substrate is provided.

Step S1802, a gate dielectric layer is formed by depositing high k dielectric materials on the substrate.

Step S1803, a metal-containing adjusting layer is formed by implanting metal ions into the gate dielectric layer.

In one embodiment, the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer.

Step S1804, a metal gate electrode layer is formed by depositing metal gate materials on the gate dielectric layer.

Step S1805, the semiconductor structure is annealed.

The method shown in Fig. 18 may be substantially the same as that shown in Fig. 13, except that the metal ions are implanted into the gate dielectric layer before the metal gate electrode layer is formed.

According to an embodiment of the present disclosure, the work function of the semiconductor structure may be adjusted by implanting metal ions into the semiconductor structure. Meanwhile, the oxygen atoms in the interfacial layer may also be absorbed in the metal-containing adjusting layer, thus thinning the interface layer, increasing the crystallization temperature of the gate dielectric, decreasing EOT (equivalent oxide thickness), and improving the performance of the semiconductor device.

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that changes, alternatives, and modifications all falling into the scope of the claims and their equivalents may be made in the embodiments without departing from spirit and principles of the disclosure.

**WHAT IS CLAIMED IS:**

1. A semiconductor structure, comprising:

a substrate;

a gate dielectric layer formed on the substrate;

a metal gate electrode layer formed on the gate dielectric layer; and

at least one metal-containing adjusting layer for adjusting a work function of the semiconductor structure,

wherein an interfacial layer is formed between the substrate and the gate dielectric layer, and an energy of a bond between a metal atom in the metal-containing adjusting layer and an oxygen atom is larger than that between an atom in the gate dielectric layer or in the interfacial layer and an oxygen atom.

2. The semiconductor structure according to claim 1, wherein

the metal-containing adjusting layer is formed in a lower part of the metal gate electrode layer;

the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer;

one part of the metal-containing adjusting layer is formed in the gate dielectric layer, and the other part of the metal-containing adjusting layer is formed in the metal gate electrode layer; or

the gate dielectric layer comprises a first gate dielectric layer and a second gate dielectric layer, and the metal-containing adjusting layer is formed between the first gate dielectric layer and the second gate dielectric layer.

3. The semiconductor structure according to claim 1, wherein a metal in the metal-containing adjusting layer is at least one metal selected from a group consisting of Er, Y, Gd, and Al.

4. The semiconductor structure according to claim 1, wherein

a work function of the metal in the metal-containing adjusting layer for a NMOS semiconductor structure is lower than that of a metal in the metal electrode layer; and

a work function of the metal in the metal-containing adjusting layer for a PMOS semiconductor structure is higher than that of the metal in the metal electrode layer.

5. The semiconductor structure according to claim 1, wherein the metal-containing adjusting layer is formed by implanting a metal ion, or the metal-containing adjusting layer is formed by atomic layer deposition, plasma enhanced chemical vapor deposition, or sputtering process.

6. The semiconductor structure according to claim 5, wherein:

an implantation depth of the metal-containing adjusting layer in a transversal direction of the semiconductor structure is same;

an implantation depth of the metal-containing adjusting layer in a part of the semiconductor structure near a source or near a drain in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in a middle part of the semiconductor structure in the transversal direction thereof;

the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source or near the drain in the transversal direction of the semiconductor structure is smaller than that of the metal-containing adjusting layer in the middle part of the semiconductor structure in the transversal direction thereof;

the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof; or

the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the drain region in the transversal direction of the

semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof.

7. The semiconductor structure according to claim 5, wherein:

the metal-containing adjusting layer is formed near a source region in a transversal direction of the semiconductor structure;

the metal-containing adjusting layer is formed near the source region and in a middle part of the semiconductor structure in the transversal direction thereof;

the metal-containing adjusting layer is formed near the source and a drain region in the transversal direction of the semiconductor structure; or

the metal-containing adjusting layer is formed in the middle part of the semiconductor structure in the transversal direction thereof.

8. A method for forming a semiconductor structure, comprising steps of:

providing a substrate;

forming a gate dielectric layer by depositing high k dielectric materials on the substrate;

forming a metal gate electrode layer by depositing metal gate materials on the gate dielectric layer;

forming a metal-containing adjusting layer for adjusting a work function of the semiconductor structure in the gate dielectric layer and/or the metal gate electrode layer; and

annealing the semiconductor structure,

wherein an interfacial layer is formed between the substrate and the gate dielectric layer, and an energy of bond between a metal atom in the metal-containing adjusting layer and an oxygen atom is larger than that between an atom in the gate dielectric layer or in the interfacial layer and an oxygen atom.

9. The method according to claim 8, wherein

the metal-containing adjusting layer is formed in a lower part of the metal gate electrode layer;

the metal-containing adjusting layer is formed in an upper part of the gate dielectric layer;

one part of the metal-containing adjusting layer is formed in the gate dielectric layer, and the other part of the metal-containing adjusting layer is formed in the metal gate electrode layer; or

the gate dielectric layer comprises a first gate dielectric layer and a second gate dielectric layer, and the metal-containing adjusting layer is formed between the first gate dielectric layer and the second gate dielectric layer.

10. The method according to claim 8, wherein a metal in the metal-containing adjusting layer is at least one metal selected from a group consisting of Er, Y, Gd, and Al.

11. The method according to claim 8, wherein

a work function of the metal in the metal-containing adjusting layer for a NMOS semiconductor structure is lower than that of a metal in the metal electrode layer; and

a work function of the metal in the metal-containing adjusting layer for a PMOS semiconductor structure is higher than that of the metal in the metal electrode layer.

12. The method according to claim 8, wherein the metal-containing adjusting layer is formed by implanting a metal ion, or the metal-containing adjusting layer is formed by atomic layer deposition, plasma enhanced chemical vapor deposition, or sputtering process.

13. The method according to claim 12, wherein:

an implantation depth of the metal-containing adjusting layer in a transversal direction of the semiconductor structure is same;

an implantation depth of the metal-containing adjusting layer in a part of the semiconductor structure near a source and a drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in a middle part of the semiconductor structure in the transversal direction thereof;

the implantation depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source and the drain region in the transversal direction of the semiconductor structure is smaller than that of the metal-containing adjusting layer in the middle part of the semiconductor structure in the transversal direction thereof;

the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the source region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof; or

the implanting depth of the metal-containing adjusting layer in a part of the semiconductor structure near the drain region in the transversal direction of the semiconductor structure is larger than that of the metal-containing adjusting layer in other parts of the semiconductor structure in the transversal direction thereof.

14. The semiconductor structure according to claim 12, wherein:

the metal-containing adjusting layer is formed near a source region in a transversal direction of the semiconductor structure;

the metal-containing adjusting layer is formed near the source region and in a middle part of the semiconductor structure in the transversal direction thereof;

the metal-containing adjusting layer is formed near the source and a drain region in the transversal direction of the semiconductor structure; or

the metal-containing adjusting layer is formed in the middle part of the semiconductor structure in the transversal direction thereof.

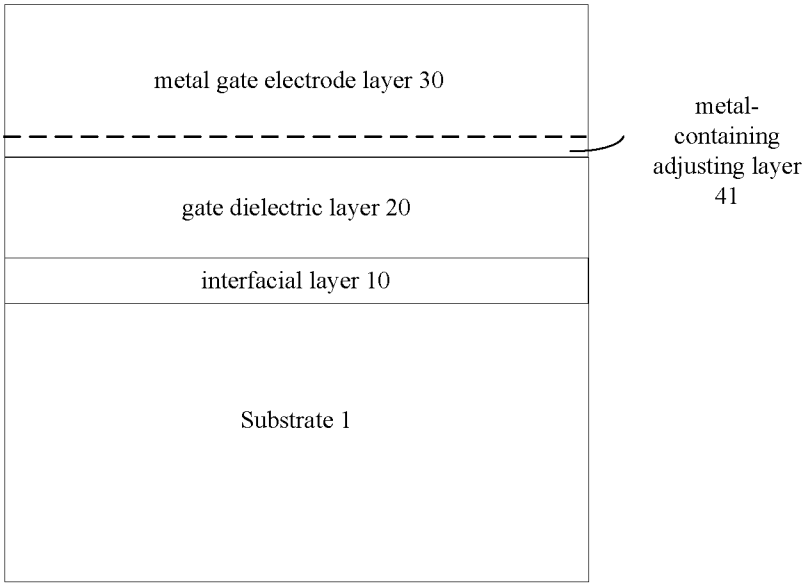

metal gate electrode layer 30
metal-containing adjusting layer 41
gate dielectric layer 20
interfacial layer 10
Substrate 1

Fig. 1

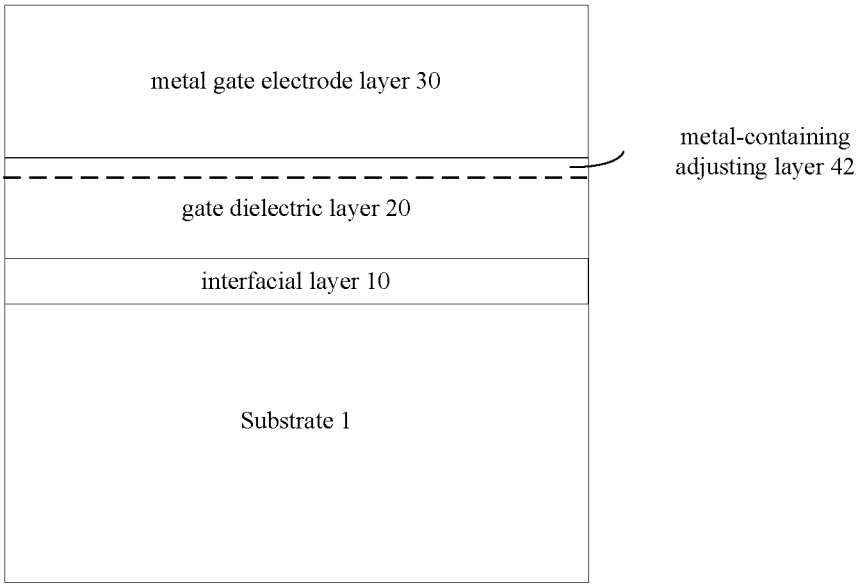

metal gate electrode layer 30
metal-containing adjusting layer 42
gate dielectric layer 20
interfacial layer 10
Substrate 1

Fig. 2

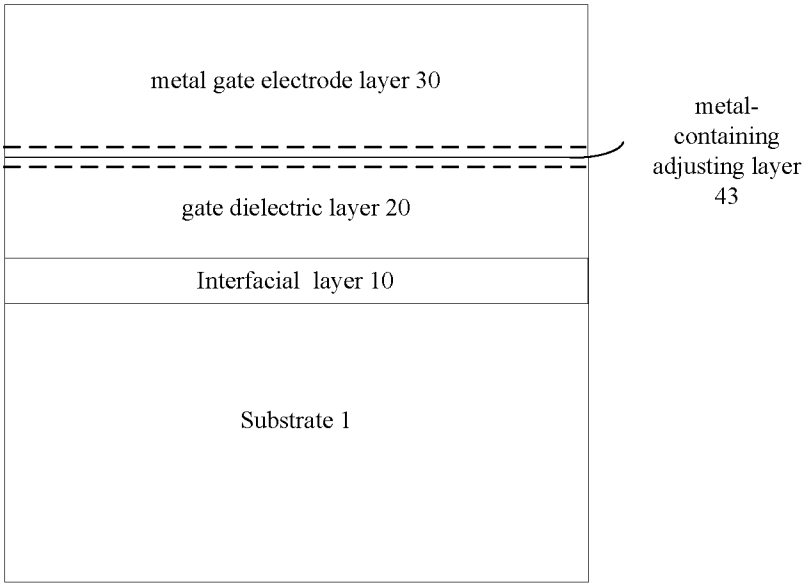

metal gate electrode layer 30
metal-containing adjusting layer 43
gate dielectric layer 20
Interfacial layer 10
Substrate 1

Fig. 3

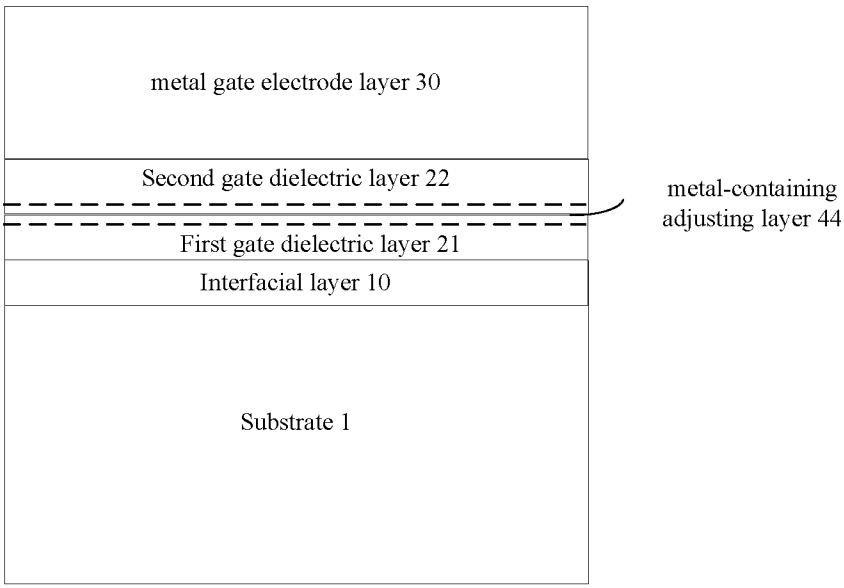

metal gate electrode layer 30
Second gate dielectric layer 22
metal-containing adjusting layer 44
First gate dielectric layer 21
Interfacial layer 10
Substrate 1

Fig. 4

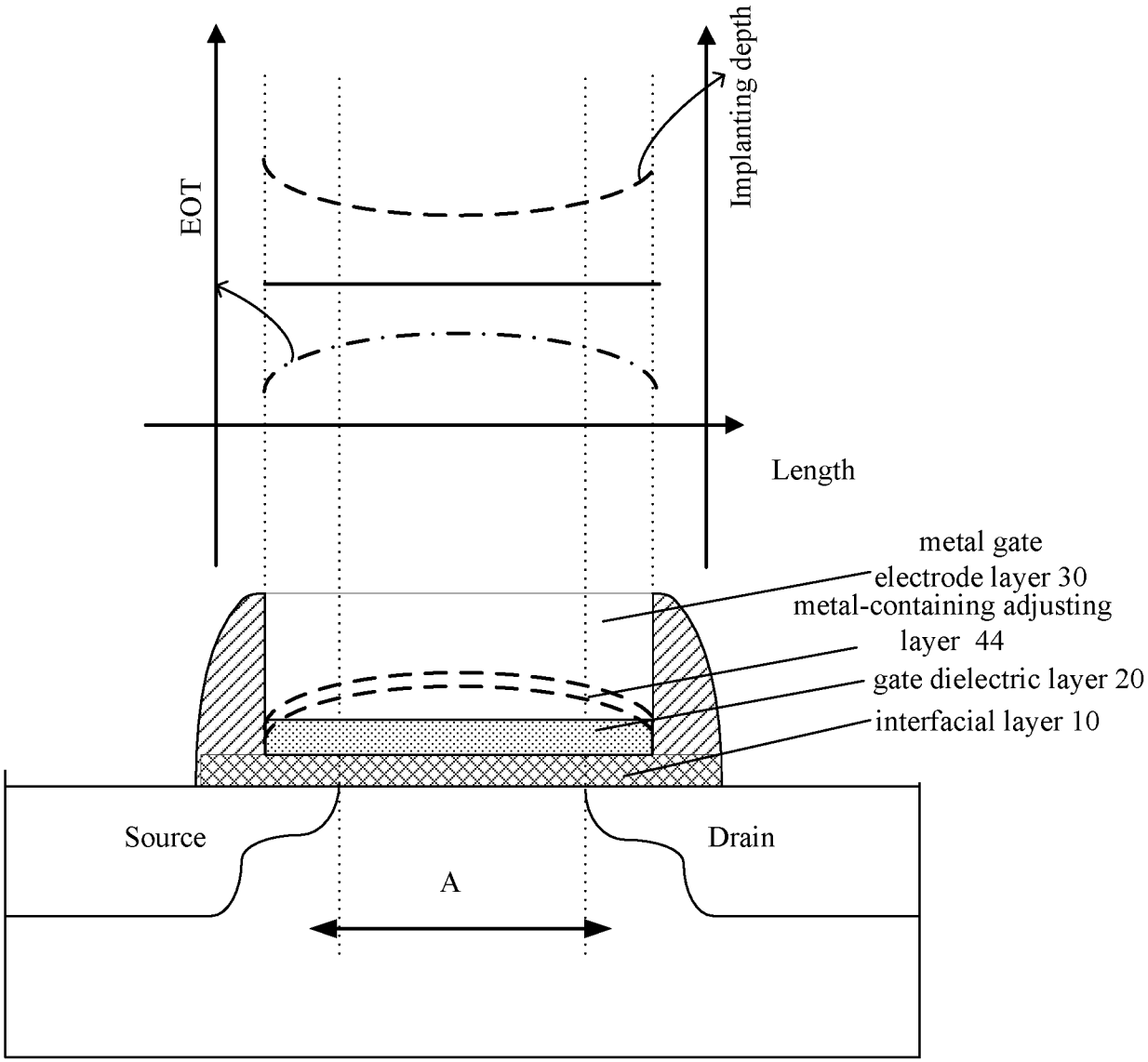

EOT
Implanting depth
Length
metal gate
electrode layer 30
metal-containing adjusting
layer 44
gate dielectric layer 20
interfacial layer 10
Source
Drain
A

Fig. 5

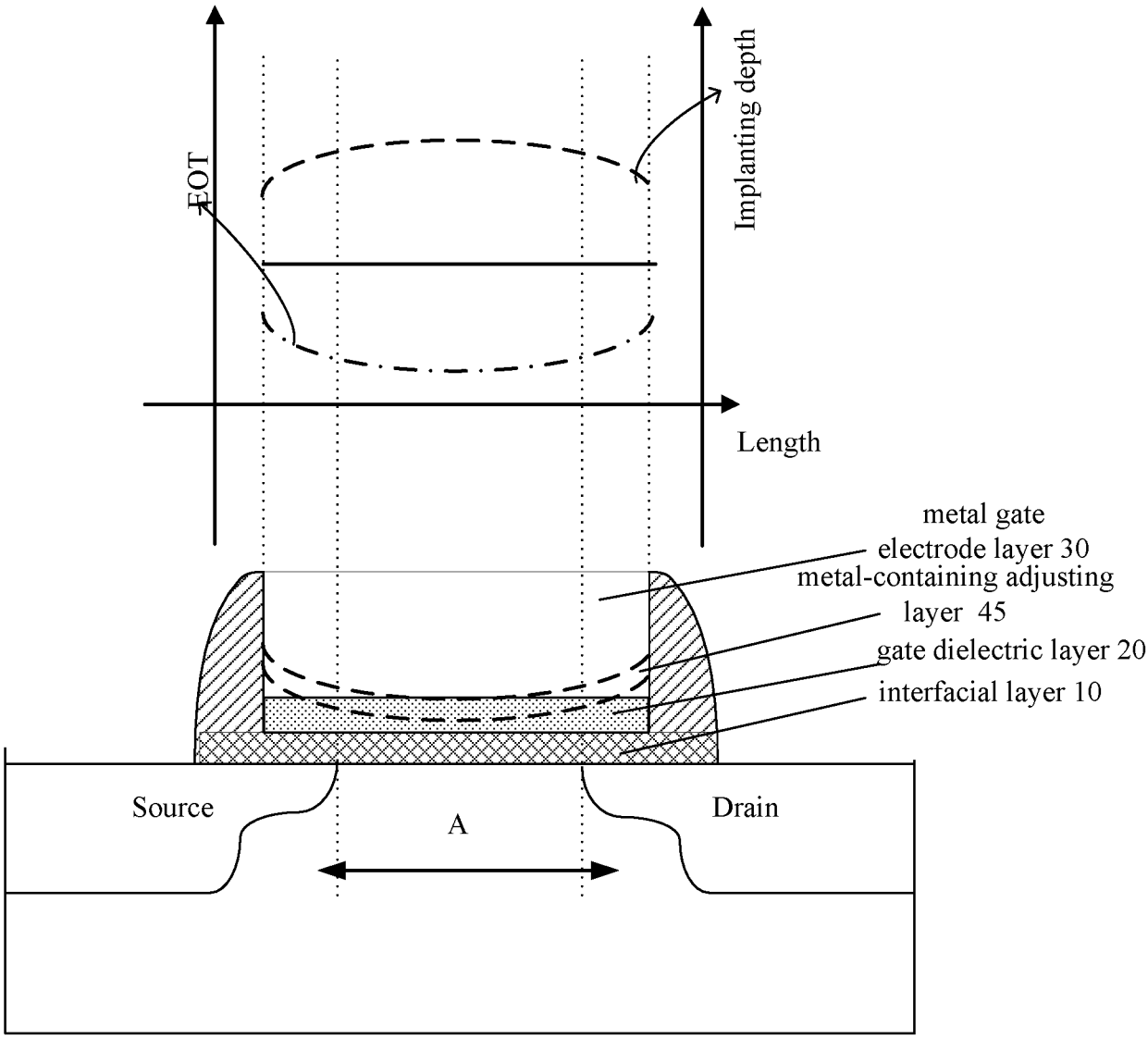

EOT
Implanting depth
Length
metal gate
electrode layer 30
metal-containing adjusting
layer 45
gate dielectric layer 20
interfacial layer 10
Source
A
Drain

Fig. 6

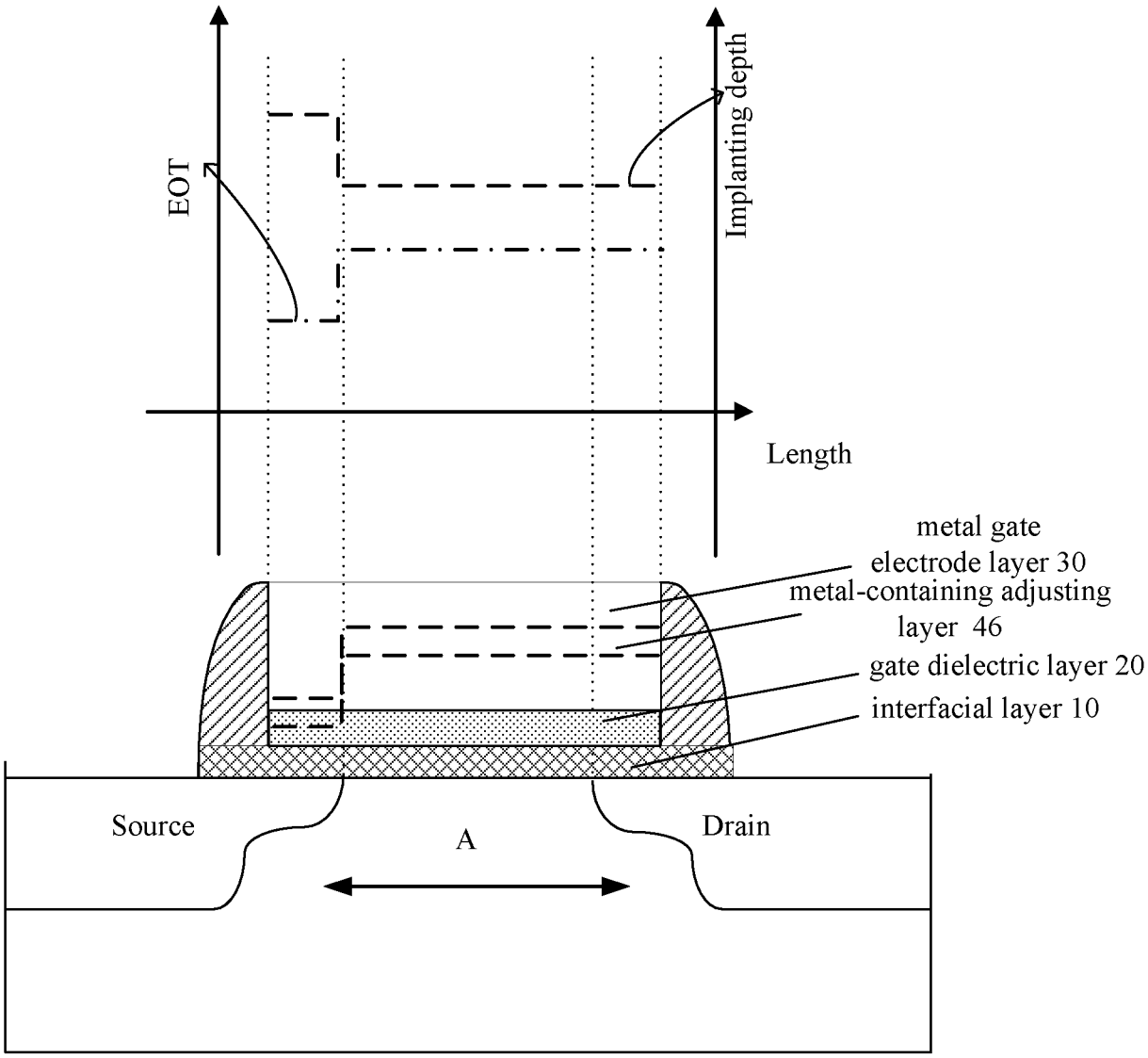

EOT
Implanting depth
Length
metal gate
electrode layer 30
metal-containing adjusting
layer 46
gate dielectric layer 20
interfacial layer 10
Source
A
Drain

Fig. 7

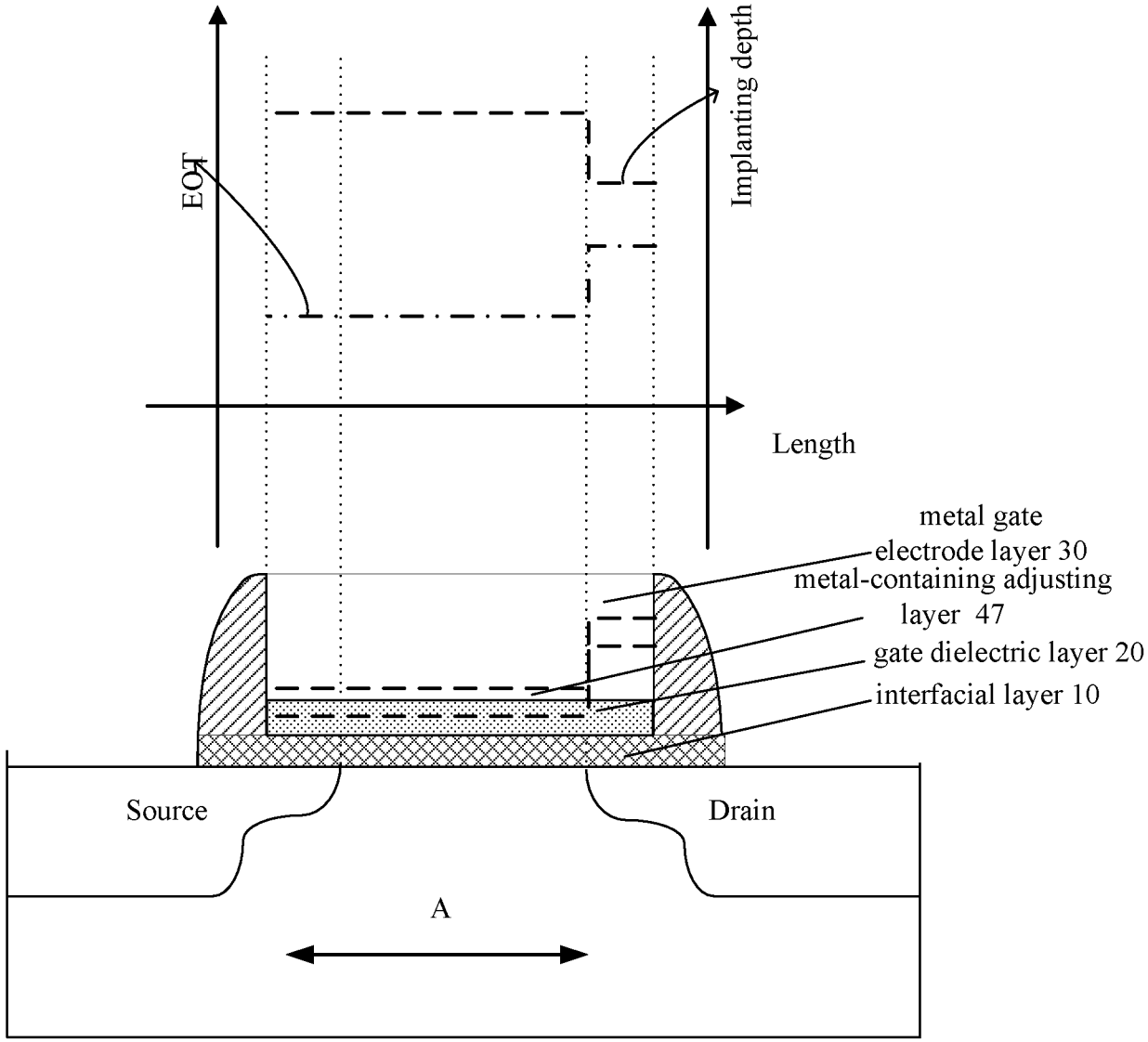

EOT
Implanting depth
Length
metal gate
electrode layer 30
metal-containing adjusting
layer 47
gate dielectric layer 20
interfacial layer 10
Source
Drain
A

Fig. 8

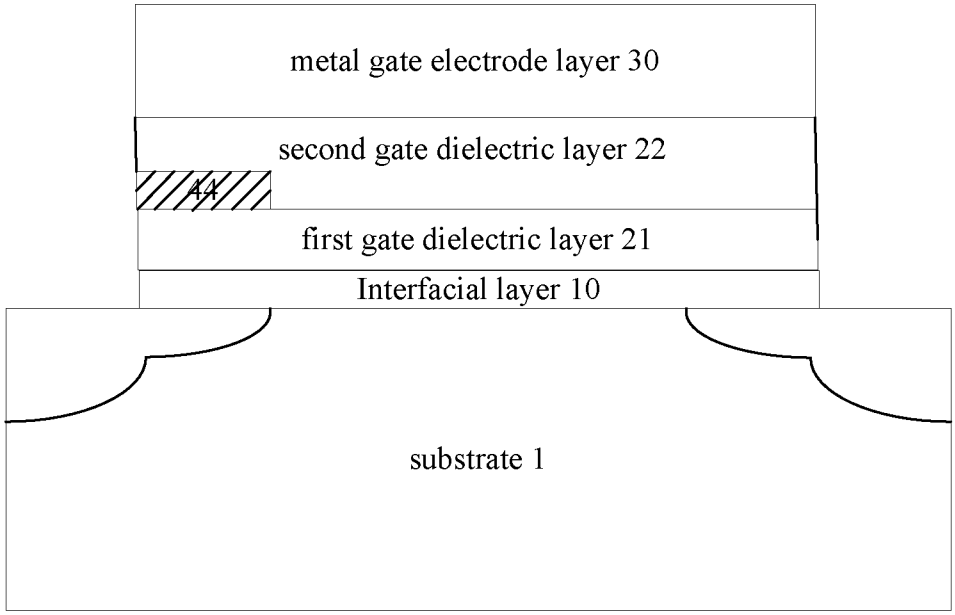

metal gate electrode layer 30
second gate dielectric layer 22
44
first gate dielectric layer 21
Interfacial layer 10
substrate 1

Fig. 9

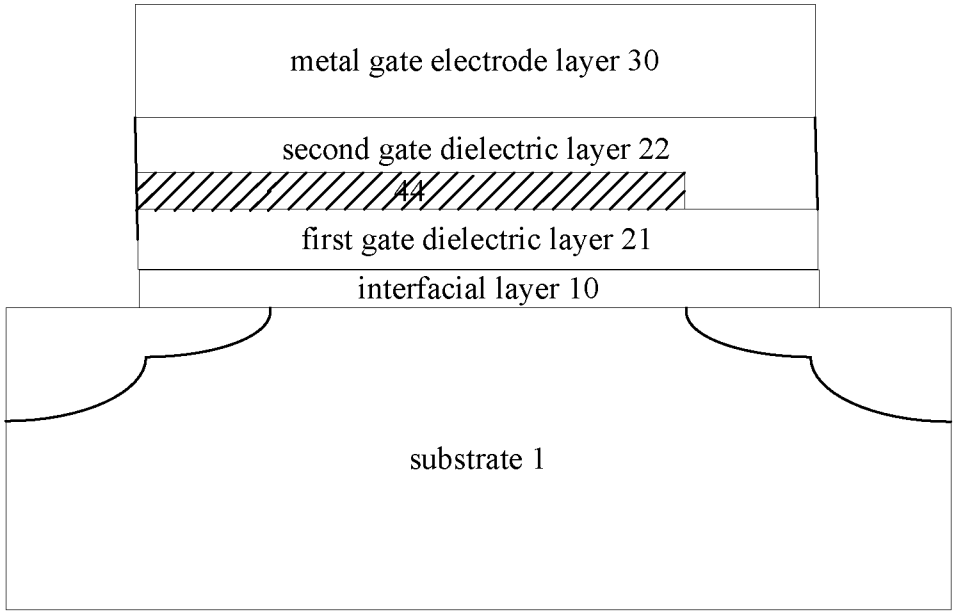

metal gate electrode layer 30
second gate dielectric layer 22
44
first gate dielectric layer 21
interfacial layer 10
substrate 1

Fig. 10

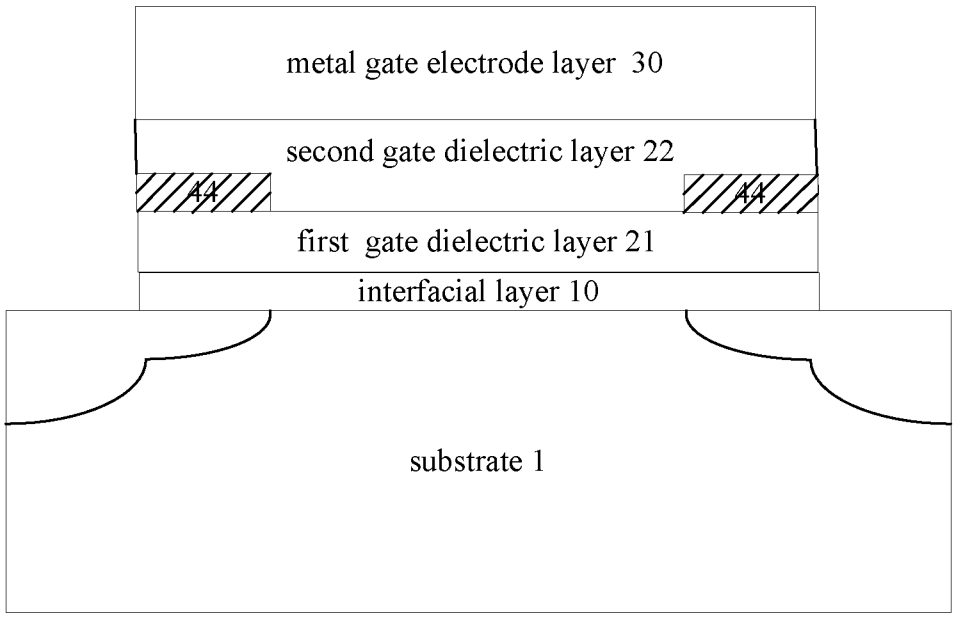

metal gate electrode layer 30
second gate dielectric layer 22
44
44
first gate dielectric layer 21
interfacial layer 10
substrate 1

Fig. 11

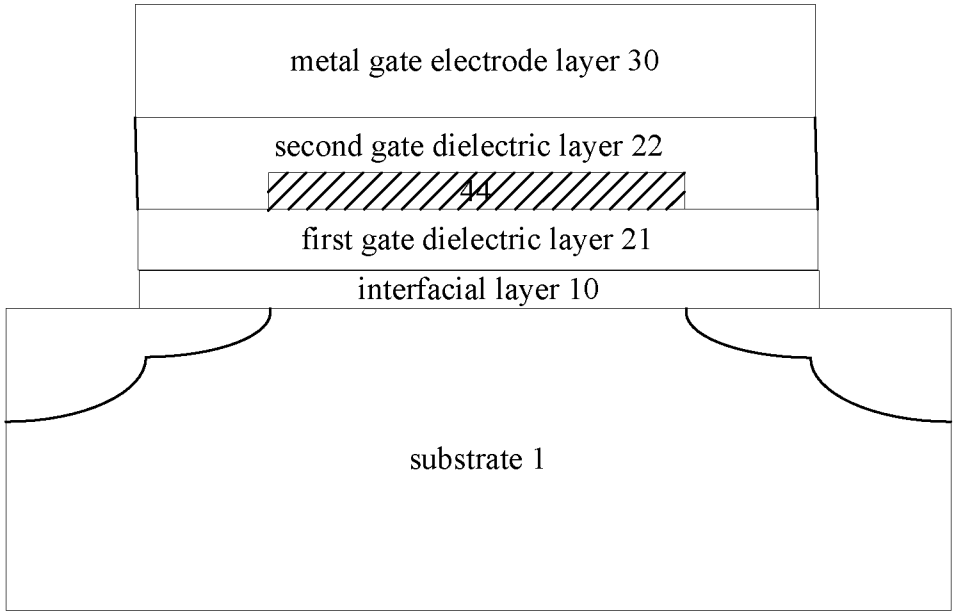

metal gate electrode layer 30
second gate dielectric layer 22
44
first gate dielectric layer 21
interfacial layer 10
substrate 1

Fig. 12

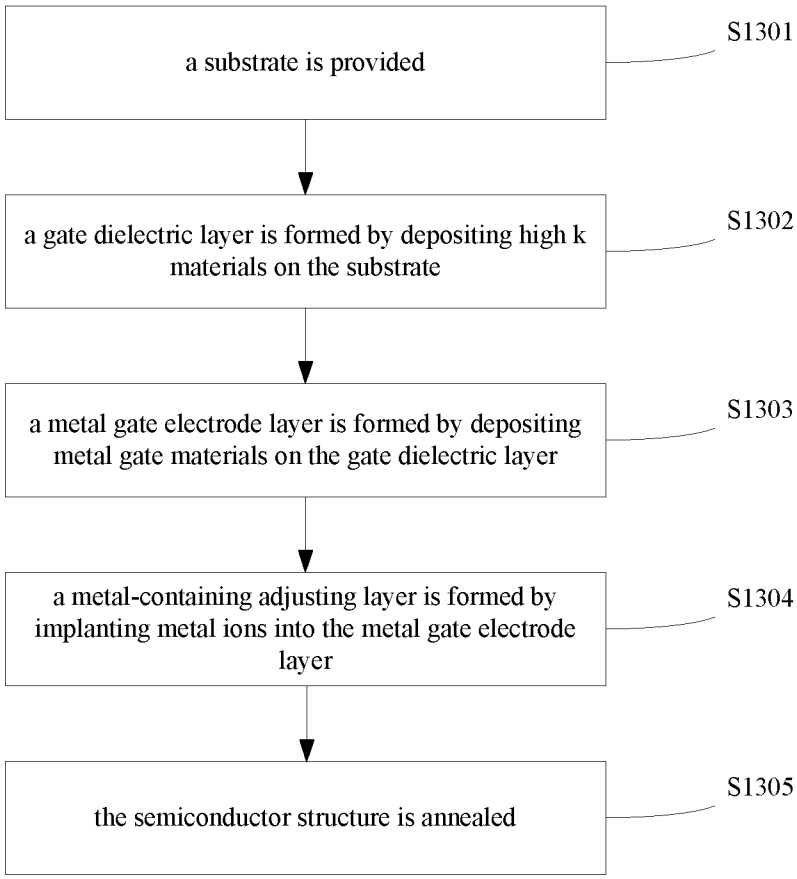

a substrate is provided
S1301
a gate dielectric layer is formed by depositing high k materials on the substrate
S1302
a metal gate electrode layer is formed by depositing metal gate materials on the gate dielectric layer
S1303
a metal-containing adjusting layer is formed by implanting metal ions into the metal gate electrode layer
S1304
the semiconductor structure is annealed
S1305

Fig. 13

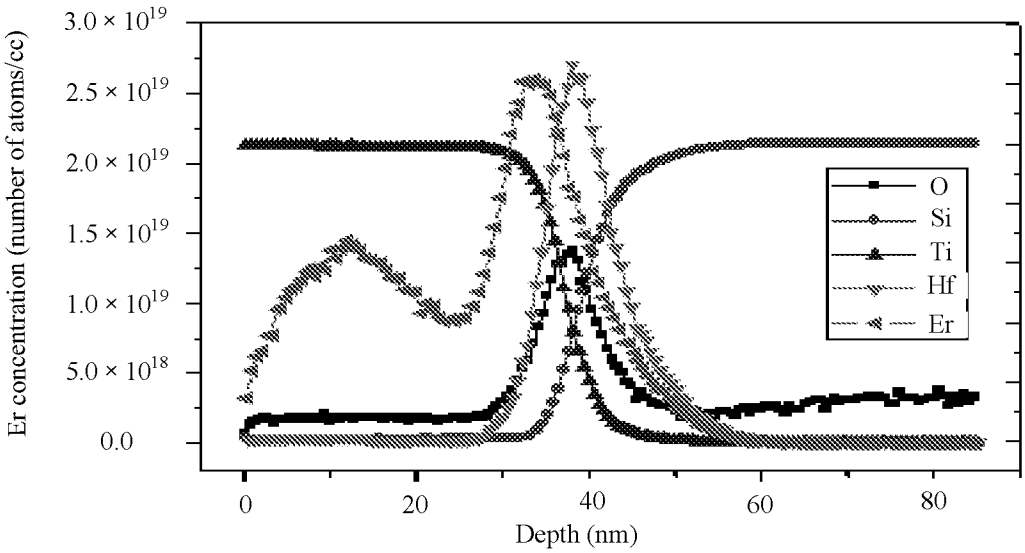

Er concentration (number of atoms/cc)
3.0 × 10^19
2.5 × 10^19
2.0 × 10^19
1.5 × 10^19
1.0 × 10^19
5.0 × 10^18
0.0
0
20
40
60
80
Depth (nm)
O
Si
Ti
Hf
Er

Fig. 14

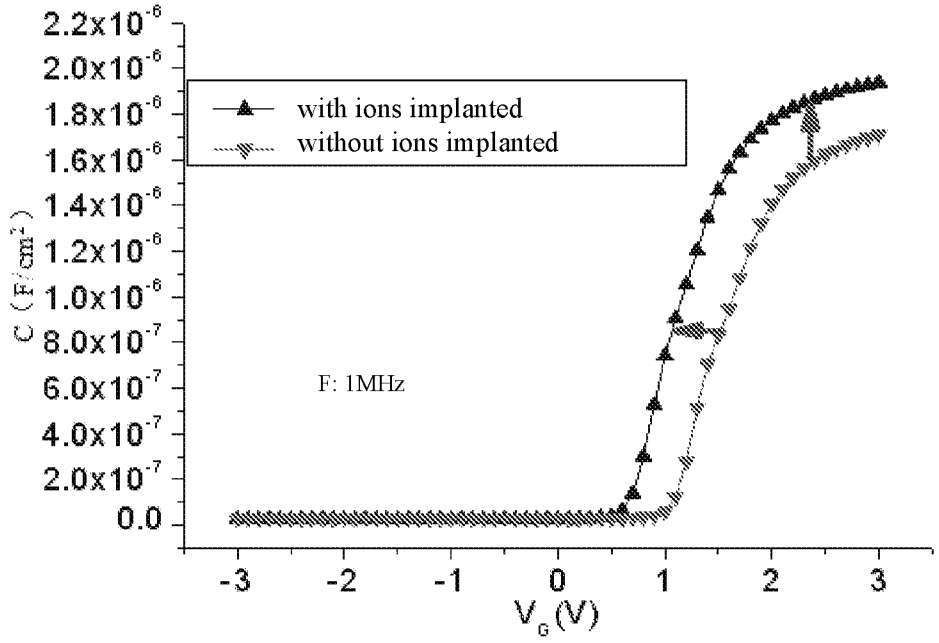

2.2x10-6
2.0x10-6
1.8x10-6
1.6x10-6
1.4x10-6
1.2x10-6
1.0x10-6
8.0x10-7
6.0x10-7
4.0x10-7
2.0x10-7
0.0
C (F/cm2)
with ions implanted
without ions implanted
F: 1MHz
-3
-2
-1
0
1
2
3
VG (V)

Fig. 15

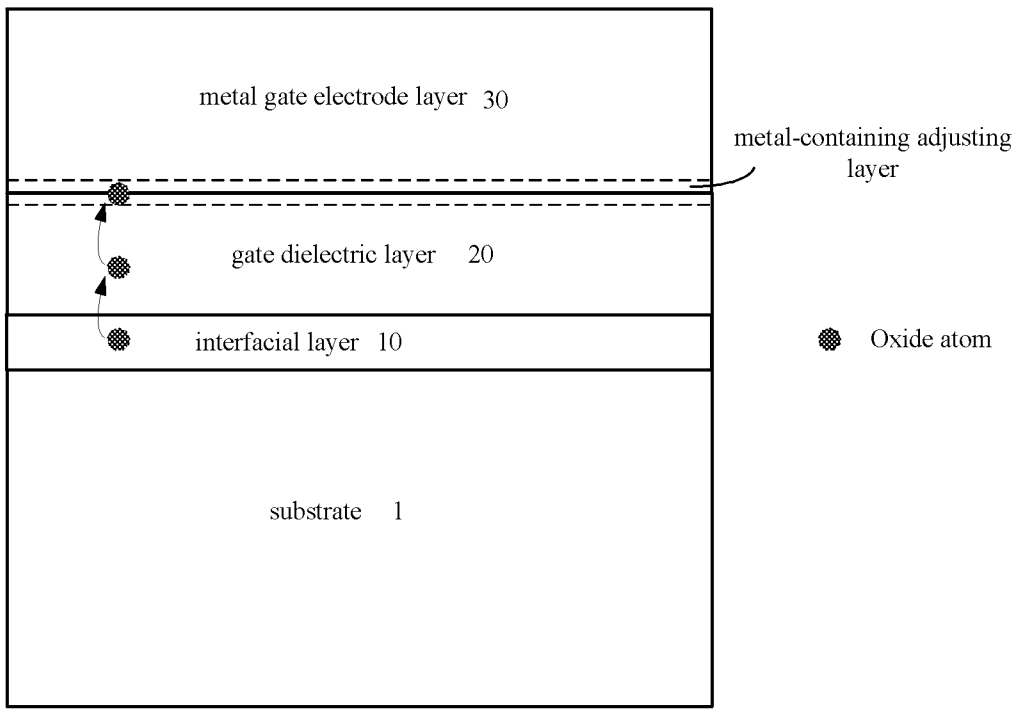

metal gate electrode layer 30
metal-containing adjusting layer
gate dielectric layer 20
interfacial layer 10
Oxide atom
substrate 1

Fig. 16

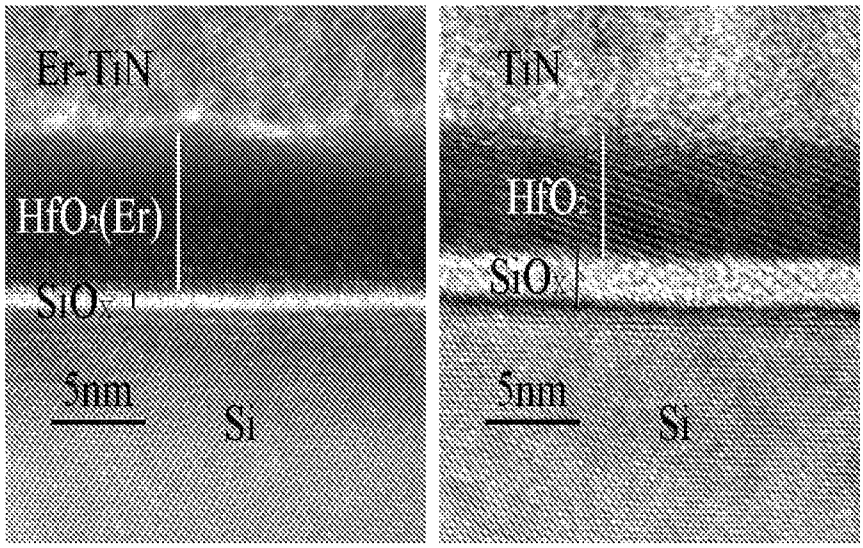



Fig. 17a Fig.17b

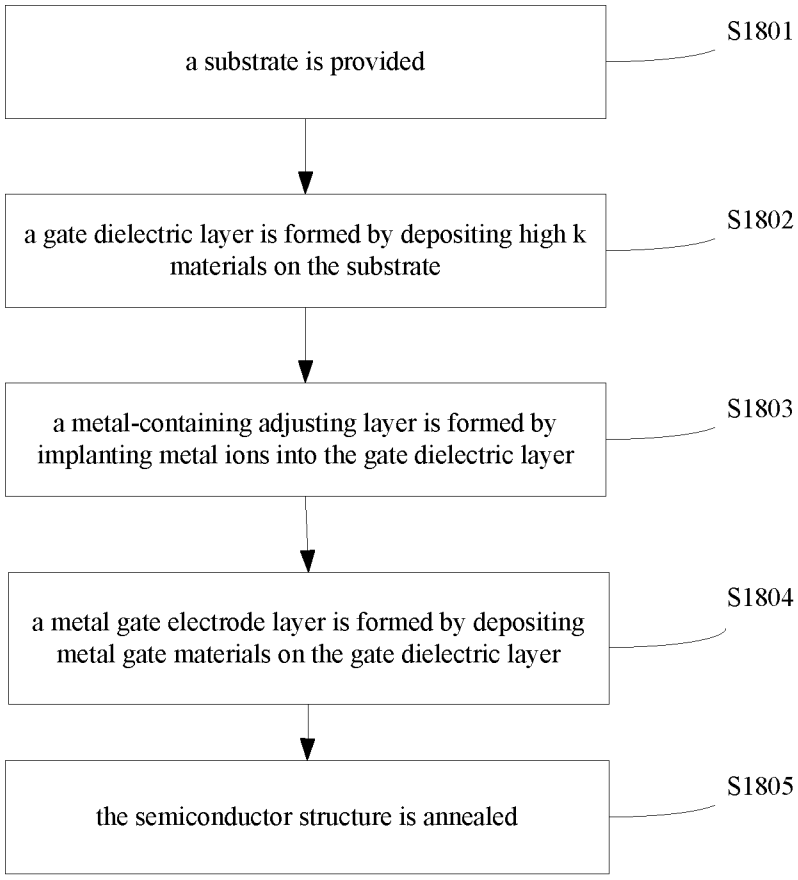



Fig. 18

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/077934

**A. CLASSIFICATION OF SUBJECT MATTER**

See the extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: gate, dielectric, interface, equivalent oxide, EOT, oxygen, getter, absorb, capture, attract, anneal, semiconductor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | CN101656214A,(TAIWAN SEMICONDUCTOR MFG), 24 February 2010(24.02.2010), page 3 line 7 to page 6 line 19 of the description; figures 1-6 | 1-14 |
| X | CN101930996A,(IBM CORP), 29 December 2010(29.12.2010), paragraphs [0017]-[0025],[0058] of the description; figures 1,2 | 1-14 |
| X | CN1949532A,(INST IND TECHNOLOGY), 18 April 2007(18.04.2007), page 5 line 17 to page 9 line 15 of the description; figures 1,3,4 | 1-14 |
| X | US6797572B1,(ADVANCED MICRO DEVICES INC), 28 September 2004(28.09.2004), column 2 line 61 to column 4 line 47 of the description; figures 1,2 | 1-14 |
| X | CN101661883A,(TAIWAN SEMICONDUCTOR MFG), 03 March 2010(03.03.2010), page 3 line 13 to page 7 line 21 of the description; figures 10-14 | 1-14 |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 10 February 2012(10.02.2012) | **08 Mar. 2012 (08.03.2012)** |
| Name and mailing address of the ISA/CN<br>The State Intellectual Property Office, the P.R.China<br>6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088<br>Facsimile No. 86-10-62019451 | Authorized officer<br>XU, Ying<br>Telephone No. (86-10)62412106 |

Form PCT/ISA /210 (second sheet) (July 2009)

# INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/077934

| Patent Documents referred in the Report | Publication Date | Patent Family | Publication Date |
|---|---|---|---|
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| | | TW201009956A | 01.03.2010 |
| CN101930996A | 29.12.2010 | US2010320547A1 | 23.12.2010 |
| | | JP2011003899A | 06.01.2011 |
| | | KR20100136406A | 28.12.2010 |
| | | US7989902B2 | 02.08.2011 |
| | | US2011207280A1 | 25.08.2011 |
| CN1949532A | 18.04.2007 | NONE | |
| US6797572B1 | 28.09.2004 | US6991990B1 | 31.01.2006 |
| CN101661883A | 03.03.2010 | US2010048010A1 | 25.02.2010 |
| | | TW201009936A | 01.03.2010 |
| | | US7989321B2 | 02.08.2011 |

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/077934

Continuation of classification of subject matter:

H01L29/51(2006.01)i

H01L29/78(2006.01)i

H01L21/28(2006.01)i

H01L21/265(2006.01)i

H01L21/8238(2006.01)i