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(54) Title: ETCHING PROCESS FOR SEMICONDUCTORS
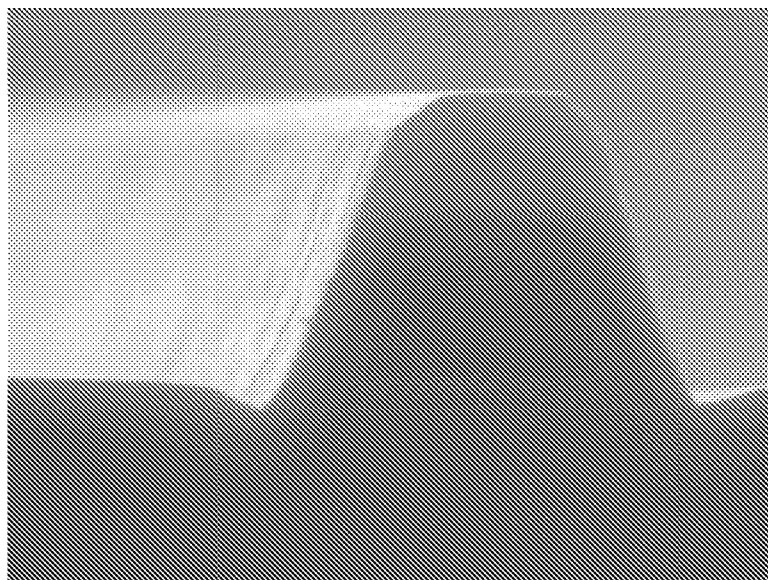
Fig. 3   1μm

(57) **Abstract**: A process for etching semiconductors, such as II-VI or III-V semiconductors is provided. The method includes sputter etching the semiconductor through an etching mask using a nonreactive gas, removing the semiconductor and cleaning the chamber with a reactive gas. The etching mask includes a photoresist. Using this method, light-emitting diodes with light extracting elements or nano/micro-structures etched into the semiconductor material can be fabricated.

ETCHING PROCESS FOR SEMICONDUCTORS

5

Field

This disclosure broadly relates to a process for etching semiconductors.

Background

10   The rapid development of optoelectronics has produced a need for methods of producing nanometer-sized patterns on semiconductor surfaces. Typically, these patterns are etched into semiconductor substrates by a number of techniques. For example, wet chemical etching has been used to etch a wide variety of semiconductors. However, wet chemical etching can be isotropic, thereby limiting the aspect ratio of features that can be

15   fabricated, and the uniformity of the process is low. Production industries in the optoelectronics industries require more controlled etching procedures than can be achieved using wet etching.

As a result of the shortcomings of wet chemical etching, dry etching processes have been developed for semiconductors. For example, reactive ion etching has been used

20   to produce well-controlled etching profiles in silicon substrates. Reactive ion etching involves generating chemically reactive species, such as radicals and ions, via an electric discharge in a low pressure reactive gas mixture in a reactor. The reactive species generated in this manner are accelerated towards a substrate by means of an electrical field and react with the silicon to produce volatile reaction product which are pumped away.

25   An etch mask can be applied to the substrate prior to etching to allow the reactive species to etch a pattern into the substrate. Because of the nearly vertical fall of the positively-charged reactive species, etching is much slower on the side-walls of the etched features as the etching progresses into the substrate.

Hard etch masks that are made of, for example, SiO_2, Si_3N_4, or metals are well

30   known to those of ordinary skill in the art of semiconductor photolithography. But these masks are difficult to fabricate since they typically need to be vacuum deposited in a separate step before the photoresist is applied. Hard etch masks make the process more

complicated and add more process steps. Additionally, after etching the hard masks need

to be removed by dry etching or wet etching. Furthermore, with many etching chemistries,

these materials tend to etch at a rate that is close to that of many II-VI or III-V

semiconductors which makes their use limited. While reactive-ion etching is very useful

5   for semiconductors, such as silicon, that form volatile byproducts which can be easily

eliminated from a vacuum chamber via pumping, reactive-ion etching is not very practical

for II-VI semiconductors since these materials do not easily react with reactive-ions and

typically do not form volatile byproducts. Dry etching is well-established for patterning

most semiconductor materials. Chlorine (Cl_2) based reactive ion etching (RIE) is widely

10   used in dry etching of III-V and II-VI semiconductors for fabricating various

optoelectronic devices and detectors. Other gas systems, including Cl_2/Ar, Cl_2/N_2, Cl_2/He,

$Cl_2/BCl_3/Ar$, BCl_3/Ar, $BrCl_3$, $SiCl_4/Ar$, $CCl_2F_2/H_2/Ar$, etc., have also been investigated.

However, these reactants and their products are known to be corrosive and toxic. Also,

rapid post-etching degradation has been observed when Cl-based RIE is used, due to the

15   corrosion by persistent Cl_2 residues. In the specific case of cadmium-containing

semiconductors, cadmium halides have vapor pressures which are several orders of

magnitude too low to provide the basis for useful etching. In the absence of cadmium

volatility, the most likely result is the formation of a cadmium-rich material on the surface

of the semiconductor. Therefore, CH_4/H_2 and $CH_4/H_2/Ar$ based chemistries have been

20   developed and are favored for plasma etching of Cd-containing semiconductors. However,

these processes suffer from several drawbacks including extensive polymer deposition,

which acts as an etch stop mechanism, rough surfaces, and low etch rates (less than

50nm/min).

25

Summary

A method for etching II-VI or III-V semiconductors is needed that can etch these

substrates rapidly, efficiently, selectively, and economically. A method for etching II-VI

or III-V semiconductors is needed that can be used to pattern optoelectronic devices, such

30   as, for example, light-emitting diodes (LEDs) that include such semiconductors.

Additionally, a method is needed for producing optoelectronic devices such as light-

emitting diodes that include light extracting elements or defined pixels.

A method is provided for etching a semiconductor that includes providing a semiconductor having an etching mask thereon in a vacuum chamber and sputter etching the semiconductor through the etching mask with a nonreactive etching gas to remove material from the surface of the semiconductor and to provide at least one etched surface,

5   removing the semiconductor with at least one etched surface from the vacuum chamber; and cleaning the vacuum chamber wherein the semiconductor comprises a III-V semiconductor, a II-VI semiconductor, or a combination thereof. The semiconductor can include a III-V semiconductor, a II-VI semiconductor, or a combination thereof. The provided method can be useful for II-VI semiconductors that can include, but are not

10   limited to, cadmium, magnesium, zinc, sulfur, selenium, tellurium, or combinations thereof. The provided method can also be useful for III-V semiconductors that can include, but are not limited to, aluminum, gallium, indium, arsenic, phosphorus, nitrogen, antimony, or combinations thereof. The nonreactive etching gas can include, but is not limited to, argon, krypton, xenon, helium, neon, nitrogen, or combinations thereof. The

15   provided method includes cleaning the vacuum chamber with a reactive gas.

In this disclosure:

"extraction elements" refers to any type and arrangement of nano/microstructures enhancing light extraction from self-emissive light sources such as light-emitting diodes;

"nonreactive gas" refers to a gas that can be used to etch a substrate by physical

20   sputtering. Sputter etching occurs primarily through physical bombardment of the surface with energetic species, which can displace or expel surface atoms via kinetic energy transfer; the active species do not substantially react with a substrate and the ejected material is typically non-volatile;

"reactive ion etching" refers to the process of ionizing a reactive gas in a plasma

25   discharge and accelerating it towards a substrate where the reactive species can chemically react with the substrate to form volatile species; and

"sputter etching" refers to the bombardment of a substrate with ions so as to remove material from the substrate by transfer of momentum from the ions to the material on the substrate; it is differentiated from reactive ion etching in that the species in the

30   etching gas physically remove substrate material by momentum transfer.

The provided method and structures made by the provided method can etch semiconductors, such as II-VI and III-V semiconductors. The provided method is a method that can rapidly, efficiently, selectively, and economically etch these materials and can provide optoelectronic devices, such as light-emitting diodes, that have structures, such as extraction elements, thereon.

The above summary is not intended to describe each disclosed embodiment of every implementation of the present invention. The brief description of the drawings and the detailed description which follows more particularly exemplify illustrative embodiments.

Brief Description of the Drawings

Figs. 1a – 1b are side-view schematic drawings of steps in the provided process.

Fig. 2 is a side-view schematic drawing of an exemplary semiconductor construction useful in the provided process.

Fig. 3 is a scanning electron photomicrograph of the etched semiconductor produced in Example 1.

Fig. 4a is a scanning electron photomicrograph of the etched semiconductor produced in Example 2.

Fig. 4b is a dark field optical photomicrograph of the etched semiconductor produced in Example 2.

Fig. 5a is a scanning electron photomicrograph of photoresist patterns used in Example 3.

Figs. 5b and 5c are scanning electron photomicrographs of etched semiconductors produced in Example 3.

Detailed Description

In the following description, reference is made to the accompanying set of drawings that form a part of the description hereof and in which are shown by way of illustration several specific embodiments. It is to be understood that other embodiments are contemplated and may be made without departing from the scope or spirit of the

present invention. The following detailed description, therefore, is not to be taken in a limiting sense.

Unless otherwise indicated, all numbers expressing feature sizes, amounts, and physical properties used in the specification and claims are to be understood as being
5   modified in all instances by the term "about." Accordingly, unless indicated to the contrary, the numerical parameters set forth in the foregoing specification and attached claims are approximations that can vary depending upon the desired properties sought to be obtained by those skilled in the art utilizing the teachings disclosed herein. The use of numerical ranges by endpoints includes all numbers within that range (e.g. 1 to 5 includes
10   1, 1.5, 2, 2.75, 3, 3.80, 4, and 5) and any range within that range.

The provided process can use conventional etching equipment and can thus obviate the need for special equipment. The provided process uses sputter etching instead of reactive-ion etching, and is thus useful on semiconductors that are not reactive with reactive-ions, for example, semiconductors made from non-silicon materials. In some
15   embodiments, these semiconductors include, for example, III-V semiconductors such as, for example, GaAs, InP, AlGaAs, GaInAsP, or GaInNAs. In other embodiments the provided process is useful for etching II-VI semiconductors such as, for example, materials that can include cadmium, magnesium, zinc, sulfur, selenium, tellurium, and combinations thereof. An exemplary II-VI semiconductor material can include CdMgZnSe alloy. Other
20   II-VI semiconductors such as CdZnSe, ZnSSe, ZnMgSSe, ZnS, CdS, ZnSe, ZnTe, ZnSeTe, HgCdSe, and HgCdTe can also be etched using the provided process.

The provided process relates to a method of sputter etching a semiconductor. The semiconductor is provided with an etching mask thereon that resists etching and thereby defines the part of the semiconductor surface that is etched. Typical etching masks can be
25   made of hard materials such as SiO_2, Si_3N_4, and metals such as titanium or tungsten. However, masks made of these hard materials are somewhat time-consuming to fabricate (since they must be deposited and then patterned using photoresist) and they can be etched by sputter etching, sometimes at rates similar to that of the rate of etching the semiconductor. Photoresists alone can also be useful as etching masks. Photoresist
30   etching masks can include positive photoresists comprised of a polymer that becomes soluble in a basic developer upon exposure to radiation, and negative photoresists that

cross-link and become insoluble upon exposure to radiation. Exemplary positive photoresists include UV5 photoresist and Shipley 1813 photoresist (both available from Rohm and Hass Electronic Materials, Marlborough, MA). Exemplary negative photoresists include UVN 30 (available from Rohm and Haas Electronic Materials), and

5   FUTURREX negative photoresists, such as NR9-1000P and NR9-3000PY (available from Futurrex, Franklin, NJ). Photoresists are well known to those of ordinary skill in the art of semiconductor lithography. A process for sputter etching II-VI or III-V semiconductors using a photoresist etching mask is described in copending application, Agent Docket No. 65811US002, filed on the same day herewith.

10   The semiconductor material can be sputter etched in areas not blocked by the etching mask by bombardment of the semiconductor surface with ions of a nonreactive etching gas. The etching gas ions can remove or eject material (byproducts) from an exposed surface of the semiconductor. The etching typically occurs on surfaces of the semiconductor that are not protected by the etching mask. The etching mask can have

15   patterned openings that, for example, define image pixels or provide patterns for producing light extractors on the surface of the semiconductor material. The nonreactive etching gas ions can impinge on the surface of the semiconductor material in a substantially vertical manner. That is, the etchant ions can be configured to strike the surface of the semiconductor material in essentially a straight line—typically at or near right angles to the

20   surface of the semiconductor material. The etchant can remove or expel exposed molecules from the semiconductor material by transfer of kinetic energy.

Exemplary nonreactive etching gases (etchants) can include argon, krypton, xenon, nitrogen, or combinations thereof. These gases have little or no tendency to react with semiconductor material since they are substantially inert gases. Thus, they tend to etch by

25   physical bombardment, transferring momentum to the molecules on the exposed surface of the semiconductor material. This material then can be ejected and deposit on other previously etched surfaces, such as the etched vertical surface of the semiconductor wall. Alternatively, the ejected material can deposit elsewhere in the vacuum chamber as debris. The debris can build up and eventually contaminate the etching process. It is typically

30   removed periodically by cleaning the vacuum chamber.

It has been found, surprisingly, that etching masks made from photoresist can have high selectivity towards sputter etching compared to II-VI or III-V semiconductors when both are subjected to sputter etching with a nonreactive gas such as, for example, argon. For example, when the photoresist is a negative photoresist, such as NR9-1000P or NR9-

5   3000PY (available from Futurrex, Franklin, NJ), and the semiconductor is a II-VI semiconductor such as CdMgZnSe, the semiconductor has been found to etch at a rate of from 6 to 12 times faster than the photoresist. In some embodiments of the provided process, the semiconductor can be etched at a rate of greater than about 100 nm/min, greater than about 300 nm/min, greater than about 500 nm/min, or even greater than about

10   1000 nm/min. In some embodiments, the photoresist etching mask can be etched at a rate of less than about 100 nm/min, less than about 50 nm/min, or even less than about 25 nm/min. In some embodiments, the ratio of the semiconductor etch rate to the photoresist etch rate is greater than about 3, greater than about 6, greater than about 10, or even greater than about 12.

15   The provided method can be better understood by references to the drawings. Figs. 1a-1b are side-view schematic drawings of steps in the provided method. Fig. 1a is a drawing that includes semiconductor material 102 with patterned photoresist 104 disposed thereon. Patterned photoresist 104 has trenches 103 that expose portions of semiconductor material 102. Sputter etching of semiconductor material 102 is performed using a

20   nonreactive gas. Fig. 1b shows that after sputter etching, trench 103 has been extended so that a portion of exposed semiconductor material 102 that is not covered by photoresist 104 has been etched below the original surface of semiconductor material 102.

The provided method of anisotropic etching of semiconductors can be used to form etched features, such as, for example, light extraction elements, into semiconductors. In

25   some embodiments, the provided method can be used to etch extraction elements that define small pixels in displays on electronic devices made using II-VI semiconductors. These pixels can be very small. For example, the pixels can have a longest dimension of less than about 10 micrometers. The pixels can be separated by trenches that are about 1 micron. Such exemplary devices include down-converted light-emitting diodes (LEDs).

30   In other embodiments, the provided method can be used to form light extractors on the face of LEDs made from II-VI semiconductors. Such light extractors can increase the

amount of light emitted from the LED face. Exemplary light extraction elements are not limited to any types of structures. In some embodiments, light extraction elements can include diffracting or scattering nanostructures as disclosed, for example, in U. S. Pat. Publ. No. 2009/0015757 (Potts et al.); structures with risers as disclosed, for example, in

5   U. S. Pat. Nos. 6,347,874 and 6,379,016 (both Boyd et al.); and structures such as those disclosed in PCT Pat. Publ. No. WO 2008/083188 (Lu et al.). In some embodiments, the light extraction elements can have dimensions as small as about 500 nm.

         Typically, argon gas is used as the nonreactive etching gas since it tends to effectively etch II-VI or III-V semiconductors without degrading the semiconductor

10   properties as much as do gases that etch by reactive-ion interaction such as, for example, chlorine gas. However, as described above, unwanted debris can be produced by sputtering of semiconductors. These debris can deposit on the interior surfaces of the plasma etching system, and thereby change the electrical properties of the system, resulting in an unstable etch rate. Debris can also potentially re-deposit on the sample. Thus, when

15   using a nonreactive etching gas, it is desirable to periodically remove the semiconductor from the vacuum chamber, fill the chamber with a reactive gas, such as, for example, chlorine, oxygen, or a combination thereof to react with and volatilize the debris that have accumulated inside of the vacuum chamber. A wide variety of reactive gases and combinations of reactive gases can be used to clean the chamber. These include, for

20   example, chlorine, oxygen, boron trichloride, silicon tetrachloride, and hydrogen. Typically these reactive gases can be mixed with a nonreactive gas such as argon, helium, or nitrogen.

         In cases in which it is desired to sputter etch the semiconductor to a greater depth, it may be advantageous to sputter etch the sample to a fraction of the target depth, remove

25   the sample from the chamber, clean the chamber, and then return the sample to the chamber for further etching. This etch-and-clean cycle may be repeated to reach any desired etch depth.

         Objects and advantages of this invention are further illustrated by the following examples, but the particular materials and amounts thereof recited in these examples, as

30   well as other conditions and details, should not be construed to unduly limit this invention.

Examples

A II-VI semiconductor color converter layer structure based upon CdMgZnSe alloy was grown by molecular beam epitaxy on an InP substrate. The color converter layer structure is shown schematically in Fig. 2, and the layer thicknesses and compositions are shown in Table I below.   Fig. 2 is a schematic of color converter layer 200 that includes top window 202, absorber 204, and a graded compositional layer 206 that gradually changes from the composition of top window 202 to absorber 204. Embedded in the absorber layer (not shown) are quantum wells that capture carriers generated when pump light is absorbed in the absorber layer and re-emit light at a longer wavelength. Details of color converter structures may be found, for example, in U. S. Pat. No. 7,402,831 (Miller et al.).

Table I

Composition of Color Converter Layer Structure

Layer	Parts Cd	Parts Mg	Parts Zn	Parts Se	Thickness (μm)
Top Window	0.15	0.55	0.30	1.00	0.50
Grading Layer	0.15-0.29	0.55-0.34	0.30-0.37	1.00	0.25
Absorber	0.29	0.34	0.37	1.00	1.50

Comparative Example 1 – Cl_2 reactive ion etching of a II-VI semiconductor

A photoresist pattern of ridges was created on the II-VI semiconductor structure described above using a negative photoresist (NR1-1000P, available from Futurrex, Franklin, NJ) and conventional contact lithography. The sample was then cleaved into small pieces for etching as described in the following examples. The etching was conducted in a commercial reactive ion system (RIE, Model PLASMA LAB System 100, available from Oxford Instruments, Yatton, UK).

A small cleaved sample of the II-VI semiconductor with the photoresist mask thereon was put on a Si carrier wafer, loaded into the RIE chamber, and plasma etched using 80 sccm Cl_2, 5 sccm Ar, 75-200 Watts Radio Frequency (RF) power, 1200 Watts inductively coupled plasma power, at a pressure of 6 mTorr and an etch time of 4 x 30

second intervals. The photoresist was severely damaged by the Cl_2 plasma etching. The
etching rate of the photoresist was measured as 1000 nm/min. The ratio of the etching rate
of the semiconductor to that of the photoresist was 0.19. Thus, the reactive species
produced by chlorine reacts with the photoresist and etches the photoresist much more
5   rapidly than it does the II-VI semiconductor.

Example 1 – Ar etching of II-VI semiconductor with a photoresist mask
        A sample of the II-VI semiconductor color converter described above was
overcoated with a photoresist mask with stripe patterns using NR9-1000P negative
10   photoresist, available from Futerrex, Franklin, NJ. The stripe patterns had dimensions of 2
μm and 100 μm. A small cleaved sample of the II-VI semiconductor with the photoresist
mask thereon was put on a Si carrier wafer, loaded into the RIE chamber, and plasma
etched using 5-50 sccm Ar, 20-200 Watts Rf power, 700-2000 Watts inductively coupled
plasma power (ICP), at a pressure of 4-30 mTorr and an etch time of 5 x 60 second
15   intervals. Pixel stripes having widths as small as 2 μm continued to exhibit strong
photoluminescence for several months after processing. An identical sample etched with
Cl_2 under identical conditions as those in Comparative Example 1 except that the etch time
was 6 x 30 second intervals (to allow for cooling of the substrate during the intervals)
showed rapid degradation of photoluminescence after one day. Fig. 3 is a
20   photomicrograph of the semiconductor etched using the argon sputter etching process.
The etch profile that was obtained had about a 63 degree wall angle. The ratio of the
etching rate of the semiconductor to the photoresist varied from about 6 to about 12 and
could be controlled by changing the RF power. Lower RF power increased the ratio but
decreased the speed of etching. The etch rate of the II-VI semiconductor color convertor
25   ranged from 300 nm/min to 500 nm/min.

Example 2 – Ar etching of 3 micrometer trenches in II-VI semiconductor material
        A patterned photoresist upon on a II-VI semiconductor color converter structure as
described above in Table 1 was made by optical lithography with NR9-3000PY negative
30   photoresist available from, available from Futurrex, Franklin, NJ) was etched using the
procedure of Example 1. Fig. 4a is a scanning electron photomicrograph of the resultant

structure and shows a pattern of trenches 3 μm wide leaving ridges approximately 6 μm across. Fig. 4b is a dark field optical photomicrograph showing photoluminescence of the semiconductor ridges. What is observed is a series of emitting "pixels" where the semiconductor color converter has been left intact (protected during etching by the photoresist).

Example 3 – Ar plasma etching of II-VI semiconductor for light extraction.

A patterned photoresist upon on a II-VI semiconductor color converter structure as described above in Table 1 was made as follows. 2-dimensional grating patterns with holes or post structures for light extraction were created in TELR-P003PM photoresist (available from Shipley, Marlborough, MA) using interference lithography based upon a laser diode source. The grating had 400-500 nm features on a 1 μm pitch. The patterned photoresist-coated semiconductor was subjected to Ar etching under conditions similar to those described in Example 1. Fig. 5a is a scanning electron micrograph of the photoresist pattern with post structures 400 nm in diameter on the semiconductor before etching. Fig. 5b shows the same view as Fig. 5a after Ar plasma etching, with the photoresist still in place. After etching, the remaining photoresist was pyramidal in structure and the semiconductor around the photoresist had been etched leaving conical posts under the resist (the boundary between the residual photoresist and the semiconductor can be seen in Figure 5b, roughly two-thirds of the way from the base to the vertex of the conical structure). Further Ar etching yielded the pattern in the semiconductor shown in Fig. 5c. Photoluminescence measurements showed an external quantum efficiency of 50.4% for the etched sample illustrated in Fig. 5c. Photoluminescence measurements of the planar sample before etching showed an external quantum efficiency of 29.7%. This example shows how light extraction structures on a II-VI semiconductor increase the yield of the light that is emitted.

Various modifications and alterations to this invention will become apparent to those skilled in the art without departing from the scope and spirit of this invention. It should be understood that this invention is not intended to be unduly limited by the illustrative embodiments and examples set forth herein and that such examples and embodiments are presented by way of example only with the scope of the invention

intended to be limited only by the claims set forth herein as follows. All references cited in this disclosure are herein incorporated by reference in their entirety.

What is claimed is:

1.   A method of etching a semiconductor comprising:

        providing a semiconductor having an etching mask thereon in a vacuum chamber; and

5   sputter etching the semiconductor through the etching mask with a nonreactive etching gas to remove material from the surface of the semiconductor and to provide at least one etched surface,

        removing the semiconductor with at least one etched surface from the vacuum chamber; and

10   cleaning the vacuum chamber.

wherein the semiconductor comprises a III-V semiconductor, a II-VI semiconductor, or a combination thereof, and

wherein cleaning the vacuum chamber comprises introducing a reactive gas into the vacuum chamber and forming a plasma with the reactive gas to volatilize deposits inside

15   the vacuum chamber.

2.   A method according to claim 1, wherein the semiconductor comprises a II-VI semiconductor.

20   3.   A method according to claim 2, wherein the II-VI semiconductor comprises cadmium, magnesium, zinc, selenium, tellurium, or combinations thereof.

4.   A method according to claim 3, wherein the semiconductor comprises a CdMgZnSe alloy.

25

5.   A method according to claim 1, wherein the etching mask comprises a negative photoresist.

6.   A method according to claim 1, wherein the nonreactive etching gas comprises

30   argon, krypton, xenon, nitrogen, helium, neon or combinations thereof.

7.   A method according to claim 6, wherein the nonreactive etching gas comprises argon.

8.   A method according to claim 1, wherein the semiconductor is etched at rate of greater than about 300 nm/min.

9.   A method according to claim 8, wherein the semiconductor is etched at a rate of greater than about 500 nm/min.

10.   A method according to claim 1, wherein the photoresist is etched at a rate of less than about 50 nm/min.

11.   A method according to claim 1, wherein the ratio of the semiconductor etch rate to the photoresist etch rate is greater than about 6.

12.   A method according to claim 11, wherein the ratio of the semiconductor etch rate to the photoresist etch rate is greater than about 10.

13.   A method according to claim 1, wherein the reactive gas comprises chlorine.

14.   An etched semiconductor made according to claims 1 to 13.

15.   An optoelectronic device comprising an etched semiconductor according to claim 14.

16.   A method according to claim 1, further comprising:
        returning the semiconductor with at least one etched surface to the vacuum chamber after cleaning the chamber; and
        further sputter etching the semiconductor through the etching mask with a nonreactive etching gas.
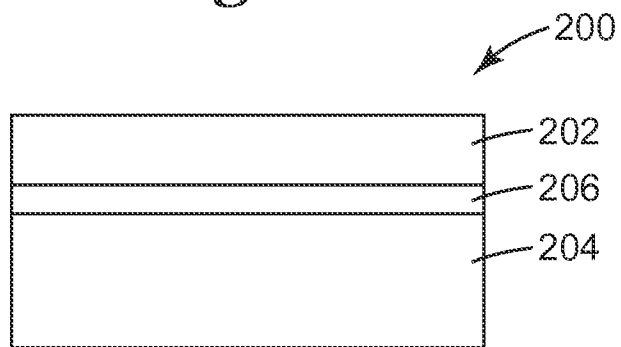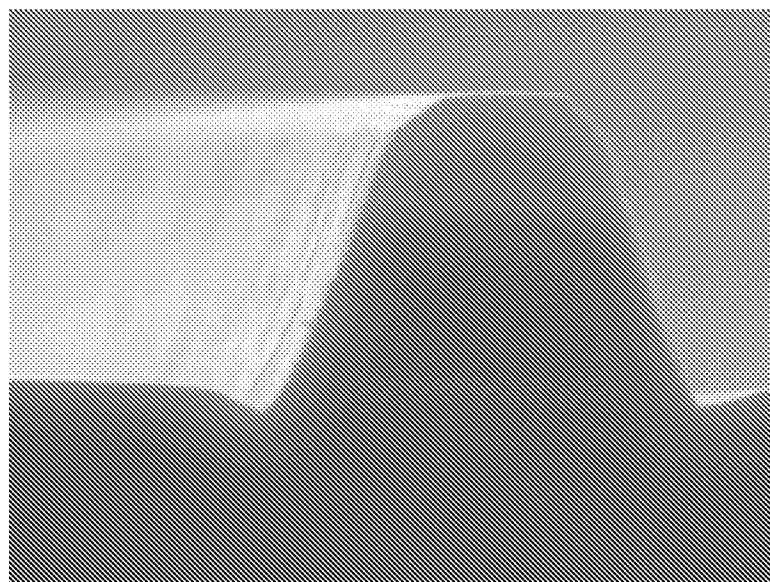
Fig. 1a

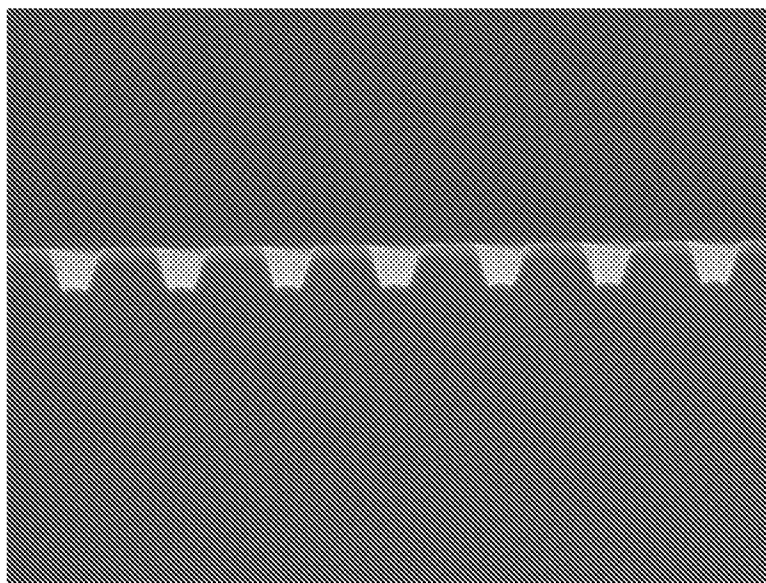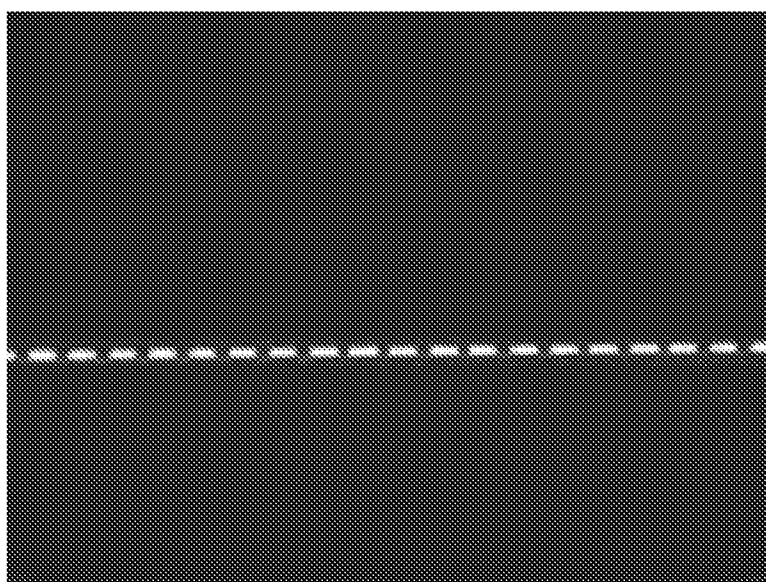*Fig. 1b*

Fig. 2

Fig. 3

1μm

10μm

Fig. 4a

Fig. 4b

1.00µm

Fig. 5a

1.00µm

Fig. 5b

1.00μm

Fig. 5c