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(54) **CURRENT-CONTROLLED CMOS (C3MOS) FULLY DIFFERENTIAL INTEGRATED DELAY CELL WITH VARIABLE DELAY AND HIGH BANDWIDTH**

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(63) Continuation of application No. 11/320,401, filed on Dec. 28, 2005, now Pat. No. 7,598,788.

(60) Provisional application No. 60/714,814, filed on Sep. 6, 2005.

Publication Classification

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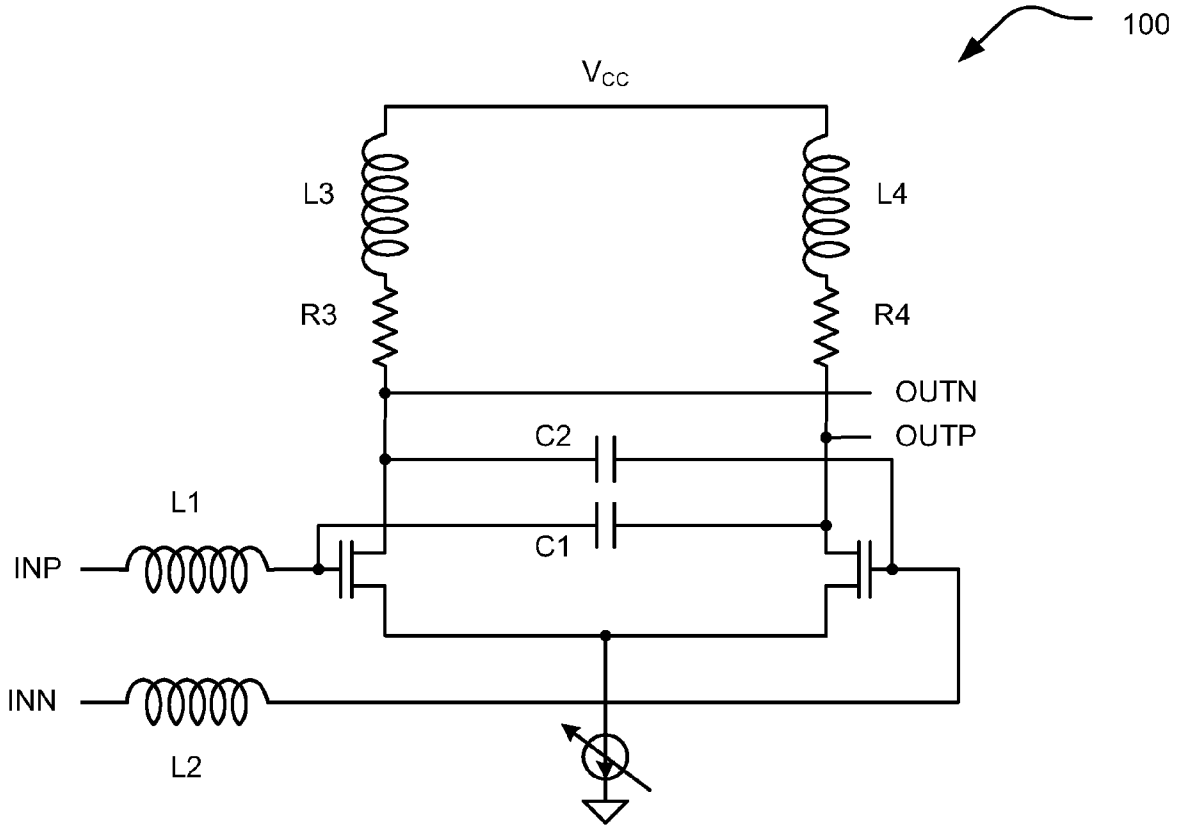
(52) **U.S. Cl.** **327/266**; 327/274; 327/280; 327/287

(57) **ABSTRACT**

Current-controlled CMOS (C3MOS) fully differential integrated delay cell with variable delay and high bandwidth. A novel implementation includes a wideband differential transistor pair and a cross-coupled differential transistor pair. The wideband differential transistor pair can be implemented with appropriate input and output impedances to extend its bandwidth for use in broadband applications. These two stages, (1) buffer stage (or data amplifier stage) and (2) cross-coupled differential pair stage, are both very fast operating stages. This design does not incur any increased loading to previous or subsequent stages in a device. In addition, there is no increase in the total amount of current that is required.



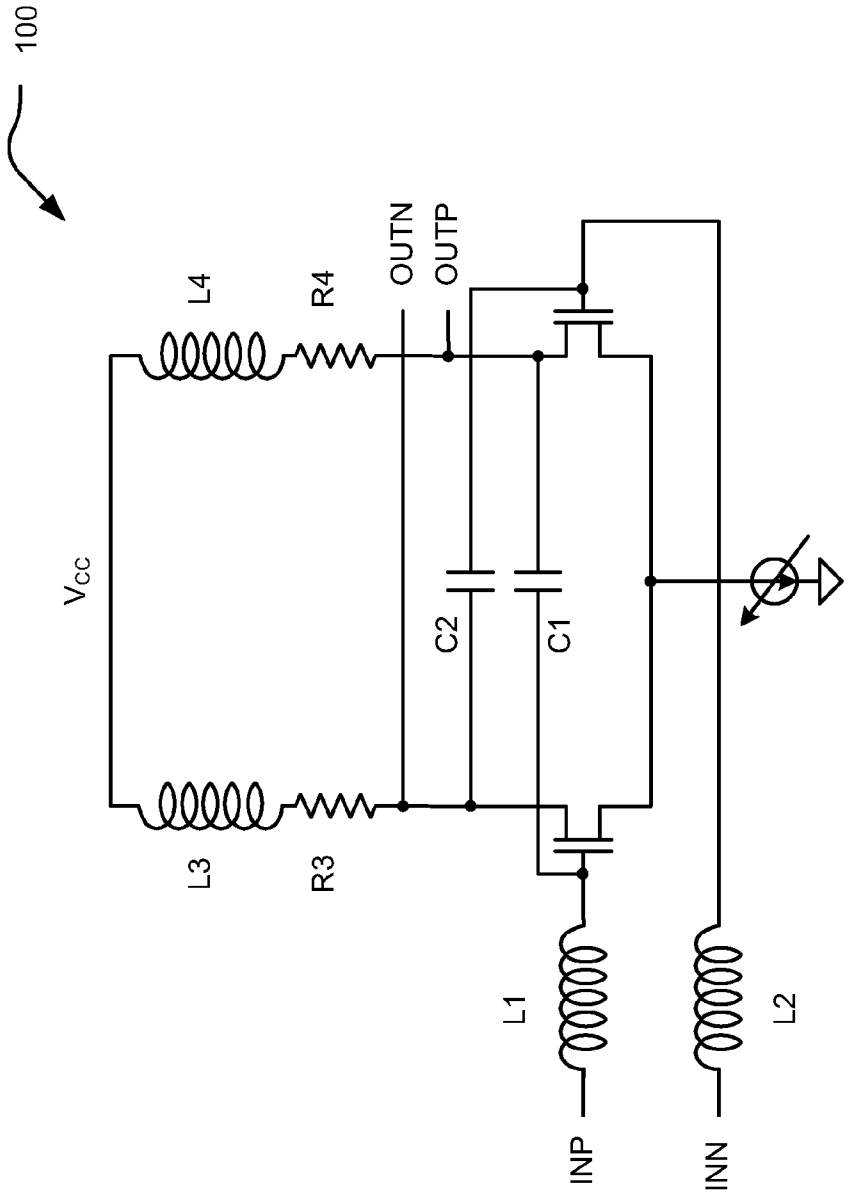


Fig. 1

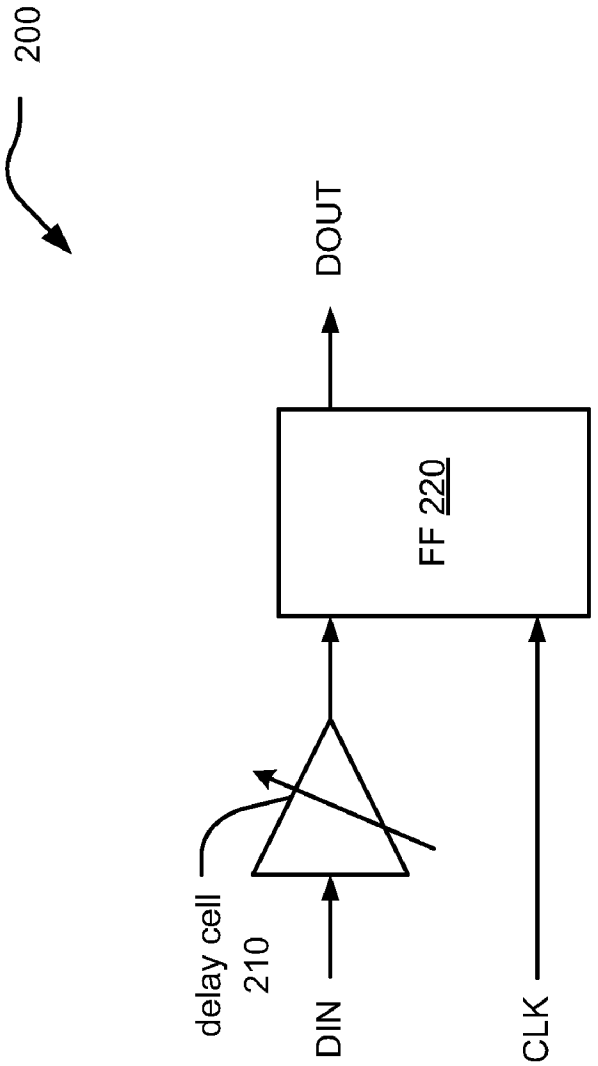


Fig. 2

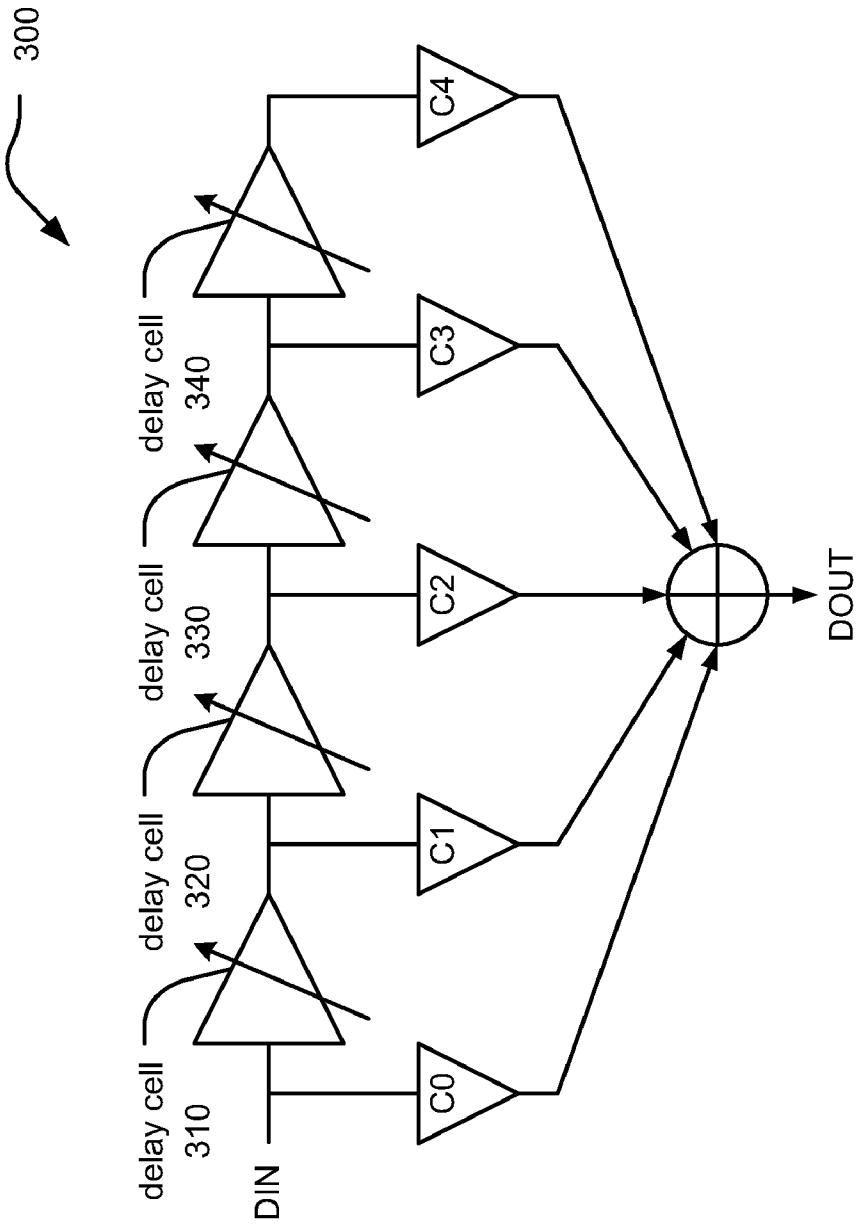

300
delay cell 310
delay cell 320
delay cell 330
delay cell 340
DIN
C0
C1
C2
C3
C4
DOUT

Fig. 3

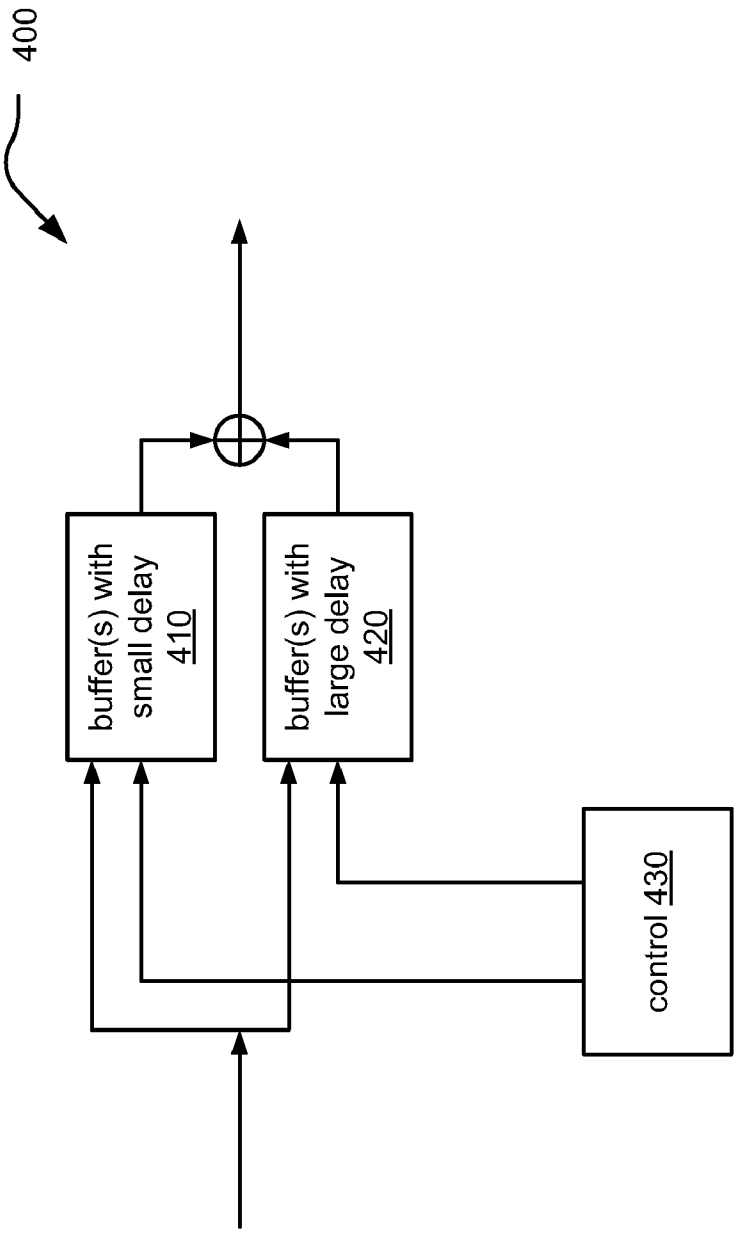

400
buffer(s) with small delay 410
buffer(s) with large delay 420
control 430

Fig. 4

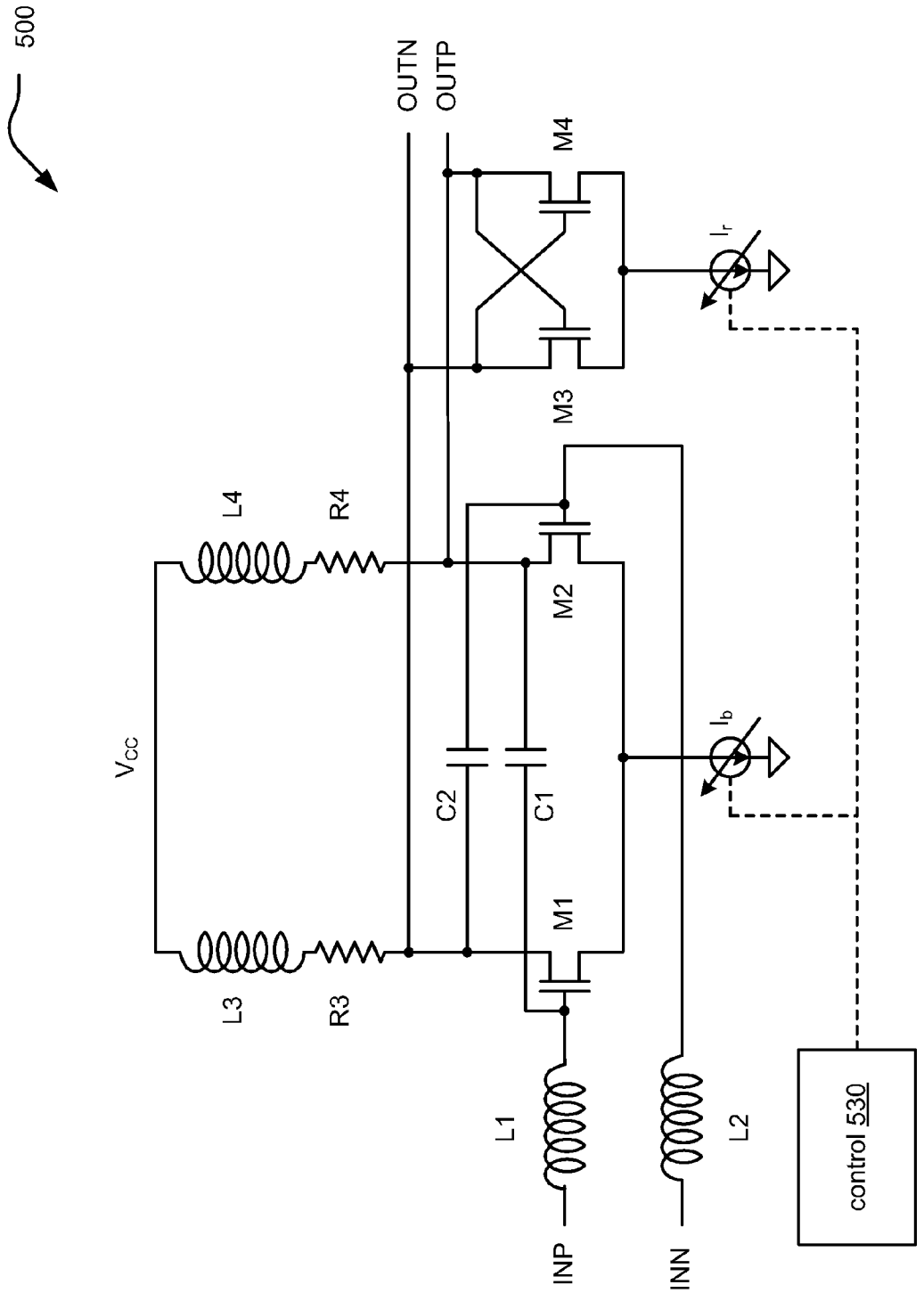

500
OUTN
OUTP
M4
M3
I_r
L4
R4
M2
V_{CC}
I_b
C2
C1
M1
L3
R3
L1
L2
INP
INN
control 530

Fig. 5

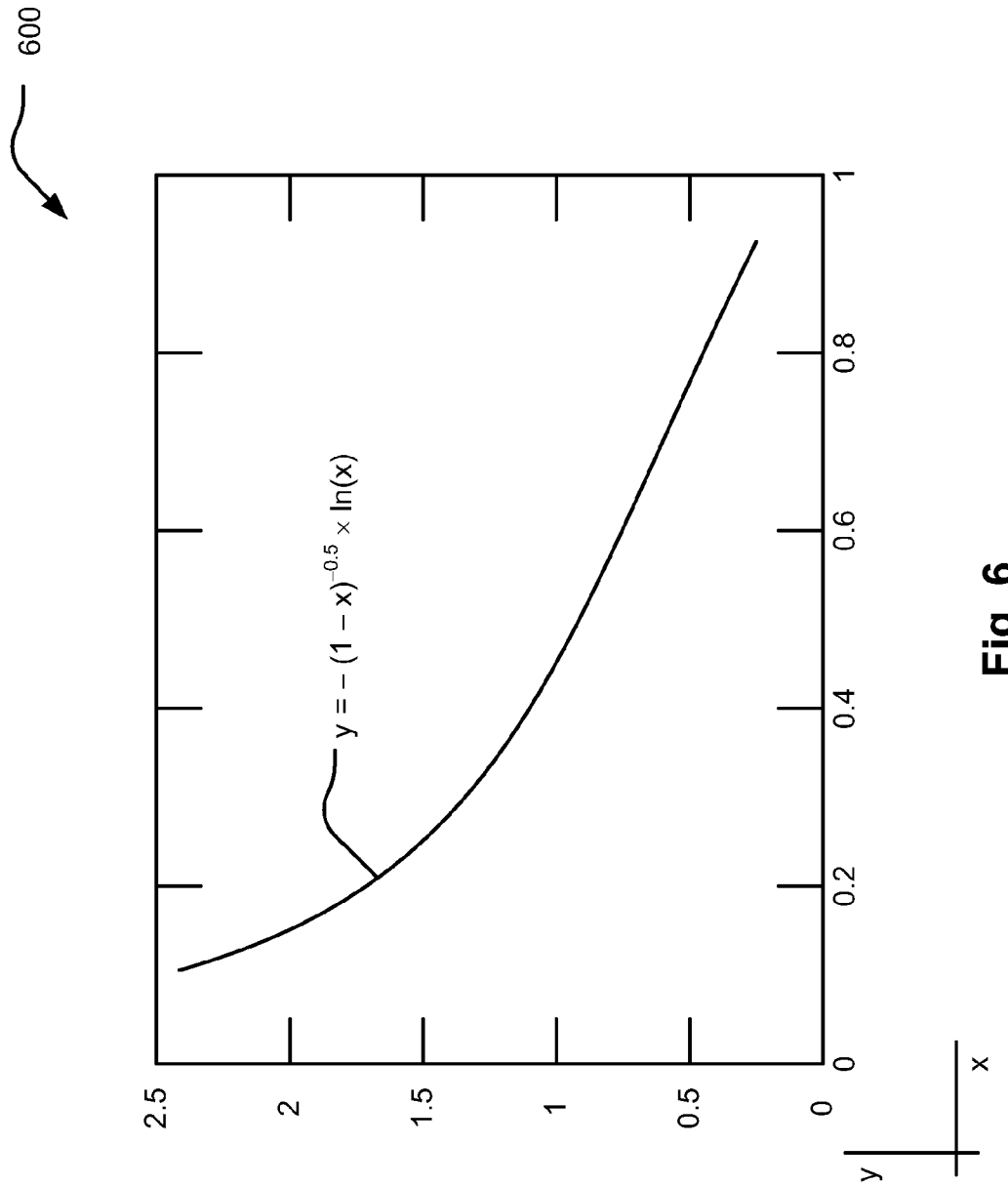


Fig. 6

CURRENT-CONTROLLED CMOS (C3MOS) FULLY DIFFERENTIAL INTEGRATED DELAY CELL WITH VARIABLE DELAY AND HIGH BANDWIDTH

CROSS REFERENCE TO RELATED PATENTS/PATENT APPLICATIONS

Continuation Priority Claim, 35 U.S.C. §120

[0001] The present U.S. Utility patent application claims priority pursuant to 35 U.S.C. §120, as a continuation, to the following U.S. Utility patent application which is hereby incorporated herein by reference in its entirety and made part of the present U.S. Utility patent application for all purposes:

[0002] 1. U.S. Utility application Ser. No. 11/320,401, entitled "Current-controlled CMOS (C3MOS) fully differential integrated delay cell with variable delay and high bandwidth," (Attorney Docket No. BP4881), filed Dec. 28, 2005, pending, and scheduled to be issued as U.S. Pat. No. 7,598,788 on Oct. 6, 2009, which claims priority pursuant to 35 U.S.C. §119(e) to the following U.S. Provisional Patent Application which is hereby incorporated herein by reference in its entirety and made part of the present U.S. Utility patent application for all purposes:

[0003] a. U.S. Provisional Application Ser. No. 60/714,814, entitled "Current-controlled CMOS (C3MOS) fully differential integrated delay cell with variable delay and high bandwidth," (Attorney Docket No. BP4881), filed Sep. 6, 2005, now expired.

INCORPORATION BY REFERENCE

[0004] The following U.S. Utility patent applications are hereby incorporated herein by reference in their entirety and made part of the present U.S. Utility Patent Application for all purposes:

[0005] 1. U.S. Utility patent application Ser. No. 09/484,856, entitled "Current-controlled CMOS logic family," (Attorney Docket No. BP1645), filed Jan. 18, 2000, now U.S. Pat. No. 6,424,194 B1, issued on Jul. 23, 2002.

[0006] 2. U.S. Utility patent application Ser. No. 09/610,905, entitled "Current-controlled CMOS circuits with inductive broadbanding," (Attorney Docket No. BP1652), filed Jul. 6, 2000, now U.S. Pat. No. 6,340,899 B1, issued on Jan. 22, 2002.

[0007] 3. U.S. Utility patent application Ser. No. 10/028,806, entitled "Current-controlled CMOS wideband data amplifier circuits," (Attorney Docket No. BP1817), filed Oct. 25, 2001, now U.S. Pat. No. 6,624,699 B2 issued on Sep. 23, 2003.

BACKGROUND OF THE INVENTION

[0008] 1. Technical Field of the Invention

[0009] The invention relates generally to the field of communication devices; and, more particularly, it relates to the field of delay cells that can be implemented within such communication devices.

[0010] 2. Description of Related Art

[0011] Data communication systems have been under continual development for many years. In many broadband data communication system application, variable delay cells are employed. In such applications, it is oftentimes desirable to adjust timing control between various components. One such possible implementation of a delay cell is within the context of a delay locked loop (DLL). A common approach to designing a DLL is to employ a number of delay blocks. In the prior art, each of the individual delay blocks can be undesirably power consumptive. It would be desirable to have a delay block design that is more energy efficient.

[0012] For appropriate alignment and control of the various components within a communication system, it is very often desirable to ensure having some means by which the various signal therein can be adjusted to ensure proper alignment and timing. As such, there has been and continues to be a need for better and more efficient means by which delay cells may be implemented within communication systems and within various communication devices within such communication systems.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention is directed to apparatus and methods of operation that are further described in the following Brief Description of the Several Views of the Drawings, the Detailed Description of the Invention, and the claims. Other features and advantages of the present invention will become apparent from the following detailed description of the invention made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0014] FIG. **1** illustrates an embodiment of a current-controlled CMOS (C3MOS) wideband data amplifier circuit.

[0015] FIG. **2** illustrates an embodiment of a variable delay cell.

[0016] FIG. **3** illustrates another embodiment of a variable delay cell.

[0017] FIG. **4** illustrates an embodiment of a two-path adjustable high bandwidth delay cell.

[0018] FIG. **5** illustrates an embodiment of a wideband variable delay cell.

[0019] FIG. **6** illustrates an embodiment of delay through a cross-coupled differential pair (normalized) in response to current in a buffer stage (normalized).

DETAILED DESCRIPTION OF THE INVENTION

[0020] Various embodiments of the invention provide for ultra high-speed logic circuitry implemented in silicon complementary metal-oxide-semiconductor (CMOS) process technology. A distinction is made herein between the terminology "CMOS process technology" and "CMOS logic." CMOS process technology as used herein refers generally to a variety of well established CMOS fabrication processes that form a field-effect transistor over a silicon substrate with a gate terminal typically made of polysilicon material disposed on top of an insulating material such as silicon dioxide. CMOS logic, on the other hand, refers to the use of complementary CMOS transistors (n-channel and p-channel, implemented using NMOS (Negative-Channel Metal-Oxide Semiconductor) transistors or PMOS (Positive-Channel Metal-Oxide Semiconductor) transistors) to form various logic gates and more complex logic circuitry, wherein zero static current is dissipated. Embodiments of the invention use current-controlled mechanisms to develop a family of very fast current-controlled CMOS (C3MOS or C^3MOS^{TM}) logic that can be fabricated using a variety of conventional CMOS process technologies, but that unlike

conventional CMOS logic does dissipate static current. C3MOS logic or current-controlled metal-oxide-semiconductor field-effect transistor (MOSFET) logic are used herein interchangeably.

[0021] Various C3MOS circuit techniques are described in greater detail in commonly-assigned U.S. patent application Ser. No. 09/484,856, now U.S. Pat. No. 6,424,194 B1, entitled "Current Controlled CMOS Logic Family," by A. Hairapetian, which is hereby incorporated by reference in its entirety for all purposes as indicated above.

[0022] Other techniques have been developed to increase the gain-bandwidth product of CMOS circuitry. For example, shunt peaking is one approach that has resulted in improved gain-bandwidth product. Shunt peaking involves putting an inductor in series with the output resistor to expand the bandwidth of the circuit. Such inductive broadbanding technique combined with C3MOS circuitry is described in greater detail in commonly-assigned U.S. patent application Ser. No. 09/610,905, now U.S. Pat. No. 6,340,899 B1, entitled "Current-Controlled CMOS Circuits with Inductive Broadbanding," by M. Green, which is hereby incorporated by reference in its entirety for all purposes as indicated above.

[0023] In commonly-assigned U.S. patent application Ser. No. 10/028,806, now U.S. Pat. No. 6,624,699 B2, entitled "Current-controlled CMOS wideband data amplifier circuits," by Guangming Yin and Jun Cao, which is hereby incorporated by reference in its entirety for all purposes as indicated above, the current-controlled CMOS wideband data amplifier circuits disclosed therein having expanded bandwidth are designed to achieve such the goal of having a flat frequency response over a very wide frequency range, where maximum bandwidth expansion is achieved by using series inductor peaking with Miller capacitance cancellation technique and shunt inductor peaking in current controlled CMOS (C3MOS or Current-controlled CMOS wideband data amplifier circuits) circuits.

[0024] FIG. **1** illustrates an embodiment **100** of a current-controlled CMOS (C3MOS) wideband data amplifier circuit. A current source transistor can be biased by a bias voltage so that a constant current flows from drain to source in the current source transistor. Two separate differential transistors compose a wideband differential transistor pair. A first differential transistor has its gate tied to the negative end of a first series peaking inductor L**1**, while a positive differential input signal INP is coupled to the positive end of the first series peaking inductor L**1**. Similarly, a second differential transistor has its gate tied to the negative end of a second series peaking inductor L**2**, while a negative differential input signal INN is coupled to the positive end of the second series peaking inductor L**2**.

[0025] Assuming that the first and second differential transistors are identical, then the first and second series peaking inductors L**1** and L**2** have the same inductance. A first output resistor R**3** has its negative end tied to the drain of the first differential transistor, and has its positive end tied to the negative end of a first shunt peaking inductor L**3**. A second output resistor R**4** has its negative end tied to the drain of the second differential transistor, and has its positive end tied to the negative end of a second shunt peaking inductor L**4**. The positive ends of the first and second shunt peaking inductors L**3** and L**4** are tied to the positive supply voltage (shown as V_{CC}).

[0026] Preferably, the first and second output resistors R**3** and R**4** have the same resistance value R, and the first and second shunt peaking inductors L**3** and L**4** have the same inductances. A first capacitor C**1** (which may be referred to as a first Miller cancellation capacitor C**1**) has its positive end coupled to the drain of the second differential transistor, and has its negative end coupled to the gate of the first differential transistor. A second capacitor C**2** (which may be referred to as a second Miller cancellation capacitor C**2**) has its positive end coupled to the drain of the first differential transistor, and has its negative end coupled to the gate of the second differential transistor. A first output signal OUTP is taken at the drain of the second differential transistor, and the second output signal OUTN is taken at the drain of the first differential transistor.

[0027] Input series inductors (L**1** and L**2**) resonate with the capacitance at the input of the differential pair at high frequencies and thus extend the bandwidth of the amplifier. In addition, at high frequencies, the inductors (L**1** and L**2**) act as high impedance chokes between the termination resistors (shown as two series connected 50Ω resistors) and the capacitors and thus also improve the input reflection for the C3MOS wideband data amplifier circuit of this embodiment **100**.

[0028] FIG. **2** illustrates an embodiment **200** of a variable delay cell. As mentioned above, there is a need in the art for delay cells within many broadband data communication applications. Also, variable delay cells provide for even greater flexibility and applicability than fixed delay type delay cells. This embodiment **200** shows a basic building block of a data synchronization circuit. The input data (DIN) is retimed by a flip-flop (FF) **220** driven by a clock signal (CLK). For the FF **220** to operate correctly, the input data (DIN) and clock (CLK) must satisfy one or more certain timing requirements. A delay cell **210** is often inserted between the input data (DIN) and the FF **220** so that the timing relation between the clock (CLK) and data (DIN) at the input of the FF **220** can be adjusted to compensate for any phase variations of the input signals or circuit delay variations due to changes in process, voltage supply or temperature (PVT). As the input data (DIN) runs at an ever increasing rate, the delay cell needs to have continuously higher and higher bandwidth in order to preserve the signal integrity of the input data.

[0029] FIG. **3** illustrates another embodiment **300** of a variable delay cell. This embodiment **300** is another example by which a variable delay cell can be employed. The embodiment **300** is a 5-tap finite impulse response (FIR) filter that is constructed to process the input data (DIN). For the FIR filter to work as designed, each delay cell (i.e., delay cells **310**, **320**, **330**, and **340**) should have the same delay in time which is usually inversely proportional to the data rate. Similar to the embodiment **200** of the FIG. **2**, variable delay cells are desirable to compensate the circuit delay variations due to changes in PVT conditions. Furthermore, if the input data rate may vary, the delay cell also needs to provide corresponding changes in delay. Since multiple delay cells (i.e., delay cells **310**, **320**, **330**, and **340**) are usually connected in tandem, it's very important for the delay cells to have relatively high bandwidth in regard to the data rate.

[0030] In the embodiment **300** of a variable delay cell implemented using a 5-tap FIR filter, a goal is to have a data stream with an equal delay (e.g., Δt_n) between each of the various components of the data stream. In the embodiment **300**, there are 5 components of the data stream. Typically, this delay (e.g., Δt_n) is the same, and the delays of each of these delay cells **310**, **320**, **330**, and **340** may be adjusted together.

[0031] Another possible embodiment by which a variable delay cell can be implemented is to add a variable capacitive load at the output of conventional data buffers (e.g., differential pairs). However, there is a fundamental limitation on such an approach. For those circuits whose small-signal transfer function can be approximated by a single-pole response, the bandwidth and delay are directly coupled together. For example, the 10%-90% rise/fall time in response to an input step equals to 0.35/BW (where BW is the −3 dB bandwidth of the small signal response of the circuit). The larger is the delay amount, then the smaller is the bandwidth. As a result, the minimum bandwidth requirement on the delay cell puts an upper limit of the delay amount if such a circuit is employed. On the other hand, the smaller is the delay amount, then the larger is the bandwidth the circuit needs to have, which usually means more power and larger area the delay cell needs to have if a simple single-pole buffer is employed.

[0032] FIG. **4** illustrates an embodiment **400** of a two-path adjustable high bandwidth delay cell. This embodiment **400** employs two separate data paths for the input data. One of the data paths has a relatively smaller amount of propagation delay (shown as buffer(s) with small delay **410**), and the other of the data paths has a relatively larger amount of propagation delay (shown as buffer(s) with large delay **420**). The signal passes through the two different paths are then combined together at a summing stage. The relative strength of the two paths can be adjusted (using a control block **430**) and thus enable the overall data path to have a variable delay. To implement the slow path, several fast buffers can be connected in series in order to have a large enough propagation delay while preserving signal integrity.

[0033] For transmission rates of 10 Gbps (Giga-bits per second) or higher, CMOS data buffers generally consume a significant amount of power due to limitations of the technology. In the two-path embodiment **400** of the FIG. **4** for a variable delay cell, at least three high-speed blocks need to be powered up, including the summer. The summer is especially power consumptive because it has two pairs of full-rate data input which will add a significant amount lot of parasitic loading to the high speed data path. Furthermore, the input data are connected to both the quick path and the slow path. If this combined input is connected to the output of a front buffer, this configuration will significantly increase the loading to the previous stage and thus reduce the overall bandwidth of the data path. If the combined input is connected to the input pads of the chip directly, it will cause a severe degradation of the matching between the input of the receiver and the traces on the printed circuit board (PCB) due to the excessive capacitance loading. This results in large amount of reflections and will degrade the integrity of the input data significantly. Another potential issue of the two path implementation is when the signals that have been passed going through the two different paths are combined together at the summer, additional jitter may be generated if the delay between the two path differs significantly. It would be most desirable to have a high bandwidth variable delay cell that would not have increased power and loading requirements across a wide variety of applications.

[0034] The embodiment **400** mixes two types of buffers together: a slow buffer and a fast buffer. The larger delay that is required or desired in a particular application inherently incurs a lower bandwidth in the embodiment **400**. The lower bandwidth in such an instance acts as a low pass filter (LPF). This LPF filtering may corrupt the signal undesirably due to the low frequency cut-off. Undesirable inter-symbol Interference (ISI) may also be introduced because of this LPF filtering. In very high speed, broadband application, such effects can significantly reduce overall performance.

[0035] FIG. **5** illustrates an embodiment **500** of a wideband variable delay cell. In this embodiment **500**, the input of the signal is connected to a current-controlled CMOS (C3MOS) wideband data amplifier circuit having expanded bandwidth that is similar to the embodiment **100** of the FIG. **1**. The operation of such a wideband data amplifier circuit having expanded bandwidth is also described in commonly-assigned U.S. patent application Ser. No. 10/028,806, now U.S. Pat. No. 6,624,699 B2, entitled "Current-controlled CMOS wideband data amplifier circuits," by Guangming Yin and Jun Cao. In such a C3MOS wideband data amplifier circuit having expanded bandwidth, maximum bandwidth expansion is achieved by using series inductor peaking with miller capacitance cancellation technique and shunt inductor peaking in current controlled CMOS circuit (C3MOS or C3MOS).

[0036] Connected to the output of the wideband data buffer having expanded bandwidth (that includes the differential transistor pair M**1** and M**2**, i.e. a wideband differential transistor pair) is a cross-coupled differential pair (that includes the differential transistor pair M**3** and M**4**, i.e. a cross-coupled differential transistor pair) as the regenerative stage for the data. In this embodiment **500**, there are therefore two very fast operating blocks [(1) wideband data buffer and (2) cross-coupled differential pair] that operate cooperatively to perform the functionality of a wideband variable delay cell that is appropriate for broadband applications.

[0037] To vary the delay, the currents of the buffer stage and the cross-coupled differential pair stage can be adjusted (e.g., using a control block **530**). When all the current passes through the buffer stage and the cross-coupled differential pair stage current source is turned off, the circuit behaves just like a wideband data amplifier having expanded bandwidth as described and referenced above (i.e., the embodiment **100** of the FIG. **1** and within U.S. Pat. No. 6,624,699 B2). With the high bandwidth achieved by various design skills, the delay through the delay cell can be very small. To increase the delay, the current going through the buffer stage is reduced and the current going through the cross-coupled differential pair stage is increased by the same amount. For the output signal to reach full swing, it has to go through the regenerative process at the cross-coupled differential pair to be amplified, and thus the delay is increased. A first-order analysis of the embodiment **500** of such a variable delay cell can be done based on a two-step approximation, as shown below.

[0038] Since the buffer stage of the variable delay cell has very high bandwidth, the delay from input to output at this stage is very small. It is reasonable to assume the delay through the buffer stage is a relatively constant value (denoted as T_b); the delay variation of the delay cell is mostly contributed by the regenerative process of the cross-coupled differential pair stage (denoted as T_r). In the two-step approximation, the signal through the delay cell is divided into two steps. In the first step, the signal V_{in} is buffered by the input stage and appear at the output after a delay of T_0, taking a value of $V_m \cdot V_m$ is equal to the current passing through the buffer stage (I_b) times the load resistance (R). In the second step, the signal V_m at the input of the cross-coupled differential pair goes through the positive feedback of the cross-coupled differential pair and gets regenerated until reaching the value of V_0,

after a delay of T_r. The voltage, V_0, is a fixed value, determined by the total current ($I_0=I_b+I_r$) and load resistance ($V_0=R\cdot I_0$).

[0039] If it assumed that $I_b=x\cdot I_0$, then $I_r=(1-x)\cdot I_0$. The value of x can be changed between 1 and 0, where x=1 means that all the current is going through the buffer stage. At the output, which is also the input of the cross-coupled differential pair (that includes the differential transistor pair M**3** and M**4**), after T_0 of delay $v_m=x\cdot I_0\cdot R$. It is noted that the output voltage of a regenerative cross-coupled differential pair increases exponentially with time and is proportional to the initial voltage as indicated below.

$$V(t)=V_m\cdot e^{(t/\tau)}$$

[0040] where τ is the characteristic time constant of the cross-coupled differential pair, which is inversely proportional to the gain of the cross-coupled differential pair. For CMOS transistors, the gain is proportional to the square root of the biasing current in the first order as indicated below.

$$\tau = \frac{k}{\sqrt{(1-x)\cdot I_0}}$$

$$V(T_r) = V_0 = V_m \cdot e^{(T_r/\tau)}$$

$$T_r = \tau \cdot \ln\left(\frac{V_0}{V_m}\right) = -k \cdot I_0^{-0.5} \cdot (1-x)^{-0.5} \cdot \ln(x)$$

[0041] FIG. **6** illustrates an embodiment **600** of delay through a cross-coupled differential pair (normalized) in response to current in a buffer stage (normalized). This embodiment **600** shows the normalized delay through the cross-coupled differential pair stage, $T_r/(k\cdot I_0^{-0.5})$ as a function of the normalized current in the buffer stage

$$\left(x = \frac{I_b}{I_0}\right).$$

It is evident that as the current passing through the buffer stage becomes smaller, the delay through the cross-coupled differential pair stage becomes bigger. The total delay through the delay cell is $T=T_b+T_r$. Thus by changing the current distribution between the buffer stage (including the differential transistor pair M**1** and M**2**) and cross-coupled differential pair stage (including the differential transistor pair M**3** and M**4**) (i.e., which involves changing the value of x), the amount of the delay can be readily adjusted.

[0042] This control of the two currents, I_b and I_r and their relationship, may be performed using a control block (e.g., control block **530** in the embodiment **500** of the FIG. **5**). It is noted that the total current ($I_0=I_b+I_r$) required in the embodiment **500** is kept constant, but merely the relationship (or relationship) between these 2 currents, I_b and I_r, is controlled thereby controlling the overall delay. For example, a variable delay of such a variable delay cell circuit can be controlled by adjusting at least one of a first current, b, in a first variable current source and a second current, I_r in the second variable current source. A variable delay of such a variable delay cell circuit can be controlled can be viewed as being a function of a ratio of a first current, I_b, in the first current source divided by a sum that includes the first current in the first current source and the second current in the second current source (e.g., total current ($I_0=I_b+I_r$)). Also, because this total current ($I_0=I_b+I_r$) remains unchanged, then the DC level of the delay cell output incurred by the load resistance also remains unchanged.

[0043] As the value of x approaches 1, then the total delay a variable delay cell (e.g., the embodiment **500** of the FIG. **5**) approaches the delay of the wideband data buffer (that includes the differential transistor pair M**1** and M**2**). As the value of x approaches 0 (zero), then the total delay a variable delay cell (e.g., the embodiment **500** of the FIG. **5**) approaches the maximum possible delay of the device that includes the delay of both the wideband data buffer (that includes the differential transistor pair M**1** and M**2**) and the cross-coupled differential pair (that includes the differential transistor pair M**3** and M**4**).

[0044] Various embodiments of the invention presented herein provide for a large amount of delay to be incurred (which is selectable and variable, as desired in any of a wide variety of applications) with a minimal amount of signal quality degradation (i.e., minimal or no ISI).

[0045] One of many advantages of this novel design is that all the bandwidth extension techniques as referenced above with respect to a wideband data amplifier circuit having expanded bandwidth can be readily applied to the variable delay cell. In the embodiment **500** of FIG. **5**, series input inductors L**1** and L**2**, shunt peaking inductors L**3** and L**4**, and negative miller capacitors C**1** and C**2** are all added so that the stage including differential transistor pair M**1** and M**2** can achieve high bandwidth with minimum increase of power. As the bandwidth of the buffer stage increases, a lower end of the delay value reduces and thus the variable delay range is increased without compromising the signal integrity. In addition, as the buffer stage becomes much faster than the cross-coupled differential pair stage, the predictions of the two-step approximation become more accurate.

[0046] By eliminating the double path (as depicted in the embodiment **400** of the FIG. **4**), the embodiment **500** of the FIG. **5** shows an integrated delay cell that does not require the summing stage and thus reduces the power significantly. There is no extra capacitive loading added to the high speed path at the input. The additional capacitance due to the drains of the cross-coupled differential pair transistors at the output can be easily compensated by the shunt inductor. As a result, it is much easier to incorporate the integrated stage into the data path without compromising the signal integrity or degrading the impedance matching.

[0047] From the embodiment **500** of the FIG. **5**, it is clear that the amount of delay can be changed continuously by implementing continuous control signals for the two current sources (i.e., using control block **530**). A programmable delay cell can also be readily implemented by replacing the two current sources (I_b and I_r) with a series of smaller current source, each can be turned on or off using digital control signals.

[0048] In summary, a fully differential current-controlled CMOS (C3MOS) integrated wideband delay cell is presented herein. At the buffer stage, bandwidth extension techniques such as shunt peaking, series inductive peaking can be readily applied to increase the range of the flat frequency response. A cross-coupled differential pair stage is added to the output of the buffer to add delay from input to output through the regenerative process of the cross-coupled differential transistor pair connected in a positive feedback configuration. The delay can be adjusted by varying the current distribution between the buffer stage and the cross-coupled differential

pair stage. The integrated delay cell can then accommodate a large amount of delay while at the same time maintain a high bandwidth for the data path, without adding load to the input and without adding power consumption.

[0049] It is also noted that the methods described within the preceding figures can also be performed within any appropriate system and/or apparatus design (communication systems, communication transmitters, communication receivers, communication transceivers, and/or functionality described therein) without departing from the scope and spirit of the invention.

[0050] In view of the above detailed description of the invention and associated drawings, other modifications and variations will now become apparent. It should also be apparent that such other modifications and variations can be effected without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit, comprising:

a first differential transistor having a first source, a first gate that is operative to receive a first differential input, and a first drain;

a second differential transistor having a second source that is connected to the first source, a second gate that is operative to receive a second differential input, and a second drain;

a third differential transistor having a third source, a third gate, and a third drain;

a fourth differential transistor having a fourth source that is connected to the third source, a fourth gate, and a fourth drain;

wherein the first drain, the third drain, and the fourth gate are connected at a first node that is a first differential output;

wherein the second drain, the fourth drain, and the third gate are connected at a second node that is a second differential output;

a first variable current source transistor having a fifth drain connected to the connected first source and second source, having a fifth gate, and having a fifth source that is grounded;

a second variable current source transistor having a sixth drain connected to the connected third source and fourth source, having a sixth gate, and having a sixth source that is grounded; and

a control module that is operative to adjust a delay of the circuit by adjusting a first DC bias voltage provided to the fifth gate to set a first DC bias current in the first variable current source transistor and by adjusting a second DC bias voltage provided to the sixth gate to set a second DC bias current in the second variable current source transistor.

2. The circuit of claim **1**, wherein:

the control module that is operative to keep a sum of the first DC bias current and the second DC bias current constant.

3. The circuit of claim **1**, further comprising:

a first inductor connected to the first gate; and

a second inductor connected to the second gate.

4. The circuit of claim **1**, further comprising:

a first impedance component whose ends are connected to the first drain and to a power supply voltage of the circuit, respectively; and

a second impedance component whose ends are connected to the second drain and to the power supply voltage of the circuit, respectively.

5. The circuit of claim **4**, wherein:

the first impedance component includes a first output resistor and a first inductor connected in series; and

the second impedance component includes a second output resistor and a second inductor connected in series.

6. The circuit of claim **1**, further comprising:

a first capacitor whose ends are connected to the first drain and to the second gate, respectively; and

a second capacitor whose ends are connected to the second drain and to the first gate, respectively.

7. The circuit of claim **1**, wherein:

the sum of the first DC bias current and the second DC bias current being constant keeps a DC level of the first differential output and the second differential output constant.

8. The circuit of claim **1**, wherein:

the delay of the circuit is a function of a ratio of the first DC bias current divided by the sum of the first DC bias current and the second DC bias current.

9. The circuit of claim **1**, wherein:

the circuit is one delay cell of a plurality of delay cells implemented within an n-tap finite impulse response (FIR) filter.

10. The circuit of claim **1**, further comprising:

a flip-flop (FF); and wherein:

the first node and the second node are connected to an input of a FF; and

the FF is operative to receive a clock signal.

11. The circuit of claim **1**, wherein:

the first differential transistor, the second differential transistor, the third differential transistor, the fourth differential transistor, the first variable current source, and the second variable current source are NMOS (Negative-Channel Metal-Oxide Semiconductor) transistors.

12. A circuit, comprising:

a first differential transistor having a first source, a first gate, and a first drain;

a second differential transistor having a second source that is connected to the first source, a second gate, and a second drain;

a first inductor whose ends are connected to a first differential input and to the first gate, respectively;

a second inductor whose ends are connected to a second differential input and to the second gate, respectively;

a third differential transistor having a third source, a third gate, and a third drain;

a fourth differential transistor having a fourth source that is connected to the third source, a fourth gate, and a fourth drain;

wherein the first drain, the third drain, and the fourth gate are connected at a first node that is a first differential output;

wherein the second drain, the fourth drain, and the third gate are connected at a second node that is a second differential output;

a first variable current source transistor having a fifth drain connected to the connected first source and second source, having a fifth gate, and having a fifth source that is grounded;

a second variable current source transistor having a sixth drain connected to the connected third source and fourth source, having a sixth gate, and having a sixth source that is grounded; and

a control module that is operative to:

adjust a delay of the circuit by adjusting a first DC bias voltage provided to the fifth gate to set a first DC bias current in the first variable current source transistor and by adjusting a second DC bias voltage provided to the sixth gate to set a second DC bias current in the second variable current source transistor;

the control module that is operative to keep a sum of the first DC bias current and the second DC bias current constant.

13. The circuit of claim **12**, further comprising:

a first impedance component whose ends are connected to the first drain and to a power supply voltage of the circuit, respectively; and

a second impedance component whose ends are connected to the second drain and to the power supply voltage of the circuit, respectively.

14. The circuit of claim **13**, wherein:

the first impedance component includes a first output resistor and a first inductor connected in series; and

the second impedance component includes a second output resistor and a second inductor connected in series.

15. The circuit of claim **12**, further comprising:

a first capacitor whose ends are connected to the first drain and to the second gate, respectively; and

a second capacitor whose ends are connected to the second drain and to the first gate, respectively.

16. The circuit of claim **12**, wherein:

the sum of the first DC bias current and the second DC bias current being constant keeps a DC level of the first differential output and the second differential output constant.

17. The circuit of claim **12**, wherein:

the delay of the circuit is a function of a ratio of the first DC bias current divided by the sum of the first DC bias current and the second DC bias current.

18. A circuit, comprising:

a first differential transistor having a first source, a first gate that is operative to receive a first differential input, and a first drain;

a second differential transistor having a second source that is connected to the first source, a second gate that is operative to receive a second differential input, and a second drain;

a first capacitor whose ends are connected to the first drain and to the second gate, respectively;

a second capacitor whose ends are connected to the second drain and to the first gate, respectively;

a third differential transistor having a third source, a third gate, and a third drain;

a fourth differential transistor having a fourth source that is connected to the third source, a fourth gate, and a fourth drain;

wherein the first drain, the third drain, and the fourth gate are connected at a first node that is a first differential output;

wherein the second drain, the fourth drain, and the third gate are connected at a second node that is a second differential output;

a first variable current source transistor having a fifth drain connected to the connected first source and second source, having a fifth gate, and having a fifth source that is grounded;

a second variable current source transistor having a sixth drain connected to the connected third source and fourth source, having a sixth gate, and having a sixth source that is grounded; and

a control module that is operative to:

adjust a delay of the circuit by adjusting a first DC bias voltage provided to the fifth gate to set a first DC bias current in the first variable current source transistor and by adjusting a second DC bias voltage provided to the sixth gate to set a second DC bias current in the second variable current source transistor; and

keep a sum of the first DC bias current and the second DC bias current constant thereby keeping a DC level of the first differential output and the second differential output constant; and wherein:

the delay of the circuit is a function of a ratio of the first DC bias current divided by the sum of the first DC bias current and the second DC bias current.

19. The circuit of claim **18**, further comprising:

a first impedance component whose ends are connected to the first drain and to a power supply voltage of the circuit, respectively; and

a second impedance component whose ends are connected to the second drain and to the power supply voltage of the circuit, respectively.

20. The circuit of claim **18**, wherein:

the first differential transistor, the second differential transistor, the third differential transistor, the fourth differential transistor, the first variable current source, and the second variable current source are NMOS (Negative-Channel Metal-Oxide Semiconductor) transistors.

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