

[54] CAPACITIVELY DRIVEN CHARGE
TRANSFER DEVICES

[72] Inventor: George Elwood Smith, Murray Hill,
N.J.

[73] Assignee: Bell Telephone Laboratories, Incor-
porated, Murray Hill, N.J.

[22] Filed: March 29, 1971

[21] Appl. No.: 128,999

[52] U.S. Cl. 307/304, 317/235 R, 317/235 G,
307/221 C

[51] Int. Cl. H011 11/14

[58] Field of Search 317/235 B, 235 G; 307/304,
307/221

[56] References Cited
UNITED STATES PATENTS

3,623,026	11/1971	Engeler	317/235
3,651,349	3/1972	Kahng et al.....	317/235

Primary Examiner—Jerry D. Craig
Attorney—R. J. Guenther and Arthur J. Torsiglieri

[57] ABSTRACT

This application describes arrangements for capaci-
tively driving a charge transfer device. In particular, a
charge transfer device is disposed between the plates
of a capacitor and is adapted such that the desired
unidirectionality of transfer of charge therethrough is
achieved in response to application of an alternating
potential to the capacitor.

12 Claims, 5 Drawing Figures

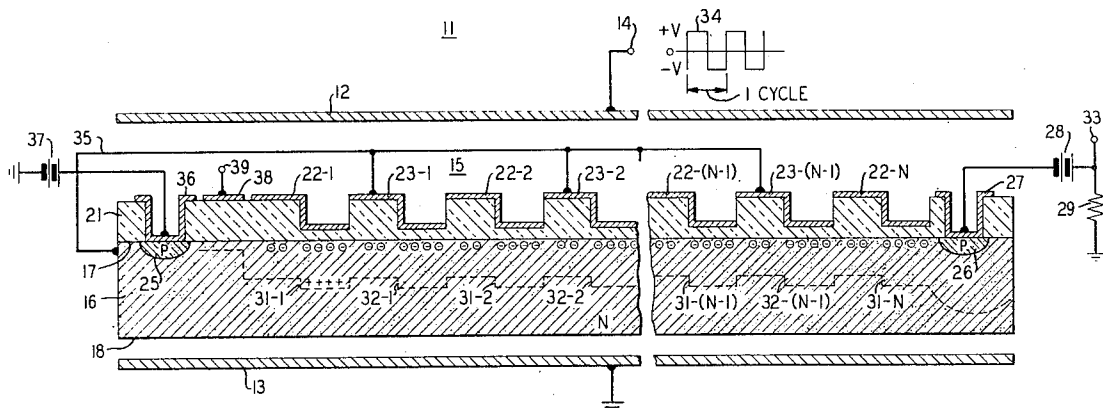
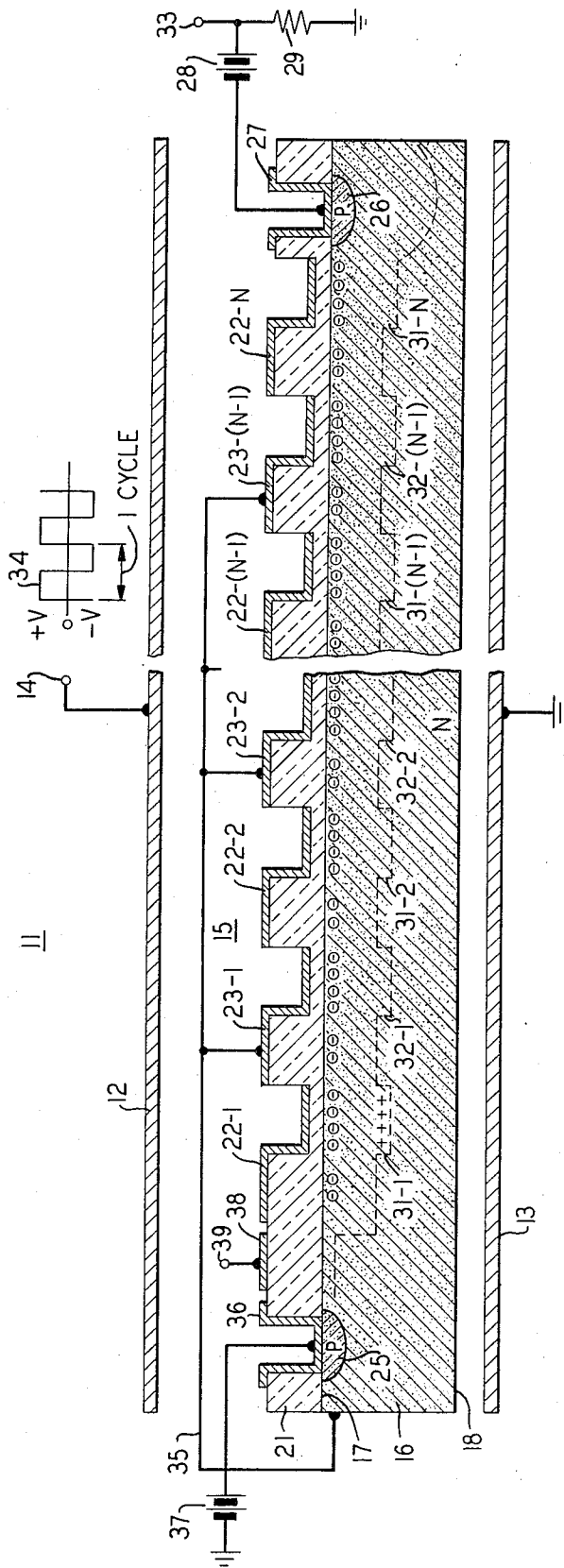


FIG. 1



INVENTOR
G. E. SMITH
BY
A. J. Torsigliesi
ATTORNEY

FIG. 2

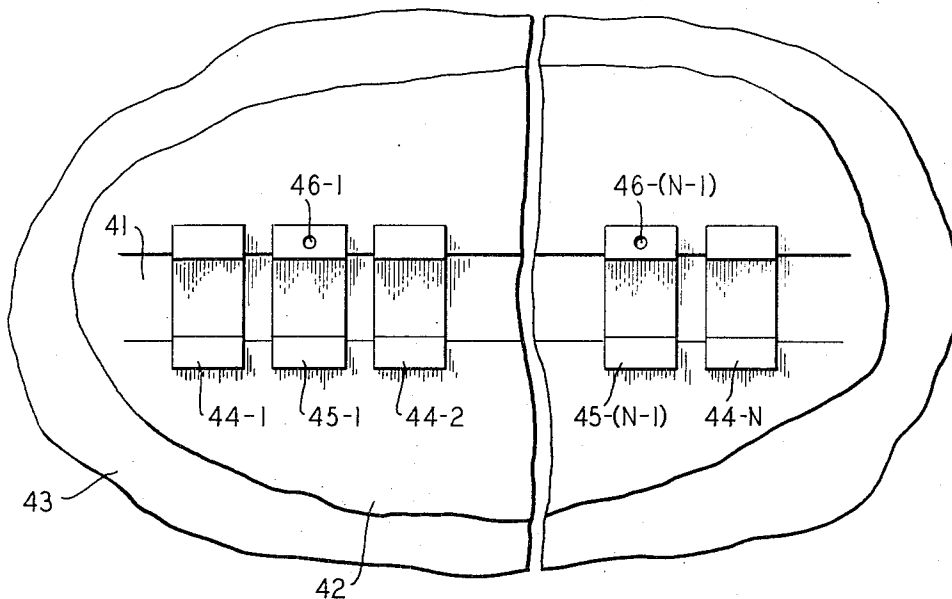


FIG. 3

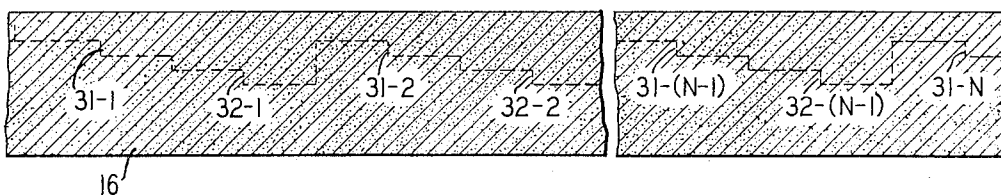


FIG. 4

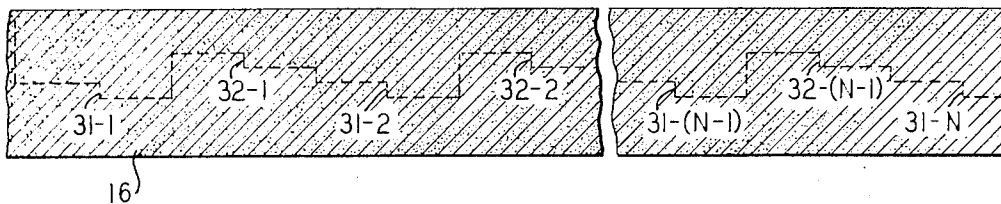
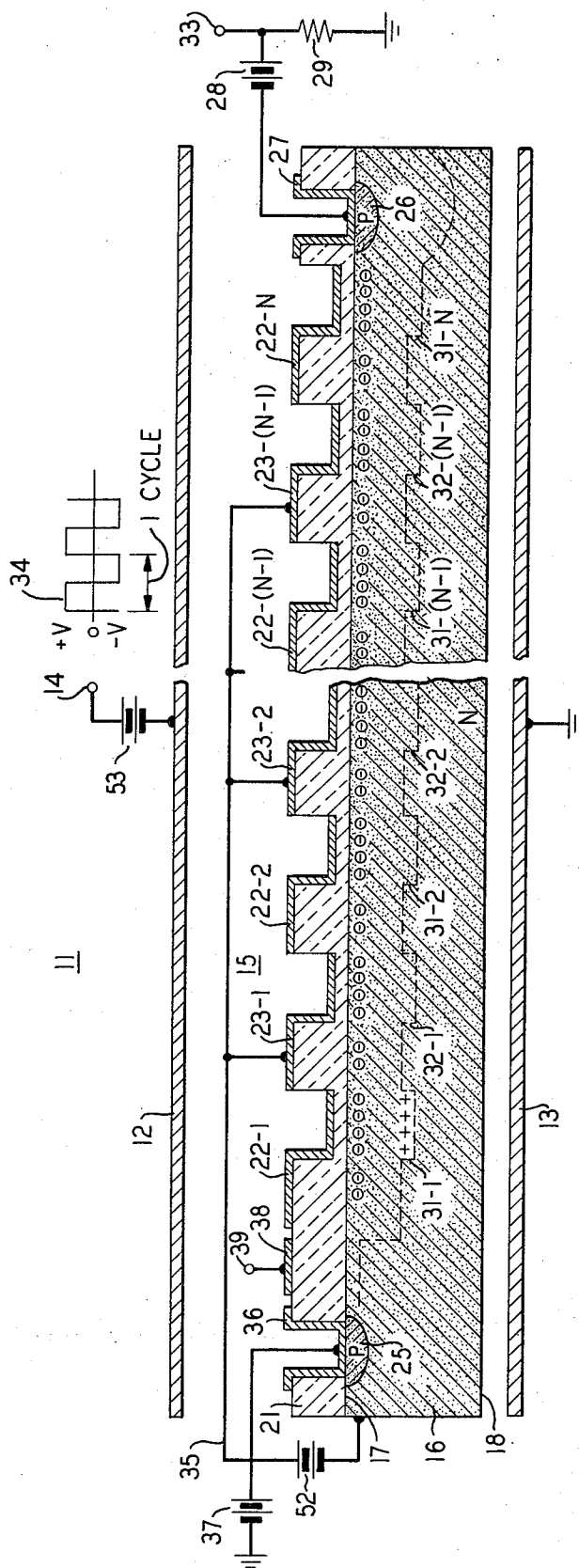


FIG. 5



CAPACITIVELY DRIVEN CHARGE TRANSFER DEVICES

BACKGROUND OF THE INVENTION

This invention relates to charge transfer devices and, more particularly, to arrangements for capacitively driving such devices.

In United States Pat. application Ser. No. 11,541 filed Feb. 16, 1970, now abandoned by W. S. Boyle and G. E. Smith and assigned to the assignee hereof, there is disclosed a new class of devices, referred to therein as "charge transfer devices," which are adapted for storing and sequentially transferring electronic signals representing information in the form of packets of mobile charge localized in artificially induced potential wells, e.g., such as can be associated with a metal-insulator-semiconductor (MIS) structure. Essentially, in the MIS embodiments, a plurality of metal field plate electrodes are disposed in a row over the insulator (dielectric) which, in turn, overlies and is contiguous with the surface of a storage medium which comprises a semiconductor body. Sequential application of drive voltages to the metal field plate electrodes induces potential wells adjacent the surface of the semiconductor body in which packets of excess charge carriers can be stored and between which these packets can be transferred. Heretofore, as disclosed in U. S. Pat. No. 3,651,349 filed on Feb. 16, 1970, and issued Mar. 21, 1972, to D. Kahng et al. at least two clock signals have been used to effect unidirectional transfer of charge packets between potential wells. This is a problem for some applications in that separate conduction paths must be used for each clock signal. It is usually desirable to minimize the number of conduction paths (and attendant conduction path cross-overs) in charge transfer devices.

It is, therefore, a broad object of the present invention to provide an arrangement by which charge transfer within a charge transfer device can be accomplished using a reduced number of conduction paths and a single clock signal.

SUMMARY OF THE INVENTION

In accordance with a broad aspect of the invention, a charge transfer device (CTD) is disposed between the plates of a capacitor and is adapted such that the desired unidirectionality of transfer of charge is achieved in response to application of an alternating potential to the capacitor.

In one embodiment, such adaptation is accomplished by asymmetrically distributing charge under each CTD field plate electrode for inducing thereunder an asymmetrical potential well and, additionally, by conductively coupling every second one of the field plate electrodes to the CTD storage medium.

In response to an electric field produced within the capacitor, voltage differences are induced between the storage medium and each of the field plate electrodes other than every second field plate electrode. These voltage differences, in turn, increase or diminish the depths of the potential wells induced by the asymmetrical charge distribution under their associated field plate electrodes. The field within the capacitor does not induce voltage differences between the storage medium and each of the second field plate electrodes because each of these electrodes is conductively cou-

pled to the medium. Thus, the potential wells induced by the charge distribution under the second field plate electrodes are isolated from the electric field and do not change depth in response thereto. Charge is moved unidirectionally through the CTD by varying the field within the capacitor such that the depths of the responsive potential wells are increased above and then diminished below the depths of the nonresponsive potential wells.

In another embodiment, such adaptation is achieved by applying constant voltage biases to the field plate electrodes and, additionally, by employing a dielectric layer of nonuniform thickness under each electrode. More particularly, the bias applied to every second one of the field plate electrodes is provided by an external source coupled between each electrode and the storage medium. The bias applied to the remaining electrodes, on the other hand, is provided by impressing a bias voltage to the capacitor.

The bias applied to each field plate electrode induces thereunder an asymmetrical potential well. The induced wells are asymmetrical because of the nonuniform thickness of the dielectric layer under their respective field plate electrodes. In response to a voltage superimposed on the bias voltage applied to the capacitor, the depths of the potential wells induced by the latter bias voltage are diminished or increased in depth. Suitable variation of the superimposed voltage, in turn, causes the depths of the potential wells, responsive thereto, to vary in depth such that charge introduced into the CTD is transferred therethrough.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood from the following more detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 shows a cross-sectional view of an arrangement for transferring charge through a charge transfer device, in accordance with the principles of the present invention;

FIG. 2 shows a top view of one way of fabricating the charge transfer device of FIG. 1;

FIGS. 3 and 4, included for the purposes of explanation, illustrate the approximate shapes of the potential wells in the charge transfer device of FIG. 1 during different half cycles of an applied clock signal; and

FIG. 5 shows a cross-sectional view of a modification of the embodiment of FIG. 1.

DETAILED DESCRIPTION

In FIG. 1 is shown apparatus 11 for effecting charge transfer in a charge transfer device, in accordance with the principle of the present invention.

Apparatus 11 comprises first and second conductive plates 12 and 13, which form a capacitor C_1 . One plate of capacitor C_1 (i.e., plate 12) is coupled to a control or clock terminal 14. The other plate (i.e., plate 13) is coupled to electrical ground.

Disposed between capacitor plates 12 and 13 is a CTD 15. The latter device has a storage medium which includes a semiconductor bulk portion 16 of a first type of conductivity (shown here illustratively as N-type). Semiconductor portion 12 has two major surfaces 17 and 18. Overlying surface 17 and contiguous therewith is an insulator (dielectric) layer 21. This layer is

preferably of nonuniform thickness, as is shown, but a layer of uniform thickness can also be employed. Serially disposed along layer 21 are a plurality of field plate electrodes 22-1, 23-1, 22-2, . . . 23-(N-1), 22-N. Each field plate electrode overlies a portion of the layer having two distinct thicknesses. In particular, the insulator is thickest under the left most portion of each field plate electrode and thinnest under the rightmost portion of each field plate electrode.

Typically, an actual structure for device 15 might employ 10 ohm-cm N-type silicon for bulk portion 16. The insulator layer 21 could be silicon oxide having a thickness of about 1000 Å. over its thin portions and a thickness of about 3000 Å. over its thick portions. Each of the field plate electrodes might be a two level metalization arrangement in which the first metallic level is highly doped silicon and the second metallic level is aluminum. For field plate electrodes of the latter type, the spacing between each electrode typically might be about 1000 Å.

As will be described hereinbelow, pulses representing information are coupled into device 15 by means of a localized P-type zone 25, in combination with an electrode 36 which makes a low resistance contact thereto, a battery 37, an electrode 38, which is adjacent to electrode 36, and an input port 39 which is connected to electrode 38.

Detection of any excess minority carriers which may be in the potential well under the last field plate electrode 22-N is accomplished by means of a localized P-type zone 26, in combination with an electrode 27, which makes a low resistance contact thereto, a battery 28 and a resistor 29, as is also described in greater detail hereinbelow.

Each of the electrodes 23 are conductively coupled to semiconductor portion 16. Preferably such coupling is realized by internal connection within the device 15 itself. An actual structure having such internal interconnections might be fabricated as illustrated in FIG. 2. In FIG. 2, a channel 41 of thin nonuniform dielectric is cut in a thick outside dielectric layer 42. The thick outside layer 42, in turn, overlies and is contiguous with a semiconductor layer 43. Serially disposed along channel 41 and contiguous therewith are a plurality of metallic electrodes 44-1, 45-1, 44-2, . . . 45-(N-1), 44-N. Portions of each electrode extend beyond the ends of channel 41 and are contiguous with layer 42. Holes 46-1, . . . 46-(N-1) are cut through the portions of electrodes 45 which lie outside channel 41. These holes extend through layer 42 to semiconductor 43, and are filled with a conductive material to effect electrical connection between the latter electrodes and the semiconductor.

In FIG. 1, however, the coupling between electrodes 23 and the semiconductor 16 is schematically illustrated by showing each electrode coupled to a common electrical path 35, which in turn is connected to semiconductor 16.

CTD 15 is disposed between capacitor plates 12 and 13 such that its surface 18 faces plate 13, and its field plate electrodes face plate 12. As shown, the plates 12 and 13 extend over the entire length of the device 15, but it should be noted that plates which extend only over that portion of the device between the first field plate electrode 22-1 and the last field plate electrode 22-N, can also be employed.

It will be appreciated that FIG. 1 is intended to be only a schematic representation. The actual structure might be fabricated, for example, by depositing a dielectric layer over device 15, and then appropriately depositing thereon a first conductive layer to provide plate 12 and a second conductive layer to provide plate 13.

As shown in FIG. 1, quantities of fixed negative charge, indicated as "θ," are disposed near the semiconductor dielectric interface under each of the field plate electrodes of CTD 15. In the instant illustrative embodiment, the fixed negative charge is located in the semiconductor portion 16 of the CTD. Alternatively, the fixed charge could have been disposed in dielectric layer 21. In any case, more negative charge is disposed under the rightmost portion of each field plate electrode and less negative charge is disposed under the rightmost portion of each electrode. It will be appreciated that the fixed charge can be introduced into semiconductor 16 in any well known manner such as, e.g., by ion implantation.

The fixed charge under each field plate electrode induces thereunder, at the semiconductor dielectric interface, an asymmetrical potential well which is more negative under the rightmost portion of the electrode and less negative under the leftmost portion of the electrode. The profiles (31-1 to 31-N and 32-1 to 32-(N-1)), of these induced potential wells are illustrated in FIG. 1. As shown, potential wells 31-1 to 31-N lie under electrodes 22-1 to 22-N, respectively, and potential wells 32-1 to 32-(N-1) lie under electrodes 23-1 to 23-(N-1), respectively.

At this point, it is important to note the affect on the aforesaid built-in potential wells when a voltage is applied between plates 12 and 13 of capacitor C₁. With respect to the potential wells under the electrodes 22, the applied voltage induces a potential which either opposes or aids the existing built-in potentials. It will be appreciated, therefore, that a positive voltage applied to capacitor C₁ decreases the depths of the potential wells under the electrodes 22, while a negative voltage increases the depths of the latter potential wells.

The applied voltage, on the other hand, has no affect on the built-in potential wells under electrodes 23. This is due to the fact that an electric field cannot be externally induced between electrodes 23 and semiconductor 16, since the electrodes and the semiconductor are always at the same potential, as a result of their being conductively coupled.

In operation, an input pulse applied to input terminal 39 causes a number of minority carriers (holes), indicated as "+" and referred to herein as a "charge packet," to be drawn from P-type zone 25 into the region under the rightmost portion of electrode 22-1, in much the same manner as a negative pulse applied to the gate of an IGFET causes minority carriers to be drawn from the source to the drain of the IGFET. Until a signal is applied to capacitor C₁, the charge packet will remain stored under the rightmost portion of electrode 22-1, since there is a local region of most negative potential, i.e., a local potential energy minimum.

Transfer of the charge packet is realized by applying a clock signal 34 to capacitor C₁ through port 14. During the first half cycle, the clock signal is a positive pulse of voltage +V. As hereinabove described, the application of a positive voltage across the capacitor

plates causes the potential wells under the field plate electrodes 22 to decrease in depth, while it has no affect on the potential wells under the field plate electrodes 23. Thus, with the voltage +V applied, the profiles of the potential wells are as shown in FIG. 3. As can be observed, the potential well under each electrode 22 has been decreased in depth such that its lowest point is above the highest point of the potential well under the next adjacent electrode (i.e., the electrode 23 to its immediate right). Hence, the charge packet, originally stored under electrode 22-1, is transferred or drawn to the local region of most negative potential which region is now under the rightmost portion of electrode 23-1.

During the next half cycle, clock signal 34 is a negative pulse of voltage -V. With this voltage applied to capacitor C₁, the potential wells under the electrodes 22 are increased in depth while those under electrodes 23 continue to remain unchanged. The profiles of the resultant depletion regions are illustrated in FIG. 4. It is readily apparent from FIG. 3 that with this voltage applied, the lowest point of the potential well under each electrode 23 is now higher than the highest point of the potential well under its next adjacent electrode 22. As a result, the charge packet, stored under electrode 23-1, is drawn under the local region of most negative potential which is now the rightmost portion of the potential well under electrode 22-2.

The transfer operation is completed when the clock signal returns to zero voltage. This returns the depletion regions to their original depths, as illustrated in FIG. 1. The charge packet, however, now lies under the rightmost portion of electrode 22-2.

In like fashion, successive cycles of the clock signal cause the charge packet to be transferred to the rightmost portions of the potential wells under successive electrodes 22. After a succession of N-1 cycles, the charge packet has moved into the rightmost portion of the potential well under the last field plate electrode 22-N. This is the output end of the apparatus. Battery 28 supplies a sufficient voltage through electrode 27 to keep the PN junction associated with localized zone 26 reverse-biased by an amount sufficient that its potential well partially overlaps the potential well 31-N under electrode 22-N. Accordingly, the charge packet is swept to the right across the P-N junction and, thus, may be considered to be collected by the P-N junction in much the same manner as carriers are collected in the collector-base junction of an ordinary transistor. This charge carrier collection manifests itself in a current which flows through battery 28 and resistor 29, causing a corresponding voltage to be developed at terminal 33 which can then be detected as the output.

FIG. 5 shows a modification of the embodiment of FIG. 1 wherein, the asymmetrical potential wells under field plate electrodes 22 and the asymmetrical potential wells under field plate electrodes 23 are induced by constant, negative voltages derived from sources 52 and 53, respectively, instead of by fixed charge in the semiconductor or dielectric layer. It should be noted also that, in this embodiment, the asymmetric of the potential wells induced by the latter constant voltages is a result of the nonuniform thickness of the dielectric layer under each electrode.

As shown, source 52 is coupled between semiconductor 16 and each of the field plate electrodes 23 so that a potential well is induced under each of these electrodes. Because of the differences in capacitive coupling, the potential well induced under each electrode is more negative under that portion of the electrode which overlies a thin portion of dielectric layer 21 (i.e., the rightmost portion of the electrode) and is less negative under that portion of the electrode which overlies a thick portion of the layer (i.e., the leftmost portion of the electrode). Thus, the potential wells induced under the electrodes 23 possess the same type of asymmetry as those induced by the fixed charge employed in the embodiment of FIG. 1.

Source 53, on the other hand, is connected between plate 13 and terminal 14. Although not shown, the latter terminal is coupled to ground when no clock signal is being applied thereto. Thus, the negative voltage supplied by source 43 appears across capacitor C₁. This voltage induces potential wells at the semiconductor dielectric interface under the electrodes 22 which possess the same type of asymmetry as those under electrodes 23. Thus, asymmetrical potential wells are induced under electrodes 22 similar to those induced in the embodiment of FIG. 1. It should also be noted that the voltage across capacitor C₁ has no affect upon the potentials under electrodes 23, since these potentials are fixed by the low impedance voltage source 42.

Operation of this embodiment is substantially similar to that of the embodiment of FIG. 1. In particular, after a charge packet has been stored in the potential well under electrode 22-1, clock signal 34 is superimposed on the constant voltage signal of source 53, by coupling the clock signal to terminal 14. During the first half cycle of the clock signal, the superimposed signals cause the voltage appearing across capacitor C₁ to become less negative, while during the next half cycle, the latter signals cause the capacitor voltage to become more negative. As a result, the depths of the asymmetrical potential wells are varied in an analogous manner as heretofore described, thereby causing the charge packet to be transferred through device 14 from potential well to potential well.

Although the present invention has been disclosed in terms of specific embodiments, it is to be understood that these embodiments are merely illustrative of the principles of the invention, and that various other arrangements can readily be devised in accordance with the teachings of the present invention without departing from the spirit and scope of the invention.

For example, while the present invention has been described in terms of a capacitive drive arrangement for transferring charge through a charge transfer device whose storage medium is a semiconductor, it will be appreciated that a capacitive drive can be used, in a completely analogous manner, to transfer charge through a charge transfer device whose storage medium is other than a semiconductor.

Thus, for example, device 15 of FIG. 1 could just as well have been a charge transfer device of the type described in U. S. patent application, Ser. No. 47,205, filed June 18, 1970, pending in 235 by D. Kahng. In the latter type of devices, the storage medium may, for example, be an insulator or a semi-insulating semiconductor which may or may not be characterized by any particular conductivity type.

Moreover, it will be further appreciated that a capacitive drive arrangement can be analogously employed to transfer charge through charge transfer devices of the type presently being referred to in the art as "bucket brigade" charge transfer devices. Devices of this type are disclosed in U. S. Pat. No. 3,660,697 filed Feb. 16, 1970, issued May 2, 1972, to C. N. Berglund and H. J. Boll. In such devices, packets of charge carriers are gated sequentially from zone to zone along the surface of a semiconductor body which includes a bulk portion of one type semiconductivity and a plurality of spaced localized regions of the other type conductivity. In these devices, each zone is operated as a potential well, the boundary of which is defined by the P-N junction which defines the zone.

What is claimed is:

1. Apparatus comprising:

a first conductive plate for forming one plate of a capacitor;

a second conductive plate for forming the other plate of said capacitor;

a charge transfer device disposed between said plates; said charge transfer device of the type adapted for the storage and serial transfer, from an input to an output, of charge carriers localized in induced potential energy minima along a surface portion of a suitable storage medium by sequentially applying differing potentials to portions of the surface through field plate electrodes;

means for inducing an asymmetrical potential well under each of said field plate electrodes;

and means for isolating the potential well under every second one of said field plate electrodes from the affects of an electric field produced within said capacitor.

2. Apparatus in accordance with claim 1 in which the asymmetry of said potential wells is such as to enhance movement of charge from said input to said output.

3. Apparatus in accordance with claim 1 in which the means for inducing the asymmetrical potential wells under said field plate electrodes comprises quantities of fixed charge disposed under said electrodes.

4. Apparatus in accordance with claim 3 wherein

said quantities of fixed charge are disposed within said storage medium.

5. Apparatus in accordance with claim 3 in which the quantity of fixed charge under each electrode is disposed thereunder such that it induces a potential well whose asymmetry is such as to enhance the movement of charge from said input to said output.

6. Apparatus in accordance with claim 1 wherein said means for isolating the potential well under every second one of said field plate electrodes from an electric field within said capacitor comprises a plurality of conduction paths, each of which conductively couples a different one of said second field plate electrodes to said storage medium.

7. Apparatus in accordance with claim 1 wherein said charge transfer device further includes a dielectric layer which overlies and is contiguous with said surface of said medium, and upon which said field plate electrodes are serially disposed.

8. Apparatus in accordance with claim 7 wherein said dielectric layer is of nonuniform thickness.

9. Apparatus in accordance with claim 8 wherein said means for inducing an asymmetrical potential well under each of said field plate electrodes comprises:

a first voltage source connected between said storage medium and every second one of said field plate electrodes for inducing under each of said second field plate electrodes an asymmetrical potential well;

a second voltage source connected between said capacitor plates for inducing under each of the remaining field plate electrodes an asymmetrical potential well.

10. Apparatus in accordance with claim 1 wherein said storage medium is a semiconductor.

11. Apparatus in accordance with claim 1 wherein said storage medium is an insulator.

12. Apparatus in accordance with claim 1 which includes, in addition, means for applying a variable voltage between said capacitor plates thereby causing a charge packet, introduced into said input of said charge transfer device, to be transferred therethrough to said output of said device.

* * * * *

45

50

55

60

65