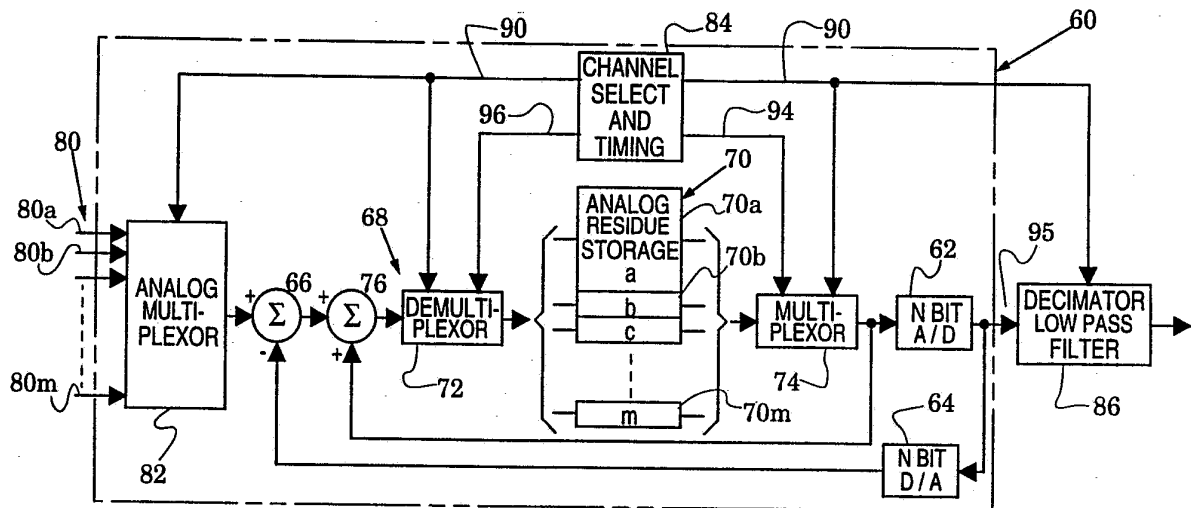




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(54) Title: METHOD AND APPARATUS FOR MULTIPLEXED OVERSAMPLED ANALOG TO DIGITAL MODULATION



(57) Abstract

Apparatus for time multiplexed oversampled analog to digital modulation is provided. Embodiments include modulators (60, 300 and 450) and focal plane optical imagers (100, 160 and 200). Embodiments generally include a plurality of storage elements (70) to hold modulation residues. Multiplexor and demultiplexor structures (72, 74) enable residues to be updated and stored for a plurality of modulated signals. Specific embodiments (500, 600) are shown in CMOS and mixed CMOS-CCD technologies.

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## TITLE

Method and Apparatus for  
Multiplexed Oversampled Analog to Digital Modulation

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## FIELD OF THE INVENTION

The present invention relates generally to analog to digital (A/D) conversion and more particularly to a multiplexed oversampled analog to digital modulator suitable for processing an array of analog inputs, as for  
15 example, in a optical imager, to produce a digital output.

## BACKGROUND OF THE INVENTION

Present approaches in focal-plane video imaging systems use some  
20 form of analog mutiplexing of the pixel data in order to read the image information. It is this multiplexing which defines the so called video data rates. In broadcast television, for example, the 30 hertz pixel data rate is multiplexed to the 4 megahertz video data rate. This same situation exists in industrial and military video systems where pixel rates are usually  
25 below 3 kilohertz and analog multiplexing is used with resulting megahertz video rates.

These multiplexing approaches have necessitated the use of analog to digital conversion processes employing high speed circuitry which, as a practical matter cannot be readily integrated with a focal-plane sensor.  
30 Moreover, the typical A/D converter in these applications comprises a high-speed video, flash converter which is generally considered too expensive for use in consumer applications.

As is discussed in Oversampling Delta-Sigma Data Converters, edited by James C. Candy and Gabor C. Temes, IEEE Press, 1992, New York,  
35 oversampled analog to digital (A/D) converters are known which use coarse quantization at a high sampling rate combined with negative feedback and digital filtering to achieve increased resolution at a lower sampling rate.

Such converters may, therefore, exploit the speed and density advantages of modern very large scale integration (VLSI) while at the same time reducing the requirements for component accuracy.

In a type of oversampled A/D converter generally known as a  
5 delta-sigma modulator, the analog input is sampled at a rate well above the  
Nyquist frequency and fed to a quantizer via an integrator. The quantized  
output is fed back and subtracted from the input. This feedback forces the  
average value of the quantized output to track the average analog input  
value.

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## SUMMARY OF THE INVENTION

The present invention is directed to low cost analog to digital (A/D) conversion apparatus suitable for processing an array of analog inputs  
5 derived from an energy imager, such as an optical imager used in video cameras.

More specifically, the invention is directed to such A/D conversion apparatus which is capable of being located on or adjacent to the focal-plane sensor of an optical imager and which is characterized by the  
10 use of a time multiplexed oversampled conversion technique.

In accordance with a preferred embodiment, an array of analog inputs are time multiplexed into an oversampled A/D modulator which produces, for each input, a single-bit output that oscillates about the true value of the input at rates well above the Nyquist rate (the Nyquist rate being twice the  
15 highest signal frequency of interest). A plurality of analog storage elements are provided, each for storing the analog residue associated with the modulation of a different one of the analog inputs. Each analog storage element is periodically connected into the modulator circuit for modulation in a feedback loop to produce an updated residue value which is then stored  
20 in one of the analog storage elements.

The conversion apparatus thus produces at its output, a bit stream which is representative of the multiplexed analog inputs. This output may, subsequently, be processed through a digital filter that averages its coarse, single bit values and reduces the data rate to produce a high resolution  
25 output at the Nyquist rate.

In a preferred system embodiment, the analog inputs are generated by an array of light sensitive (including visible, infrared and ultraviolet) elements, e.g. charge control devices (CCD), mounted coincident with the focal plane of an image apparatus onto which an image is focused. The A/D  
30 conversion apparatus thus produces a bit stream output representative of the light energy received by the elements of the array. Other input signals associated with the reproduction of the image (e.g. audio, light intensity control) can be produced by a related array of light insensitive elements which also be multiplexed into the bit stream.

35 In accordance with a further system embodiment, the integration function associated with the oversampled modulation and the analog storage elements for storing each analog residue are realized with an array

of integration elements (e.g. CCD wells) arranged in close physical relationship with the light sensitive array.

The novel features of the invention are set forth with particularity in the appended claims. The invention will be best understood from the following description when read in conjunction with the accompanying drawings.

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## BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a delta-sigma modulator connected between an analog signal and a decimator;

5 FIG. 2A is a block diagram illustrating a preferred embodiment of a multiplexed oversampling analog to digital modulator in accordance with the present invention;

FIG. 2B is a timing diagram pertaining to the modulator of FIG. 2A;

10 FIG. 3A is a block diagram of a preferred optical imager embodiment in accordance with the present invention;

FIG. 3B is a schematic diagram of the imager of FIG. 3A;

FIG. 3C illustrates an alternate position of the switches of FIG. 3B;

FIG. 3D is a timing diagram pertaining to the modulator of FIGS. 3A, 3B and 3C;

15 FIG. 4A is a block diagram of another preferred optical imager embodiment;

FIG. 4B is a schematic diagram of the imager of FIG. 4A;

FIG. 5 is a schematic diagram of another preferred optical imager embodiment;

20 FIG. 6 is a block diagram of an optical imager and monitor system in accordance with the present invention;

FIG. 7 is a block diagram of another preferred multiple input analog to digital oversampling modulator embodiment;

25 FIG. 8 is a schematic diagram of a typical focal plane analog readout system;

FIG. 9 is a block diagram of an analog to digital modulator in accordance with the invention;

FIG. 10A is a schematic diagram of a multiplexed oversampled analog to digital conversion system incorporating the modulator of FIG. 9;

30 FIG. 10B is a timing diagram of the system of FIG. 10A;

FIG. 11A is a schematic diagram of another multiplexed oversampled analog to digital conversion system incorporating the modulator of FIG. 9; and

35 FIG. 11B is a plan view of the CCD structure of a sensor circuit of FIG. 11A.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a block diagram of a prior art oversampling A/D modulator 20 of a type described in *Oversampling Delta-Sigma Data Converters*, edited by James C. Candy and Gabor C. Temes, IEEE Press, 1992, New York. The modulator 20 responds to an analog input from signal source 22 to produce a bit stream output 14. The modulator 20 includes a differencer 28 having a + input terminal to which the analog input is applied. The output of differencer 28 is connected through an integrator 30 to an N bit A/D converter 32 which produces the output bit stream 24. A feedback loop 33, from the output of converter 32 to the - input terminal of differencer 28, includes an N bit D/A converter 34. Configurations of the modulator 20 using single bit converters 32, 34; i.e. where  $N = 1$ , are generally referred to as delta-sigma modulators. The portion of the modulator 20 comprised of converters 32 and 34 is frequently referred to as a quantizer 26.

In operation, the converter 32 produces a bit stream output 24 responsive to the output 42 of integrator 30. Converter 34 produces an analog output 40 comprising a somewhat coarse analog estimate of the output 42. The output 40 is subtracted from the analog input 22 at the differencer 28 to form a quantizer error 44. Integrator 30 integrates this error 44 to form an integrated quantizer error over time at its output 42. The negative feedback of the loop acts to minimize the integrated quantizer error over time so that the average value of the encoded signal representation, at the modulator output 24, is forced to track the average analog input from source 22.

A decimator/low pass filter 50 removes the noise produced by the modulator's coarse quantization and processes the bit stream 24 to produce, at its output 52, a finer approximation of the input signal 22 at a lower rate (e.g. the Nyquist rate). As stated in the above cited reference, oversampling modulators can use simple and relatively high-tolerance analog components which facilitates their realization in modern very large scale integration (VLSI) techniques.

The present invention is based on the recognition that basic delta-sigma modulator principles can be utilized in a time multiplexed system for processing an array of analog signal inputs. This recognition leads to improved implementation of various devices, e.g. video imagers, which can be realized in modern integrated circuit techniques with



significant cost, reliability and size advantages.

Attention is now directed to FIG. 2A which illustrates an initial embodiment of the invention in the time multiplexed analog to digital modulator 60. The modulator 60 includes, in an arrangement similar to the feedback loop 33 of the modulator 20, an N bit A/D converter 62, an N bit D/A converter 64 and a differencer 66. However, the integrator of the modulator 60 is comprised of a secondary feedback loop 68 including analog memory 70, demultiplexor 72, multiplexor 74 and summer 76 which together form a sampled data integrator.

10 A plurality of analog signals 80 are time multiplexed to the differencer 66 through an input multiplexor 82 under command of a channel select and timing circuit 84. The channel select and timing 84 can command the demultiplexor 72 and multiplexor 74 to access, for each input signal 80, a corresponding storage location in the memory 70 (e.g. signal 15 80a has a corresponding storage location 70a). In a manner similar to the modulator 20, the modulator 60 output is processed through a decimator / low pass filter 86.

The concept of the modulator 60 may be addressed with reference to both FIG. 2A and the modulator timing diagram of FIG. 2B. Through the channel select lines 90, shown in FIG. 2A, the channel select and timing 84 can, in a repeating time sequence, command the input multiplexor 82 to direct signals 80a, 80b ---- and 80m to the differencer 66 and, in a corresponding time sequence, command the demultiplexor 72 and multiplexor 74 to access memory locations 70a, 70b ---- and 70m. The 25 channel select sequence is indicated by high channel select signal conditions 92a, 92b ---- and 92m in FIG. 2B.

During a first portion of the high signal condition 92a, the channel select and timing 84 commands, through a read line 94, an analog residue (the integrated quantizer error of the modulator 20 in FIG. 1), presently 30 stored in memory location 70a, to be read, via the multiplexor 74, into the summer 76 and the A/D converter 62. The A/D converter 62 and D/A converter 64 place a quantized estimate of this present residue at the differencer 66 and a digitally encoded representation at the input 95 of the decimator 86. The present estimate is differenced (subtracted) at the 35 differencer 66 from the present value of the input signal 80a to form a present error which is summed in the summer 76 with the present residue to form a new analog residue.

During a remaining portion of the high signal condition 92a, the channel select and timing 84 commands, through the write line 96, the demultiplexor 72 to write the new analog residue into the memory location 70a. In the timing diagram of FIG. 2B, the read and write time portions of the high channel select signal condition 92a are indicated by the high 97 and low 98 conditions of the read/write select signal which appears on the read line 94 and write line 96 in FIG. 2A. This process for forming and writing a new analog residue is analogous to the coarse estimate subtraction and integration of the modulator 20 of FIG. 1.

10 This processing, including reading present stored residues from the memory 70 and writing new residues to the memory 70, is repeated for each of the other input signals 80 during their corresponding high channel select conditions 92b --- 92m after which, the sequence repeats. Thus, for each input signal, modulation results in present analog residues being replaced with new analog residues to maintain the integrity of the quantizer error integration history. This enables time multiplexed oversampled analog to digital modulation of the plurality of analog input signals 80.

It should be understood that FIG. 2B illustrates general residue read / write timing relationships of the modulator 60 of FIG. 2A and is not intended to limit the order or time duration devoted by the modulator 60 to each input signal 80 to the particular sequence shown.

Oversampled modulation theory, as described in the above cited reference, indicates that selecting the value of N, for the N bit A/D converter 62 and the D/A converter 64, at a higher number increases the signal-to-noise ratio (equivalently, the number of bits of resolution) achieved by the modulator 60 for a given oversampling rate. On the other hand, selecting the value at a lower number (e.g one) simplifies the modulator 60 structure.

30 FIGS. 3A and 3B respectively depict a block diagram and a schematic diagram of another preferred embodiment, in accordance with the present invention, intended to be mounted coincident with the focal plane 101 of an optical imager 100, e.g. a video camera. In contrast to the modulator 60 of FIG. 2A, the imager 100 has its analog input signals generated by an light sensitive (including visible, infrared and ultraviolet) image collection array 102. An interline transfer array 104 then multiplexes and transfers these signals to modulators 106 associated with columns of a residue storage

array 108 (for clarity of illustration the modulators 106 of FIG. 3B are shown as a single modulator 106' in the block diagram of FIG. 3A).

In the embodiment of FIG. 3B, the interline transfer array 104 functions to perform the m-to-1 multiplexing function of multiplexor 82 of FIG. 2A. The residue storage array 108 analogously performs the 1-to-m demultiplexing function of demultiplexor 72 and the m-to-1 multiplexing function of multiplexor 74. More particularly, the arrays 102, 104 and 108 are each arranged in an orthogonal relationship with 1 through x columns (indicated at the top of the focal plane 101 for arrays 102, 104 and along 10 columns of the array 108) and m elements in each column, i.e. m rows. A modulator 106 is disposed between each column of the transfer array 104 and an associated column of the residue storage array 108.

To simplify the flow of charges through the modulators 106, the summer 110 and differencer 112 of each modulator have been transposed (a mathematically equivalent operation) from their corresponding positions in the modulator 60 of FIG. 2A. In addition, columns of the memory 108 are arranged in the feedback leg of the modulator feedback loop rather than the feedforward leg as in the modulator 60 and a separate storage well 109 is associated with each modulator.

The arrays 102, 104 and 108 and storage well 109 are preferably fabricated in charge control device (CCD) structures. Such structures, and methods of moving electrical charges along CCD wells thereof, are well known in the imager art. The signals modulated in the imager 100 are charge potentials collected for picture elements (pixels) of the focal plane 101 by the collection array 102. The collection array 102 is comprised of light sensitive collection wells 122 (also indicated by the letter C for collection), each associated with a different pixel. Light photons falling on the silicon gate surface of each CCD collection well 122 generates a signal charge which is collected in a depletion well in the semiconductor substrate 30 beneath the gate.

These light induced charges are integrated into the collection wells 122 over a predetermined optical frame time period (e.g. 1/30 of a second in a typical television system) after which each column of charges are parallel shifted into transfer wells 128a, 128b, --- 128m of an adjacent transfer column. The CCD registers forming each transfer column then transfer the collected charge potentials serially downward to the modulators 106. The columns of the collection array 102 and the interline transfer array 104 are

arranged in an interleaved relationship to facilitate the parallel transfer of charges therebetween. A pixel select and timing circuit 138 controls the flow of charges along the CCD structures of the arrays 102, 104 and 108 as required for modulation in the modulators 106 and provides timing to the  
5 decimator/low pass filter 140 for pixel identification of elements of the bit stream from the focal plane 101.

When the modulator switches 135, 136, connected to a storage well 109 and an associated storage array column 156, are in positions 135', 136' of FIG. 3B, charge potentials from a column 128 of the transfer array 104  
10 may be sequentially presented at a summer 110 along with a corresponding present residue value from an output storage element 156m of the associated column 156 of the residue storage array 108. The summed charge is quantized in the analog quantizer formed by the A/D converter 144 and D/A converter 146 and the resulting estimate differenced from the  
15 summed charge in the differencer 112 to form a new residue which is moved into the input storage element 156a of the column 156 of the residue storage array 108. As the quantization was performed, the A/D converter 144 digitally encoded the estimate and placed it on the CCD register 145 to be transferred off the focal plane 101 to the decimator 140.

20 After all m charge potentials from a column 128 of the transfer array 104 have been sequentially processed through the corresponding modulator 106 it should be apparent that the new residue values lie in the CCD wells of the residue storage array column 156 that correspond to wells of the transfer array column 128 from which the charges were transferred. The  
25 charge potentials that have, meanwhile, collected in the collection array 102 during the latest frame period may now be transferred via the transfer array 104 to the modulators 106 to start another modulation cycle.

As an alternative to the modulation cycle described above, after each charge potential from a column 128 of the transfer array 104 is presented  
30 at the corresponding modulator 106 along with the present residue from a corresponding column 156 of the storage array 108, the switches 135, 136 may be placed in the positions 135'', 136'' of FIG. 3C (a schematic of one modulator 106 and an associated residue storage array column). While each charge potential remains presented at the summer 110, it may be  
35 modulated a plurality of times through the modulator, each time reading a present residue value from the storage well 109 to the summer 110 and writing the resulting new residue into the storage well 109 from the

differencer 112. The final residue of this processing may then be placed in the residue storage array column 156 with the switches in the positions 135', 136' of FIG. 3A which shifts the next present residue from the storage array column 156 to the summer 110. At the same time the next charge  
5 potential from the transfer array 104 is presented to the modulator 106 and the switches returned to the positions 135", 136" to repeat the process.

This is continued until each charge potential from a column 128 of the transfer array 104 has been modulated a plurality of times and its final residue stored in its corresponding well of a column 156 of the residue  
10 storage array 108. In this manner a higher oversampling rate is achieved to increase the resolution of the digital representation of the charge potentials.

The above described process, which enables modulation to dwell on a pixel charge potential independently of collection array 102 frame periods,  
15 may be more easily visualized with the aid of the timing diagram of FIG. 3D which illustrates, with the aid of FIGS. 3B, 3C, a specific charge potential modulation example. In FIG. 3D the pixel select high signal conditions 150m, 150m-1, ---- 150a indicate the times during which each of the charge potentials, which were parallel shifted from the collection  
20 array 102 into the transfer array wells 128m, 128m-1, ---- 128a at the end of a frame period, are presented at the summer 110.

The signal conditions 152, 153, of the switches 135, 136 command signal, respectively indicate the times during which the switch positions 135", 136" of FIG. 3C and 135', 136' of FIG. 3B are established. Finally, the  
25 high 154 and low 155 signal conditions of the read/write command respectively represent reading of a present residue through the switch 136 (from the storage well 109 or associated storage array column 156) to the summer 110 and writing of a new residue from the differencer 112 through the switch 135 (to the storage well 109 or associated column 156).

30 After the charge potential originally in transfer well 128m is presented at the summer 110 (high signal condition 150m) and the residue stored in well 156m of the residue storage array has been written to the summer 110 (read signal 154), the switches 135, 136 are moved from positions 135', 136' to positions 135", 136" and the new residue written into  
35 the storage cell 109 (write signal 155).

In this example, three more cycles of reading and writing of residues then follow. Prior to the last write command of these cycles (write signal

155'), the switch command goes to the 153 condition which places the switches in the 135', 136' position of FIG. 3B so that the final residue is stored in storage well 156a. The switch command remains in the 153 condition until the read command 154' is completed which places the next  
5 residue in the storage column 156 (originally in well m-1) at the summer 110 for a modulation cycle as just described above.

Continuing with the sequence of high signal conditions 150 in FIG. 3D, it should be apparent that at the conclusion of the high 150a pixel select signal, each charge potential shifted from a collection array column  
10 into a transfer array column 128 at the end of a frame period, has been cycled through four modulation cycles, beginning with its corresponding residue from a residue storage array column 156, and the final residue placed back in the corresponding well of the storage array column 156.

It should be understood that the arrangement in FIG. 3B in which a  
15 modulator 106 is devoted to one column of the arrays 102, 104 is but one embodiment of the invention and numerous equivalent arrangements can be devised (e.g. several CCD array columns can be daisy chained to one modulator). To simplify the circuits of the imager 100, the A/D converters 144 and the D/A converters 146 may be configured as single bit converters.

20 Another preferred optical imager embodiment 160, arranged on a focal plane 161, is illustrated in the block diagram and schematic diagram of, respectively, FIGS. 4A and 4B. The imager 160 differs primarily from the imager 100 in that an interline integration array 162 performs the transfer, storage and integration functions associated with the interline  
25 transfer array 104, storage array 108, storage well 109 and summer 110 of the imager 100.

In a manner similar to the imager 100, the interline integration array 162 and a light sensitive collection array 164 are arranged in an orthogonal relationship with m elements in each of x columns. However, in the imager  
30 160 the charges in the integration wells 166 are not transferred to another site but rather are run through a modulation cycle and the resulting new residue returned to the associated integration well.

Thus, at the end of each succeeding frame period, the charges from a collection well 168 are added to the existing charges in a corresponding  
35 integration well 166 rather than being shifted into an empty transfer well. Therefore, the integration array 162 serves as the modulation integrator as well as storage for modulation residues.

The columns of the collection array 164 and integration array 162 are interleaved by pairs to facilitate cycling the charges of the integration array 162 through a modulation cycle. As seen in FIG. 4B, charges can thus be transferred across the top of two integration columns 169, as indicated 5 by the arrow 170, and through the remainder of the modulator at the bottom. In the imager 160, therefore, each pair of integration columns 169 and an associated modulator portion 172, containing an N bit A/D converter 174, an N bit D/A converter 176 and a differencer 178, form each modulator (for clarity of illustration only one modulator portion 172' is 10 shown in the block diagram of FIG. 4A).

As the integrated charges of an associated pair of integration array columns 169 are processed through the modulator portion 172, they are each quantized in the N bit A/D converter 174 and the N bit D/A converter 176 to form an estimate which is differenced, in the differencer 178, from 15 the original charge to form a new residue which is returned to the associated integration well. The processing continues at the end of each succeeding frame period when the collected charges from the light sensitive CCD wells 168 are summed with the residue in each corresponding integration well 166 and the modulation repeated to form and store new 20 residues. The modulation of all residues in a pair of integration columns 169 may be completed once each frame period or, for increased resolution of the analog to digital conversion process, a plurality of times each frame period. The only requirement is that new residues are returned to their corresponding integration wells 166 prior to shifting of charges from the 25 collection array 164.

As described above for the imager 100, the number of bits of the A/D converter 174 and D/A converter 176 may be increased to achieve a higher signal-to-noise ratio for a given oversampling rate or decreased to achieve structural simplicity. Pixel select and timing electronics 180 provides 30 timing signals to the interline integration array 162 for moving charges along its CCD structure and to a decimator/low pass filter 182 for identification of elements of the bit stream from the focal plane 161. The modulated bit stream from the A/D converters 174 are transferred to the edge of the focal plane 161 by a CCD register 184.

35 Another preferred imager embodiment 200 on a focal plane 201 is illustrated in the schematic diagram of FIG. 5. The imager 200 differs from the imager 160 in that a frame transfer/integration array 202 is spaced

from a collection array 204 rather than being interleaved therewith as in the case of the interline integration array 162 of FIG. 4B. Each column 206 of the frame transfer/integration array 202 is folded and connected at one end through a summer 208 to an associated collection column 210 to  
5 facilitate passing charges around the column 206 for a modulation cycle.

Present residues in the frame/transfer array 206 wells are cycled and integrated with corresponding charges shifted downward from the collection array 204 at the end of each frame period and modulated to new residues each time they are passed around the folded columns for a  
10 modulation cycle. The encoded bit stream from the analog to digital converters 212 is transferred across a CCD register 214 to the edge of the focal plane 201 and then to a decimator/low pass filter 216.

The focal plane 201 of the imager 200 also has a column 220 of light insensitive CCD wells 222 for collecting other signal inputs associated with  
15 the image focused on the array 204 (e.g. multichannel audio, light intensity control). These signals are modulated and multiplexed onto the CCD output register 214 with the modulation from the light sensitive wells of the collection array 204.

Thus the focal plane 201 includes a structure of analog signal  
20 collecting devices responsive to an energy pattern incident on the focal plane 201 wherein the energy pattern is modulated by the imager 200 into a representative multiplexed bit stream. The energy sensitive structure is defined by a combination of light sensitive devices for receiving an image focused on the focal plane and analog signal sensitive devices for receiving  
25 image associated signals.

FIG. 6 is a block diagram illustrating an optical imager / monitor system 260 in which an image represented by a bit stream 262 from an imager 264, in accordance with the present invention (e.g. optical imager embodiments 100, 160 and 200), is monitored on a display 266. The display  
30 266 can be any display having visible display elements that can be driven on or off (e.g. electro-illuminescence, liquid crystal) and which are arranged in accordance with the picture elements of the focal screen of the imager 264.

A pixel driver 268 decodes the bit stream 262 (opposite process of the  
35 encoding in the imager 264) and applies corresponding signals 270 appropriate to the type of display elements in the display 266. A clock 272 and row and column select circuits 274, 276 demultiplexes the signal 270 to



display elements of the display 266 in accordance with the manner in which charge potentials of picture elements of the imager 264 focal plane were multiplexed onto the bit stream 262

The average luminosity of each display element will be the average of the on and off duration of the imager digital output signal for each pixel. Since the human eye will integrate anything changing faster than 60 hertz, the modulated display element will appear to be a constant level (given that the imager 264 is operating at modulation rates higher than 60 hertz). The bit stream 262 contains the original analog spectrum of light intensity at each picture element of the focal plane of the imager 264. The average pulse density at the display element over a Nyquist sample interval will equal the average light intensity at the corresponding picture element of the imager 264 focal plane to within the sampling resolution. In a similar manner, the bit stream 262 could be recorded on magnetic tape for later application to a display monitor.

The teachings of the invention may be extended to higher order modulation feedback loops, which are described in the above cited reference, to achieve a higher signal-to-noise ratio (higher resolution in number of bits) for a given sampling rate. Higher order loops, however, also increase circuit complexity.

One embodiment of the invention illustrating their use is shown in the block diagram of a multiplexed analog to digital modulator 300 of FIG. 7. Compared to the modulator 60 of FIGS. 2A, 2B, the modulator 300 has a second order feedback loop 302 wherein the quantizer estimate is fed back from the D/A converter 304 to a differencer 306. A demultiplexor 310, memory 312 and multiplexor 314 are positioned in the feedforward leg of this second loop with local feedback to the summer 316. For timing purposes the demultiplexor, memory and multiplexor of the first feedback loop have been positioned in the feedback leg.

In the description above of the optical imager 100 embodiment, it was stated that the arrays 102, 104 and 108 and storage well 109 are preferably fabricated in charge control device (CCD) structures. It will now be shown that multiplexed oversampled analog to digital modulation embodiments may be realized in other integrated circuit technologies.

FIG. 8 is a schematic diagram of a system 400 typically used in the imaging art as a focal plane analog readout. In this system, an integrate and dump circuit 402a accumulates an optical signal from a buffered source

404a in the capacitor 406. The voltage developed across the capacitor 406 is applied to the gate of an FET source follower 408.

The source follower 408 is periodically sampled in response to a sampling signal 410 applied to a FET gate 412 and the sampled voltage  
5 multiplexed onto a bus 414. The capacitor 406 is then discharged by applying a reset signal 415 to FET 416 which clears the capacitor 406 for the next charge and sample cycle. While the capacitor 406 accumulates the next charge, other signal sources, for example the source 404m, are sampled and multiplexed to the bus 414. Thus, the system 400 produces a  
10 multiplexed analog output 418 from a focal plane.

Multiplexed analog sampling circuits, such as the focal plane readout of FIG. 8, can, in accordance with the invention, be replaced with the multiplexed oversampled analog to digital modulator 450 illustrated in the block diagram of FIG. 9. In the modulator 450, an analog signal 452a is  
15 integrated by feedback of the signal through a delay 454 to be summed with itself in a summer 456. The integrated signal (present residue) is periodically multiplexed to an N bit A/D 460 by placing it onto a bus 462 through a gate 464 in response to a read signal 465. The N bit A/D 460 produces a digital bit stream output 468 representative of the integrated  
20 signal and an N bit D/A 470, responsive to the bit stream 468, places a quantized estimate thereof on the bus 472.

The quantized estimate is clocked through a gate 478 by a write signal 480 to be subtracted in a differencer 482 from the present residue and summed with the present value of the analog signal 452a to form a  
25 new analog residue at the output of the summer 456. The integration, subtraction and gating functions comprise a circuit 490 which is also provided for each of the other analog signals, e.g., circuit 490m for analog signal 452m. Each of these circuits 490 are time multiplexed onto the buses 462, 472 as described above for the circuit 490a.

30 Thus, for each analog signal 452, a circuit 490 is periodically connected in a feedback loop, including the N bit A/D 460 and the N bit D/A 470, for modulation which produces a representative bit stream 468 at the output of the N bit A/D and an updated residue value from a summer 456.

The multiplexed oversampled analog to digital modulator of FIG. 9  
35 may be realized in a variety of integrated circuit technologies, e.g., charge modulation device (CMD), bulk charge modulation device (BCMD), base-stored image sensor (BASIS), static induction transistor (SIT), lateral

APS, vertical APS and double-gate floating surface transistor. Specific embodiments directed to realization in Complimentary Metal Oxide Semiconductor (CMOS) technology and in mixed CCD and transistor technologies are respectively illustrated in FIGS. 10 and 11.

5 FIG. 10A shows a multiplexed oversampled analog to digital conversion system 500 having a plurality of integration, subtraction and gating circuits 502a --- 502m multiplexed to a feedback loop including an N bit A/D 504 and an N bit D/A 506. In addition to FIG. 10A, the following description of the system 500 will refer to the timing diagram of FIG. 10B.  
10 In the circuit 502a, an analog signal 508a is collected on integration capacitor 510 which is buffered by source follower 512. Channel select signals a through m are sequentially applied to the circuits 502. During a first portion of the channel a select period, read a signal 514 goes high to switch FET 516 which connects the circuit 502a via the bus 518 to the N bit  
15 A/D 504.

Therefore, the N bit A/D 504 places a bit stream at the output 522 which is representative of the charge (present analog residue) on the capacitor 510. In response to the bit stream, the N bit A/D 506 places a voltage  $V_{est}$  (quantized estimate) on the bus 520 which makes it available  
20 at the lower end of a subtraction capacitor 524. The subtraction capacitor 524 is connected to the integration capacitor 510 by FET 525.

In the last portion of the channel a select period, write a signal 526 goes high which causes a reference voltage  $V_{ref}$  to be placed on the gate of FET 525. Consequently a charge equal to the quantity  $(V_{est} - V_{ref}) / C$ ,  
25 where  $C$  is the capacitance of the capacitor 524, is subtracted from integration capacitor 510 (where the FET 525 is assumed to be an ideal transistor having no voltage drop between gate and source). Prior to the write a pulse 526, a brief clear pulse 528 is placed on the gate 532 which is in parallel with the subtraction capacitor 524. This removes all charges  
30 from the subtraction capacitor 524 to prepare it for the write pulse.

When the write a signal 526 and read a signal 514 are both low, the analog signal 502a is again integrated in capacitor 510. Thus a quantized estimate of the present analog residue has been subtracted and the present analog signal added to store a new analog residue on the capacitor 510. In a  
35 similar manner, each of the other analog signals 502 is mulitplexed to the N bit A/D 504 and N bit D/A converter 506. In FIGS. 10A, 10B, it is assumed the clear signal 528 is common to each circuit 502 so that it is

high prior to each write signal 526.

FIG. 11A illustrates an active pixel sensor (APS) 600 combining a plurality of sensor circuits 602 in a multiplexed oversampled analog to digital modulation mode. The embodiment 600 combines CCD integration  
5 and subtraction with CMOS sampling, readout and multiplexing.

In a representative sensor circuit 602a, an analog signal produced by an image light ray 604 is integrated, during a charge cycle, in CCD wells 605, 606 beneath photogates 607 and 608. The wells are defined by a potential 609 indicated in broken lines. The integrated charge of both wells  
10 is then transferred via transfer gates 610, 611 and summed into the CCD well 612 from where a voltage proportional to the summed charge is available via sense gate 614 and source follower 615 (timing precharge 616 applied through the gate of FET 617 is required to create the well 612). Periodically, this voltage is multiplexed over a bus 618 to N bit A/D 619 by  
15 a read command applied to FET 620.

As in the system 500 of FIG. 10A, the N bit A/D 619 places a bit stream representative of the summed charge at an output 626. The N bit D/A 622, in response to the digital output 626, places a voltage  $V_{est}$  on the bus 628 to enable the subtraction of a quantized estimate from the summed  
20 charge in CCD well 612.

To effect this subtraction, the CCD wells 605, 606 are separated by a potential barrier 630 shown in FIG. 11B which is a plan view of the sensor circuit 602a CCD structure. The height of the potential barrier 630 is proportional to the voltage  $V_{est}$ . A signal is also applied to transfer gate  
25 609 which causes the summed charge in CCD well 612 to flow into CCD well 605 with the excess charge flowing over the potential barrier into CCD well 606. For nonzero digital outputs, CCD well 605 is then emptied into the diffusion 632 by a signal applied to the drain gate 634. The subtracted (emptied) charge is, therefore, proportional to the output voltage of the N  
30 bit A/D 622.

Therefore, a quantized estimate is subtracted and during the next integration cycle, the input signal 603A is integrated into CCD wells 605, 606 to form a new residue charge. The formation of wells 605, 606 and 610 and movement of charges therebetween as described above is well known  
35 in the CCD art.

From the foregoing, it should now be recognized that embodiments for multiplexed oversampled analog to digital conversion have been disclosed

herein utilizing means for preserving modulation integration history for each of an array of analog input signals (array as used herein refers generally to a plurality of input signals and more particularly, where specified, to a plurality arranged in a physical relationship, e.g. 5 orthogonally as in the arrays 102, 104 and 108 of FIG. 3A).

The teachings of the invention enable an all digital video camera/recorder to be manufactured with an improved image quality and at lower cost. The teachings permit all of the analog electronics conventionally used in video and sound detection to be replaced with a 10 monolithic on focal plane imager having a binary output.

A preferred implementation can use CCD (charge coupled device) electronics to detect and digitally process images, sound and camera controls for virtually noise free recording and display. The binary output can be used to drive modulated flat panel displays directly or can be used 15 with conventional filtering to interface raster scan analog displays. Other preferred embodiments can be effected in various integrated circuit technologies.

The preferred embodiments of the invention described herein are exemplary and numerous modifications and rearrangements can be readily 20 envisioned to achieve an equivalent result, all of which are intended to be embraced within the scope of the appended claims.

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What is claimed is:

1. Apparatus responsive to an array of m analog inputs for producing a bit stream output representative thereof, said apparatus comprising:

5 m storage elements, each capable of storing an analog value;

N bit A/D converter means, responsive to an applied analog value, for producing a bit stream output representative thereof;

10 multiplexing means for periodically applying a residue analog value from each of said m storage elements to said A/D converter means, each residue analog value associated with a different one of said m analog inputs;

N bit D/A converter means, responsive to said A/D converter means bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter means;

15 means for summing each of said m analog inputs and its associated residue analog value and differencing the quantized value associated therewith to form a new residue analog value; and

demultiplexing means for storing each new residue analog value in one of said m storage elements.

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2. Apparatus of claim 1 wherein said N bit A/D converter means comprises a single bit A/D converter and said N bit D/A converter means comprises a single bit D/A converter.

25 3. Apparatus of claim 1 wherein said m storage elements each comprise a charge control device well.

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4. An imager responsive to an energy pattern incident on a focal plane for producing a bit stream representative thereof, said imager comprising:  
an array of energy sensitive elements disposed on said focal plane for producing m analog signals;
- 5 M storage elements, each capable of storing an analog value;  
N bit A/D converter means, responsive to an applied analog value, for producing a bit stream output representative thereof;  
multiplexing means for periodically applying a residue analog value from each of said m storage elements to said A/D converter means, each  
10 residue analog value associated with a different one of said m analog signals;
- N bit D/A converter means, responsive to said A/D converter means bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter means;
- 15 means for summing each of said m analog signals and its associated residue analog value and differencing the quantized value associated therewith to form a new residue analog value; and  
demultiplexing means for storing each new residue analog value in one of said m storage elements.
- 20
5. The imager of claim 4 wherein said energy sensitive elements comprise light sensitive elements for each generating a charge potential related to the energy of light focused thereon.
- 25 6. The imager of claim 4 wherein said array of energy sensitive elements comprises an orthogonal array of charge control devices.
7. The imager of claim 4 wherein said N bit A/D converter means comprises a single bit A/D converter and said N bit D/A converter means comprises a  
30 single bit D/A converter.

8. An imager responsive to an energy pattern incident on a focal plane for producing an output bit stream representative of said pattern, said imager comprising:

an array of  $m$  energy collection elements, each capable of producing an analog signal related to the amount of energy incident thereon;

means mounting each of said  $m$  energy collection elements for collecting energy from a different area of said focal plane;

means for storing  $m$  analog residues, each associated with a different one of said collection elements;

A/D converter means sequentially responsive to said  $m$  analog residues for producing an output stream comprised of bits, each related to one of said analog residues;

D/A converter means responsive to said output stream bits for respectively producing analog quantized estimates, each related to one of said analog residues; and

processing means for periodically modifying the stored value of each analog residue as a function of the analog signal produced by the associated collection element and the analog quantized estimate produced by said D/A converter means.

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9. The imager of claim 8 wherein said processing means includes means sequentially summing each presently stored analog residue with the analog signal produced by the associated collection element and differencing that quantity with the associated quantized estimate for modifying the presently stored analog residue to produce a new analog residue.

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10. The imager of claim 9 wherein said means for storing  $m$  analog residues comprises;

$m$  serially connected storage elements including an input storage element and an output storage element; and

means for shifting said analog residues through said  $m$  serially connected storage elements from said input to said output storage element.

11. The imager of claim 10 wherein said processing means derives each presently stored analog residue from said output storage element and delivers each new analog residue to said input storage element.

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12. The imager of claim 10 wherein each of said m storage elements is mounted proximate to a different one of said m collection elements; and further comprising means for periodically transferring the analog signal produced by each collection element to the storage element mounted  
5 proximate thereto.

13. The imager of claim 8 wherein said m energy collection elements comprise light sensitive elements arranged in a two-dimensional array substantially coincident with said focal plane.

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14. The imager of claim 10 including:

an array of m transfer elements, each coupled to a different one of said m collection elements;

means for periodically transferring the analog signal produced by each  
15 collection element to the transfer element coupled thereto;

said m transfer elements being serially arranged and including an output transfer element;

means for shifting said analog residues through said m serially connected transfer elements to said output transfer element; and

20 wherein said processing means sequentially derives said analog signals from said output transfer element.

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15. A method for producing a bit stream output representative of an array of m analog inputs, said method comprising the steps of:

- providing m storage elements, each capable of storing an analog value;
- providing an N bit A/D converter, responsive to an applied analog value, for producing a bit stream output representative thereof;
- 5 applying, periodically, a residue analog value from each of said m storage elements to said A/D converter means, each residue analog value associated with a different one of said m analog inputs;
- providing an N bit D/A converter, responsive to said A/D converter bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter;
- 10 summing each of said m analog inputs and its associated residue analog value and differencing the quantized value associated therewith to form a new residue analog value; and
- 15 storing each new residue analog value in one of said m storage elements.

16. A method for producing an output bit stream representative of an energy pattern incident on a focal plane, comprising the steps of:

- 20 providing an array of m energy collection elements, each capable of producing an analog signal related to the amount of energy incident thereon;
- mounting each of said m energy collection elements for collecting energy from a different area of said focal plane;
- 25 storing m analog residues, each associated with a different one of said collection elements;
- performing analog-to-digital conversion sequentially of said m analog residues to produce an output stream comprised of bits, each related to one of said analog residues;
- 30 performing digital-to-analog conversion of said output stream bits to respectively produce analog quantized estimates, each related to one of said analog residues; and
- modifying, periodically, the stored value of each analog residue as a function of the analog signal produced by the associated collection element
- 35 and the analog quantized estimate produced by said digital-to-analog conversion.

17. A method for producing a bit stream output representative of an energy pattern incident on a focal plane, comprising the steps of:

disposing an array of energy sensitive elements on said focal plane for producing m analog signals;

5 providing m storage elements, each capable of storing an analog value; providing an N bit A/D converter, responsive to an applied analog value, for producing a bit stream output representative thereof;

applying, periodically, a residue analog value from each of said m storage elements to said A/D converter means, each residue analog value  
10 associated with a different one of said m analog signals;

providing an N bit D/A converter, responsive to said A/D converter bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter;

summing each of said m analog signals and its associated residue  
15 analog value and differencing the quantized value associated therewith to form a new residue analog value; and

storing each new residue analog value in one of said m storage elements.

20 18. The method of claim 17 wherein said disposing step comprises the steps of:

mounting on said focal plane an array of light sensitive elements; and

generating, with each of said elements, a charge potential related to the energy of light focused thereon.

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19. Apparatus responsive to an array of  $m$  analog inputs for producing a bit stream output representative thereof, said apparatus comprising:

$m$  storage elements, each capable of storing an analog value;

5  $N$  bit A/D converter means, responsive to an applied analog value, for producing a bit stream output representative thereof;

multiplexing means for periodically applying a residue analog value from each of said  $m$  storage elements to said A/D converter means, each residue analog value associated with a different one of said  $m$  analog inputs;

10  $N$  bit D/A converter means, responsive to said A/D converter means bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter means;

demultiplexing means for periodically supplying said quantized values to each of said  $m$  storage elements; and

15 means for summing each of said  $m$  analog inputs and its associated residue analog value and differencing the quantized value associated therewith to form a new residue analog value.

20. Apparatus of claim 19 wherein each of said storage elements comprises  
20 a capacitor.

21. Apparatus of claim 19 wherein each of said storage elements comprises  
a CCD well.

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22. An imager responsive to an energy pattern incident on a focal plane for producing a bit stream representative thereof, said imager comprising:

an array of energy sensitive elements disposed on said focal plane for producing  $m$  analog signals;

5  $M$  storage elements, each capable of storing an analog value;

$N$  bit A/D converter means, responsive to an applied analog value, for producing a bit stream output representative thereof;

multiplexing means for periodically applying a residue analog value from each of said  $m$  storage elements to said A/D converter means, each  
10 residue analog value associated with a different one of said  $m$  analog signals;

$N$  bit D/A converter means, responsive to said A/D converter means bit stream output, for producing quantized values each coarsely representative of a residue analog value applied to said A/D converter means;

15 demultiplexing means for periodically supplying said quantized values to each of said  $m$  storage elements; and

means for summing each of said  $m$  analog inputs and its associated residue analog value and differencing the quantized value associated therewith to form a new residue analog value.

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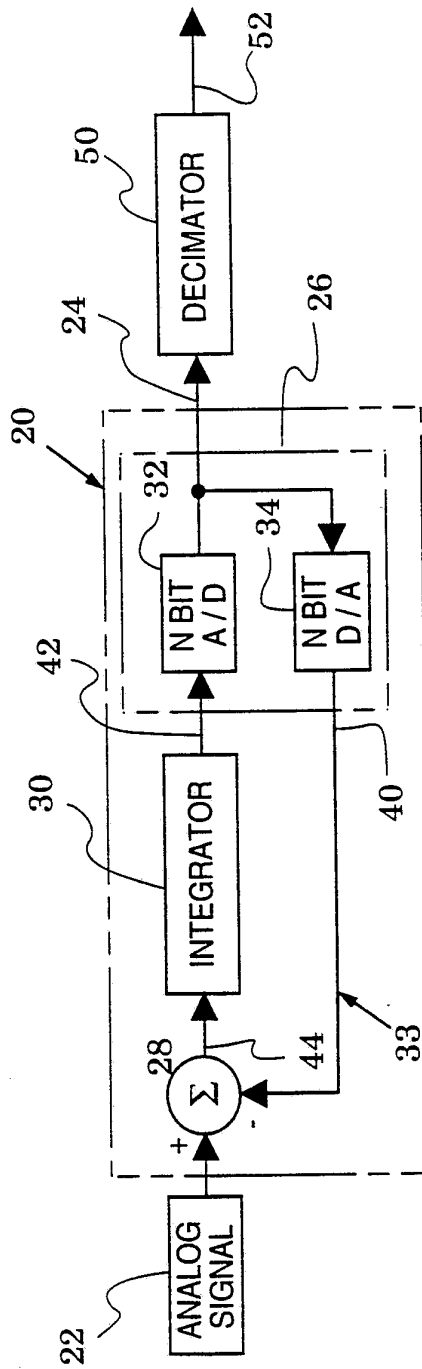


FIG. 1  
(Prior Art)

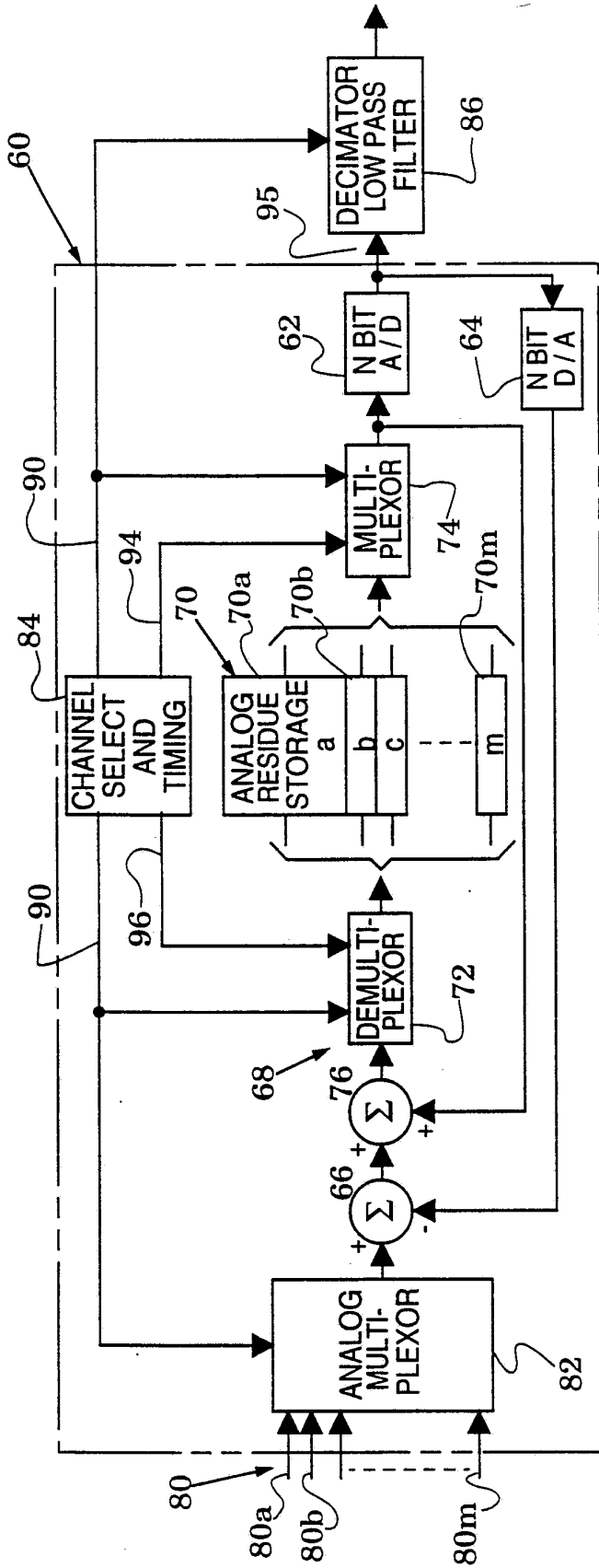


FIG. 2A

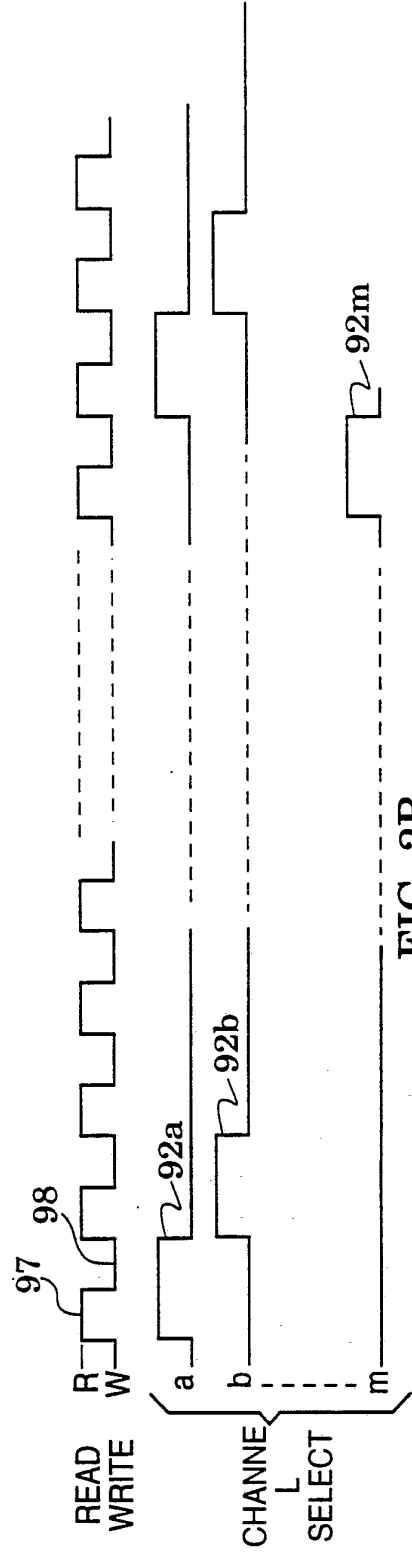


FIG. 2B

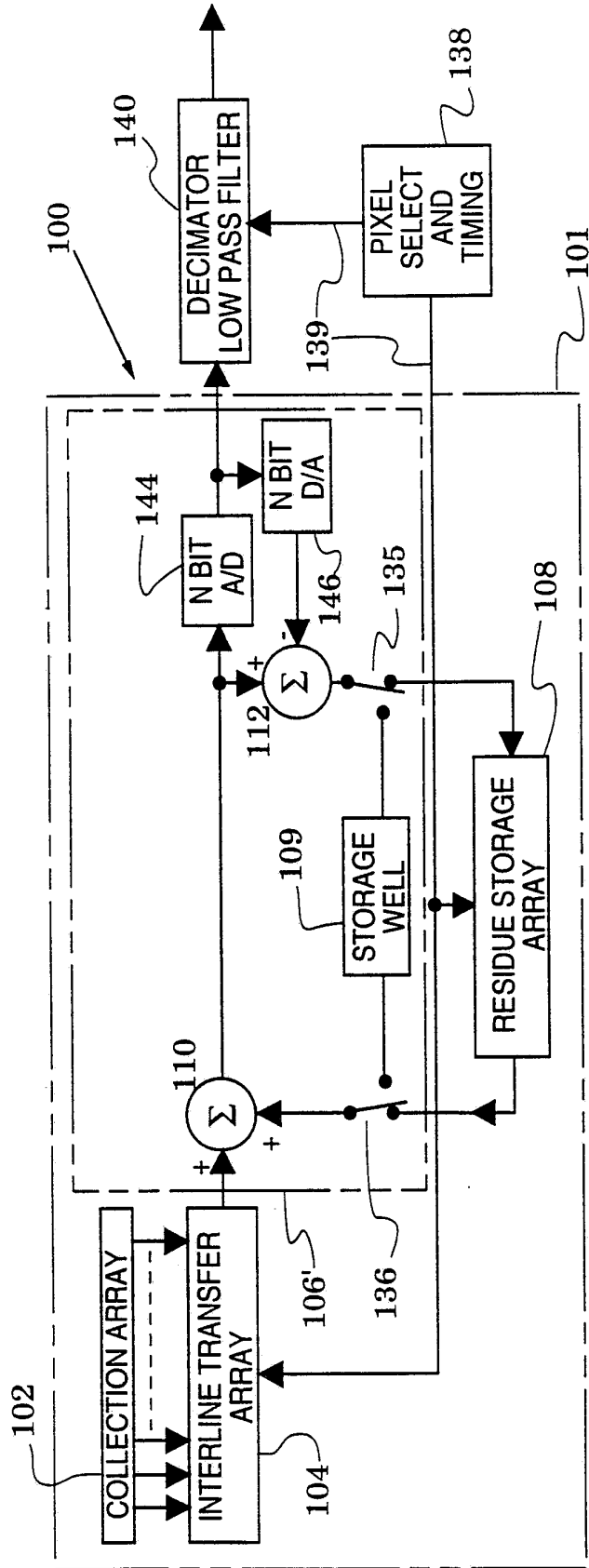


FIG. 3A



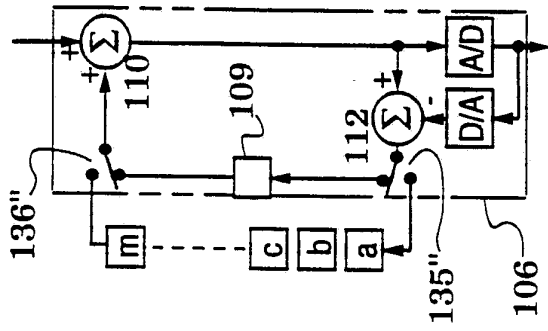


FIG. 3C

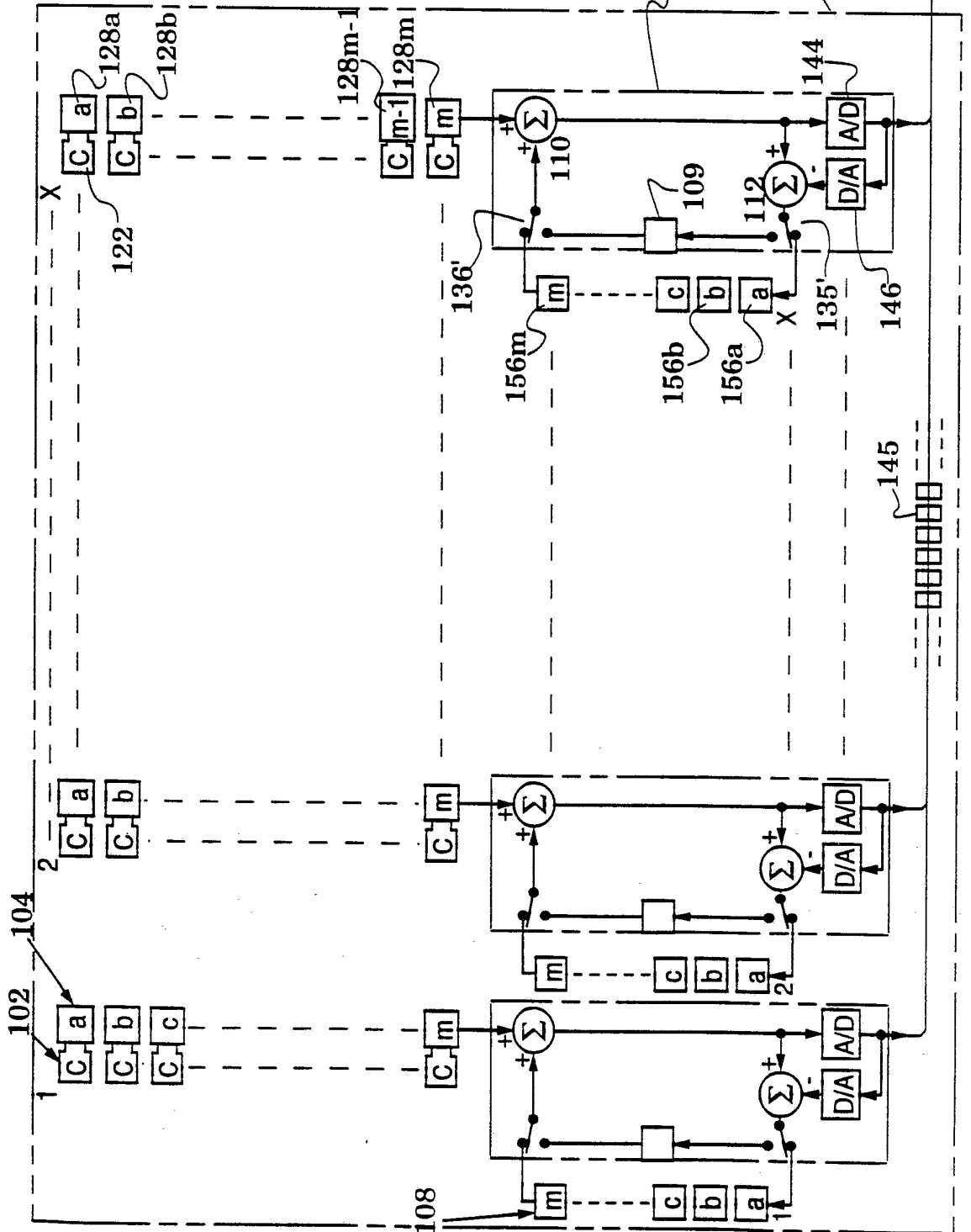


FIG. 3B

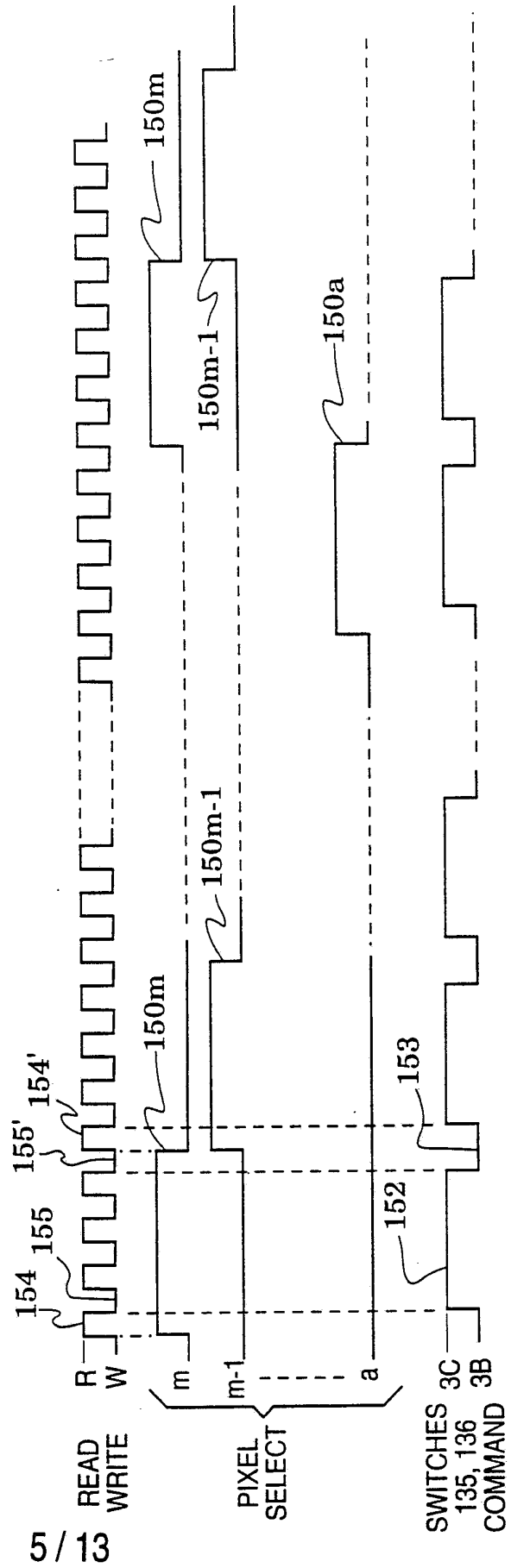


FIG. 3D

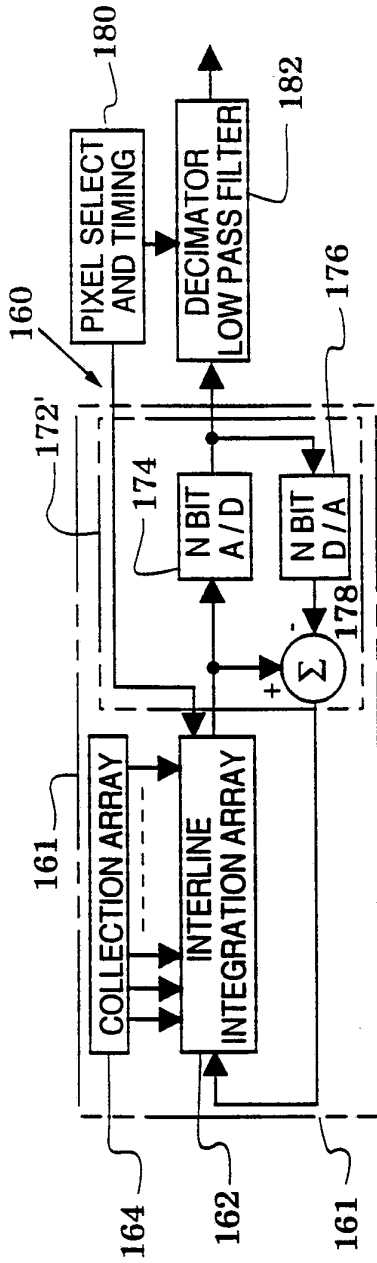


FIG. 4A

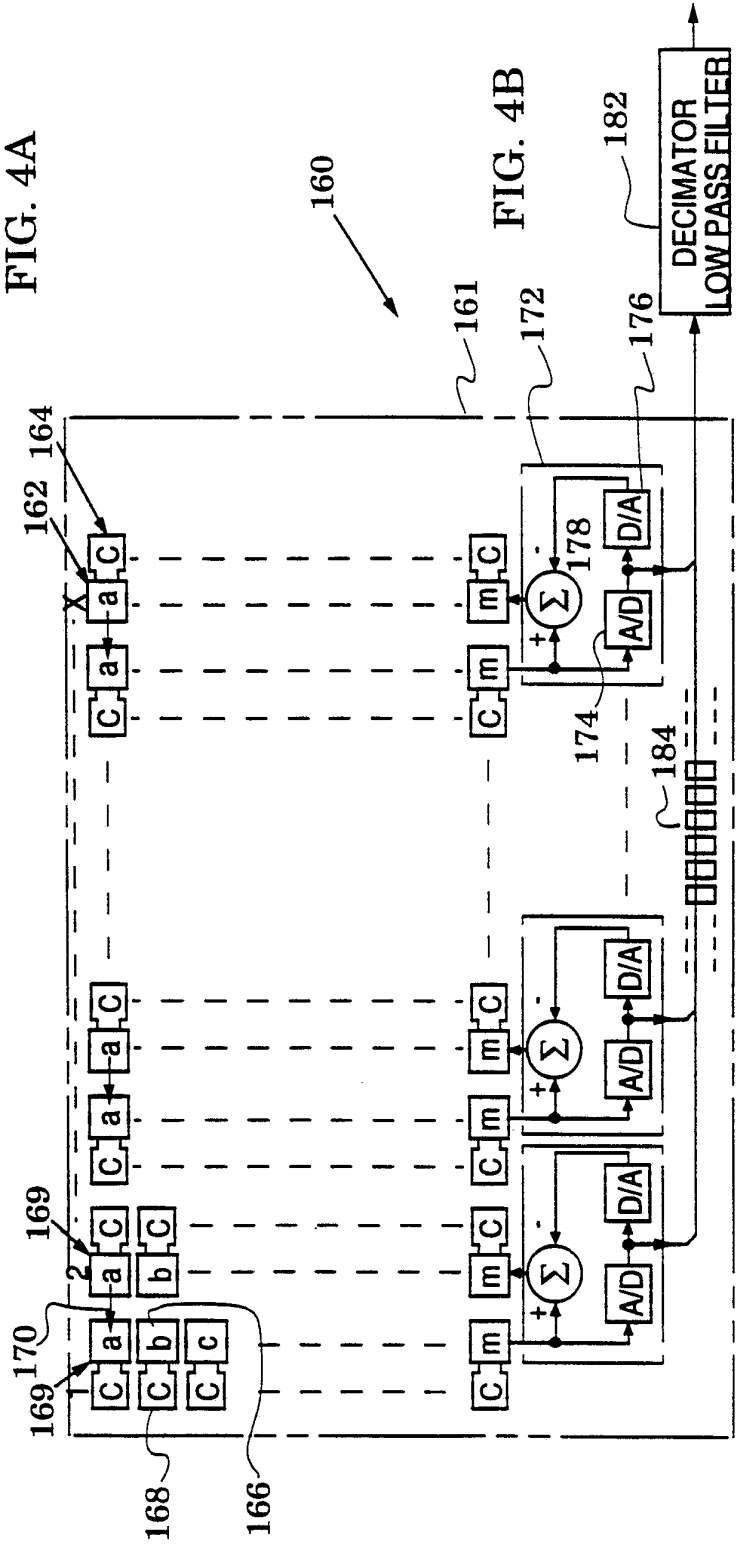
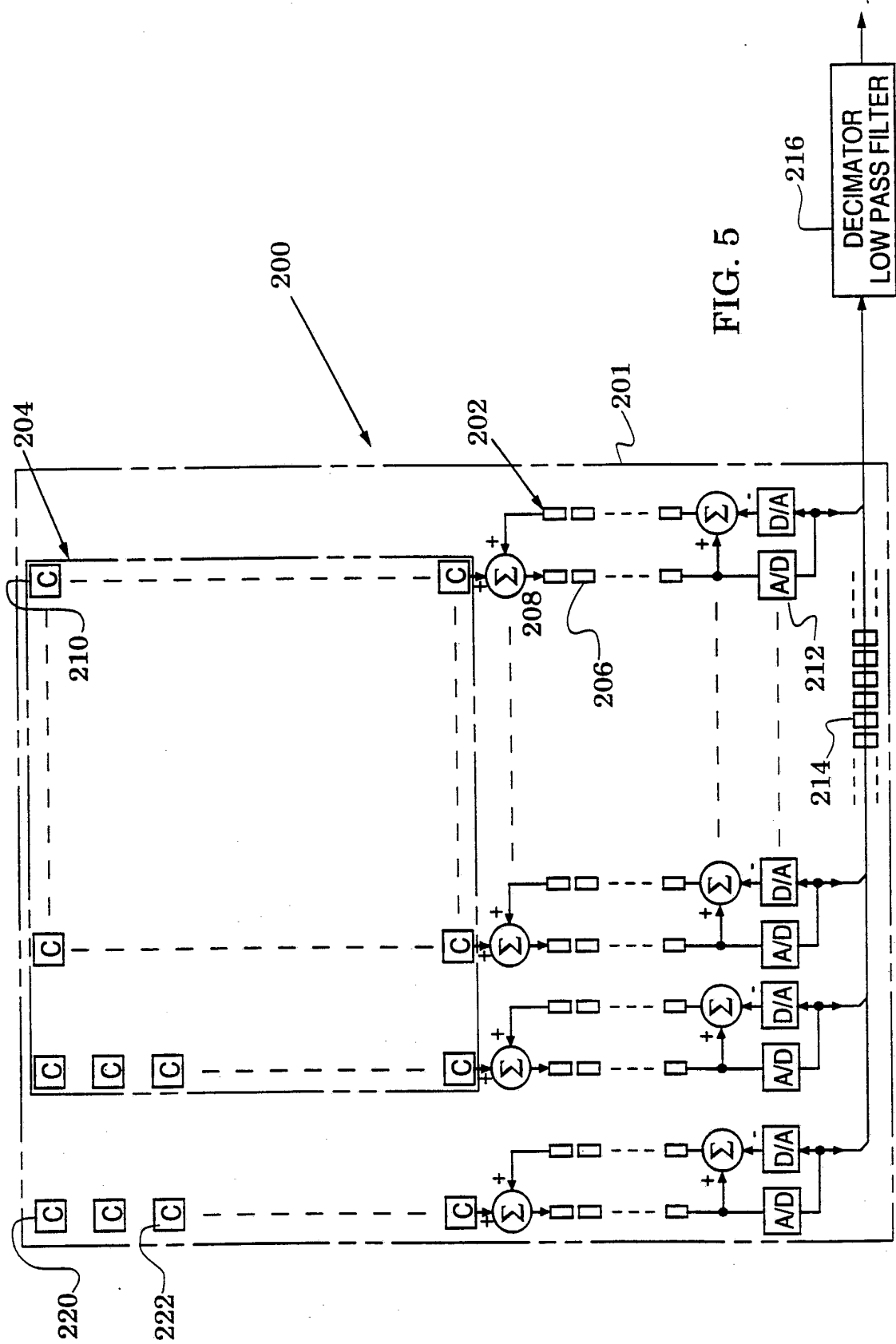


FIG. 4B



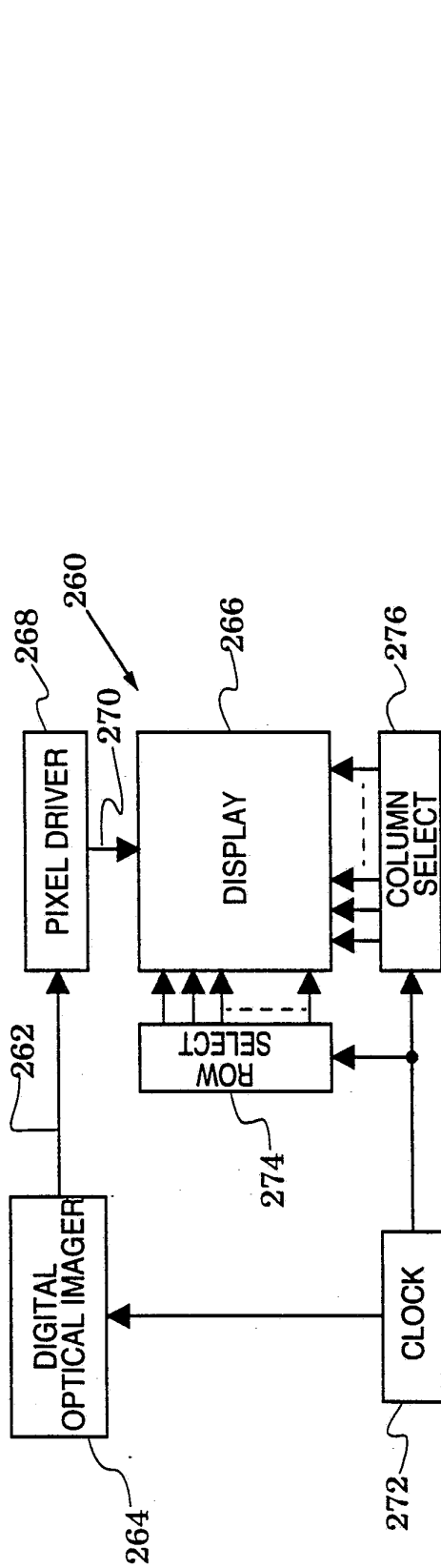


FIG. 6

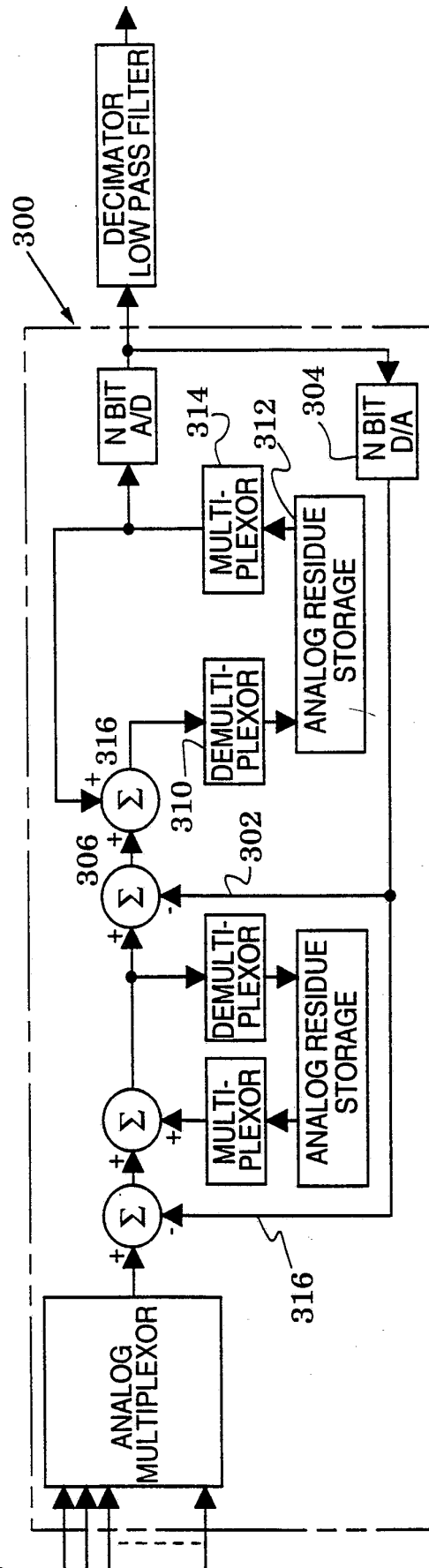


FIG. 7

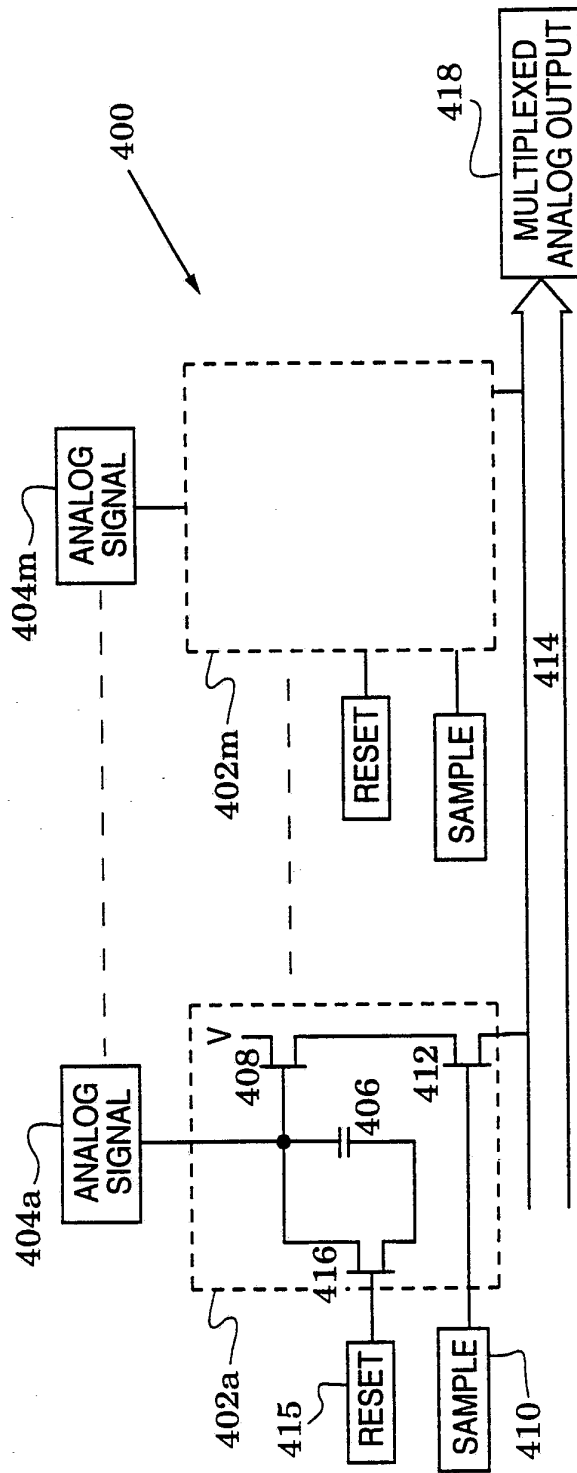


FIG. 8  
(Prior Art)

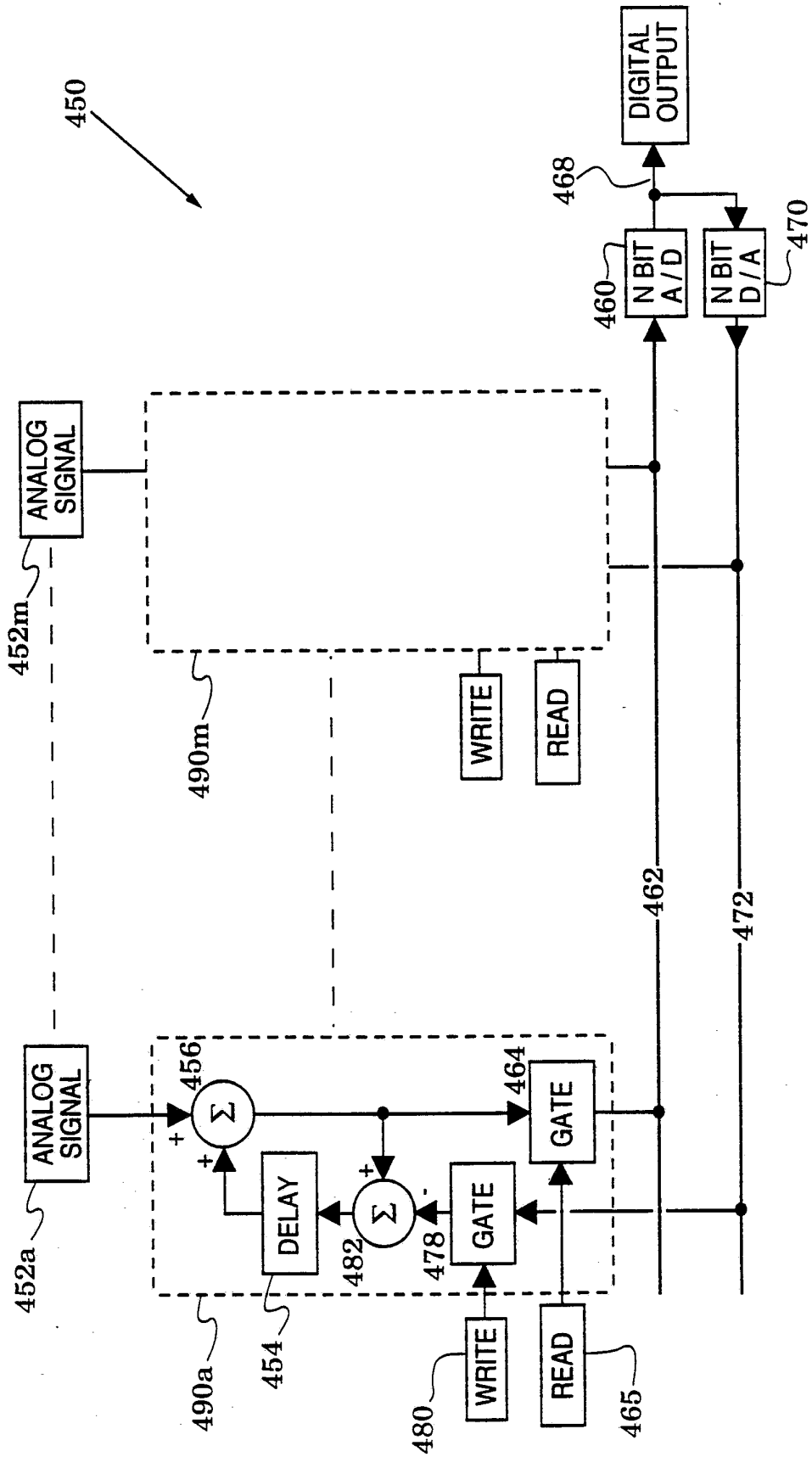


FIG. 9

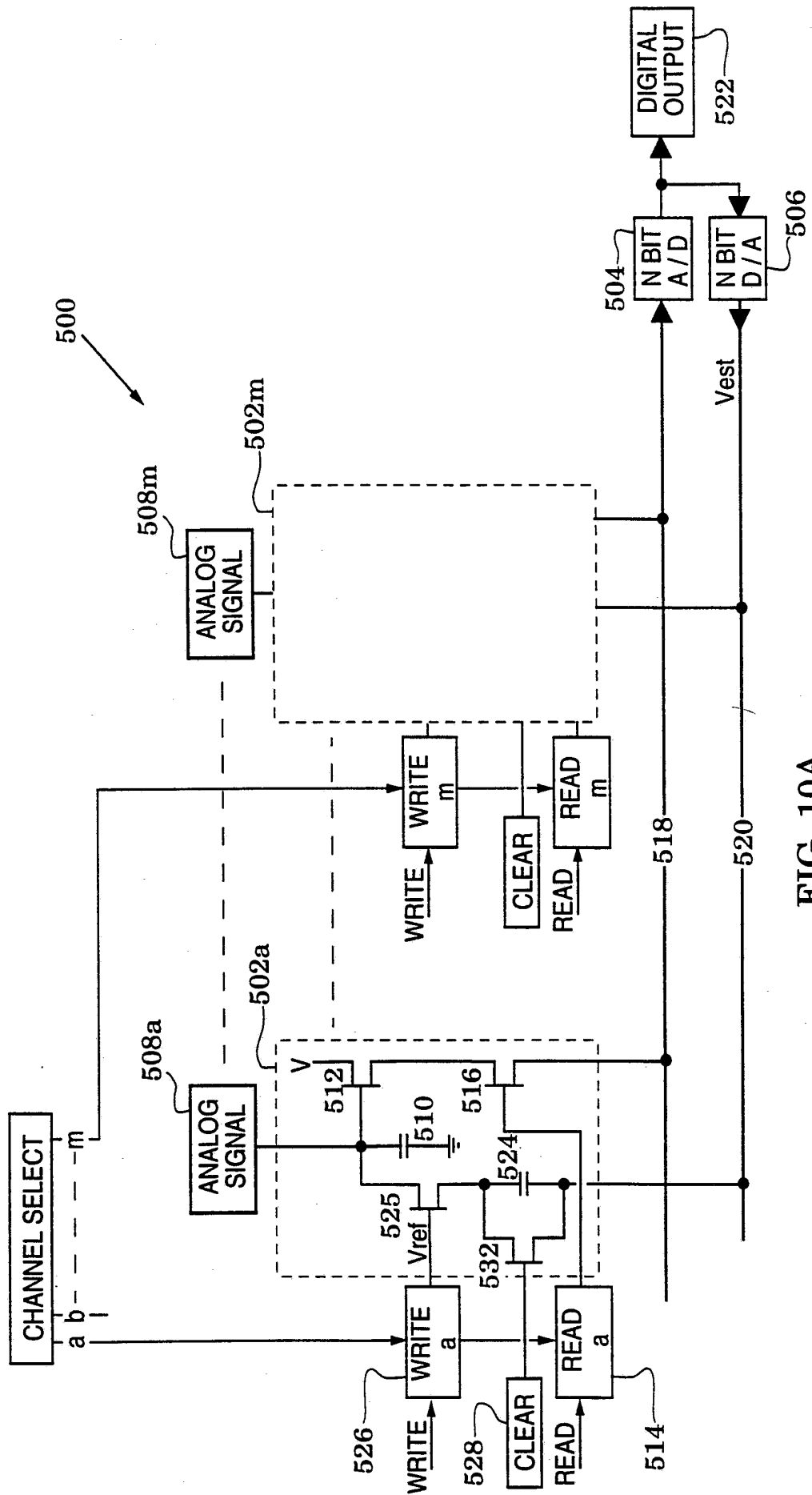


FIG. 10A



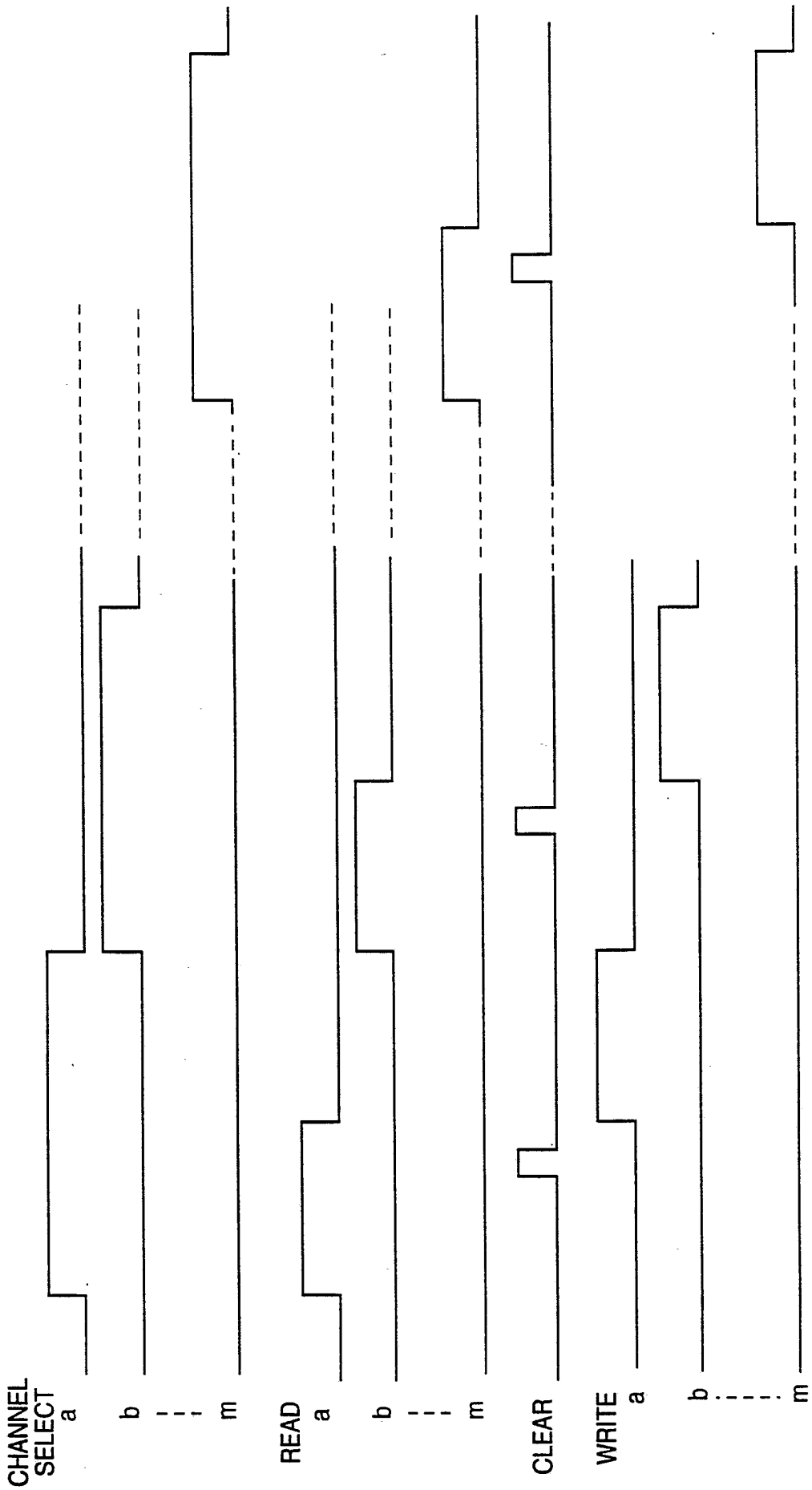


FIG. 10B

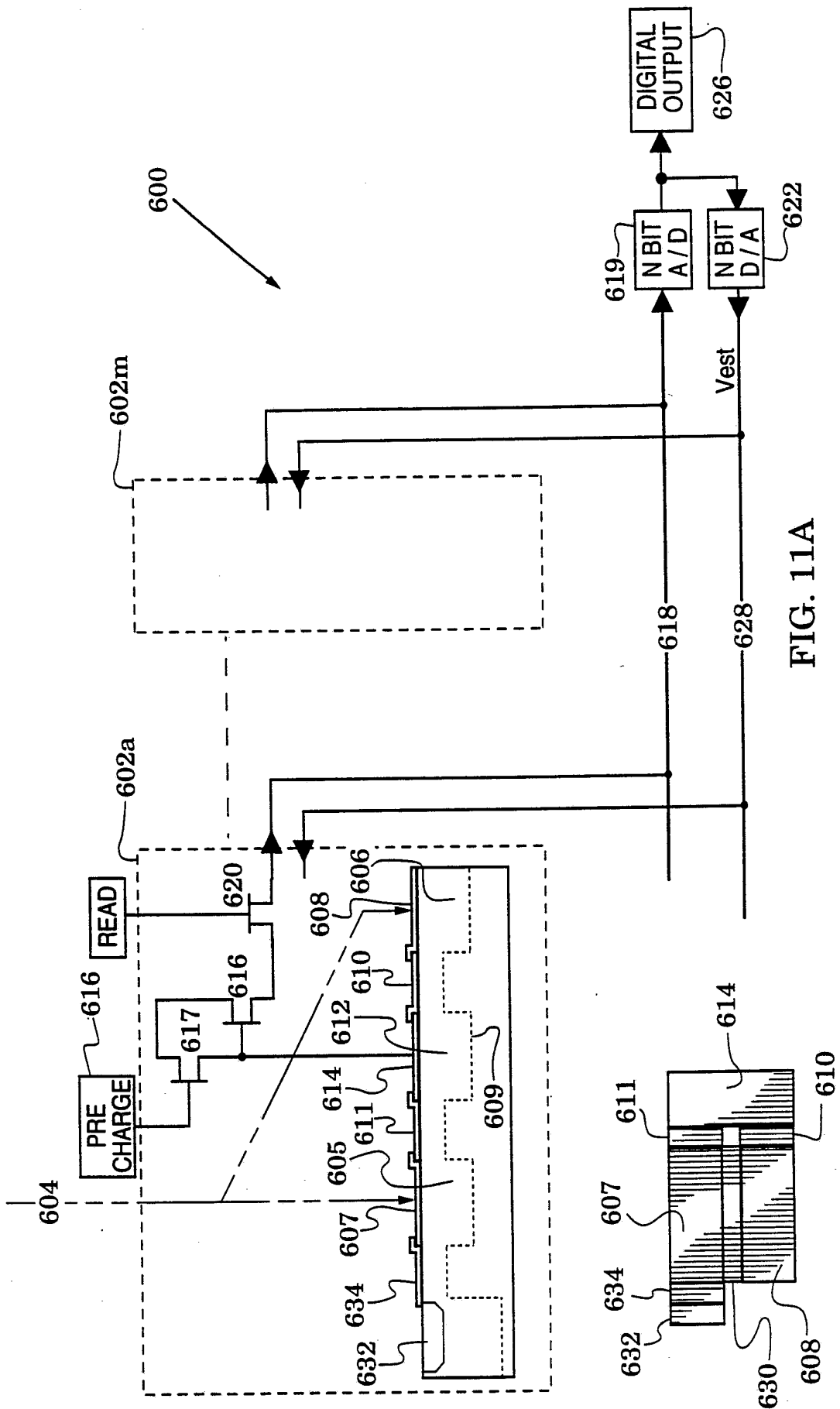


FIG. 11A

FIG. 11B

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US93/04627**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) :H03M 3/00

US CL :341/141

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 341/143, 172; 358/41, 209

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US, A, 5,150,120 (Yunus) 22 September 1992, see figure 1	1
A,P	US, A, 5,142,286 (Ribner et al.) 25 August 1992, see figure 1	1
A	US, A, 5,075,679 (Gazsi) 24 December 1991, see figure 1	1
A	US, A, 5,030,953 (Chiang) 09 July 1991, see columns 1-3	1
A	US, A, 5,014,059 (Seckora) 07 May 1991, see abstract and figure 1	1
A	US, A, 4,353,057 (Bernet et al.) 05 October 1982, see figure 1	

 Further documents are listed in the continuation of Box C.
  See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be part of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"G" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

15 JULY 1993

Date of mailing of the international search report

29 JUL 1993

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