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(54) Title: CMOS SRAM/ROM UNIFIED BIT CELL

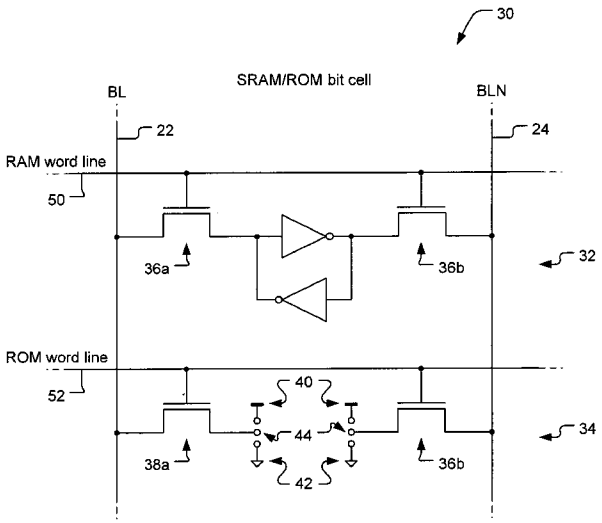

FIG. 2

(57) Abstract: A memory cell (30) including a bit (BL) and bitnot (BLN) sense lines, and a random access memory (RAM) word line (50) and a read only memory (ROM) word line (52). The memory cell includes a static RAM (SRAM) bit cell (32) and a ROM bit cell. The SRAM bit cell is coupled between the bit and bitnot sense lines, and is responsive to a signal on the RAM word line. The ROM bit cell is also coupled between the bit and bitnot sense lines, and is responsive to a signal on the ROM word line. The ROM bit cell includes first (38a) and second (38b) ROM pass transistors, a first node for permanently programming connection of the first ROM pass transistor to either a voltage line or a ground line, and a second node (44) for permanently programming connection of the second ROM pass transistor to either the voltage line or the ground line.

WO 2008/088696 A8

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